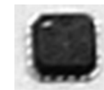
ULTRA-PRECISION 1:8 CML FANOUT BUFFER WITH INTERNAL I/O TERMINATION

Precision Edge®
SY58031U



Precision Edge®

FEATURES

- **Precision 1:8, 400mV CML fanout buffer**
- **Guaranteed AC performance over temperature and voltage:**
  - **Clock frequency range: DC to >6GHz**
  - **<60ps t_r / t_f time**
  - **<270ps t_{pd}**
  - **<20ps ouput-to-output skew**
- **Low-jitter performance:**
  - **<10ps$_{PP}$ total jitter (clock)**
  - **<1ps$_{RMS}$ random jitter**
  - **<1ps$_{RMS}$ cycle-to-cycle jitter**
- **50ý source-terminated CML outputs**
- **400mV CML output swing into 50ý load**
- **Fully differential I/O**
- **Accepts an input signal as low as 100mV**
- **Unique, patent-pending input termination and VT pin accepts DC-coupled and AC-coupled differential inputs: (LVPECL, LVDS, and CML)**
- **Power supply 2.5V ±5% or 3.3V ±10%**
- **Industrial temperature range: –40°C to +85°C**
- **Available in 32-pin (5mm x 5mm) MLF® package**

DESCRIPTION

The SY58031U is a 2.5V/3.3V precision, high-speed, fully differential CML 1:8 fanout buffer. The SY58031U is optimized to provide eight identical output copies with less than 20ps of skew and less than 10ps$_{PP}$ total jitter. It can process clock signals as fast as 6GHz.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the SY58031U to directly interface to CML, LVPECL, and LVDS differential signals (AC- or DC-coupled) without any level-shifting or termination resistor networks in the signal path. The result is a clean, stub-free, low-jitter interface solution. The CML outputs feature 400mV typical swing into 50ý loads and provide an extremely fast rise/fall time guaranteed to be less than 60ps.

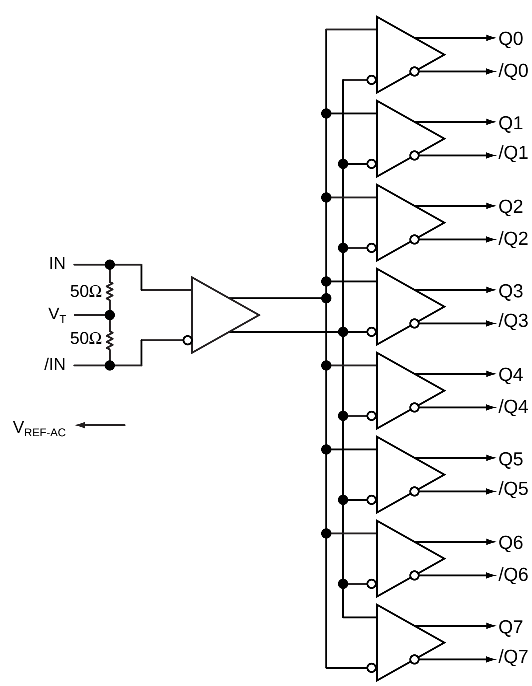
The SY58031U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require high-speed 1:8 LVPECL fanout buffers, consider the SY58032U and SY58033U. The SY58031U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at www.micrel.com.

APPLICATIONS

- **All SONET and all GigE clock distribution**
- **All Fibre Channel clock and data distribution**
- **Network routing engine timing distribution**
- **High-end, low-skew multiprocessor synchronous clock distribution**

FUNCTIONAL BLOCK DIAGRAM



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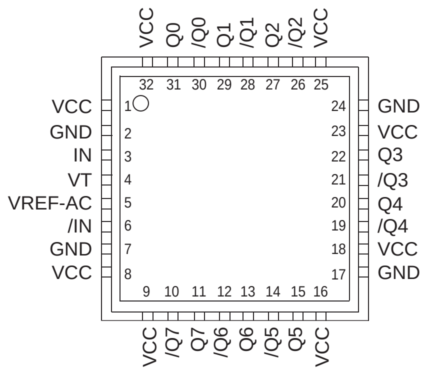
*Micro*LeadFrame and MLF are registered trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



32-Pin MLF® (MLF-32)

Ordering Information(1)

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58031UMI	MLF-32	Industiral	SY58031U	Sn-Pb
SY58031UMITR(2)	MLF-32	Industiral	SY58031U	Sn-Pb
SY58031UMG(3)	MLF-32	Industiral	SY58031U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58031UMGTR(2, 3)	MLF-32	Industiral	SY58031U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
3, 6	IN, /IN	Differential Signal Input: Each pin of this pair internally terminates with 50ý to the VT pin. Note that this input will default to an indeterminate state if left open. See "Input Interface Applications" section.
4	VT	Input Termination Center-Tap: Each input terminates to this pin. The VT pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See "Input Interface Applications" section.
2, 7, 17, 24	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
1, 8, 9, 16 18, 23, 25, 32	VCC	Positive Power Supply: Bypass with 0.1µF™™0.01µF low ESR capacitors as close to the pins as possible.
31, 30, 29, 28, 27, 26, 22, 21, 20, 19, 15, 14, 13, 12, 11, 10	Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3, Q4, /Q4, Q5, /Q5, Q6, /Q6, Q7, /Q7	CML Differential Output Pairs: Differential buffered output copy of the input signal. The CML output swing is typically 400mV into 50ý. Unused output pairs may be left floating with no impact on jitter. See "CML Output Termination" section.
5	VREF-AC	Bias Reference Voltage: Equal to V_{CC}–1.2V (typical), and used for AC-coupled applications. See "Input Interface Applications" section. When using V_{REF-AC}, bypass with 0.01µF capacitor to V_{CC}. Maximum sink/source current is 0.5mA.

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{CC}) .... –0.5V to +4.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC}
Current (V_T)
Source or sink current on V_T pin .... ±100mA
Input Current (V_T)
Source or sink current on IN, /IN .... ±50mA
Current (V_{REF})
Source or sink current on V_{REF-AC}(3) .... ±1.5mA
Lead Temperature Soldering, (20 sec.) .... 260°C
Storage Temperature Range (T_S) ....–65°C to +150°C

Operating Ratings(2)

Power Supply Voltage (V_{CC}) .... +2.375V to +3.60V
Ambient Temperature Range (T_A) ....–40°C to +85°C
Package Thermal Resistance(4)
MLF® (θ_{JA})
Still-Air .... 35°C/W
MLF® (ψ_{JB})
Junction-to-Board .... 20°C/W

DC ELECTRICAL CHARACTERISTICS(5)

T_A= –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	2.5V nominal 3.3V nominal	2.375 3.0	2.5 3.3	2.625 3.6	V V
I_{CC}	Power Supply Current	V_{CC} = max. no lead. Includes current through 50ý pull-ups.		265	330	mA
V_{IH}	Input HIGH Voltage	IN1, /IN1, Note 6	V_{CC}–1.6		V_{CC}	V
V_{IL}	Input LOW Voltage	IN1, /IN1	0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing	IN1, /IN1, see Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN0, /IN0|, |IN1, /IN1|	IN1, /IN1, see Figure 1b.	0.2			V
R_{IN}	In-to-V_T Resistance		40	50	60	ý
$V_{T\ IN}$	Max. In-to-V_T (IN, /IN)				1.28	V
V_{REF-AC}			V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

CML DC ELECTRICAL CHARACTERISTICS(5)

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 100ý across Q and /Q; T_A= –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC}–0.020		V_{CC}	V
V_{OUT}	Output Voltage Swing	see Figure 1a.	325	400		mV
V_{DIFF_OUT}	Differential Voltage Swing	see Figure 1b.	650	800		mV
R_{OUT}	Output Source Impedance		40	50	60	ý

Notes:

1. Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Thermal performance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential (GND) on the PCB. ψ_{JB} uses 4-layer θ_{JA} in still-air number unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above tables after thermal equilibrium has been established.
6. V_{IH} (min) not lower tha 1.2V.

AC ELECTRICAL CHARACTERISTICS(7)

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 100ý across each output pair or equivalent; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	V_{OUT} ž 200mV Clock	6			GHz
t_{pd}	Propagation Delay (IN-to-Q)		120	230	270	ps
$t_{pd\ tempco}$	Differential Propagation Delay Temperature Coefficient			35		fs/°C
t_{SKEW}	Output-to-Output (Within Device)	**Note 8**		7	20	ps
	Part-to-Part	**Note 9**			100	ps
t_{JITTER}	Clock Cycle-to-Cycle	**Note 10**			1	ps_{RMS}
	Total Jitter (Clock)	**Note 11**			10	ps_{PP}
	Random Jitter (RJ)	**Note 12**			1	ps_{RMS}
t_r, t_f	Output Rise/Fall Time	20% to 80%, at full output swing	20	45	60	ps

Notes:

7. High frequency AC electricals are guaranteed by design and characterization. All outputs loaded, V_{IN} ž100mV.
8. Output-to-output skew is measured between outputs under identical transitions.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. Part-to-part skew includes variation in t_{pd}.
10. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, $T_n – T_{n–1}$ where T is the time between rising edges of the output signal.
11. Total jitter definition: With an ideal clock input of frequency - f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
12. Random jitter is measured with a K28.7 comma detect character pattern, measured at 1.25Gbps and 2.5Gbps.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

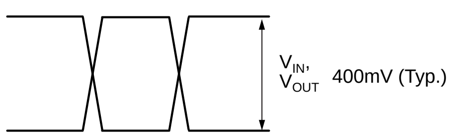


Figure 1a. Single-Ended Voltage Swing

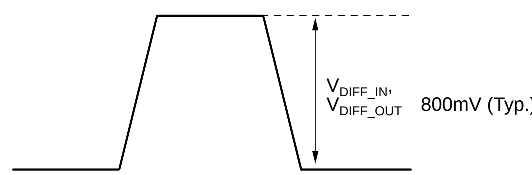
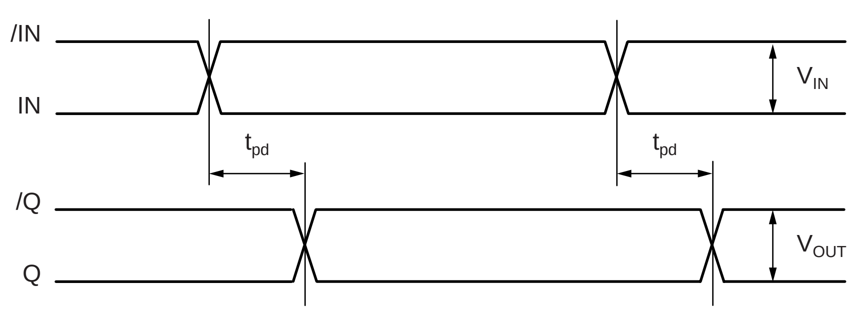


Figure 1b. Differential Voltage Swing

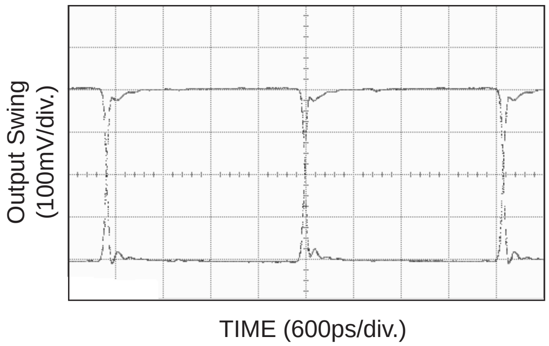
TIMING DIAGRAM



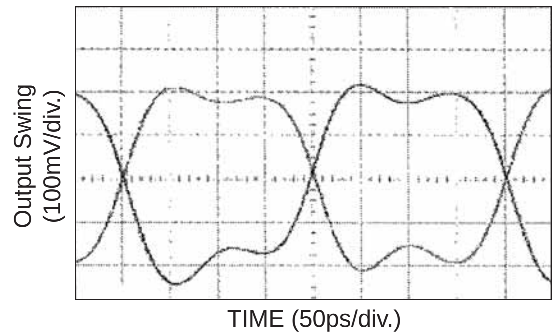
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 2.5V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

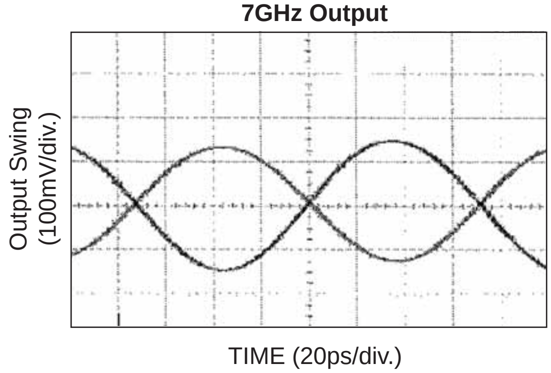
200MHz Output



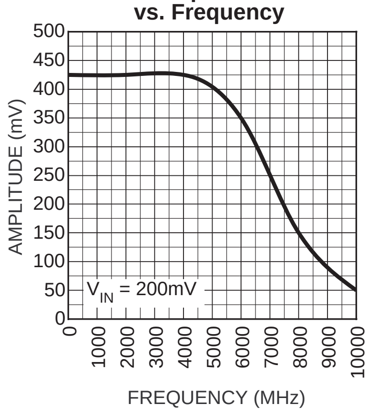
2.5GHz Output



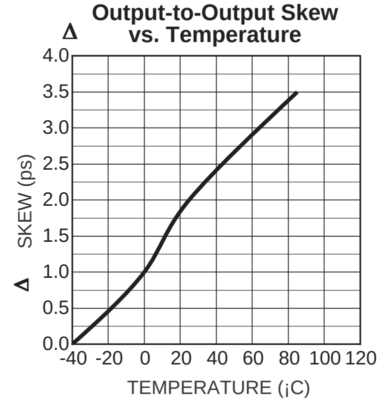
7GHz Output



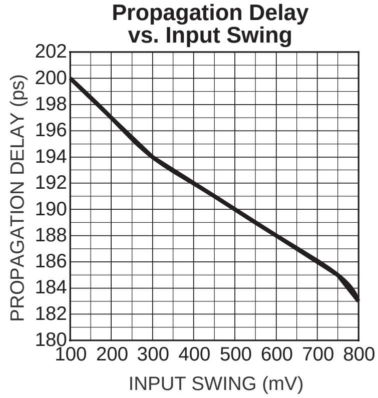
Amplitude vs. Frequency



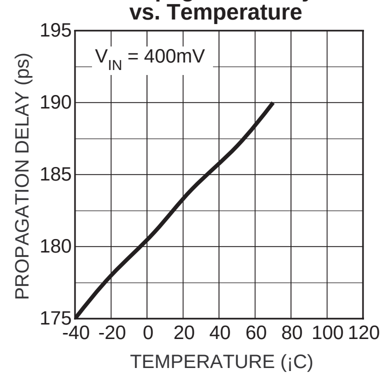
Output-to-Output Skew vs. Temperature



Propagation Delay vs. Input Swing



Propagation Delay vs. Temperature



INPUT BUFFER

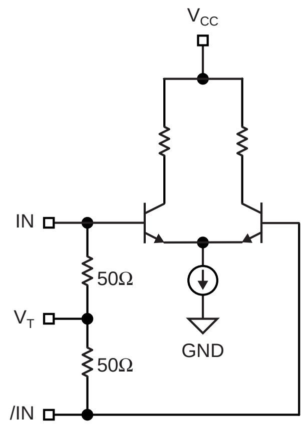
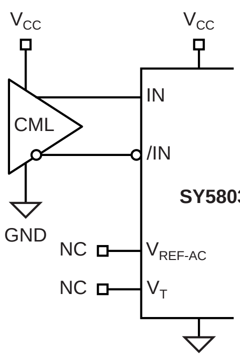


Figure 2. Simplified Differential Input Buffer

INPUT INTERFACE APPLICATIONS



Option: May connect V_T to V_{CC}.

Figure 3a. DC-Coupled CML Input Interface

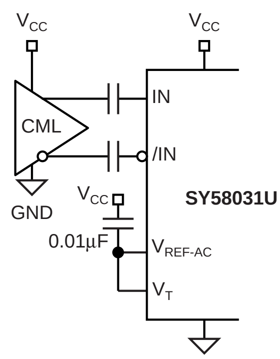
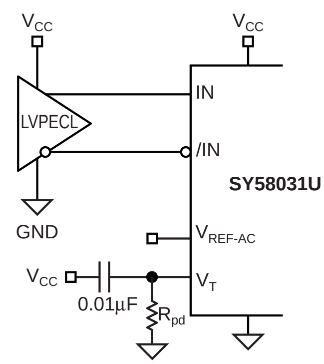


Figure 3b. AC-Coupled CML Input Interface



For 2.5V, R_{pd} = 19Ω
For 3.3V, R_{pd} = 50Ω

Figure 3c. LVPECL Input Interface

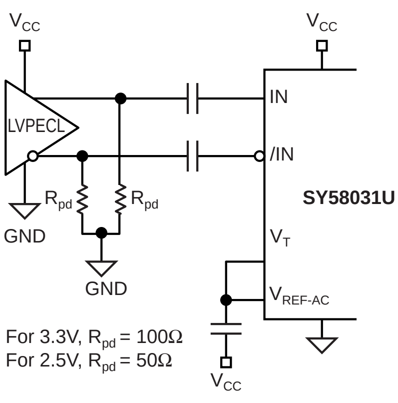


Figure 3d. AC-Coupled LVPECL Input Interface

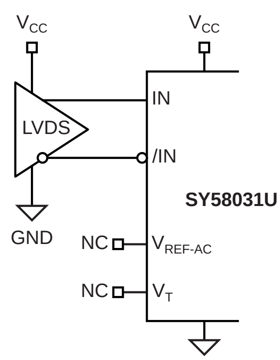


Figure 3e. LVDS Input Interface

CML OUTPUT TERMINATION

Figure 4 and Figure 5 illustrate how to terminate a CML output using both the AC- and DC-coupled configuration. All outputs of the SY58031U are 50ý with a 16mA current source.

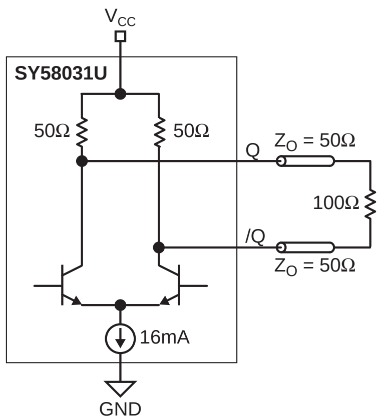


Figure 4. CML DC-Coupled Termination

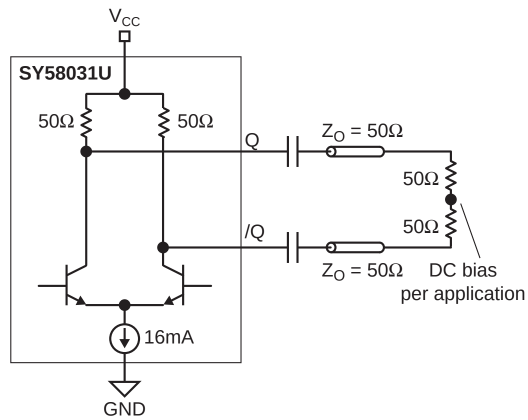
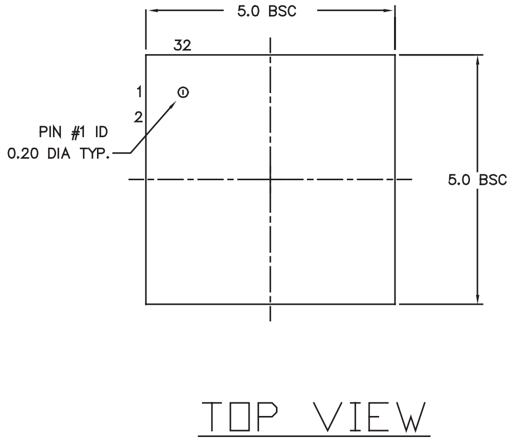


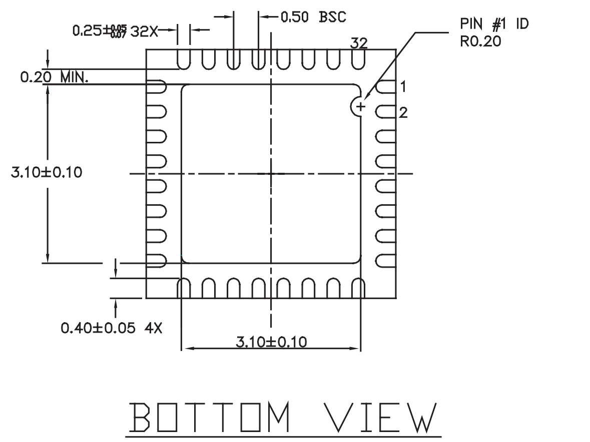
Figure 5. CML AC-Coupled Termination

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

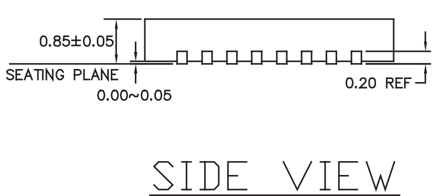
Part Number	Function	Data Sheet Link
SY58031U	Ultra-Precision 1:8 CML Fanout Buffer with Internal I/O Termination	http://www.micrel.com/product-info/products/sy58031u.shtml
SY58032U	Ultra-Precision 1:8 LVPECL Fanout Buffer with Internal Termination	http://www.micrel.com/product-info/products/sy58032u.shtml
SY58033U	Ultra-Precision 1:8 400mV Fanout Buffer with Internal Termination	http://www.micrel.com/product-info/products/sy58033u.shtml
	32-MLF® Manufacturing Guidelines Exposed Pad Application Note	www.amkor.com/products/notes_papers MLF_AppNote.pdf
	HBW Solutions	http://www.micrel.com/product-info/as/solutions.shtml

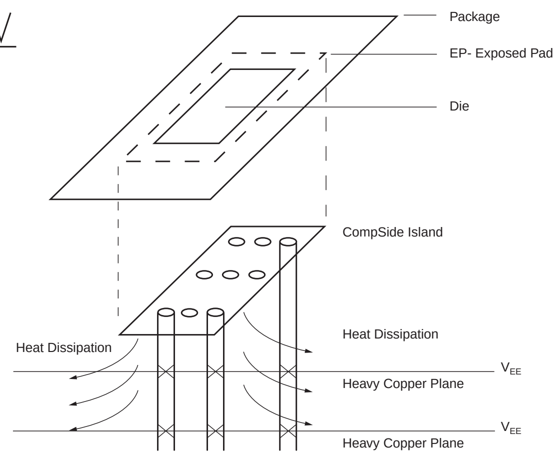
32-PIN *Micro*LeadFrame® (MLF-32)





NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.





PCB Thermal Consideration for 32-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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