



# 1 Characteristics

**Table 1. Absolute ratings (limiting values)**

Symbol	Parameter and test conditions	Value	Unit
$T_j$	Maximum junction temperature	125	°C
$T_{op}$	Operating temperature range	- 40 to + 85	°C
$T_{stg}$	Storage temperature range	- 55 to + 150	°C

**Table 2. Electrical characteristics (Tamb = 25° C)**

Symbol	Parameter
$V_{BR}$	Breakdown voltage
$I_{RM}$	Leakage current @ $V_{RM}$
$V_{RM}$	Stand-off voltage
$C_{line}$	Input capacitance per line

The graph plots current  $I$  on the vertical axis against voltage  $V$  on the horizontal axis. It shows a typical diode-like characteristic with a sharp increase in current at the breakdown voltage  $V_{BR}$ . Specific points are marked:  $V_{BR}$  (breakdown voltage),  $V_{RM}$  (stand-off voltage),  $I_R$  (leakage current at  $V_{RM}$ ), and  $I_{RM}$  (leakage current at  $V_{BR}$ ).

Symbol	Test conditions	Tolerance	Min.	Typ.	Max.	Unit
$V_{BR}$	$I_R = 1 \text{ mA}$		6		9	V
$I_{RM}$	$V_{RM} = 5 \text{ V per line}$				1	$\mu\text{A}$
$R_1, R_2$	$I = 10 \text{ mA}$	$\pm 5\%$		33		$\Omega$
$R_3$	$I = 1 \text{ mA}$	$\pm 5\%$		1.5		$\text{k}\Omega$
$C_{line}$	@ 0 V			30		pF
Matching	Serial resistance matching			1		%

Figure 1. S21 (dB) attenuation measurement      Figure 2. Analog crosstalk measurements

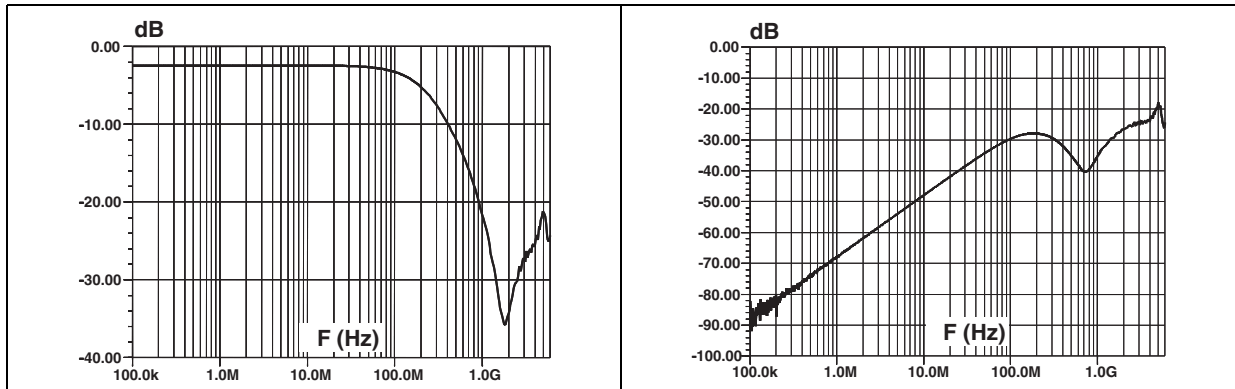


Figure 3. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (Vin) and on one output (Vout)

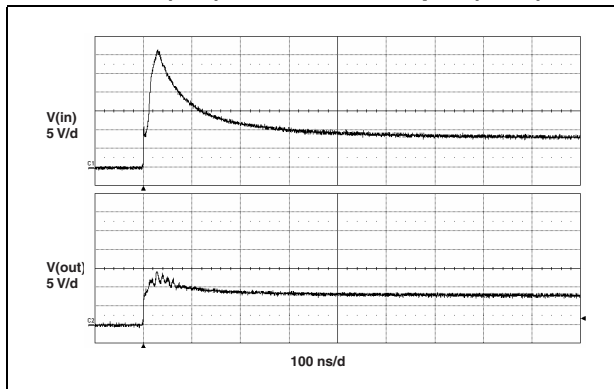


Figure 4. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (Vin) and on one output (Vout)

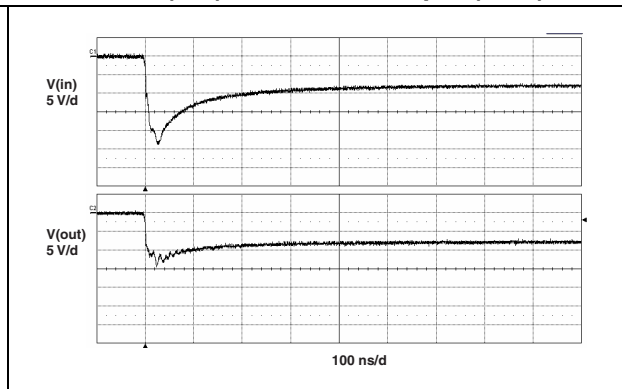
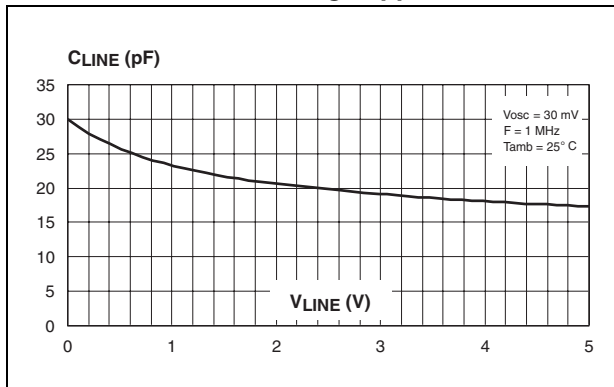


Figure 5. Junction capacitance versus reverse voltage applied





### 3 Package information

Figure 8. Flip-Chip package dimensions

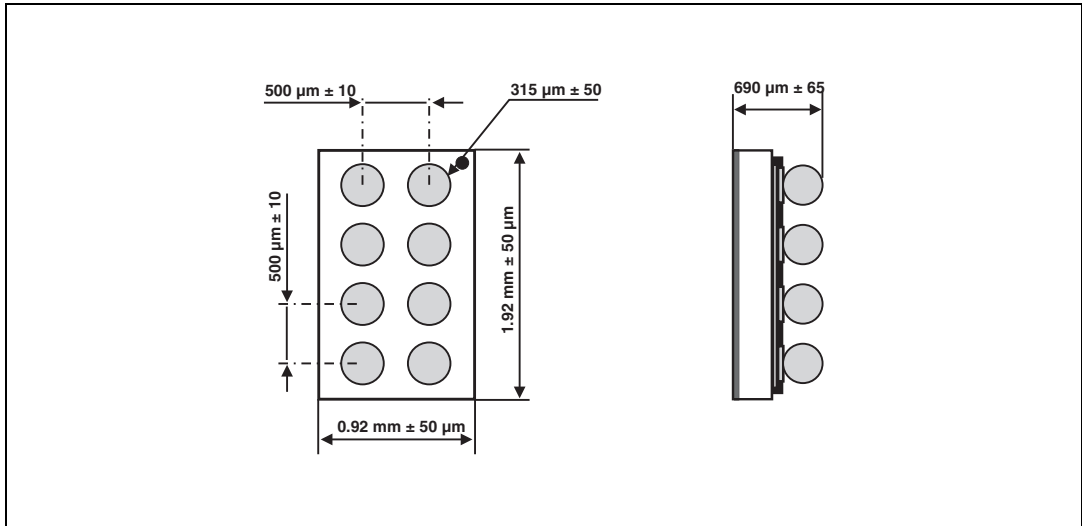


Figure 9. Foot print recommendations      Figure 10. Marking

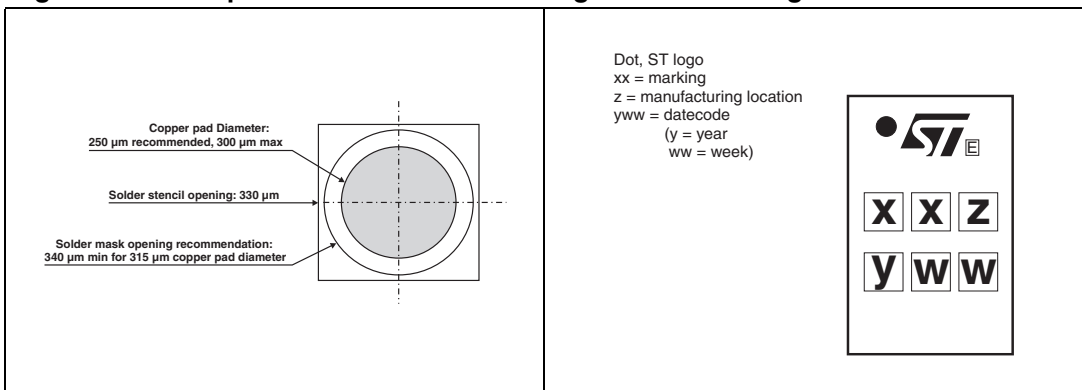
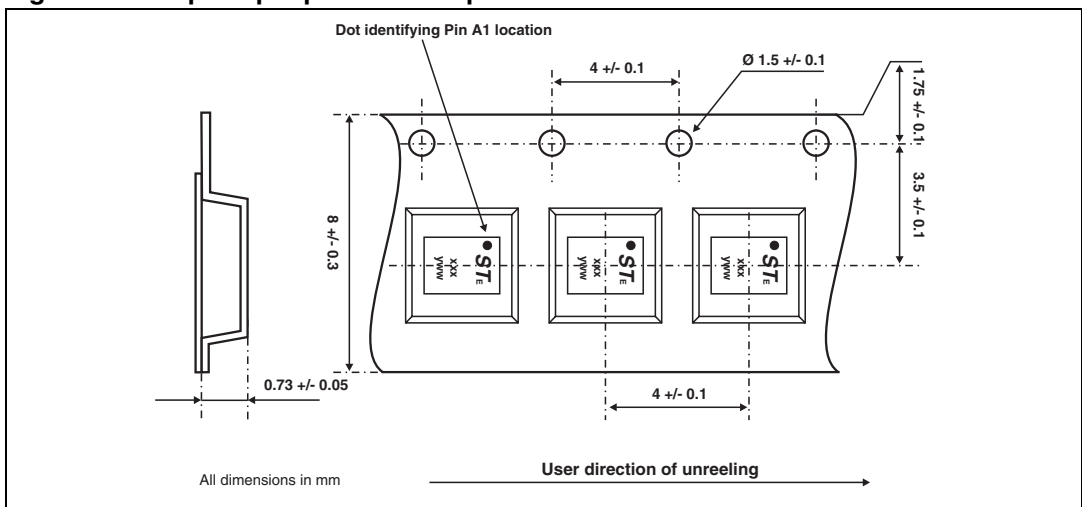


Figure 11. Flip-Chip tape and reel specification



*Note: More packing information is available in the application notes*

*AN1235: "Flip-Chip: Package description and recommendations for use"*

*AN1751: "EMI Filters: Recommendations and measurements"*

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

## 4 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-USB05C2	GV	Flip-Chip	2.7 mg	5000	Tape and reel 7"

## 5 Revision history

Date	Revision	Changes
14-Mar-2005	1	Initial release.
13-Nov-2006	2	Reformatted to current standards. Modified functional diagram on page 1 to show connections. Updated Aplac model information.

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