MIC4102

100V Half Bridge MOSFET Driver with Anti-Shoot Through Protection

PRELIMINARY SPECIFICATIONS

General Description

The MIC4102 is a high frequency, 100V Half Bridge MOSFET driver IC featuring internal anti-shoot-through protection. The low-side and high-side gate drivers are controlled by a single input signal to the PWM pin. The MIC4102 implements adaptive anti-shoot-through circuitry to optimize the switching transitions for maximum efficiency. The single input control also reduces system complexity and greatly simplifies the overall design.

The MIC4102 also features a low-side drive disable pin. This gives the MIC4102 the capability to operate in a non-synchronous buck mode. This feature allows the MIC4102 to start up into applications where a bias voltage may already be present without pulling the output voltage down.

Under-voltage protection on both the low-side and high-side supplies forces the outputs low. An on-chip boot-strap diode eliminates the discrete diode required with other driver ICs.

The MIC4102 is available in the SOIC-8L package with a junction operating range from –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

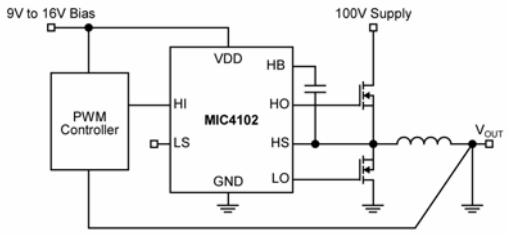
Features

- Drives high- and low-side N-Channel MOSFETs with single input
- Adaptive anti-shoot-through protection
- Low side drive disable pin
- Bootstrap supply voltage to 118V DC
- Supply voltage up to 16V
- TTL input thresholds
- On-chip bootstrap diode
- Fast 30ns propagation times
- Drives 1000pF load with 10ns rise and 6ns fall times
- Low power consumption
- Supply under-voltage protection
- 2.5Ω pull up , 1.5Ω pull down output resistance
- Space saving SOIC-8L package
- –40°C to +125°C junction temperature range

Applications

- High voltage buck converters
- Networking / Telecom power supplies
- Automotive power supplies
- Current Fed Push-Pull Topologies
- Ultrasonic drivers
- Avionic power supplies

Typical Application

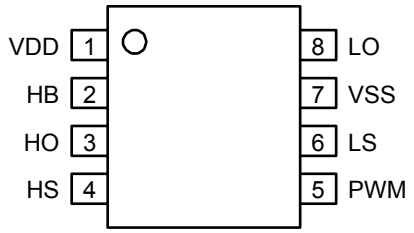


100V Buck Regulator Solution

Ordering Information

Part Number		Input	Junction Temp. Range	Package
Standard	**Pb-Free**			
MIC4102BM	MIC4102YM	TTL	–40° to +125°C	SOIC-8L

Pin Configuration



SOIC-8L (M)

Pin Description

Pin Number	Pin Name	Pin Function
1	VDD	Positive Supply to lower gate drivers. Decouple this pin to VSS (Pin 7). Bootstrap diode connected to HB (pin 2).
2	HB	High-Side Bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.
3	HO	High-Side Output. Connect to gate of High-Side power MOSFET.
4	HS	High-Side Source connection. Connect to source of High-Side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
5	PWM	Control Input. PWM high signal makes high-side HO output high, and low-side LO output low. PWM low signal makes high-side HO output low, and low-side LO output high.
6	LS	Low-Side Disable. When pulled low, this control signal immediately terminates the low-side LO output drive. The low-side LO output drive will remain low until this signal is removed. HS drive is not affected by the LS signal. Here is the logic table: LS PWM LO HO 0 0 0 0 0 1 0 1 1 0 1 0 1 1 0 1
7	VSS	Chip negative supply, generally will be grounded.
8	LO	Low-Side Output. Connect to gate of Low-Side power MOSFET.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}, V_{HB} – V_{HS}) ..... -0.3V to 18V
Input Voltages ($V_{PWM,}$ V_{LS}) ..... -0.3V to V_{DD} + 0.3V
Voltage on LO (V_{LO}) ..... -0.3V to V_{DD} + 0.3V
Voltage on HO (V_{HO}) ..... V_{HS} - 0.3V to V_{HB} + 0.3V
Voltage on HS (continuous) ..... -1V to 110V
Voltage on HB 118V
Average Current in VDD to HB Diode 100mA
Junction Temperature (T_J) ..... –55°C to +150°C
Storage Temperature (T_s) ..... -60°C to +150°C
EDS Rating[3] ..... Note 3

Operating Ratings[2]

Supply Voltage (V_{DD}) ..... +9V to +16V
Voltage on HS ..... -1V to 100V
Voltage on HS (repetitive transient) ..... -5V to 105V
HS Slew Rate 50V/ns
Voltage on HB ..... V_{HS} + 8V to V_{HS} + 16V
and ..... V_{DD} - 1V to V_{DD} + 100V
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
SOIC-8L (θ_{JA}) ..... 140°C/W

Electrical Characteristics[4]

V_{DD} = V_{HB} = 12V; V_{SS} = V_{HS} = 0V; No load on LO or HO; T_A = 25°C; unless noted. **Bold** values indicate –40°C≤ T_J ≤ +125°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Supply Current						
I_{DD}	V_{DD} Quiescent Current	PWM = 0V		150	450 **600**	µA
I_{DDO}	V_{DD} Operating Current	f = 500kHz		3	3.5 **4.0**	mA
I_{HB}	Total HB Quiescent Current	PWM = 0V		25	150 **200**	µA
I_{HBO}	Total HB Operating Current	f = 500kHz		1.5	2.5 **3**	mA
I_{HBS}	HB to VSS Current, Quiescent	V_{HS} = V_{HB} = 110V		0.05	1 **30**	µA
Input Pins (TTL)						
V_{IL}	Low Level Input Voltage Threshold		**0.8**	1.5		V
V_{IH}	High Level Input Voltage Threshold			1.5	**2.2**	V
R_I	Input Pull-down Resistance		**100**	200	**500**	kΩ
Under Voltage Protection						
V_{DDR}	V_{DD} Rising Threshold		**6.5**	7.3	**8.0**	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		**6.0**	7.0	**8.0**	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
Boost Strap Diode						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100µA		0.4	0.55 **0.70**	V
V_{DH}	Low-Current Forward Voltage	I_{VDD-HB} = 100mA		0.7	0.8 **1.0**	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100mA		1.0	1.5 **2.0**	Ω

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
LO Gate Driver						
V_{OLL}	Low Level Output Voltage	I_{LO} = 160mA		0.18	0.3 **0.4**	V
V_{OHL}	High Level Output Voltage	I_{LO} = -100mA, $V_{OHL} = V_{DD} - V_{LO}$		0.25	0.3 **0.45**	V
I_{OHL}	Peak Sink Current	V_{LO} = 0V		3		A
I_{OLL}	Peak Source Current	V_{LO} = 12V		2		A
HO Gate Driver						
V_{OLH}	Low Level Output Voltage	I_{HO} = 160mA		0.22	0.3 **0.4**	V
V_{OHH}	High Level Output Voltage	I_{HO} = -100mA, $V_{OHH} = V_{HB} – V_{HO}$		0.25	0.3 **0.45**	V
I_{OHH}	Peak Sink Current	V_{HO} = 0V		3		A
I_{OLH}	Peak Source Current	V_{HO} = 12V		2		A
Switching Specifications (Anti-Shoot-Through Circuitry)						
t_{LOOFF}	Delay between PWM going high to LO going low			30	45 **60**	ns
V_{LOOFF}	Voltage threshold for LO MOSFET to be considered OFF			1.7		V
t_{HOON}	Delay between LO OFF to HO going High			30	50 **60**	ns
t_{HOOFF}	Delay between PWM going Low to HO going low			45	65 **70**	ns
V_{SWth}	Switch Node Voltage Threshold when HO turns off		1	2.5	4	V
t_{LOON}	Delay between HO MOSFET being considered off to LO turning ON			30	60 **70**	ns
t_{LSOFF}	Delay between LS going low and LO turning OFF	C_L = 1000pF		36	45 **70**	ns
t_{SWTO}	Forced LO ON, if VLOTH is not detected		**120**	250	**450**	ns
Switching Specifications						
t_R	Either Output Rise Time (3V to 9V)	C_L = 1000pF		10		ns
t_F	Either Output Fall Time (3V to 9V)	C_L = 1000pF		6		ns
t_R	Either Output Rise Time (3V to 9V)	CL = 0.1µF		0.33	0.6 **0.8**	µs
t_F	Either Output Fall Time (3V to 9V)	CL = 0.1µF		0.2	0.3 **0.4**	µs

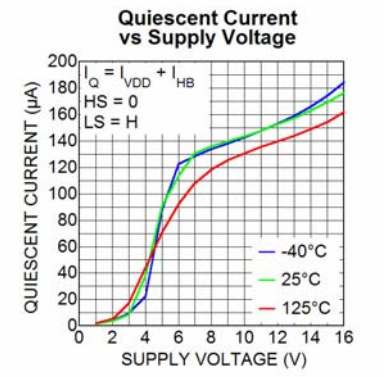
Electrical Characteristics (cont.)

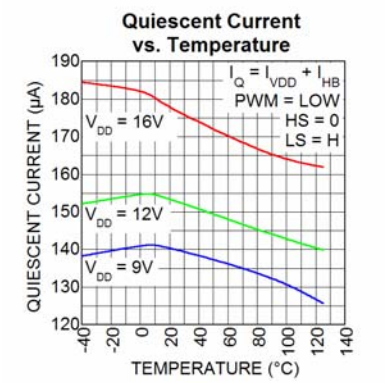
Symbol	Parameter	Condition	Min	Typ	Max	Units
Switching Specifications (cont.)						
t_{PW}	Minimum Input Pulse Width that changes the output with LS=5V	C_L=0 Note 6		40	**60**	ns
t_{PW}	Minimum Output Pulse Width on HO with min pulse width on PWM with LS=5V	C_L=0 Note 6		15		ns
t_{PW}	Minimum Input Pulse Width that changes the output with LS=0V	C_L=0 Note 6		13	**20**	ns
	Minimum Output Pulse Width on HO with min pulse width on PWM with LS=0V	C_L=0 Note 6		20		
t_{BS}	Bootstrap Diode Turn-On or Turn-Off Time			10		ns

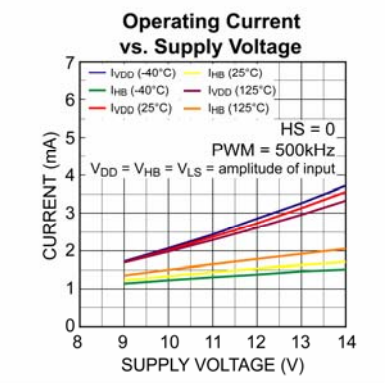
Notes:

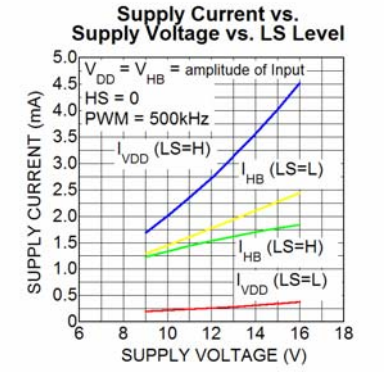
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
4. Specification for packaged product only.
5. All voltages relative to pin7, V_{SS} unless otherwise specified.
6. Guaranteed by design. Not production tested.

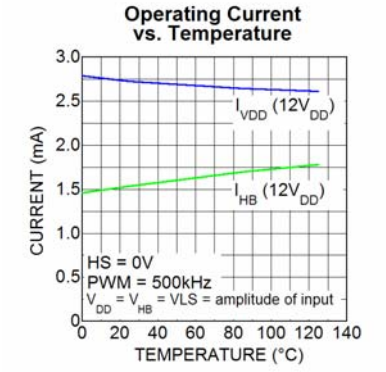
Typical Characteristics

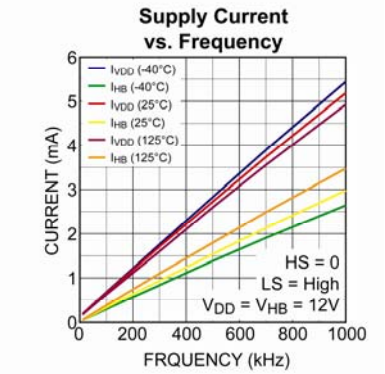


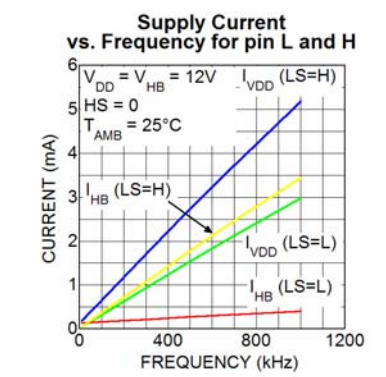


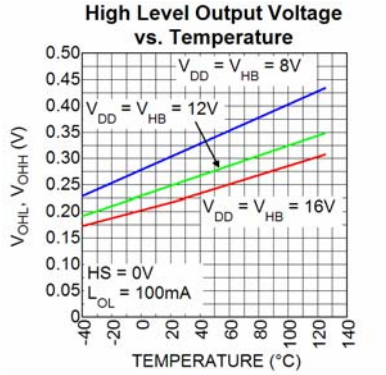


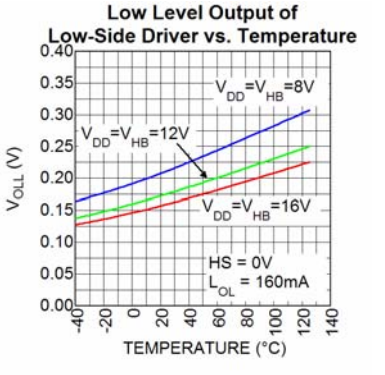


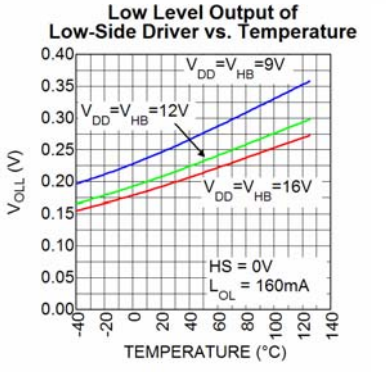


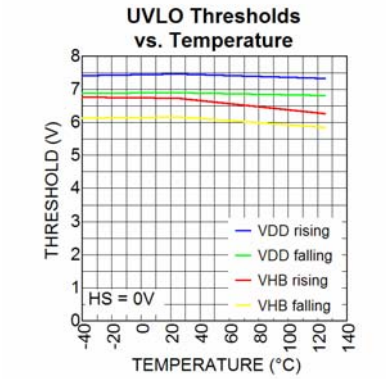


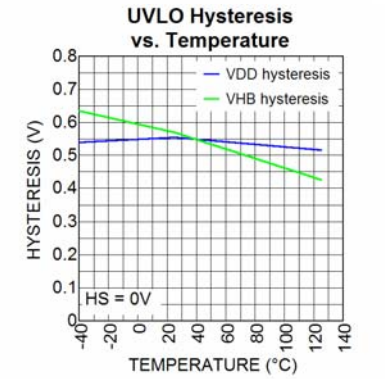




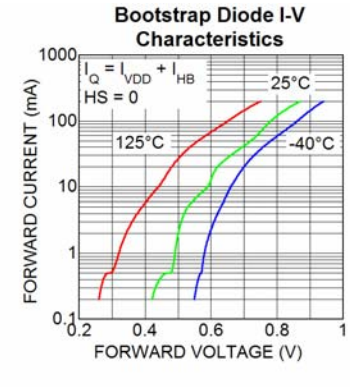


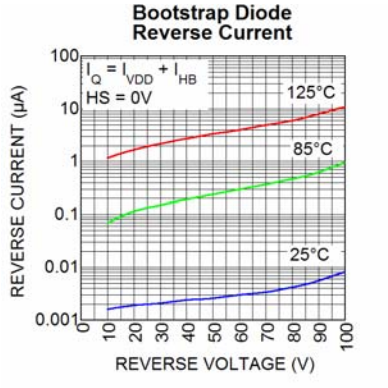




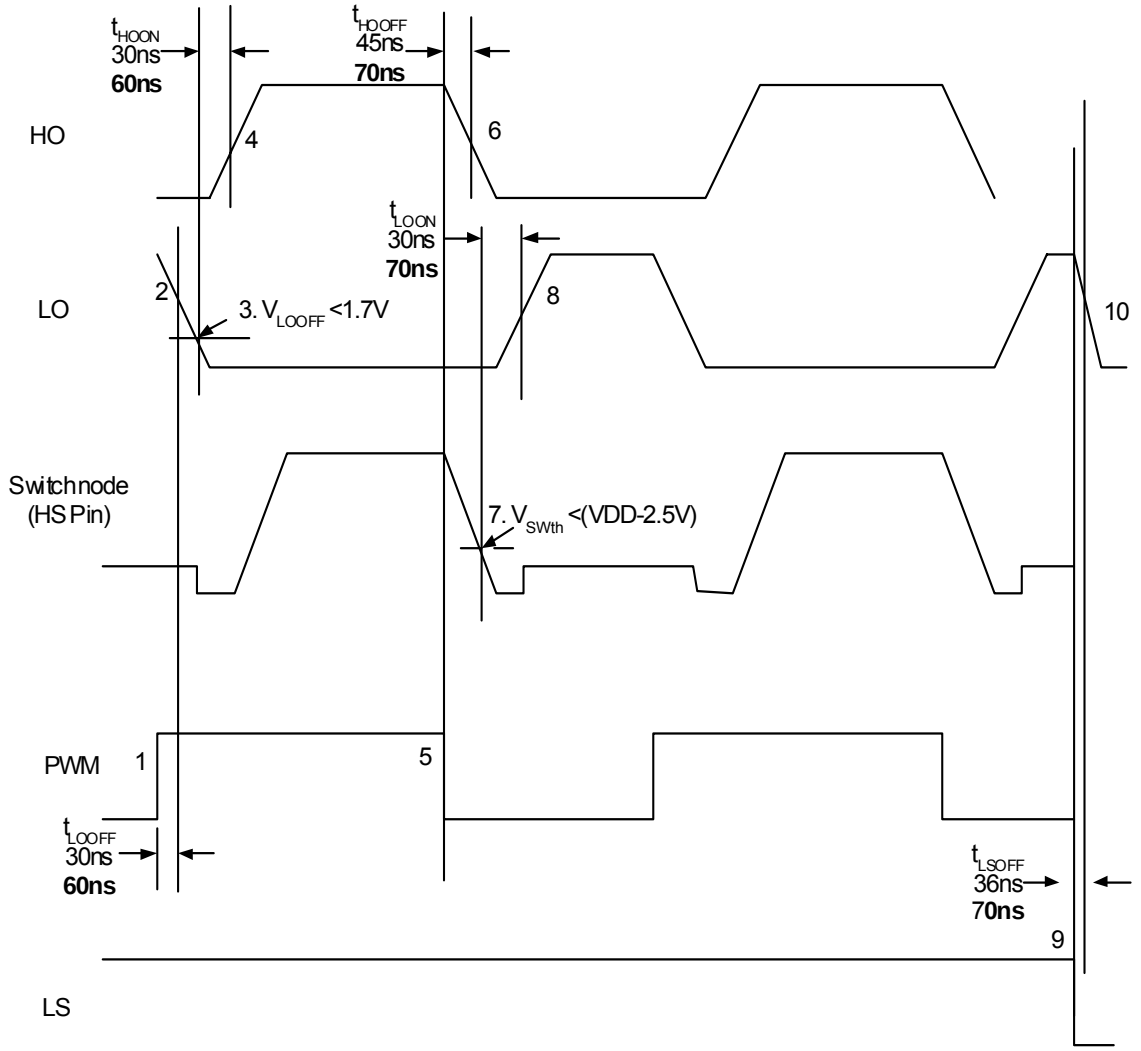


Typical Characteristics (cont.)





Timing Diagrams



Time Point Action

1-2 PWM signal goes high. This initiates the LO signal to go low. The delay between PWM high to (V_{LO} –10%) is typically 30ns (t_{LOOFF})

2-4 LO goes low. When LO reaches 1.7V (V_{LOOFF}) the low side MOSFET is deemed to be off. The high side output HO then goes high. The delay between 3 and 4 is typically 30ns (T_{HOON}); this allows for large turn off delay times of MOSFETs.

5-7 PWM goes low; HO goes low, typically within 45ns, t_{HOOFF}. The switch node (HS pin) is then monitored; when the switch node is VDD-2.5V (V_{SWTH}) the high side MOSFET is deemed to be off and the LO output goes high within typically 30ns (t_{LOON}). This is controlled by a one shot and remains high until PWM goes high. This is because it is possible to have the SW node oscillate, and could easily bounce through 10V level. If the LO high transition has not happened within 250ns, it is forced to happen, unless the LS input is low.

8-10 If at any time after 7 has occurred and LS pin goes low, the LO output will turn off within 36ns (V_{LSOFF}). HO will remain off. The LS pin overrides all shoot through control logic. If LS is low at the start of the next cycle when PWM signal goes high then HO shall switch transition 1-4 as normal. I.e. PWM signal equals HO output, LO = 0V.

Functional Diagram

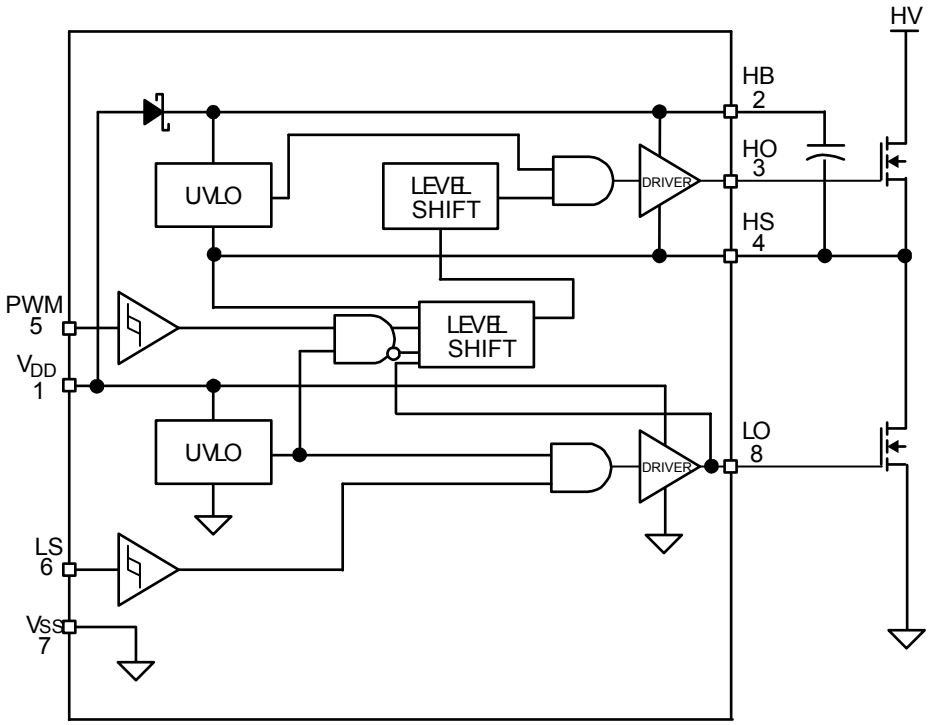


Figure 1. MIC4102 Functional Block Diagram

Functional Description

The MIC4102 is a high voltage, non-inverting, synchronous MOSFET driver that uses a single PWM input signal to alternately drive both high-side and low-side N-Channel MOSFETs. The block diagram of the MIC4102 is shown in Figure 1.

The MIC4102 input is TTL compatible. The high-side output buffer includes a high speed level-shifting circuit that is referenced to the HS pin. An internal diode is used as part of a bootstrap circuit to provide the drive voltage for the high-side output.

Startup and UVLO

The UVLO circuit forces both driver outputs low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the VDD and VSS pins. The high-side UVLO circuit monitors the voltage between the HB and HS pins. Hysteresis in the UVLO circuit prevents noise and finite circuit impedance from causing chatter during turn-on.

The VDD pin voltage is supplied to the HS pin through the internal bootstrap diode. The HB pin voltage will always be a diode drop less than VDD.

Input Stage

The MIC4102 utilizes a TTL compatible input stage. The PWM input pin is referenced to the VSS pin. The voltage state of the input signal does not change the quiescent current draw of the driver. The threshold level is independent of the VDD supply voltage and there is no dependence between I_{VDD} and the input signal amplitude. This feature makes the MIC4102 an excellent level translator that will drive high threshold MOSFETs from a low voltage PWM IC.

Low-Side Driver

A block diagram of the low-side driver is shown in Figure 2. The low-side driver is designed to drive a ground (Vss pin) referenced N-channel MOSFET. Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low Rdson from the external MOSFET.

A low level applied to PWM pin will cause the HO output to go low and the LO output to go high. The upper driver FET turns on and Vdd is applied to the gate of the external MOSFET. A high level on the PWM pin forces the LO output low by turning off the upper driver and turning on the lower driver which ground the gate of the external MOSFET.

Pulling the LS pin low disables the LO pin.

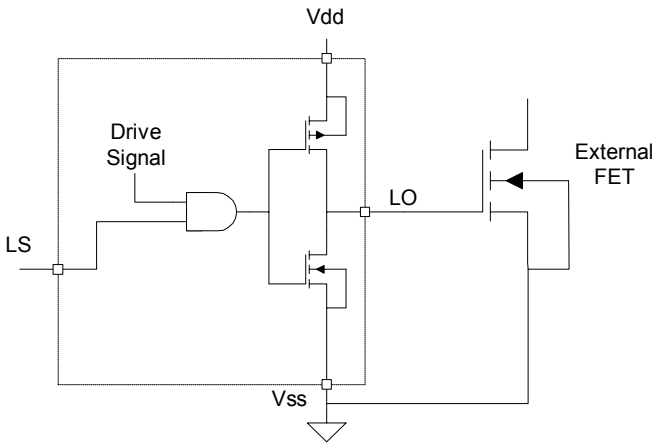


Figure 2. Low-Side Driver Block Diagram

High-Side Driver and Bootstrap Circuit

A block diagram of the high-side driver and bootstrap circuit is shown in Figure 3. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HS pin.

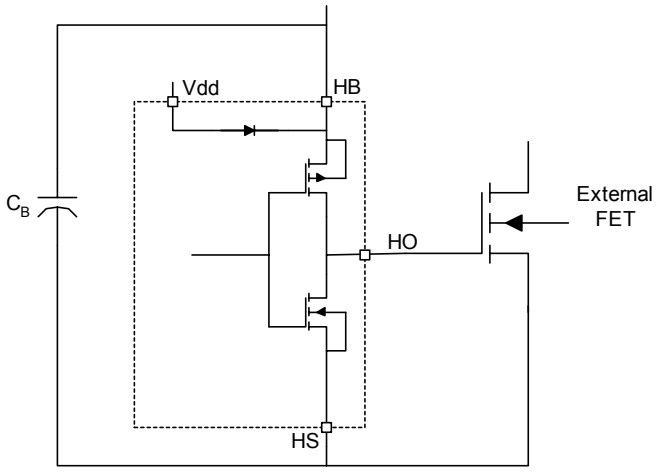


Figure 3. High-Side Driver Block Diagram

A low power, high speed, level shifting circuit isolates the low side (VSS pin) referenced circuitry from the high-side (HS pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap circuit while the voltage level of the HS pin is shifted high.

The bootstrap circuit consists of an internal diode and external capacitor, C_B. In a typical application, such as the synchronous buck converter shown in Figure 4, the HS pin is at ground potential while the low-side MOSFET is on. The internal diode allows capacitor C_B to charge up to V_{DD}-V_D during this time (where V_D is the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the HO pin turns on, the voltage across capacitor C_B is applied to the gate of the upper external MOSFET. As the upper MOSFET turns on, voltage on the HS pin rises with the source of the high-side MOSFET until it reaches V_{IN}. As the HS and HB pin rise, the internal diode is reverse biased preventing capacitor C_B from discharging.

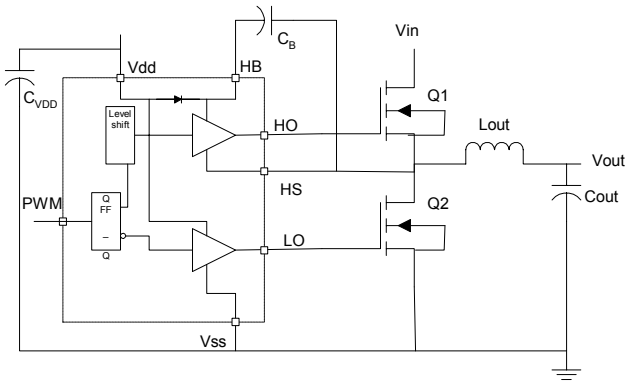


Figure 4. High-Side Driver and Bootstrap Circuit

Applications Information

Power Dissipation Considerations

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the C_B capacitor times the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by:

$$I_{F(AVE)} = Q_{gate} \times f_S$$

where : Q_{gate} = Total Gate Charge at V_{HB}

f_S = gate drive switching frequency

The average power dissipated by the forward voltage drop of the diode equals:

$$Pdiode_{fwd} = I_{F(AVE)} \times V_F$$

where : V_F = Diode forward voltage drop

The value of V_F should be taken at the peak current through the diode, however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of V_F at the average current can be used and will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically 11uA at a reverse voltage of 100V and 125C. Power dissipation due to reverse leakage is typically much less than 1mW and can be ignored.

Reverse recovery time is the time required for the injected minority carriers to be swept away from the depletion region during turn-off of the diode. Power dissipation due to reverse recovery can be calculated by computing the average reverse current due to reverse recovery charge times the reverse voltage across the diode. The average reverse current and power dissipation due to reverse recovery can be estimated by:

$$I_{RR(AVE)} = 2 \times I_{RRM} \times t_{rr} \times f_S$$

$$Pdiode_{RR} = I_{RR(AVE)} \times V_{REV}$$

where : I_{RRM} = Peak Reverse Recovery Current

t_{rr} = Reverse Recovery Time

The total diode power dissipation is:

$$Pdiode_{total} = Pdiode_{fwd} + Pdiode_{RR}$$

An optional external bootstrap diode may be used instead of the internal diode (Figure 5). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the Vdd supply voltage. A 100V Schottky diode will work for most 72V input telecom applications. The above equations can be used to calculate power dissipation in the external diode, however, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated as:

$$Pdiode_{REV} = I_R \times V_{REV} \times (1 - D)$$

where : I_R = Reverse current flow at V_{REV} and T_J

V_{REV} = Diode Reverse Voltage

D = Duty Cycle = t_{ON} / f_S

fs = switching frequency of the power supply

The on-time is the time the high-side switch is conducting. In most power supply topologies, the diode is reverse biased during the switching cycle off-time.

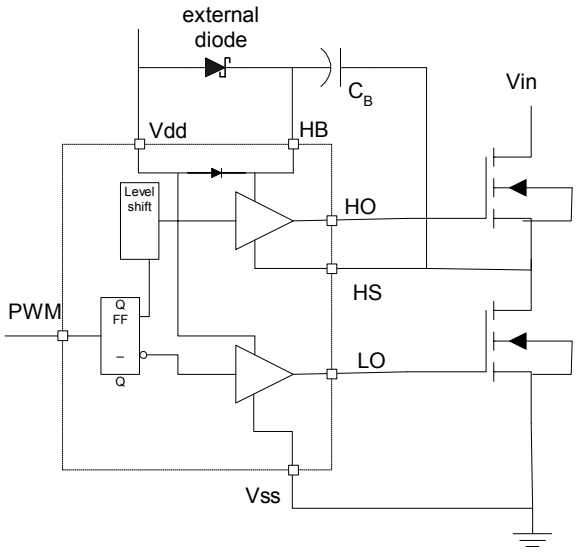


Figure 5. Optional Bootstrap Diode

Gate Drive Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET.

Figure 6 shows a simplified equivalent circuit of the MIC4102 driving an external MOSFET.

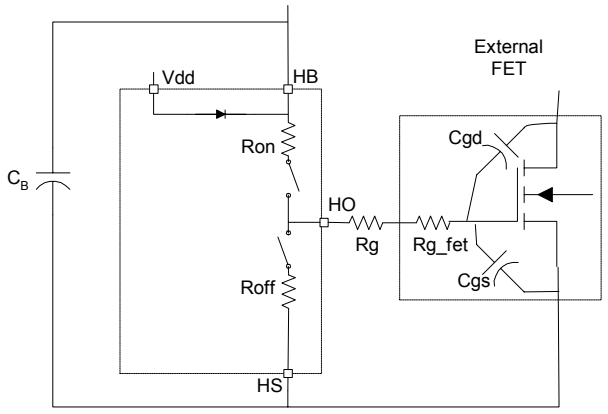


Figure 6. MIC4103 Driving an External MOSFET

Dissipation during the external MOSFET Turn-On

Energy from capacitor C_B is used to charge up the input capacitance of the MOSFET (Cgd and Cgs). The energy delivered to the MOSFET is dissipated in the three resistive components, Ron, Rg and Rg_fet. Ron is the on resistance of the upper driver MOSFET in the MIC4102. Rg is the series resistor (if any) between the driver IC and the MOSFET. Rg_fet is the gate resistance of the MOSFET. Rg_fet is usually listed in the power MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than Ron and Rg_fet.

The effective capacitance of Cgd and Cgs is difficult to calculate since they vary non-linearly with Id, Vgs, and Vds. Fortunately, most power MOSFET specifications include a typical graph of total gate charge vs. Vgs. Figure 7 shows a typical gate charge curve for an arbitrary power MOSFET. This chart shows that for a gate voltage of 10V, the MOSFET requires about 23.5nC of charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

$$E = \frac{1}{2} \times Ciss \times V_{gs}^{\ 2}$$

but

$$Q = C \times V$$

so

$$E = 1/2 \times Qg \times V_{gs}$$

where

Ciss is the total gate capacitance of the MOSFET

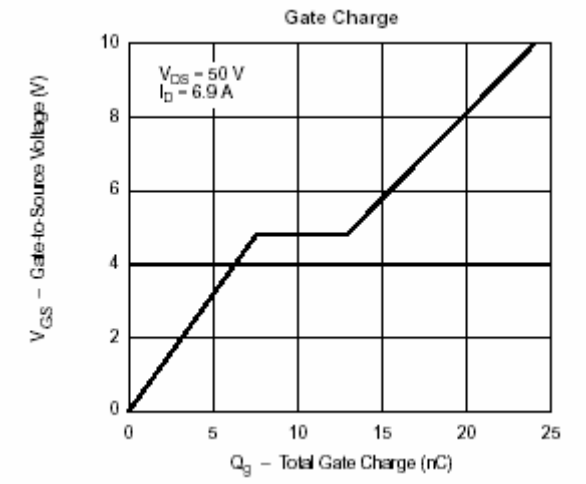


Figure 7. Typical Gate Charge vs. V_{GS}

The same energy is dissipated by Roff, Rg and Rg_fet when the driver IC turns the MOSFET off.

$$E_{driver} = \frac{1}{2} \times Qg \times V_{gs}$$

and

$$P_{driver} = \frac{1}{2} \times Qg \times V_{gs} \times fs$$

where

E_{driver} is the energy dissipated during turn - on or turn - off

P_{driver} is the power dissipated during turn - on or turn - off

Qg is the total gate charge at Vgs

Vgs is the gate to source voltage on the MOSFET

fs is the switching frequency of the gate drive circuit

The power dissipated inside the MIC4102 equals the ratio of Ron & Roff to the external resistive losses in Rg and Rg_fet. The power dissipated in the MIC4102 due to driving the external MOSFET is:

$$Pdiss_{drive} = P_{driver} \times \frac{Ron}{Ron + Rg + Rg\_fet} + P_{driver} \times \frac{Roff}{Roff + Rg + Rg\_fet}$$

Supply Current Power Dissipation

Power is dissipated in the MIC4102 even if is there is nothing being driven. The supply current is drawn by the bias for the internal circuitry, the level shifting circuitry and shoot-through current in the output drivers. The supply current is proportional to operating frequency and the Vdd and Vhb voltages. The typical characteristic graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4102 due to supply current is

$$Pdiss_{supply} = Vdd \times Idd + Vhb \times Ihb$$

Total power dissipation and Thermal Considerations

Total power dissipation in the MIC41032 equals the power dissipation caused by driving the external MOSFETs, the supply current and the internal bootstrap diode .

$$Pdiss_{total} = Pdiss_{supply} + Pdiss_{drive} + Pdiode_{total}$$

The die temperature may be calculated once the total power dissipation is known.

$$T_J = T_A + Pdiss_{total} \times \theta_{JA}$$

where :

T_A is the maximum ambient temperature

T_J is the junction temperature (°C)

$Pdiss_{total}$ is the power dissipation of the MIC4102

θ_{JC} is the thermal resistance from junction to ambient air (°C/W)

Anti Shoot-Through, Propagation Delay and other Timing Considerations

The block diagram in Figure 1 illustrates how the MIC4102 drives the power stage of a synchronous buck converter. It is important that only one of the two MOSFETs is on at any given time. If both MOSFETs are simultaneously on they will short Vin to ground, causing high current from the Vin supply to "shoot through" the MOSFETs into ground. Excessive shoot-through causes higher power dissipation in the MOSFETs, voltage spikes and ringing in the circuit. The high current and voltage ringing generate conducted and radiated EMI.

Minimizing shoot-through can be done passively, actively or though a combination of both. Passive shoot-through protection uses delays between the high and low gate drivers to prevent both MOSFETs from being on at the same time. These delays can be adjusted for different applications. Although simple, the disadvantage of this approach is the long delays required to account for process and temperature variations in the MOSFET and MOSFET driver.

Active shoot-though monitors voltages on the gate drive outputs and switch node to determine when to switch the MOSFETs on and off. This active approach adjusts the delays to account for some of the variations, but it too has its disadvantages. High currents and fast switching voltages in the gate drive and return paths can cause parasitic ringing that may turn the MOSFETs back on even though the gate driver output is low. Another disadvantage is the driver cannot monitor the gate voltage inside the MOSFET. Figure 8 shows an equivalent circuit, including parasitics, of the gate driver section. The internal gate resistance (Rg_gate) and any external damping resistor (Rg) isolate the MOSFET's gate from the driver output. There is a delay between when the driver output goes low and the MOSFET turns off. This turn-off delay is usually specified in the MOSFET data sheet. This delay increases when an external damping resistor is used.

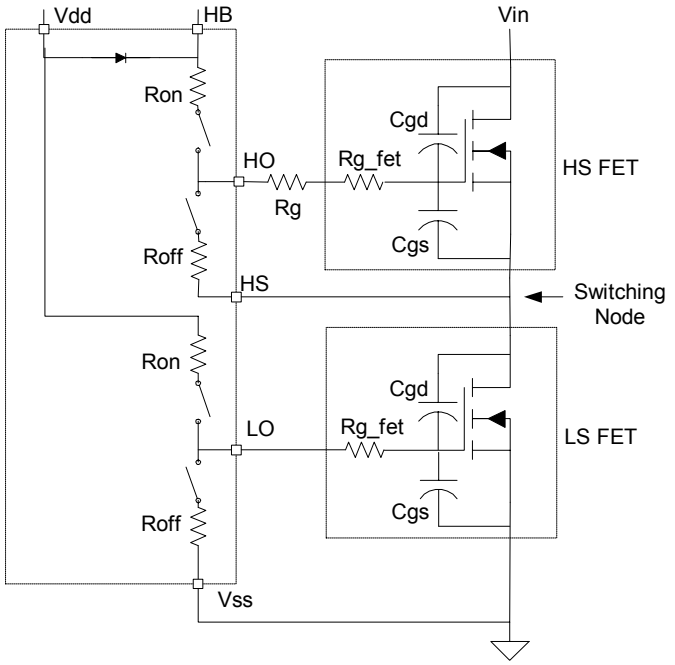


Figure 8. Gate Drive Circuit with Parasitics

The MIC4102 uses a combination of active sensing and passive delay to insure that both MOSFETs are not on at the same time and to minimize shoot-through current. The timing diagram helps illustrate how the anti-shoot-through circuitry works. A high level on the PWM pin causes the LO pin to go low. The MIC4102 monitors the LO pin voltage and prevents the HO pin from turning on until the voltage on the LO pin reaches the V_{LOOFF} threshold. After a short delay, the MIC4102 drives the HO pin high. Monitoring the LO voltage eliminates any excessive delay due to the MOSFET drivers turn-off time and the short delay accounts for the MOSFET turn-off delay as well as letting the LO pin voltage settle out. An external resistor between the LO output and the MOSFET may affect the performance of the LO pin monitoring circuit and is not recommended.

A low on the PWM pin causes the HO pin to go low after a short delay (T_{HOOFF}). Before the LO pin can go high,

the voltage on the switching node (HS pin) must have dropped to 2.5V below the Vdd voltage. Monitoring the switch voltage instead of the HO pin voltage eliminates timing variations and excessive delays due to the high side MOSFET turn-off. The LO driver turns on after a short delay (T_{LOON}). Once the LO driver is turn on, it is latched on until the PWM signal goes high. This prevents any ringing or oscillations on the switch node or HS pin from turning off the LO driver. If the PWM pin goes low and the voltage on the HS pin does not cross the V_{SWth} threshold, the LO pin will be forced high after a short delay (T_{SWTO}), insuring proper operation.

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Care must be taken to insure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is determined by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned back on.

The anti-shoot-through circuit in the MIC4102 prevents the driver from turning both MOSFETs on at the same time, however, other factors outside of the anti-shoot-through circuit's control can cause shoot-through. Some of these are ringing on the gate drive node and capacitive coupling of the switching node voltage on the gate of the low-side MOSFET.

Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low side (Vdd) and high side (HB) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs as well as minimize the voltage ripple on these pins. The capacitor from HB to HS serves double duty by providing decoupling for the high-side circuitry as well as providing current to the high-side circuit while the high-side external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended due to the large change in capacitance over temperature and voltage. A minimum value of 0.1uf is required for each of the capacitors, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability. 25V rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low voltage capacitors are use since even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for Vdd should be placed as close as possible between the Vdd and Vss pins. The bypass capacitor (C_B) for the HB supply pin must be located as close as possible between the HB and HS pins. The etch connections must be short, wide and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to the section on layout and component placement for more information.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge vs. Vgs voltage. Based on this information and a recommended ΔV_{HB} of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

$$C_B \geq \frac{Q_{gate}}{\Delta V_{HB}}$$

where : Q_{gate} = Total Gate Charge at V_{HB}

Δ_{HB} = Voltage drop at the HB pin

The decoupling capacitor for the Vdd input may be calculated in with the same formula, however, the two capacitors are usually equal in value.

Grounding, Component Placement and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MIC4102 driver require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing or circuit latch-up.

Figure 9 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also shown the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors C_{VDD} and C_B. Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate and out the Source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate voltage and can either slow down or turn off the MOSFET during the period where it should be turned on.

Current in the high-side driver is sourced from capacitor C_B and flows into the HB pin and out the HO pin, into the gate of the high side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor C_B. The high-side circuit return path usually does not have a low impedance ground plane so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback which fights the turn-on of the MOSFET.

It is important to note that capacitor CB must be placed close to the HB and HS pins. This capacitor not only provides all the energy for turn-on but it must also keep HB pin noise and ripple low for proper operation of the high-side drive circuitry.

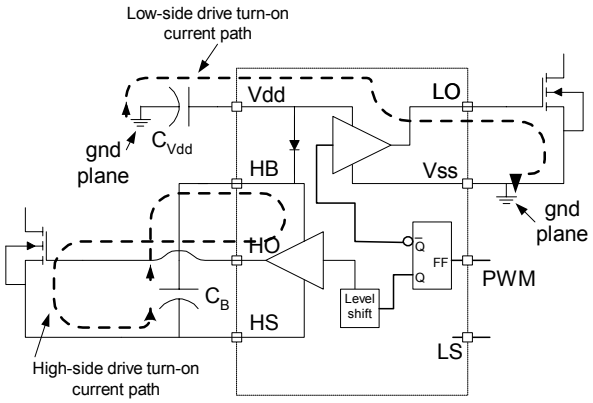


Figure 9. Turn-on Current Paths

Figure 10 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor, CB.

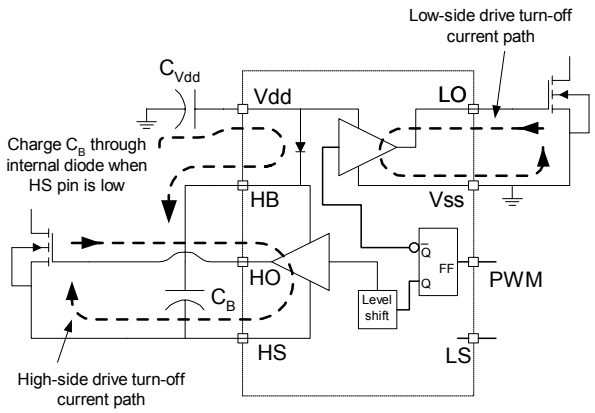


Figure 10. Turn-off Current Paths

The following circuit guidelines should be adhered to for optimum circuit performance:

1. The Vcc and HB bypass capacitors must be placed close to the supply and ground pins. It is critical that the etch length between the high side decoupling capacitor (C_B) and the HB & HS pins be minimized to reduce lead inductance.
2. A ground plane should be used to minimize parasitic inductance and impedance of the return paths. The MIC4102 is capable of greater than 3A peak currents and any impedance between the MIC4102, the decoupling capacitors and the external MOSFET will degrade the performance of the driver.
3. Trace out the high di/dt and dv/dt paths, as shown in Figures 9 and 10 to minimize the etch length and loop area for these connections. Minimizing these parameters decreases the parasitic inductance and the radiated EMI generated by fast rise and fall times. A typical layout of a synchronous Buck converter power stage using the MIC4102 (Figure 11) is shown in Figure 12.

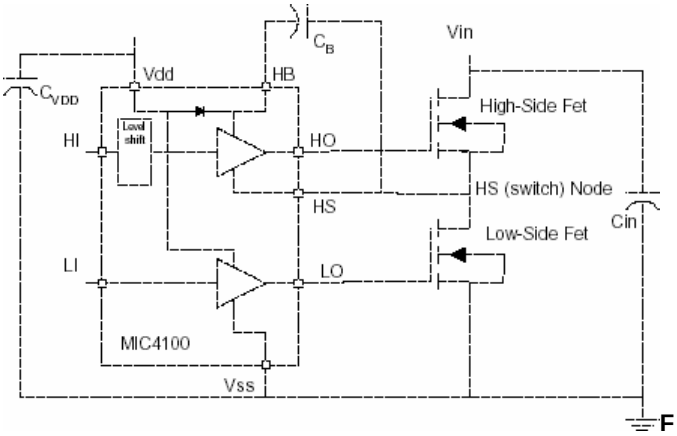


Figure 11. Typical Converter Power Stage

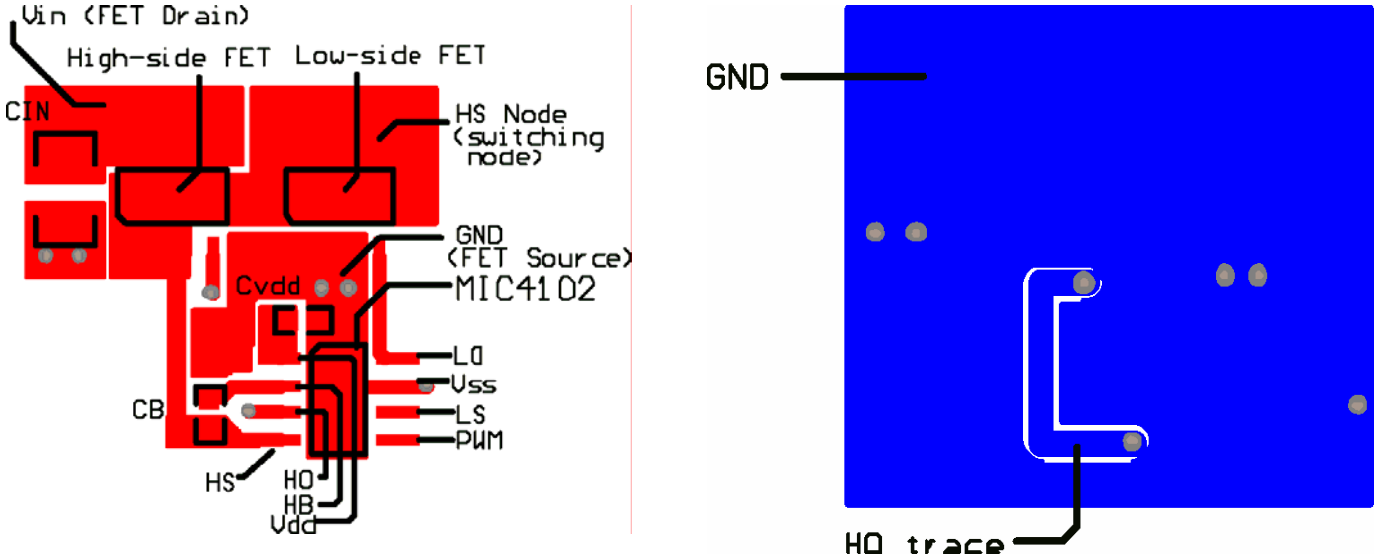
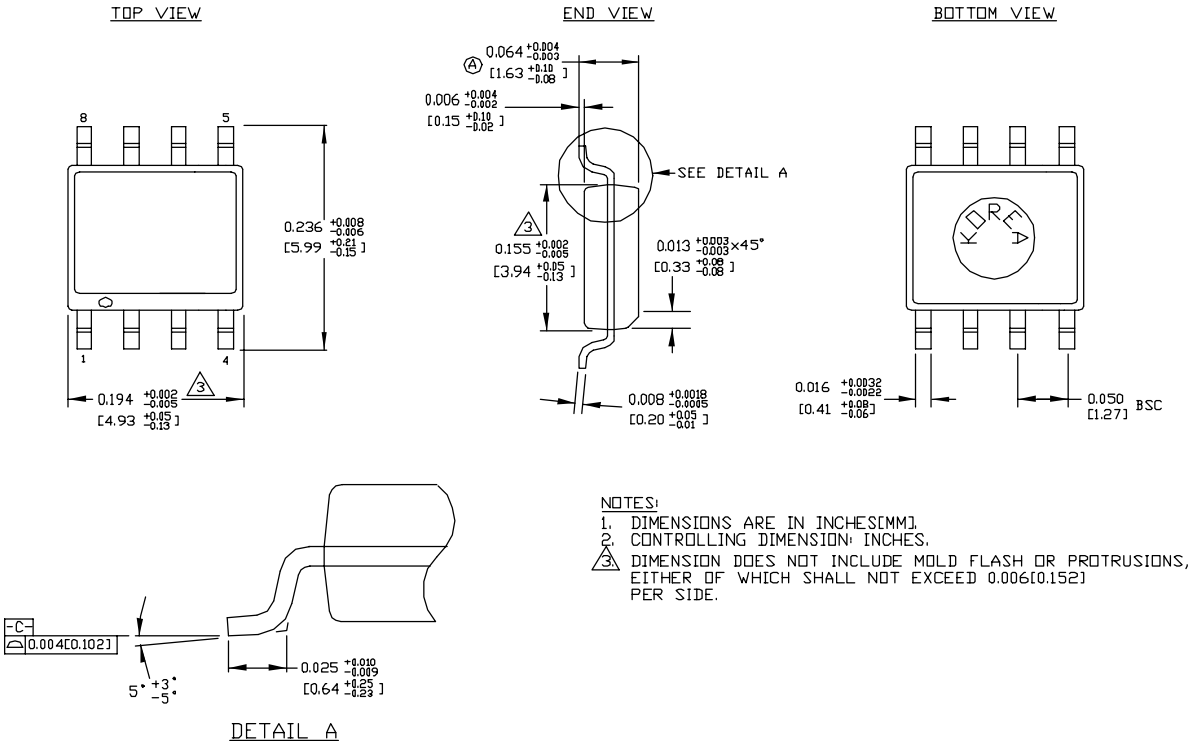


Figure 12. Typical Layout of a Synchronous Buck Converter Power Stage

1. The circuit is configured as a synchronous buck power stage. The high-side MOSFET drain connects to the input supply voltage (drain) and the source connects to the switching node. The low-side MOSFET drain connects to the switching node and its source is connected to ground. The buck converter output inductor (not shown) would connect to the switching node. The high-side drive trace, HO, is routed on top of its return trace, HS, to minimize loop area and parasitic inductance. The low-side drive trace, LO is routed over the ground plane which minimizes the impedance of that current path. The decoupling capacitors, C_B and C_{VDD} are placed to minimize etch length between the capacitors and their respective pins. This close placement is necessary to efficiently charge capacitor C_B when the HS node is low. All traces are 0.025" wide or greater to reduce impedance. Cin is used to decouple the high current path through the MOSFETs.

Package Information



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