ANALOG DEVICES

2.5 MSPS, 24-Bit, 100 dB $\Sigma\Delta$ ADC With On-Chip Buffer

AD7760

FEATURES

120 dB dynamic range at 78 kHz output data rate
100 dB dynamic range at 2.5 MHz output data rate
112 dB SNR at 78 kHz output data rate
100 dB SNR at 2.5 MHz output data rate
2.5 MHz maximum fully filtered output word rate
Programmable over-sampling rate (8× to 256×)
Fully differential modulator input
On-chip differential amplifier for signal buffering
Low-pass finite impulse response (FIR) filter with default or user-programmable coefficients
Overrange alert bit
Digital offset and gain correction registers
Filter bypass modes
Low power and power-down modes
Synchronization of multiple devices via SYNC pin

APPLICATIONS

Data acquisition systems
Vibration analysis
Instrumentation

GENERAL DESCRIPTION

The AD7760 is a high performance, 24-bit Σ-Δ analog-to-digital converter (ADC). It combines wide input bandwidth and high speed with the benefits of Σ-Δ conversion with a performance of 100 dB SNR at 2.5 MSPS, making it ideal for high speed data acquisition. Wide dynamic range combined with significantly reduced antialiasing requirements simply the design process. An integrated buffer to drive the reference, a differential amplifier for signal buffering and level shifting, an overrange flag, internal gain and offset registers, and a low-pass digital FIR filter make the AD7760 a compact, highly integrated data acquisition device requiring minimal peripheral component selection. In addition, the device offers programmable decimation rates, and the digital FIR filter can be adjusted if the default characteristics are not appropriate to the application. The AD7760 is ideal for applications demanding high SNR without a complex front end signal processing design.

The differential input is sampled at up to 40 MSPS by an analog modulator. The modulator output is processed by a series of low-pass filters, the final filter having default or user-programmable
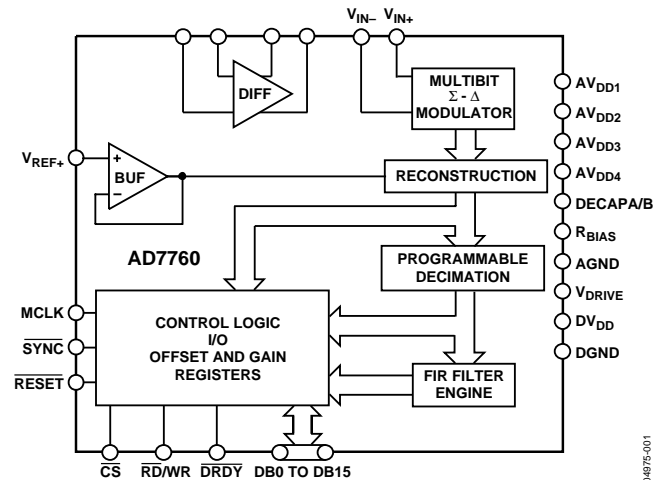
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

coefficients. The sample rate, filter corner frequencies, and output word rate are set by a combination of the external clock frequency and the configuration registers of the AD7760.

The reference voltage supplied to the AD7760 determines the analog input range. With a 4 V reference, the analog input range is ±3.2 V differential biased around a common mode of 2 V. This common-mode biasing can be achieved using the on-chip differential amplifier, further reducing the external signal conditioning requirements.

The AD7760 is available in an exposed paddle, 64-lead TQFP and is specified over the industrial temperature range from −40°C to +85°C.

Table 1. Related Devices

Part No.	Description
AD7762	24-bit, 625 kSPS, 109 dB Σ-Δ, parallel interface
AD7763	24-bit, 625 kSPS, 109 dB Σ-Δ, serial interface

AD7760

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REVISION HISTORY

7/05—Revision 0: Initial Version

SPECIFICATIONS

$AV_{DD1} = DV_{DD} = V_{DRIVE} = 2.5$ V, $AV_{DD2} = AV_{DD3} = AV_{DD4} = 5$ V, $V_{REF} = 4.096$ V, MCLK amplitude = 5 V, $T_A = 25°C$, normal mode, using on-chip amplifier with components as shown in Table 8, unless otherwise noted.[1]

Table 2.

Parameter	Test Conditions/Comments	Specification	Unit
DYNAMIC PERFORMANCE			
Decimate by 256	MCLK = 40 MHz, ODR = 78 kHz, FIN = 1 kHz		
Dynamic Range	Modulator inputs shorted	119	dB min
		120.5	dB typ
Signal-to-Noise Ratio (SNR)[2]	Input amplitude = −0.5 dBFS	112	dB typ
	Input amplitude = −60 dBFS	59	dB typ
Spurious-Free Dynamic Range (SFDR)	Nonharmonic, input amplitude = −6 dBFS	126	dBc typ
	Input amplitude = −60 dBFS	77	dBc typ
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dBFS	−105	dB typ
	Input amplitude = −6 dBFS	−106	dB typ
	Input amplitude = −60dBFS	−75	dB typ
Decimate by 32	MCLK = 40 MHz, ODR = 625 kHz, FIN =100 kHz		
Dynamic Range	Modulator inputs shorted	108	dB min
		109.5	dB typ
Signal-to-Noise Ratio (SNR)[2]	Input amplitude = −0.5dBFS	107	dB typ
Spurious-Free Dynamic Range (SFDR)	Nonharmonic, input amplitude = −6 dBFS	120	dBc typ
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dBFS	−108	dB typ
	Input amplitude = −6 dBFS	−106	dB typ
Decimate by 8	MCLK = 40 MHz, ODR = 2.5 MHz		
Dynamic Range	Modulator inputs shorted	99	dB min
		100.5	dB typ
Signal-to-Noise Ratio (SNR)[2]	FIN = 1 kHz, input amplitude = −0.5 dBFS	100	dB typ
	FIN = 100 kHz, input amplitude = −0.5 dBFS	99	dB typ
	FIN = 1 MHz, input amplitude = −0.5 dBFS	98	dB typ
Spurious-Free Dynamic Range (SFDR)	Nonharmonic, FIN = 100 kHz, input amplitude = −6 dBFS	120	dBc typ
	Nonharmonic, FIN = 1 MHz, input amplitude = −6 dBFS	114	dBc typ
Total Harmonic Distortion (THD)	Input amplitude = −0.5dBFS, FIN = 100 kHz	−103	dB typ
	Input amplitude = −6dBFS, FIN = 100 kHz	−102	dB typ
IMD 2nd Order	FIN A = 989.95 kHz, FIN B = 999.95 kHz	−115	dB typ
IMD 3rd Order	FIN A = 989.95 kHz, FIN B = 999.95 kHz	−89	dB typ
DC ACCURACY			
Resolution		24	Bits
Differential Nonlinearity	Guaranteed monotonic to 24 bits		
Integral Nonlinearity		0.00076	% typ
Zero Error		0.014	% typ
		0.02	% max
Gain Error		0.016	% typ
Zero Error Drift		0.019	%/°C typ
Gain Error Drift		0.0002	%/°C typ
DIGITAL FILTER RESPONSE			
Decimate by 8			
Group Delay	MCLK = 40 MHz	12	µs typ
Decimate by 32			
Group Delay	MCLK = 40 MHz	47	µs typ
Decimate by 256			
Group Delay	MCLK = 40 MHz	358	µs typ

AD7760

Parameter	Test Conditions/Comments	Specification	Unit
ANALOG INPUT			
Differential Input Voltage	$V_{IN}(+) - V_{IN}(-)$, V_{REF} = 2.5 V	±2	V p-p
	$V_{IN}(+) - V_{IN}(-)$, V_{REF} = 4.096 V	±3.25	V p-p
Input Capacitance	At internal buffer inputs	5	pF typ
	At modulator inputs	55	pF typ
REFERENCE INPUT/OUTPUT			
V_{REF} Input Voltage	V_{DD3} = 3.3 V ± 5%	+2.5	V max
	V_{DD3} = 5 V ± 5%	+4.096	V max
V_{REF} Input DC Leakage Current		±6	µA max
V_{REF} Input Capacitance		5	pF max
POWER DISSIPATION			
Total Power Dissipation	Normal mode	958	mW max
	Low power mode	661	mW max
Standby Mode	Clock stopped	6.35	mW max
POWER REQUIREMENTS			
AV$_{DD1}$ (Modulator Supply)	±5%	+2.5	V
AV$_{DD2}$ (General Supply)	±5%	+5	V
AV$_{DD3}$ (Diff Amp Supply)		+3.15/+5.25	V min/max
AV$_{DD4}$ (Ref Buffer Supply)		+3.15/+5.25	V min/max
DV$_{DD}$	±5%	+2.5	Volts
V$_{DRIVE}$		+1.65/+2.7	V min/max
Normal Mode			
AI$_{DD1}$ (Modulator)		49/51	mA typ/max
AI$_{DD2}$ (General)		40/42	mA typ/max
AI$_{DD4}$ (Reference Buffer)	AV$_{DD4}$ = 5 V	34/36	mA typ/max
Low Power Mode			
AI$_{DD1}$ (Modulator)		26/28	mA typ/max
AI$_{DD2}$ (General)		20/23	mA typ/max
AI$_{DD4}$ (Reference Buffer)	AV$_{DD4}$ = 5 V	9/10	mA typ/max
AI$_{DD3}$ (Diff Amp)	AV$_{DD3}$ = 5 V, both modes	41/44	mA typ/max
DI$_{DD}$	Both modes	63/70	mA typ/max
DIGITAL I/O			
MCLK Input Amplitude[3]		5	V typ
Input Capacitance		7.3	pF typ
Input Leakage Current		±5	µA max
Three-State Leakage Current (D15:D0)		±5	µA max
V$_{INH}$		$0.7 \times V_{DRIVE}$	V min
V$_{INL}$		$0.3 \times V_{DRIVE}$	V max
V$_{OH}$[4]		1.5	V min
V$_{OL}$[4]		0.1	V max

[1] See the Terminology section.
[2] SNR specifications in dBs are referred to a full-scale input, FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[3] While the AD7760 can function with an MCLK amplitude of less than 5 V, this is the recommended amplitude to achieve the performance as stated.
[4] Tested with a 400 µA load current.

TIMING SPECIFICATIONS

$AV_{DD1} = DV_{DD} = V_{DRIVE} = 2.5$ V, $AV_{DD2} = AV_{DD3} = AV_{DD4} = 5$ V, $T_A = 25°C$, normal mode, unless otherwise noted.

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{MCLK}	1	MHz min	Applied master clock frequency
	40	MHz max	
f_{ICLK}	500	kHz min	Internal modulator clock derived from MCLK.
	20	MHz max	
t_1[1, 2]	$0.5 \times t_{ICLK}$	typ	$\overline{DRDY}$ pulse width
t_2	10	ns min	$\overline{DRDY}$ falling edge to $\overline{CS}$ falling edge
t_3	3	ns min	$\overline{RD}/\overline{WR}$ setup time to $\overline{CS}$ falling edge
t_4	$(0.5 \times t_{ICLK}) + 16$ ns	max	Data access time
t_5	t_{ICLK}	min	$\overline{CS}$ low read pulse width
t_6	t_{ICLK}	min	$\overline{CS}$ high pulse width between reads
t_7	3	ns min	$\overline{RD}/\overline{WR}$ hold time to $\overline{CS}$ rising edge
t_8	11	ns max	Bus relinquish time
t_9[2]	$0.5 \times t_{ICLK}$	typ	$\overline{DRDY}$ high period
t_{10}[2]	$0.5 \times t_{ICLK}$	typ	$\overline{DRDY}$ low period
t_{11}	$(0.5 \times t_{ICLK}) + 16$ ns	max	Data access time
t_{12}	3.5	ns min	Data invalid prior to $\overline{DRDY}$ falling edge
t_{13}	5	ns min	Data invalid after $\overline{DRDY}$ falling edge
t_{14}	11	ns max	Bus relinquish time
t_{15}	$4 \times t_{ICLK}$	min	$\overline{CS}$ low write pulse width
t_{16}	$4 \times t_{ICLK}$	min	$\overline{CS}$ high period between address and data
t_{17}	5	ns min	Data setup time
t_{18}	0	ns min	Data hold time

[1] $t_{ICLK} = 1/f_{ICLK}$.
[2] When ICLK = MCLK, $\overline{DRDY}$ pulse width depends on the mark/space ratio of applied MCLK.
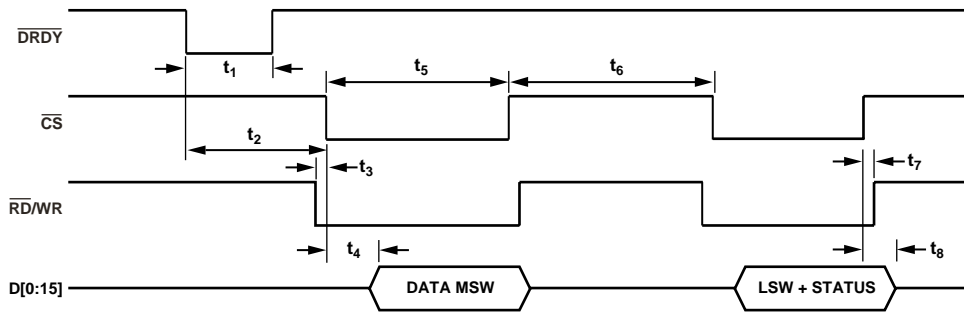
AD7760

TIMING DIAGRAMS
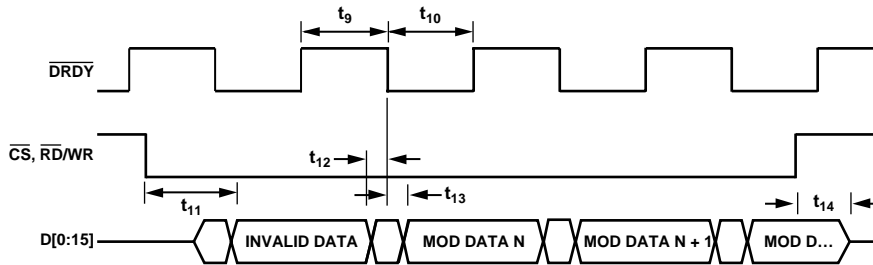

Figure 2. Parallel Interface Timing Diagram
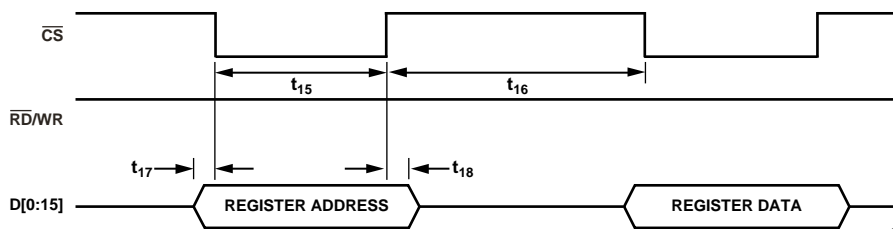

Figure 3. 20 MHz Modulator Data Output Mode

Figure 4. AD7760 Register Write

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameters	Rating
AV_{DD1} to GND	−0.3 V to +3 V
AV_{DD2}–AV_{DD4} to GND	−0.3 V to +6 V
DV_{DD} to GND	−0.3 V to +3 V
V_{DRIVE} to GND	−0.3 V to +3 V
V_{IN+}, $V_{IN−}$ to GND	−0.3 V to +6 V
Digital Input Voltage to GND[1]	−0.3 V to DV_{DD} + 0.3 V
MCLK to MCLKGND	−0.3 V to +6 V
V_{REF} to GND[2]	−0.3 V to AV_{DD4} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies[3]	±10 mA
Operating Temperature Range	
Commercial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TQFP Exposed Paddle Package	
θ_{JA} Thermal Impedance	92.7°C/W
θ_{JC} Thermal Impedance	5.1°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	600 V

[1] Absolute maximum voltage on digital inputs is 3.0 V or DV_{DD} + 0.3 V, whichever is lower.
[2] Absolute maximum voltage on V_{REF} input is 6.0 V or AV_{DD4} + 0.3 V, whichever is lower.
[3] Transient currents of up to 200 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
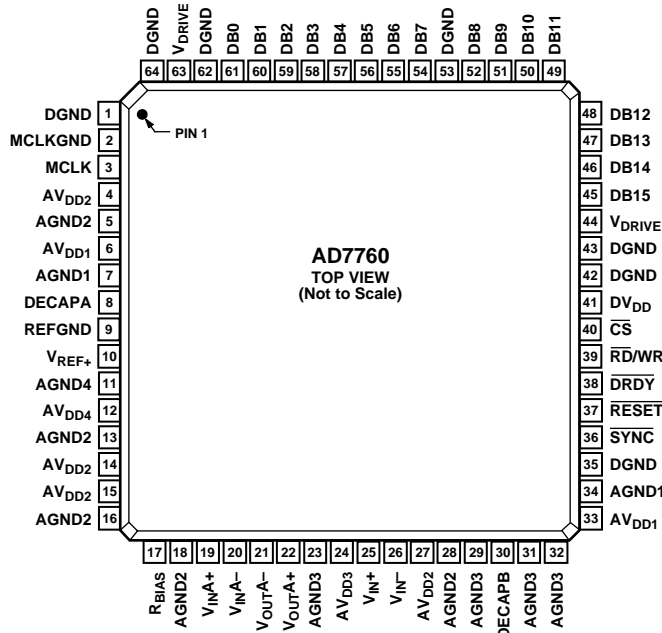
PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

Figure 5. 64-Lead TQFP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
6, 33	AV_{DD1}	2.5 V Power Supply for Modulator. These pins should be decoupled to AGND1 with 100 nF and 10 µF capacitors on each pin.
4, 14, 15, 27	AV_{DD2}	5 V Power Supply. These pins should be decoupled to AGND2 with 100 nF capacitors on each of Pin 4, Pin 14, and Pin 15. Pin 27 should be connected to Pin 14 via a 15 nH inductor.
24	AV_{DD3}	3.3 V to 5 V Power Supply for Differential Amplifier. These pins should be decoupled to AGND3 with a 100 nF capacitor.
12	AV_{DD4}	3.3 V to 5 V Power Supply for Reference Buffer. This pin should be decoupled to AGND4 with a 10 nF capacitor in series with a 10 Ω resistor.
7, 34	AGND1	Power Supply Ground for Analog Circuitry Powered by AV_{DD1}.
5, 13, 16, 18, 28	AGND2	Power Supply Ground for Analog Circuitry Powered by AV_{DD2}.
23, 29, 31, 32	AGND3	Power Supply Ground for Analog Circuitry Powered by AV_{DD3}.
11	AGND4	Power Supply Ground for Analog Circuitry Powered by AV_{DD4}.
9	REFGND	Reference Ground. Ground connection for the reference voltage.
41	DV_{DD}	2.5 V Power Supply for Digital Circuitry and FIR Filter. This pin should be decoupled to DGND with a 100 nF capacitor.
44, 63	V_{DRIVE}	Logic Power Supply Input, 1.8 V to 2.5 V. The voltage supplied at these pins determines the operating voltage of the logic interface. Both of these pins must be connected together and tied to the same supply. Each pin should also be decoupled to DGND with a100 nF capacitor.
1, 35, 42, 43, 53, 62, 64	DGND	Ground Reference for Digital Circuitry.
19	$V_{IN}A+$	Positive Input to Differential Amplifier.
20	$V_{IN}A-$	Negative Input to Differential Amplifier.
21	$V_{OUT}A-$	Negative Output from Differential Amplifier.
22	$V_{OUT}A+$	Positive Output from Differential Amplifier.
25	$V_{IN}+$	Positive Input to the Modulator.
26	$V_{IN}-$	Negative Input to the Modulator.
10	V_{REF+}	Reference Input. The input range of this pin is determined by the reference buffer supply voltage (AV_{DD4}). See the Reference Voltage Filtering section for more details.
8	DECAPA	Decoupling Pin. A 100 nF capacitor must be inserted between this pin and AGND.

Pin No.	Mnemonic	Description
30	DECAPB	Decoupling Pin. A 33 pF capacitor must be inserted between this pin and AGND3.
17	R_{BIAS}	Bias Current Setting Pin. A resistor must be inserted between this pin and AGND. For more details, see the Bias Resistor Selection section.
45 to 52, 54 to 61	DB15 to DB8 DB7 to DB0	16-Bit Bidirectional Data Bus. These are three-state pins that are controlled by the $\overline{CS}$ pin and the $\overline{RD}$/WR pin. The operating voltage for these pins is determined by the V_{DRIVE} voltage. See the AD7760 Interface section for more details.
37	$\overline{RESET}$	A falling edge on this pin resets all internal digital circuitry and powers down the part. Holding this pin low keeps the AD7760 in a reset state.
3	MCLK	Master Clock Input. A low jitter digital clock must be applied to this pin. The output data rate depends on the frequency of this clock. See the section Clocking the AD7760 for more details.
2	MCLKGND	Master Clock Ground Sensing Pin.
36	$\overline{SYNC}$	Synchronization Input. A falling edge on this pin resets the internal filter. This can be used to synchronize multiple devices in a system.
39	$\overline{RD}$/WR	Read/Write Input. This pin, in conjunction with the chip select pin, is used to read and write data to and from the AD7760. If this pin is low when $\overline{CS}$ is low, a read takes place. If this pin is high and $\overline{CS}$ is low, a write occurs. See the AD7760 Interface section for more details.
38	$\overline{DRDY}$	Data Ready Output. Each time that new conversion data is available, an active low pulse, ½ ICLK period wide, is produced on this pin. See the AD7760 Interface section for more details.
40	$\overline{CS}$	Chip Select Input. Used in conjunction with the $\overline{RD}$/WR pin to read and write data to and from the AD7760. See the AD7760 Interface section for more details.

TERMINOLOGY

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7760, it is defined as

$$THD(\text{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Nonharmonic Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component, excluding harmonics.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7760 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used.

In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dB.

Integral Nonlinearity (INL)
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1-LSB change between any two adjacent codes in the ADC.

Zero Error
The zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Zero Error Drift
The change in the actual zero error value due to a temperature change of 1°C. It is expressed as a percentage of the zero error at room temperature.

Gain Error
The first transition (from 100…000 to 100…001) should occur for an analog voltage 1/2 LSB above the nominal negative full scale. The last transition (from 011…110 to 011…111) should occur for an analog voltage 1 1/2 LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition, from the difference between the ideal levels.

Gain Error Drift
The change in the actual gain error value due to a temperature change of 1°C. It is expressed as a percentage of the gain error at room temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

$AV_{DD1} = DV_{DD} = V_{DRIVE} = 2.5$ V, $AV_{DD2} = AV_{DD3} = AV_{DD4} = 5$ V, $V_{REF} = 4.096$ V, $T_A = 25°C$, normal mode, unless otherwise noted. All FFTs are generated from 65536 samples using a 7-term Blackman-Harris window.
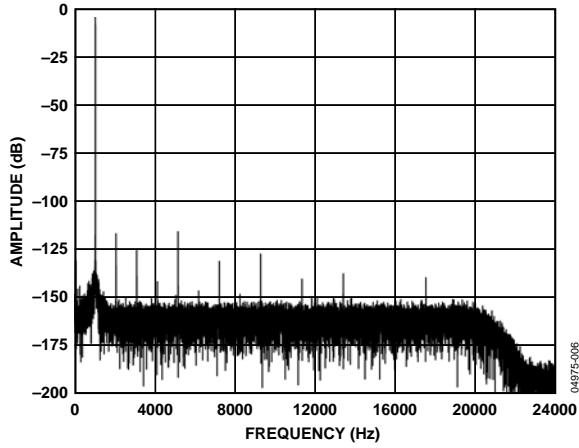

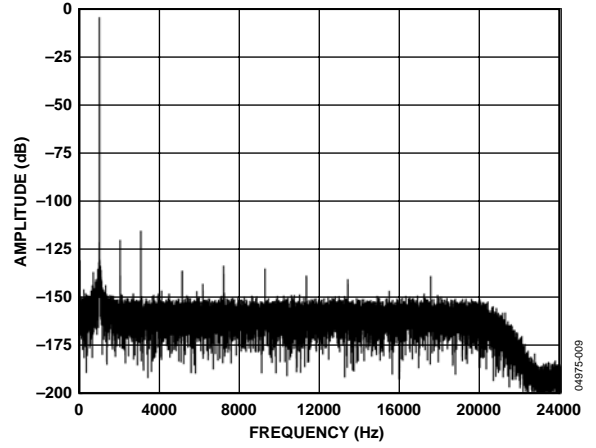*Figure 6. Normal Mode FFT, 1 kHz, −0.5 dB Input Tone, 256× Decimation*

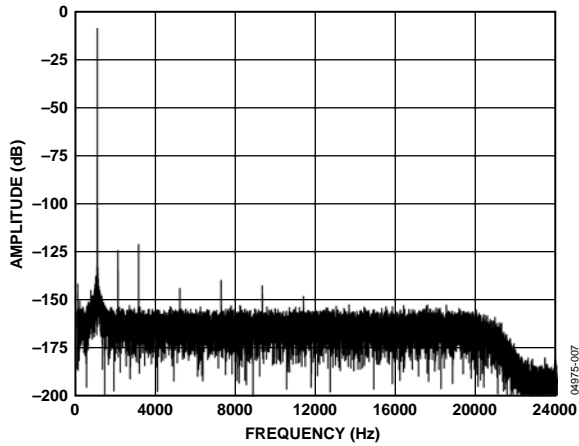*Figure 9. Low Power FFT, 1 kHz, −0.5 dB Input Tone, 256× Decimation*
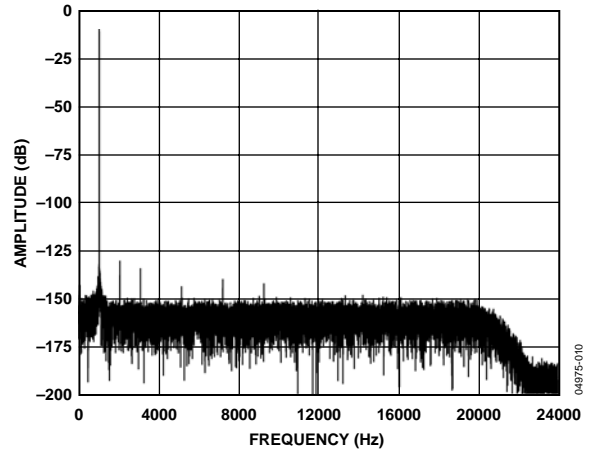

Figure 7. Normal Mode FFT, 1 kHz, −6 dB Input Tone, 256× Decimation

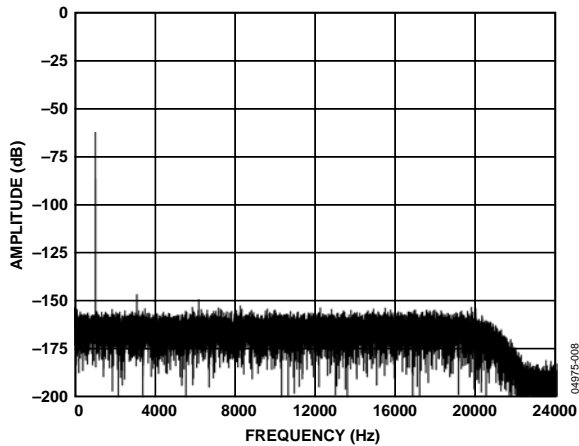*Figure 10. Low Power FFT, 1 kHz, −6 dB Input Tone, 256× Decimation*

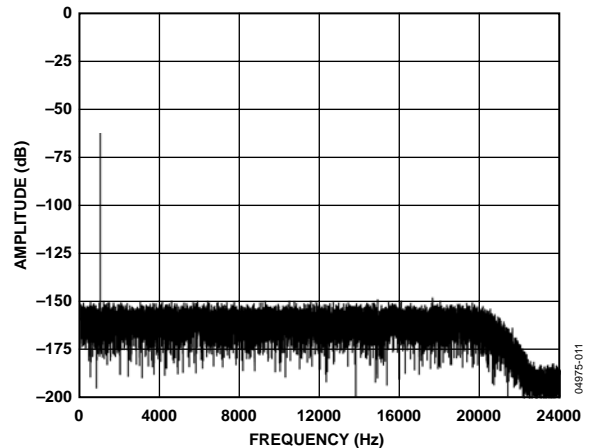*Figure 8. Normal Mode FFT, 1 kHz, −60 dB Input Tone, 256× Decimation*

Figure 11. Low Power FFT, 1 kHz, −60 dB Input Tone, 256× Decimation
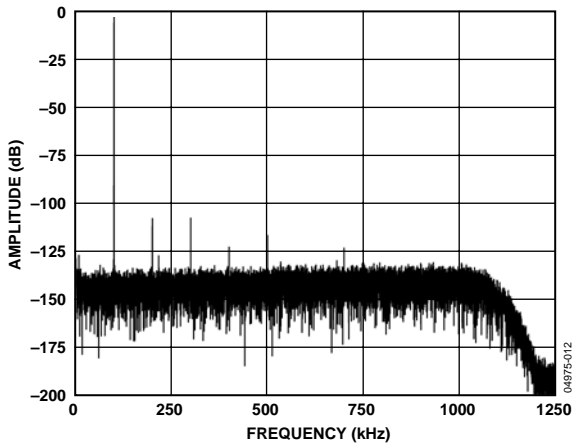
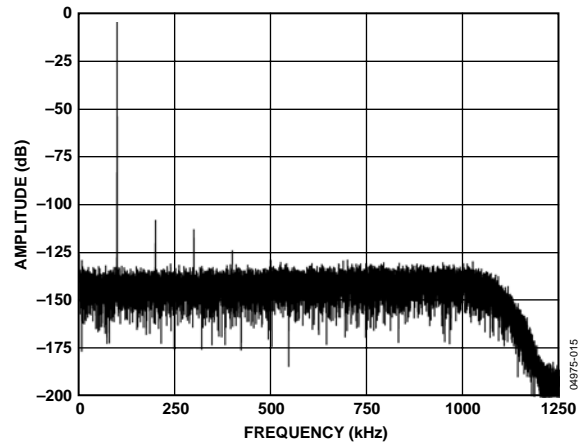Figure 12. Normal Mode FFT, 100 kHz, −0.5 dB Input Tone, 8× Decimation

Figure 15. Low Power FFT, 100 kHz, −0.5 dB Input Tone, 8× Decimation
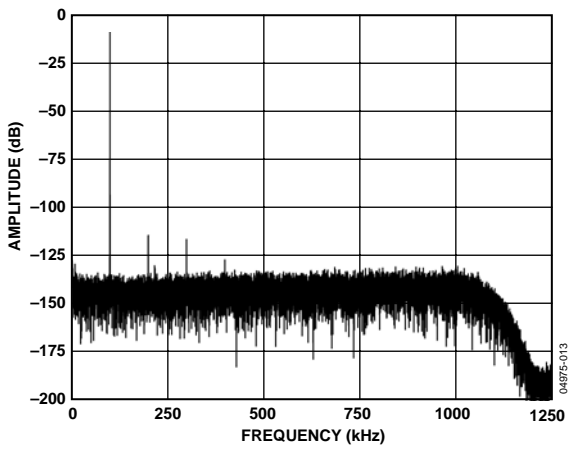

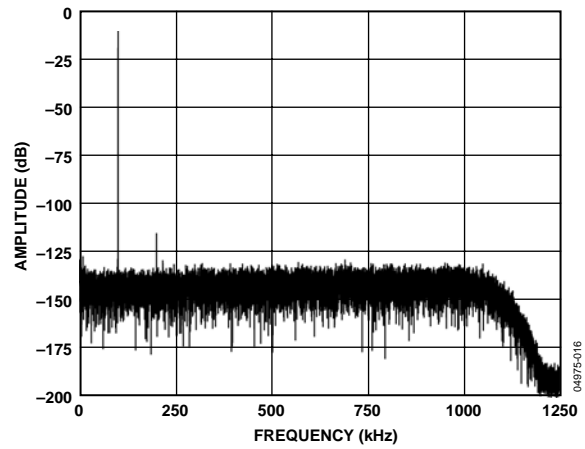Figure 13. Normal Mode FFT, 100 kHz, −6 dB Input Tone, 8× Decimation

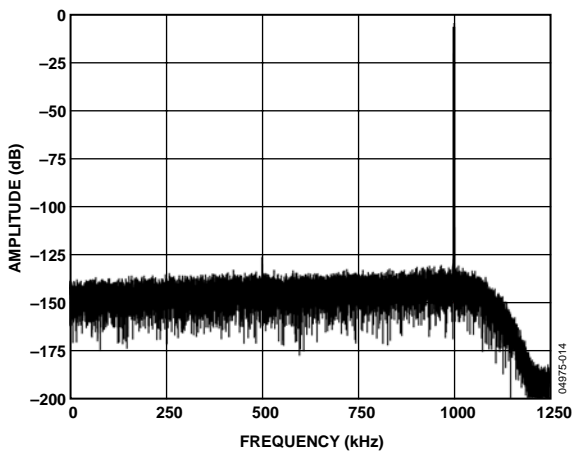Figure 16. Low Power FFT, 100 kHz, −6 dB Input Tone, 8× Decimation

Figure 14. Normal Mode FFT, 1 MHz, −0.5 dB Input Tone, 8× Decimation
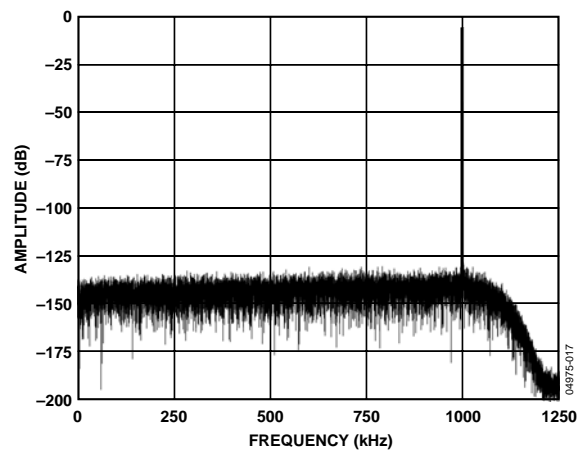

Figure 17. Low Power FFT, 1 MHz, −0.5 dB Input Tone, 8× Decimation
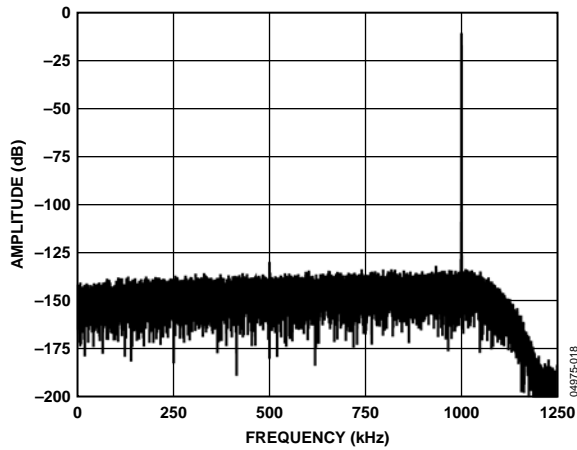
Figure 18. Normal Mode FFT, 1 MHz, −6 dB Input Tone, 8× Decimation
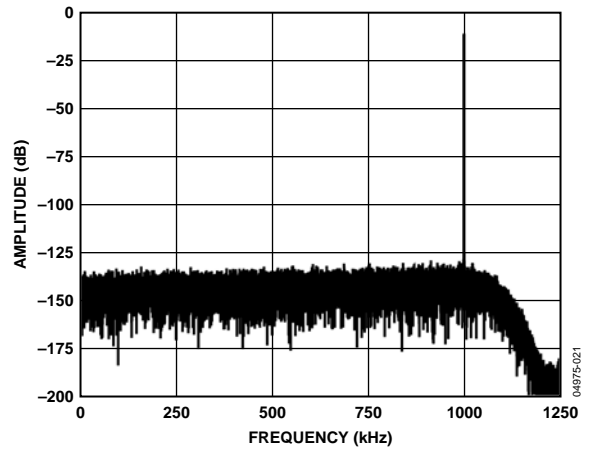
Figure 21. Low Power FFT, 1 MHz, −6 dB Input Tone, 8× Decimation

TONE A: 999.75kHz
TONE B: 1.00025MHz
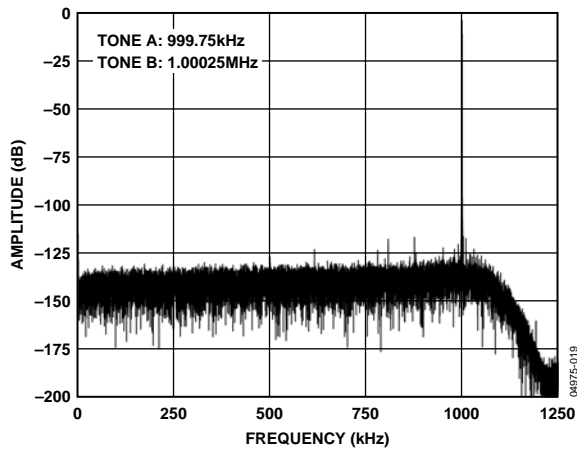
Figure 19. Normal Mode IMD, 1 MHz Center Frequency, 8× Decimation

TONE A: 999.75kHz
TONE B: 1.00025MHz
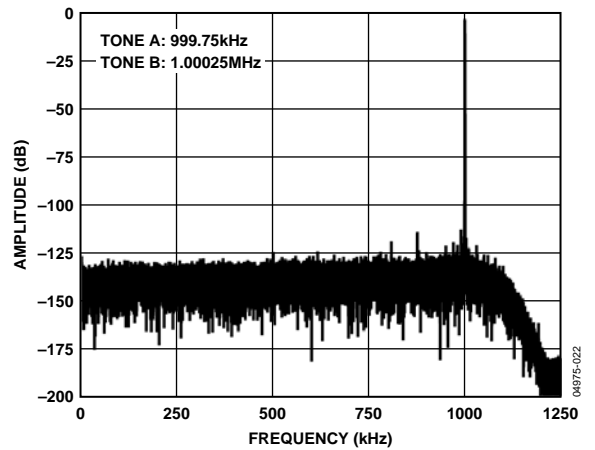
Figure 22. Low Power IMD, 1 MHz Center Frequency, 8× Decimation

TONE A: 999.75kHz
TONE B: 1.00025MHz
2ND-ORDER IMD: −105.6dB
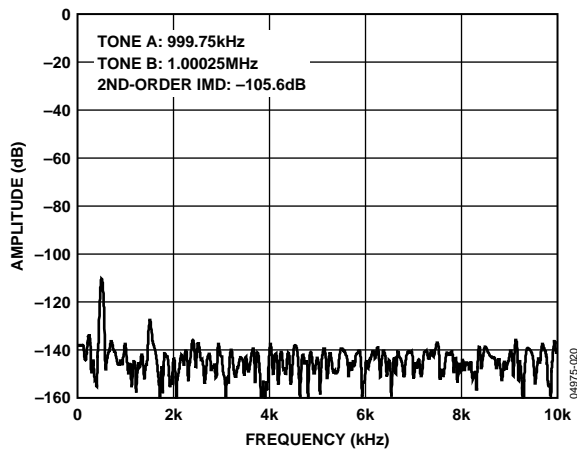
Figure 20. Normal Mode IMD, 1 MHz Center Frequency, 8× Decimation

TONE A: 999.75kHz
TONE B: 1.00025MHz
2ND-ORDER IMD: −115.7dB
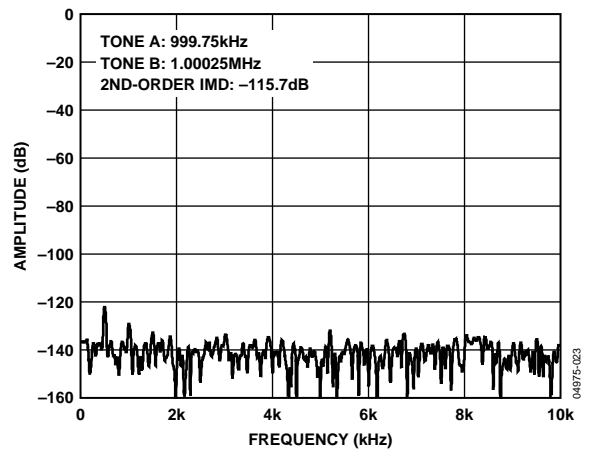
Figure 23. Low Power IMD, 1 MHz Center Frequency, 8× Decimation
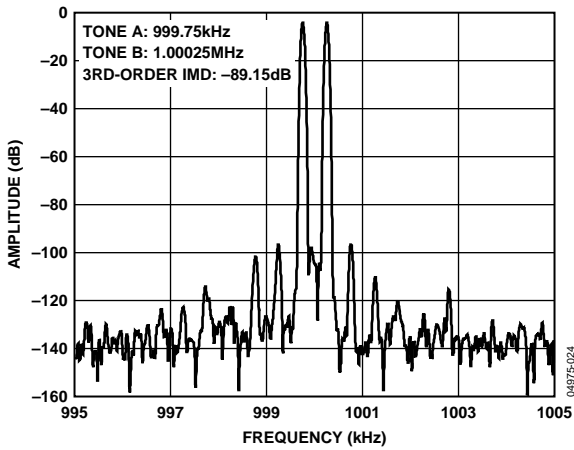
Figure 24. Normal Mode IMD, 1 MHz Center Frequency, 8× Decimation
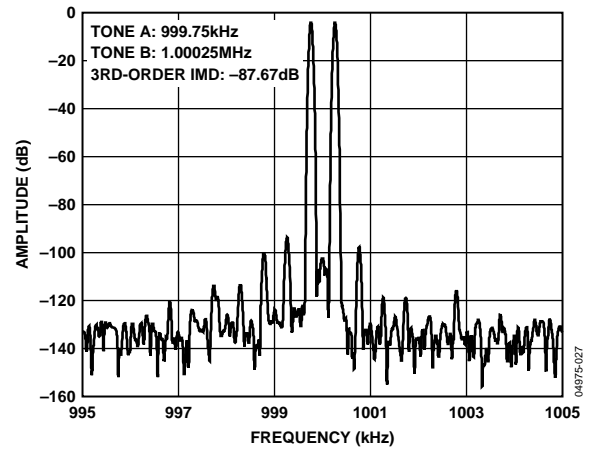
Figure 27. Normal Mode IMD, 1 MHz Center Frequency, 8× Decimation
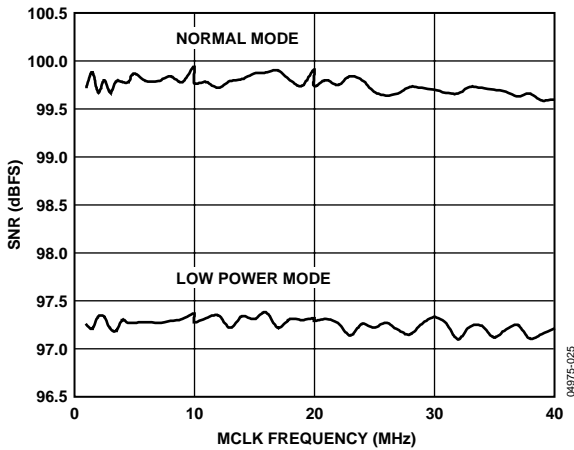
Figure 25. SNR vs. MCLK Frequency, 8× Decimation, −6 dB, 1 kHz Input Tone
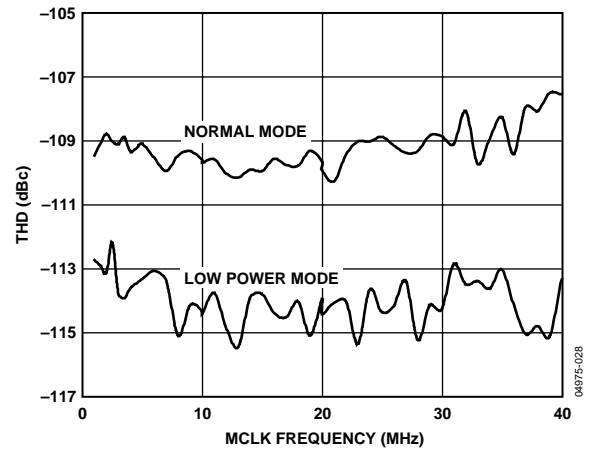
Figure 28. THD vs. MCLK Frequency, 8× Decimation, −6 dB, 1 kHz Input Tone
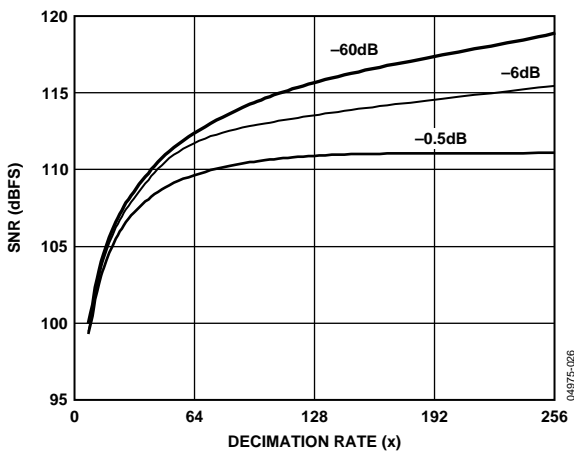
Figure 26. Normal Mode SNR vs. Decimation Rate, 1 kHz Input Tone
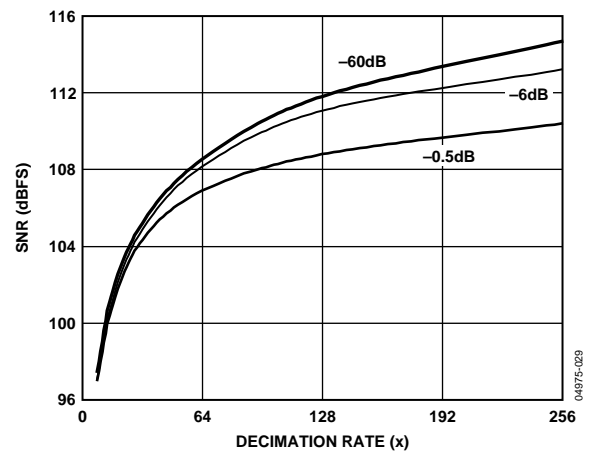
Figure 29. Low Power SNR vs. Decimation Rate, 1 kHz Input Tone
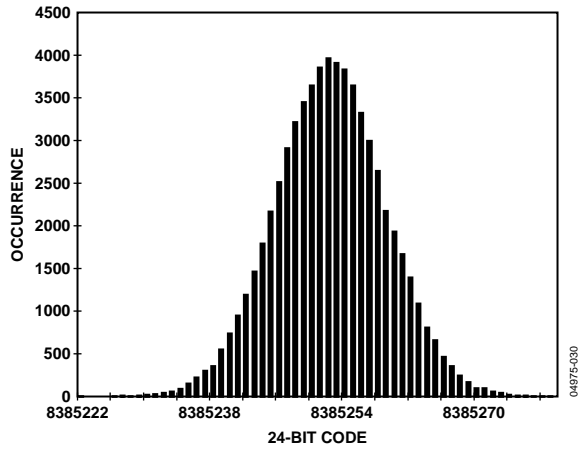
Figure 30. Normal Mode, 24-Bit Histogram, 256× Decimation

Figure 31. Normal Mode, 24-Bit Histogram, 8× Decimation

Figure 32. 24-Bit INL, Normal Mode

Figure 33. Low Power, 24-Bit Histogram, 256× Decimation

Figure 34. Low Power, 24-Bit Histogram, 8× Decimation
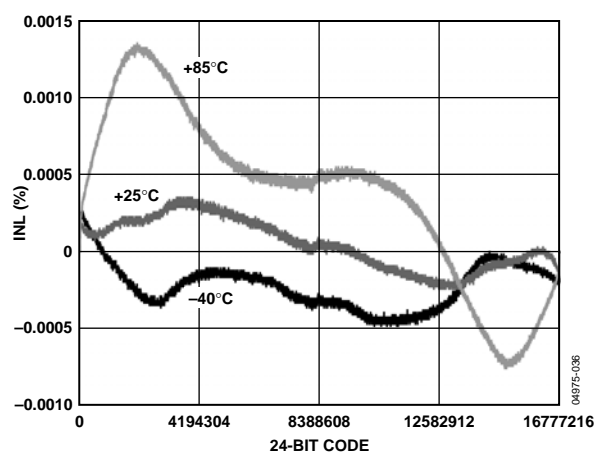
Figure 35. 24-Bit INL, Low Power Mode
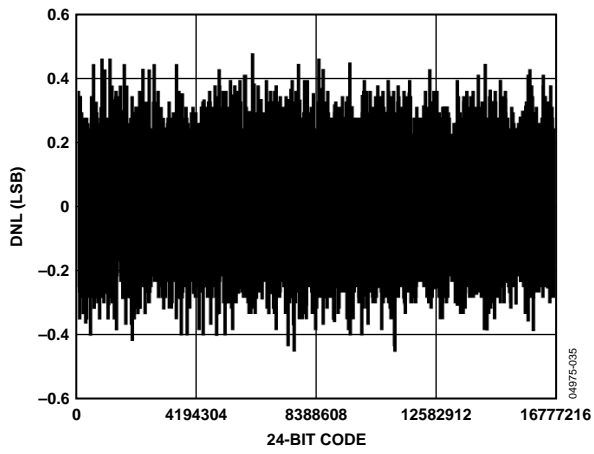
Figure 36. 24-Bit DNL

THEORY OF OPERATION

The AD7760 employs a Σ-Δ conversion technique to convert the analog input into an equivalent digital word. The modulator samples the input waveform and outputs an equivalent digital word to the digital filter at a rate equal to ICLK.

Due to the high oversampling rate, which spreads the quantization noise from 0 to f_{ICLK}, the noise energy contained in the band of interest is reduced (Figure 37 a). To further reduce the quantization noise, a high order modulator is employed to shape the noise spectrum so that most of the noise energy is shifted out of the band of interest (Figure 37 b).

The digital filtering that follows the modulator removes the large out-of-band quantization noise (Figure 37 c) while also reducing the data rate from f_{ICLK} at the input of the filter to $f_{ICLK}/8$ or less at the output of the filter, depending on the decimation rate used.

Digital filtering has certain advantages over analog filtering. It does not introduce significant noise or distortion and can be made perfectly linear phase.

The AD7760 employs three FIR filters in series. By using different combinations of decimation ratios and filter selection and bypassing, data can be obtained from the AD7760 at a large range of data rates. Multibit data from the modulator can be obtained at a rate of 20 MHz. The 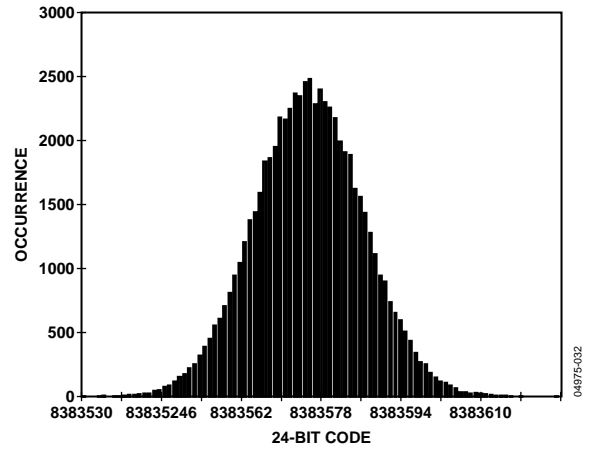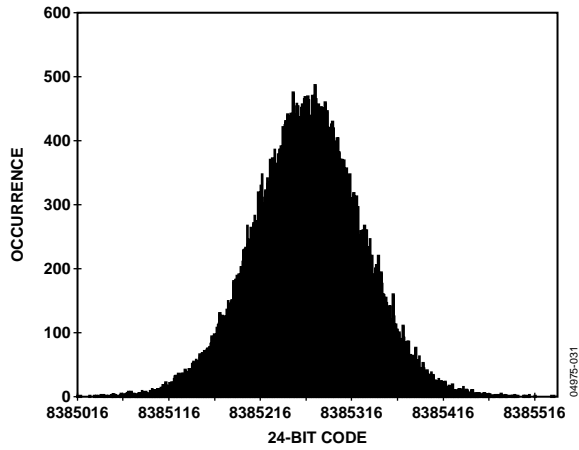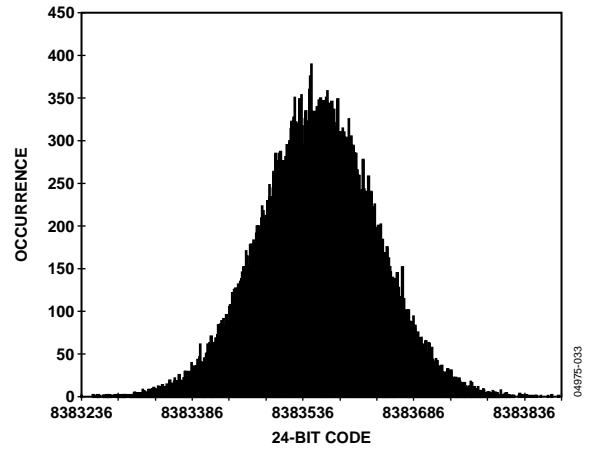first filter receives data from the modulator at 20 MHz where it is decimated by four to output data at 5 MHz. This partially filtered data can also be output at this stage. The second filter allows the decimation

rate to be chosen from 2× to 32× or to be completely bypassed. The third filter has a fixed decimation rate of 2×, is user-programmable, and has a default configuration. It is described in detail in the Programmable FIR Filter section. This filter can also be bypassed.

Table 6 shows some characteristics of the default filter. The group delay of the filter is defined to be the delay to the center of the impulse response and is equal to the computation + filter delays. The delay until valid data is available (the DVALID status bit is set) is equal to 2× the filter delay + the computation delay.
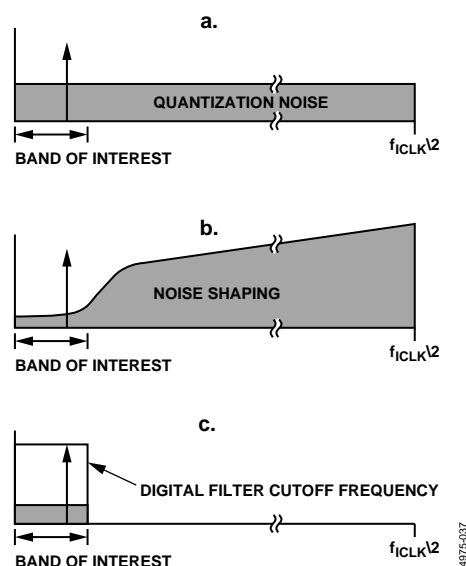
Figure 37. Σ-Δ ADC

Table 6. Configuration with Default Filter

ICLK Frequency	Filter 1	Filter 2	Filter 3	Data State	Computation Delay	Filter Delay	Pass-Band Bandwidth	Output Data Rate (ODR)
20 MHz	Bypassed	Bypassed	Bypassed	Unfiltered	0	0	(10 MHz)	20 MHz
20 MHz	4×	Bypassed	Bypassed	Partially filtered	0.325 µs	1.2 µs	1.35 MHz	5 MHz
20 MHz	4×	Bypassed	2×	Fully filtered	1.075 µs	10.8 µs	1 MHz	2.5 MHz
20 MHz	4×	2×	Bypassed	Partially filtered	1.35 µs	3.6 µs	562.5 kHz	2.5 MHz
20 MHz	4×	2×	2×	Fully filtered	1.625 µs	22.8 µs	500 kHz	1.25 MHz
20 MHz	4×	4×	Bypassed	Partially filtered	1.725 µs	6 µs	281.25 kHz	1.25 MHz
20 MHz	4×	4×	2×	Fully filtered	1.775 µs	44.4 µs	250 kHz	625 kHz
20 MHz	4×	8x	Bypassed	Partially filtered	2.6 µs	10.8 µs	140.625 kHz	625 kHz
20 MHz	4×	8×	2×	Fully filtered	2.25 µs	87.6 µs	125 kHz	312.5 kHz
20 MHz	4×	16×	Bypassed	Partially filtered	4.175 µs	20.4 µs	70.3125 kHz	312.5 kHz
20 MHz	4×	16×	2×	Fully filtered	3.1 µs	174 µs	62.5 kHz	156.25 kHz
20 MHz	4×	32×	Bypassed	Partially filtered	7.325 µs	39.6 µs	35.156 kHz	156.25 kHz
20 MHz	4×	32×	2×	Fully filtered	4.65 µs	346.8 µs	31.25 kHz	78.125 kHz
12.288 MHz	4×	8×	2×	Fully filtered	3.66 µs	142.6 µs	76.8 kHz	192 kHz
12.288 MHz	4×	16×	2×	Fully filtered	5.05 µs	283.2 µs	38.4 kHz	96 kHz
12.288 MHz	4×	32×	Bypassed	Partially filtered	11.92 µs	64.45 µs	21.6 kHz	96 kHz
12.288 MHz	4×	32×	2×	Fully filtered	7.57 µs	564.5 µs	19.2 kHz	48 kHz

AD7760 INTERFACE

READING DATA

The AD7760 uses a 16-bit bidirectional parallel interface. This interface is controlled by the $\overline{RD}/WR$ and $\overline{CS}$ pins. There are two read operating modes depending on the output data rate.

When the AD7760 is outputting data at 5 MSPS or less, the interface operates in a conventional mode, as shown in Figure 2. When a new conversion result is available, an active low pulse is output on the $\overline{DRDY}$ pin. To read a conversion result from the AD7760, two 16-bit read operations are performed. The $\overline{DRDY}$ pulse indicates that a new conversion result is available. Both $\overline{RD}/WR$ and $\overline{CS}$ go low to perform the first read operation. Shortly after both these lines go low, the data bus becomes active and the 16 most significant bits (MSBs) of the conversion result are output. The $\overline{RD}/WR$ and $\overline{CS}$ lines must return high for a full ICLK period before the second read is performed. This second read contains the 8 least significant bits (LSBs) of the conversion result along with 6 status bits. These status bits are shown in Table 7. Descriptions of the other status bits are found in Table 15.

Table 7. Status Bits During Data Read

D7							D0
DValid	Ovr	UFilt	LPwr	FiltOk	DLOk	0	0

Shortly after $\overline{RD}/WR$ and $\overline{CS}$ return high, the data bus returns to a high impedance state. Both read operations must be completed before a new conversion result is available because the new result overwrites the contents on the output register. If a $\overline{DRDY}$ pulse occurs during a read operation, the data read is invalid.

When the AD7760 is operating in modulator data output mode, that is, when the output data rate is 20 MHz, a different interfacing scheme is necessary. To obtain data from the AD7760 in this mode, both the $\overline{RD}/WR$ and $\overline{CS}$ lines must be held low. This brings the data bus out of its high impedance state. Figure 3 shows the 20 MHz output data rate operation. A $\overline{DRDY}$ pulse is generated for each word and the data is valid on the rising edge of the $\overline{DRDY}$ pulse. The $\overline{DRDY}$ pulse could be used to latch the modulator data into a FIFO or as a DMA control signal. Shortly after the $\overline{RD}/WR$ and $\overline{CS}$ lines return high, the AD7760 stops outputting data and the data bus returns to high impedance.

SHARING THE PARALLEL BUS

By its nature, the high accuracy of the AD7760 makes it sensitive to external noise sources. These include digital activity on the parallel bus. For this reason, it is recommended that the AD7760 data lines are isolated from the system data bus by means of a latch or buffer to ensure that there is no digital activity on the D0 to D15 pins that is not controlled by the AD7760. If multiple, synchronized AD7760 parts that share a properly distributed common MCLK signal exist in a system, these parts can share a common bus without being isolated from each other. This bus can then be isolated from the system bus by a single latch or buffer.

WRITING TO THE AD7760

While the AD7760 is configured to convert analog signals with the default settings on reset, there are many features and parameters that the user can change by writing to the device. Because some of the programmable registers are 16 bits wide, two write operations are required to program a register. The first write contains the register address while the second write contains the register data. An exception is when a user filter is being downloaded to the AD7760. This is described in detail in the Downloading a User-Defined Filter section. The AD7760 Registers section contains the register addresses and details.

Figure 4 shows a write operation to the AD7760. The $\overline{RD}/WR$ line is held high while the $\overline{CS}$ line is brought low for a minimum of 4 ICLK periods. The register address is latched during this period. The $\overline{CS}$ line is brought high again for a minimum of 4 ICLK periods before the register data is put onto the data bus. If a read operation occurs between the writing of the register address and the register data, the register address is cleared and the next write must be the register address again. This also provides a method to get back to a known situation if the user forgets whether the next write is an address or data.

Generally, the AD7760 is written to and configured on power-up and very infrequently, if at all, after that. Following any write operation, the full group delay of the filter must pass before valid data is output from the AD7760.

READING STATUS AND OTHER REGISTERS

The AD7760 features a number of programmable registers. To read back the contents of these registers or the status register, the user must first write to the control register of the device, setting a bit corresponding to the register to be read. The next read operation outputs the contents of the selected register instead of a conversion result. The AD7760 Registers section provides more information on the relevant bits in the control register.

CLOCKING THE AD7760

The AD7760 requires an external low jitter clock source. This signal is applied to the MCLK pin, and the MCLKGND pin is used to sense the ground from the clock source. An internal clock signal (ICLK) is derived from the MCLK input signal. The ICLK controls all internal operations of the AD7760. The maximum ICLK frequency is 20 MHz, but due to an internal clock divider, a range of MCLK frequencies can be used. There are two ways to generate the ICLK:

$$ICLK = MCLK \ (\overline{CDIV} = 1)$$

$$ICLK = MCLK/2 \ (\overline{CDIV} = 0)$$

These options are selected from the control register. (See the AD7760 Registers section for more details.) On power-up, the default is ICLK = MCLK/2 to ensure that the part can handle the maximum MCLK frequency of 40 MHz. For output data rates equal to those used in audio systems, a 12.288 MHz ICLK frequency can be used. As shown in Table 6, output data rates of 192 kHz, 96 kHz, and 48 kHz are achievable with this ICLK frequency. As mentioned previously, this ICLK frequency can be derived from different MCLK frequencies.

The MCLK jitter requirements depend on a number of factors and are given by

$$t_{j(rms)} = \frac{\sqrt{OSR}}{2 \times \pi \times f_{IN} \times 10^{\frac{SNR(dB)}{20}}}$$

where:

OSR = Over-sampling ratio = $\dfrac{f_{ICLK}}{ODR}$

f_{IN} = Maximum input frequency

SNR(dB) = Target SNR

EXAMPLE 1

This example can be taken from Table 6, where:

ODR = 2.5 MHz
f_{ICLK} = 20 MHz
f_{IN} (max) = 1 MHz
SNR = 108 dB

$$t_{j(rms)} = \frac{\sqrt{8}}{2 \times \pi \times 10^6 \times 10^{5.4}} = 1.79 \ ps$$

This is the maximum allowable clock jitter for a full-scale, 1 MHz input tone with the given ICLK and output data rate.

EXAMPLE 2

Take a second example from Table 6, where:

ODR = 48 kHz
f_{ICLK} = 12.288 MHz
f_{IN} (max) = 19.2 kHz
SNR = 120 dB

$$t_{j(rms)} = \frac{\sqrt{256}}{2 \times \pi \times 19.2 \times 10^3 \times 10^6} = 133 \ ps$$

The input amplitude also has an effect on these jitter figures. If, for example, the input level was 3 dB below full-scale, the allowable jitter would be increased by a factor of √2, increasing the first example to 2.53 ps rms. This happens when the maximum slew rate is decreased by a reduction in amplitude. Figure 38 and Figure 39 illustrate this point, showing the maximum slew rate of a sine wave of the same frequency but with different amplitudes.
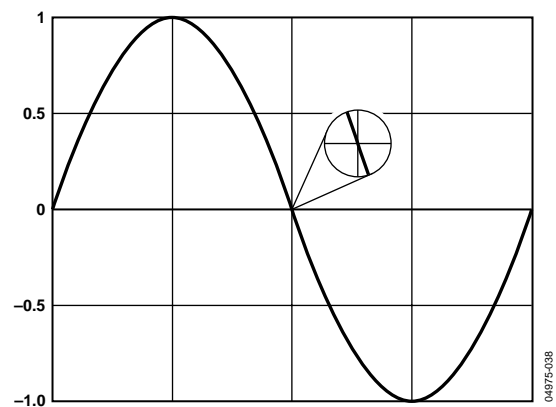
Figure 38. Maximum Slew Rate of Sine Wave with Amplitude of 2 V p-p
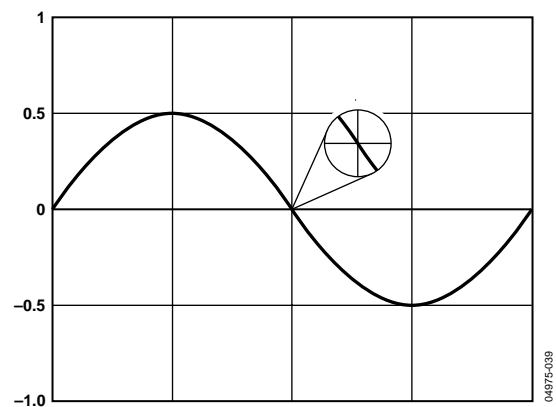
Figure 39. Maximum Slew Rate of Same Frequency Sine Wave with Amplitude of 1 V p-p

DRIVING THE AD7760

The AD7760 has an on-chip differential amplifier that operates with a supply voltage (AV$_{DD3}$) from 3.15 V to 5.25 V. For a 4.096 V reference, the supply voltage must be 5 V.

To achieve the specified performance in normal mode, the differential amplifier should be configured as a first-order antialias filter, as shown in Figure 40. Any additional filtering should be carried out in previous stages using low noise, high performance op amps, such as the AD8021.

Suitable component values for the first-order filter are listed in Table 8. Using the values in the table as an example yields a 10 dB attenuation at the first alias point of 19 MHz.
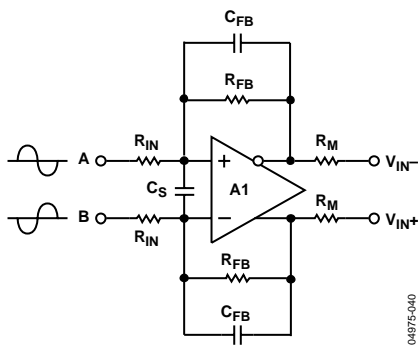
Figure 40. Differential Amplifier Configuration

Table 8. Normal Mode Component Values

V$_{REF}$	R$_{IN}$	R$_{FB}$	R$_M$	C$_S$	C$_{FB}$
4.096 V	1 kΩ	655 Ω	18 Ω	5.6 pF	33 pF

Figure 41 shows the signal conditioning that occurs using the circuit in Figure 40 with a ±2.5 V input signal biased around ground and having the component values and conditions in Table 8. The differential amplifier always biases the output signal to sit on the optimum common mode of V$_{REF}$/2, in this case 2.048 V. The signal is also scaled to give the maximum allowable voltage swing with this reference value. This is calculated as 80% of V$_{REF}$, that is, 0.8×4.096 V ≈ 3.275 V p-p on each input.

To obtain maximum performance from the AD7760, it is advisable to drive the ADC with differential signals. Figure 42 shows how a bipolar, single-ended signal biased around ground can drive the AD7760 with the use of an external op amp, such as the AD8021.

With a 4.096 V reference, a 5 V supply must be provided to the reference buffer (AV$_{DD4}$). With a 2.5 V reference, a 3.3 V supply must be provided to AV$_{DD4}$.
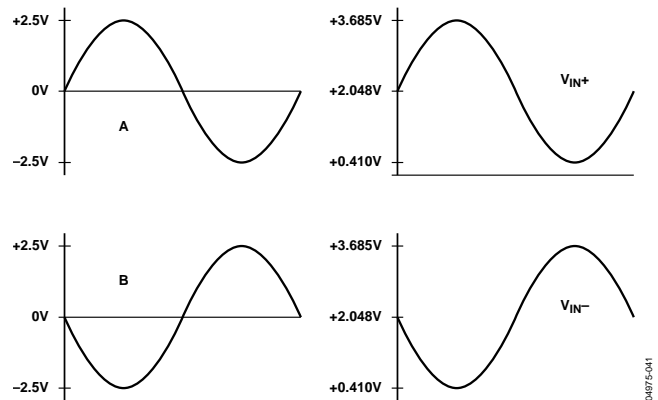
Figure 41. Differential Amplifier Signal Conditioning
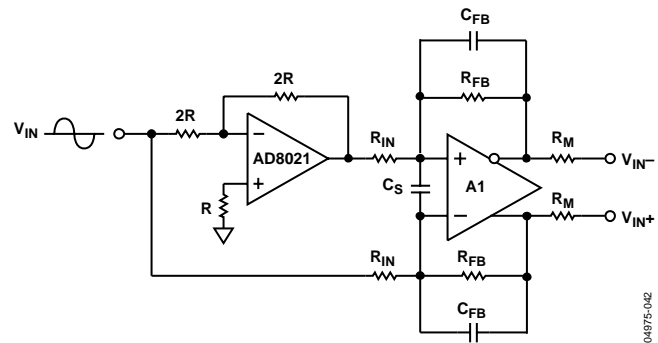
Figure 42. Single-Ended to Differential Conversion
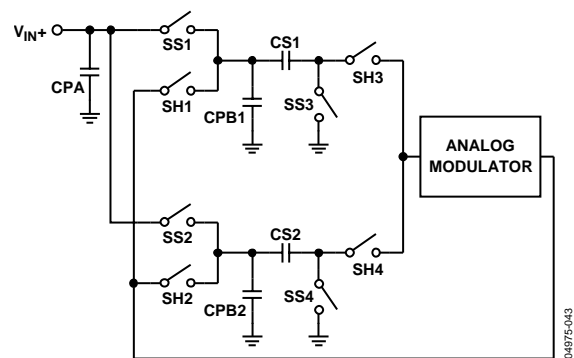
Figure 43. Equivalent Input Circuit

The AD7760 employs a double sampling front end, as shown in Figure 43. For simplicity, only the equivalent input circuit for V$_{IN}$+ is shown. The equivalent input circuitry for V$_{IN}$− is the same.

The sampling switches SS1 and SS3 are driven by $\overline{\text{ICLK}}$, whereas the sampling switches SS2 and SS4 are driven by $\overline{\text{ICLK}}$. When ICLK is high, the analog input voltage is connected to CS1. On the falling edge of ICLK, the SS1 and SS3 switches open, and the analog input is sampled on CS1. Similarly, when ICLK is low, the analog input voltage is connected to CS2. On the rising edge of ICLK, the SS2 and SS4 switches open, and the analog input is sampled on CS2.

Capacitors CPA, CPB1, and CPB2 represent parasitic capacitances that include the junction capacitances associated with the MOS switches.

Table 9. Equivalent Component Values

Mode	CS1	CS2	CPA	CPB1/2
Normal	51 pF	51 pF	12 pF	20 pF
Low Power	13 pF	13 pF	12 pF	5 pF

USING THE AD7760

The following is the recommended sequence for powering up and using the AD7760.

1. Apply power.

2. Start the clock oscillator, applying MCLK.

3. Take $\overline{\text{RESET}}$ low for a minimum of 1 MCLK cycle.

4. Wait a minimum of 2 MCLK cycles after $\overline{\text{RESET}}$ has been released.

5. Write to Control Register 2 to power up the ADC and the differential amplifier as required. The correct clock divider ($\overline{\text{CDIV}}$) ratio should be programmed at this time.

6. Write to Control Register 1 to set the output data rate.

7. Wait a minimum of 5 MCLK cycles after $\overline{\text{CS}}$ has been released.

8. Take $\overline{\text{SYNC}}$ low for a minimum of 4 MCLK cycles, if required, to synchronize multiple parts.

Data can then be read from the part using the default filter, offset, gain, and overrange threshold values. The conversion data read is not valid, however, until the group delay of the filter has passed. When this has occurred, the DVALID bit read with the data LSW is set, indicating that the data is indeed valid.

The user can then download a different filter, if required (see Downloading a User-Defined Filter). Values for gain, offset, and overrange threshold registers can be written or read at this stage.

BIAS RESISTOR SELECTION

The AD7760 requires a resistor to be connected between the R_{BIAS} pin and AGND. The value for this resistor is dependant on the reference voltage being applied to the device. The resistor value should be selected to give a current of 25 μA through the resistor to ground. For a 2.5 V reference voltage, the correct resistor value is 100 kΩ, and for a 4.096 V reference, the correct resistor value is 160 kΩ.

DECOUPLING AND LAYOUT RECOMMENDATIONS

Due to the high performance nature of the AD7760, correct decoupling and layout techniques are required to obtain the performance as stated within this datasheet. Figure 44 shows a simplified connection diagram for the AD7760.
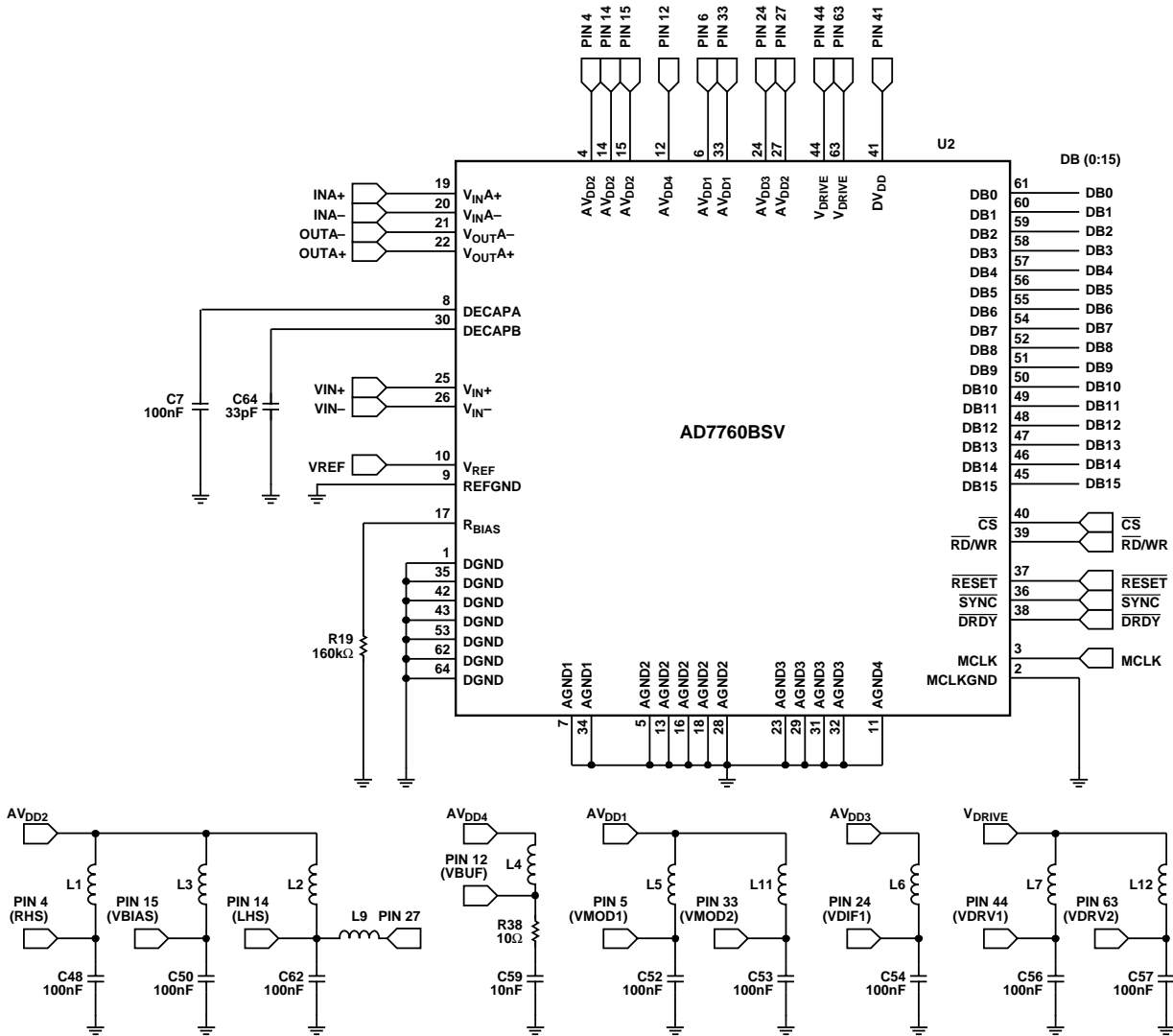

Figure 44. Simplified Connection Diagram

SUPPLY DECOUPLING

Every supply pin must be connected to the appropriate supply via a ferrite bead and decoupled to the correct ground pin with a 100 nF, 0603 case size, X7R dielectric capacitor. There are two exceptions to this:

- Pin 12 (AV_{DD4}) must have a 10 Ω resistor inserted between the pin and a 10 nF decoupling capacitor.

- Pin 27 (AV_{DD2}) does not require a separate decoupling capacitor or a direct connection to the supply, but instead is connected to Pin 14 via a 15 nH inductor.

ADDITIONAL DECOUPLING

There are two other decoupling pins on the AD7760—Pin 8 (DECAPA) and Pin 30 (DECAPB). Pin 8 should be decoupled with a 100 nF capacitor, and Pin 30 requires a 33 pF capacitor.

REFERENCE VOLTAGE FILTERING

A low noise reference source, such as the ADR431 (2.5 V) or ADR434 (4.096 V), is suitable for use with the AD7760. The reference voltage supplied to the AD7760 should be decoupled and filtered as shown in Figure 45.

The recommended scheme for the reference voltage supply is a 100 Ω series resistor connected to a 100 μF tantalum capacitor, followed by series resistor of 10 Ω, and finally a 10 nF decoupling capacitor very close to the V_{REF} pin .
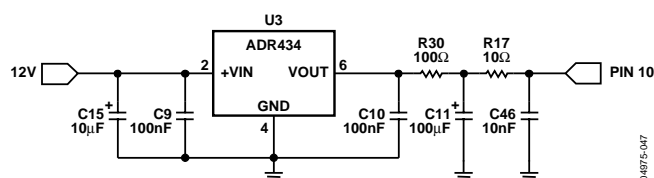
Figure 45. Reference Connection

DIFFERENTIAL AMPLIFIER COMPONENTS

The correct components for use around the on-chip differential amplifier are detailed in Table 8. Matching the components on both sides of the differential amplifier is important to minimize distortion of the signal applied to the amplifier. A tolerance of 0.1% or better is required for these components. Symmetrical routing of the tracks on both sides of the differential amplifier also assists in achieving stated performance.

LAYOUT CONSIDERATIONS

While using the correct components is essential to achieve optimum performance, the correct layout is just as important. The Design Tools section of the AD7760 product page on the Analog Devices website contains the gerber files for the AD7760 evaluation board. These files should be used as a reference when designing any system using the AD7760.

The location and orientation of some of the components mentioned in previous sections is critical, and particular attention must be paid to the components which are located close to the AD7760. Locating these components further away from the devices can have a direct impact on the maximum performance achievable.

The use of ground planes is something else which should be carefully considered. To ensure that the return currents through the decoupling capacitors are flowing to the correct ground pin, the ground side of the capacitors should be as close to the ground pin associated with that supply. A ground plane should not be relied on as the sole return path for decoupling capacitors because the return current path using ground planes is not easily predictable.

PROGRAMMABLE FIR FILTER

As previously mentioned, the third FIR filter on the AD7760 is user programmable. The default coefficients that are loaded on reset are given in Table 10 and the frequency responses are shown in Figure 46. The frequencies quoted in Figure 46 scale directly with the output data rate.

Table 10. Default Filter Coefficients

No.	Dec. Value	Hex Value	No.	Dec. Value	Hex Value
0	53656736	332BCA0	24	700847	AB1AF
1	25142688	17FA5A0	25	−70922	401150A
2	−4497814	444A196	26	-583959	408E917
3	−11935847	4B62067	27	−175934	402AF3E
4	−1313841	4140C31	28	388667	5EE3B
5	6976334	6A734E	29	294000	47C70
6	3268059	31DDDB	30	−183250	402CBD2
7	−3794610	439E6B2	31	−302597	4049E05
8	−3747402	4392E4A	32	16034	3EA2
9	1509849	1709D9	33	238315	3A2EB
10	3428088	344EF8	34	88266	158CA
11	80255	1397F	35	−143205	4022F65
12	−2672124	428C5FC	36	−128919	401F797
13	−1056628	4101F74	37	51794	CA52
14	1741563	1A92FB	38	121875	1DC13
15	1502200	16EBF8	39	16426	402A
16	−835960	40CC178	40	−90524	401619C
17	−1528400	4175250	41	−63899	400F99B
18	93626	16DBA	42	45234	B0B2
19	1269502	135EFE	43	114720	1C020
20	411245	6466D	44	102357	18FD5
21	−864038	40D2F26	45	52669	CDBD
22	−664622	40A242E	46	15559	3CC7
23	434489	6A139	47	1963	7AB

The default filter should be sufficient for almost all applications. It is a standard brick wall filter with a symmetrical impulse response. The default filter has a length of 96, in nonaliasing with 120 dB of attenuation at Nyquist. This filter not only performs signal antialiasing, but also suppresses out-of-band quantization noise produced by the analog-to-digital conversion process. Any significant relaxation in the stop-band attenuation or transition bandwidth relative to the default filter can result in a failure to meet the SNR specifications.

To create a filter, note the following:

- The filter must be even, symmetrical FIR.

- The coefficients are in sign-and-magnitude format with 26 magnitude bits and sign coded as positive=0.

- The filter length must be between 12 taps and 96 taps in steps of 12.

- Because the filter is symmetrical, the number of coefficients that must be downloaded is half the filter length. The default filter coefficients exemplify this with only 48 coefficients listed for a 96-tap filter.

- Coefficients are written from the center of impulse response (adjacent to the point of symmetry) outwards.

- The coefficients are scaled so that the in-band gain of the filter is equal to 134217726 with the coefficients rounded to the nearest integer. For a low-pass filter, this is the equivalent of having the coefficients sum arithmetically (including sign) to a +67108863 (0x3FF FFFF) positive value over the half-impulse-response coefficient set (maximum 48 coefficients). Any deviation from this introduces a gain error.
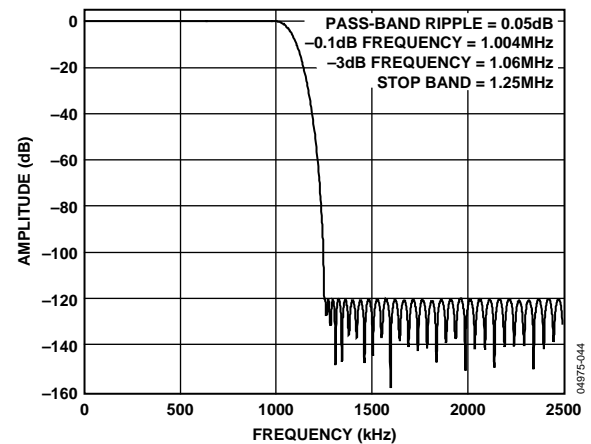

Figure 46. Default Filter Frequency Response (2.5 MHz ODR)

The procedure for downloading a user-defined filter is detailed in the Downloading a User-Defined Filter section.

DOWNLOADING A USER-DEFINED FILTER

As previously mentioned, the filter coefficients are 27 bits in length; 1 sign and 26 magnitude bits. Because the AD7760 has a 16-bit parallel bus, the coefficients are padded with 5 MSB 0s to generate a 32-bit word and split into two 16-bit words for downloading. The first 16-bit word for each coefficient becomes (00000, Sign bit, Magnitude [25:16]), while the second word becomes (Magnitude [15:0]). To ensure that a filter is downloaded correctly, a checksum must also be generated and then downloaded following the final coefficient. The checksum is a 16-bit word generated by splitting each 32-bit word into 4 bytes and summing all bytes from all coefficients up to a maximum of 192 bytes (48 coefficients × 4 bytes). The same checksum is generated internally in the AD7760 and compared with the checksum downloaded. The DL_OK bit in the status register is set if these two checksums agree.

To download a user filter:

1. Write to Control Register 1, setting the DL_Filt bit and also the correct filter length bits corresponding to the length of the filter to be downloaded (see Table 11).

2. Write the first half of the current coefficient data (00000, Sign bit, Magnitude [25:16]). The first coefficient to be written must be the one adjacent to the point of filter symmetry.

3. Write the second half of the current coefficient data (Magnitude [15:0]).

4. Repeat Step 2 and Step 3 for each coefficient.

5. Write the 16-bit checksum.

6. Use these methods to verify that the filter coefficients are downloaded correctly:

   a. Read the status register, checking the DL_OK bit.

   b. Read data and observe the status of the DL_OK bit.

Note that because the user coefficients are stored in RAM, they are cleared after a $\overline{RESET}$ operation or a loss of power.

Table 11. Filter Length Values

FLEN[3:0]	Number of Coefficients	Filter Length
0000	Default	Default
0001	6	12
0011	12	24
0101	18	36
0111	24	48
1001	30	60
1011	36	72
1101	42	84
1111	48	96

EXAMPLE FILTER DOWNLOAD

The following is an example of downloading a short user-defined filter with 24 taps. The frequency response is shown in Figure 47.
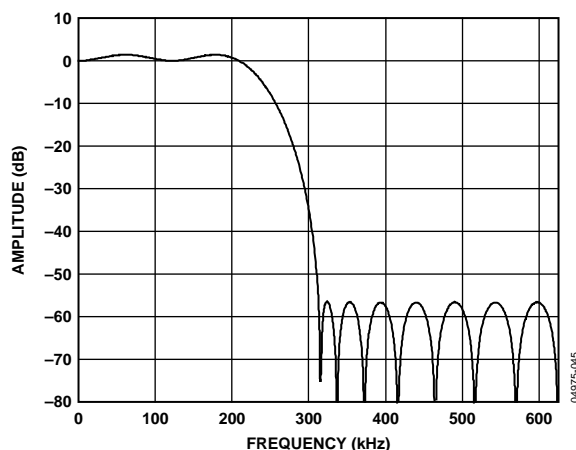
Figure 47. 24-Tap FIR Frequency Response

The coefficients for the filter are listed in Table 12 and are shown from the center of symmetry outwards. The raw coefficients were generated using a commercial filter design tool and scaled appropriately so their sum equals 67108863 (0x3FF FFFF).

Table 12. 24-Tap FIR Coefficients

Coefficient	Raw	Scaled
1	0.365481974	53188232
2	0.201339905	29300796
3	0.009636604	1402406
4	−0.075708848	−11017834
5	−0.042856209	−6236822
6	0.019944246	2902466
7	0.036437914	5302774
8	0.007592007	1104856
9	−0.021556583	−3137108
10	−0.024888355	−3621978
11	−0.012379538	−1801582
12	−0.001905756	−277343

Table 13 shows the hex values (in sign and magnitude format) that are downloaded to the AD7760 to realize this filter. The table is also split into the bytes that are all summed to produce the checksum. The checksum generated from these coefficients is 0x0E6B.

Table 13. Filter Hex Values

Coefficient	Word 1		Word 2	
	Byte 1	Byte 2	Byte 3	Byte 4
1	03	2B	96	88
2	01	BF	18	3C
3	00	15	66	26
4	04	A8	1E	6A
5	04	5F	2A	96
6	00	2C	49	C2
7	00	50	E9	F6
8	00	10	DB	D8
9	04	2F	DE	54
10	04	37	44	5A
11	04	1B	7D	6E
12	04	04	3B	5F

Table 14 lists the 16-bit words the user would write to the AD7760 to set up the ADC and download this filter, assuming an output data rate of 1.25 MHz has already been selected.

Table 14.

Word	Description
0x0001	Address of Control Register 1.
0x8079	Control register data. DL filter, set filter length = 24, set output data rate = 1.25 MHz.
0x032B	First coefficient, Word 1.
0x9688	First coefficient, Word 2.
0x01BF	Second coefficient, Word 1.
0x183C	Second coefficient, Word 2.
...	Other coefficients.
0x0404	Twelfth (final) coefficient, Word 1.
0x3B5F	Final coefficient, Word 2.
0x0E6B	Checksum. Wait (0.5 × t_{ICLK} × Number of Unused Coefficients) for AD7760 to fill remaining unused coefficients with 0s.
0x0001	Address of control register.
0x0879	Control register data. Set read status and maintain filter length and decimation settings. Read contents of status register. Check Bit 7 (DL_OK) to determine that the filter was downloaded correctly.

AD7760 REGISTERS

The AD7760 has a number of user-programmable registers. The control registers are used to set the decimation rate, the filter configuration, the clock divider, and so on. There are also digital gain, offset, and overrange threshold registers. Writing to these registers involves writing the register address first, then a 16-bit data-word. Register addresses, details of individual bits, and default values are given here.

CONTROL REGISTER 1—REG 0X0001

Default Value 0x001A

MSB															LSB
DL_ Filt	RD Ovr	RD Gain	RD Off	RD Stat	0	SYNC	FLEN3	FLEN2	FLEN1	FLEN0	$\overline{\text{BYP F3}}$	$\overline{\text{BYP F1}}$	DEC2	DEC1	DEC0

Table 15.

Bit	Mnemonic	Description
15	DL_Filt[1]	Download Filter. Before downloading a user-defined filter, this bit must be set. The Filter Length bits must also be set at this time. The write operations that follow are interpreted as the user coefficients for the FIR filter until all the coefficients and the checksum have been written.
14	RD Ovr[1, 2]	Read Overrange. If this bit has been set, the next read operation outputs the contents of the Overrange Threshold Register instead of a conversion result.
13	RD Gain[1, 2]	Read Gain. If this bit has been set, the next read operation outputs the contents of the digital gain register.
12	RD Off[1, 2]	Read Offset. If this bit has been set, the next read operation outputs the contents of the digital offset register.
11	RD Stat[1, 2]	Read Status. If this bit has been set, the next read operation outputs the contents of the status register.
10	0	0 must be written to this bit.
9	SYNC[1]	Synchronize. Setting this bit initiates an internal synchronization routine. Setting this bit simultaneously on multiple devices synchronizes all filters.
8-5	FLEN3:0	Filter Length Bits. These bits must be set when the DL Filt bit is set and before a user-defined filter is downloaded.
4	$\overline{\text{BYP F3}}$	Bypass Filter 3. If this bit is 0, Filter 3 (programmable FIR) is bypassed.
3	$\overline{\text{BYP F1}}$	Bypass Filter 1. If this bit is 0, Filter 1 is bypassed. This should only occur when the user requires unfiltered modulator data to be output.
2-0	DEC2:0	Decimation Rate. These bits set the decimation rate of Filter 2. All 0s implies that the filter is bypassed. A value of 1 corresponds to 2× decimation, a value of 2 corresponds to 4× decimation, and so on up to the maximum value of 5, corresponding to 32× decimation.

[1] Bit 15 to Bit 9 are all self-clearing bits.
[2] Only one of the bits from Bit 14 to Bit 11 can be set in any write operation because it determines the contents of the next read operation.

CONTROL REGISTER 2—ADDRESS 0X0002

Default Value 0x009B

MSB															LSB
0	0	0	0	0	0	0	0	0	0	$\overline{\text{CDIV}}$	0	PD	LPWR	1	D1PD

Table 16.

Bit	Mnemonic	Description
5	$\overline{\text{CDIV}}$	Clock Divider Bit. This sets the divide ratio of the MCLK signal to produce the internal ICLK. Setting CDIV = 0 divides the MCLK by 2. If CDIV = 1, then the ICLK frequency is equal to the MCLK.
3	PD	Power Down. Setting this bit powers down the AD7760, reducing the power consumption to 6.35 mW.
2	LPWR	Low Power. If this bit is set, the AD7760 is operating in a low power mode. The power consumption is reduced for a 6 dB reduction in noise performance.
1	1	Write 1 to this bit.
0	D1PD	Differential Amplifier Power Down. Setting this bit powers down the on-chip differential amplifier.

AD7760

STATUS REGISTER (READ ONLY)

MSB															LSB
PART 1	PART 0	DIE 2	DIE 1	DIE 0	DVALID	LPWR	OVR	DL_OK	Filter OK	U Filter	$\overline{\text{BYP F3}}$	$\overline{\text{BYP F1}}$	DEC2	DEC1	DEC0

Table 17.

Bit	Mnemonic	Comment
15, 14	PART1:0	Part Number. These bits are constant for the AD7760.
13 to 11	DIE2:0	Die Number. These bits reflect the current AD7760 die number for identification purposes within a system.
10	DVALID	Data Valid. This bit corresponds to the DVALID bit in the status word output in the second 16-bit read operation.
9	LPWR	Low Power. If the AD7760 is operating in low power mode, this bit is set to 1.
8	OVR	If the current analog input exceeds the current overrange threshold, this bit is set.
7	DL_OK	When downloading a user filter to the AD7760, a checksum is generated. This checksum is compared to the one downloaded following the coefficients. If these checksums agree, this bit is set.
6	Filter OK	When a user-defined filter is in use, a checksum is generated when the filter coefficients pass through the filter. This generated checksum is compared to the one downloaded. If they match, this bit is set.
5	U Filter	If a user-defined filter is in use, this bit is set.
4	$\overline{\text{BYP F3}}$	Bypass Filter 3. If Filter 3 is bypassed by setting the relevant bit in Control Register 1, this bit is also set.
3	$\overline{\text{BYP F1}}$	Bypass Filter 1. If Filter 1 is bypassed by setting the relevant bit in Control Register 1, this bit is also set.
2-0	DEC2:0	Decimation Rate. These correspond to the bits set in Control Register 1.

OFFSET REGISTER—ADDRESS 0X0003

Non-bitmapped, Default Value 0x0000

The offset register uses twos complement notation and is scaled such that 0x7FFF (maximum positive value) and 0x8000 (maximum negative value) correspond to an offset of +0.78125% and −0.78125%, respectively. Offset correction is applied after any gain correction. Using the default gain value of 1.25 and assuming a reference voltage of 4.096V, the offset correction range is approximately ±25 mV.

GAIN REGISTER—ADDRESS 0X0004

### Non-bitmapped, Default Value 0xA000

The gain register is scaled such that 0x8000 corresponds to a gain of 1.0. The default value of this register is 1.25 (0xA000). This gives a full-scale digital output when the input is at 80% of V_{REF}. This ties in with the maximum analog input range of ±80% of V_{REF} p-p.

OVERRANGE REGISTER—ADDRESS 0X0005

Non-bitmapped, Default Value 0xCCCC

The overrange register value is compared with the output of the first decimation filter to obtain an overload indication with minimum propagation delay. This is prior to any gain scaling or offset adjustment. The default value is 0xCCCC which corresponds to 80% of V_{REF} (the maximum permitted analog input voltage). Assuming V_{REF} = 4.096 V, the bit is then set when the input voltage exceeds approximately 6.55 V p-p differential. Note that the overrange bit is also set immediately if the analog input voltage exceeds 100% of V_{REF} for more than four consecutive samples at the modulator rate.

OUTLINE DIMENSIONS
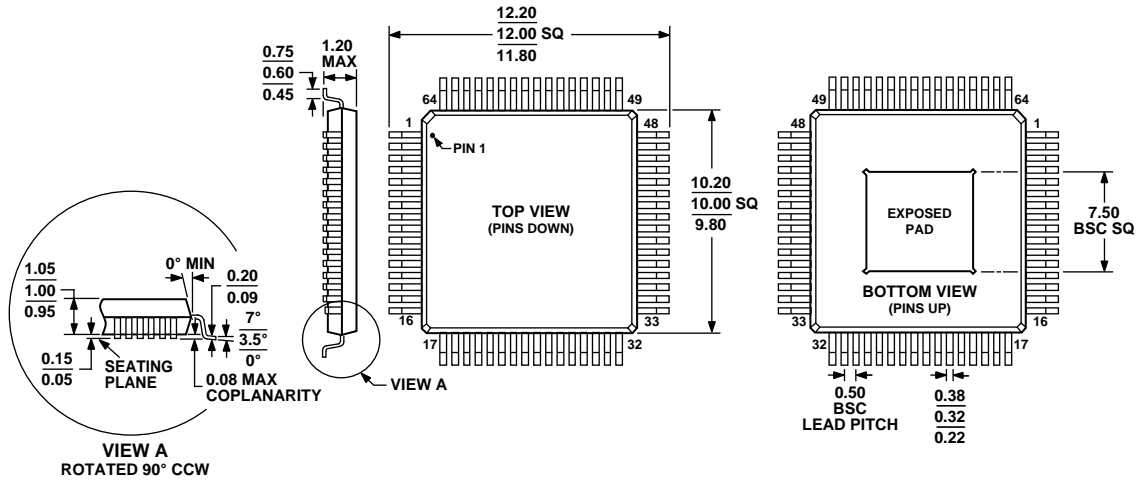
Figure 48. 64-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-64-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7760BSVZ[1]	−40°C to +85°C	64-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-64-4
AD7760BSVZ-REEL[1]	−40°C to +85°C	64-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-64-4
EVAL-AD7760EB		Evaluation Board	

[1] Z = Pb-free part.

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