Low Noise, Low Power, SPI® Bus, 256 Taps

The ISL22424 integrates two digitally controlled potentiometers (DCP), control logic and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wiper is controlled by the user through the SPI serial interface. Each potentiometer has an associated volatile Wiper Register (WRi) and a non-volatile Initial Value Register (IVRi) that can be directly written to and read by the user. The contents of the WRi control the position of the wiper. At power-up the device recalls the contents of the DCP's IVRi to the corresponding WRi.

The ISL22424 also has 13 General Purpose non-volatile registers that can be used as storage of lookup table for multiple wiper position or any other valuable information.

The ISL22424 features a dual supply, that is beneficial for applications requiring a bipolar range for DCP terminals between V- and V_{CC}.

Each DCP can be used as three-terminal potentiometer or as two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- Two potentiometers in one package
- 256 resistor taps
- SPI serial interface with write/read capability
- Daisy Chain Configuration
- Shutdown mode
- Non-volatile EEPROM storage of wiper position
- 13 General Purpose non-volatile registers
- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ T ≤ +55°C
- Wiper resistance: 70Ω typical @ 1mA
- Standby current <4µA max
- Shutdown current <4µA max
- Dual power supply
  - V_{CC} = 2.25V to 5.5V
  - V- = -2.25V to -5.5V
- 10kΩ, 50kΩ or 100kΩ total resistance
- Extended industrial temperature range: -40ºC to +125ºC
- 14 Ld TSSOP or 16 Ld QFN
- Pb-free plus anneal product (RoHS compliant)

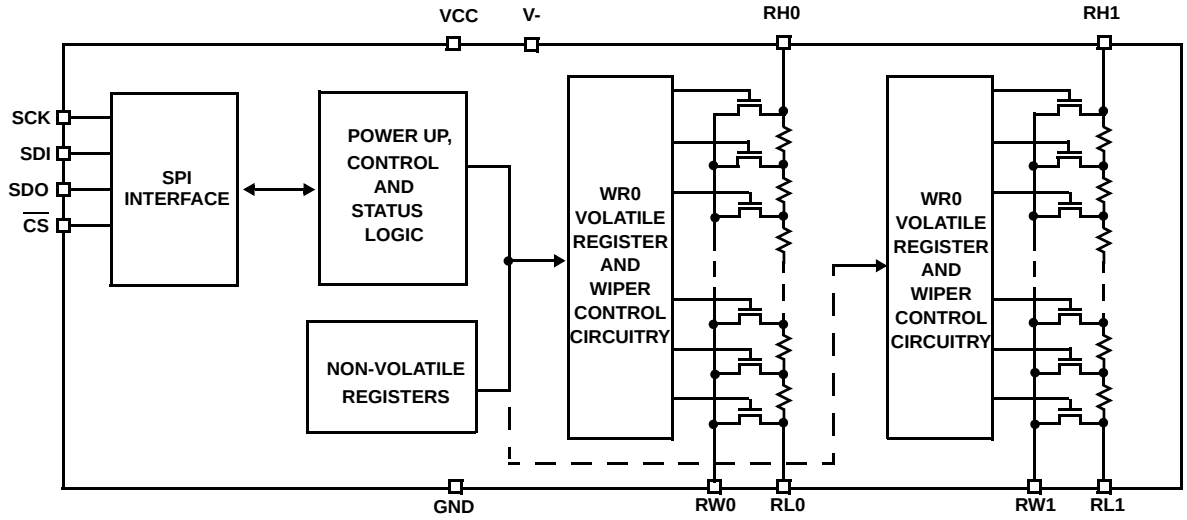
Ordering Information

PART NUMBER (NOTES 1, 2)	PART MARKING	RESISTANCE OPTION (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL22424TFV14Z	22424TFVZ	100	-40 to +125	14 Ld TSSOP	M14.173
ISL22424TFR16Z	22424TFRZ	100	-40 to +125	16 Ld QFN	L16.4x4A
ISL22424UFV14Z	22424UFVZ	50	-40 to +125	14 Ld TSSOP	M14.173
ISL22424UFR16Z	22424UFRZ	50	-40 to +125	16 Ld QFN	L16.4x4A
ISL22424WFV14Z	22424WFVZ	10	-40 to +125	14 Ld TSSOP	M14.173
ISL22424WFR16Z	22424WFRZ	10	-40 to +125	16 Ld QFN	L16.4x4A

NOTES:

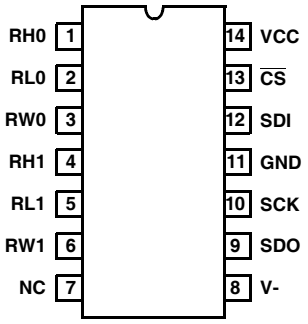
1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "-TK" suffix for 1,000 Tape and Reel option

Block Diagram

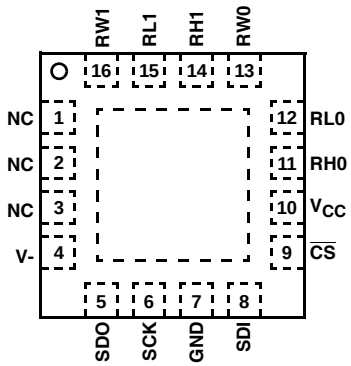


Pinouts

ISL22424
(14 LD TSSOP)
TOP VIEW



ISL22424
(16 LD QFN)
TOP VIEW



Pin Descriptions

TSSOP PIN	QFN PIN	SYMBOL	DESCRIPTION
1	11	RH0	“High” terminal of DCP0
2	12	RL0	“Low” terminal of DCP0
3	13	RW0	“Wiper” terminal of DCP0
4	14	RH1	“High” terminal of DCP1
5	15	RL1	“Low” terminal of DCP1
6	16	RW1	“Wiper” terminal of DCP1
7	1, 2, 3	NC	No connection
8	4	V-	Negative power supply pin
9	5	SDO	Data Output of the SPI serial interface
10	6	SCK	SPI interface clock input
11	7	GND	Device ground pin
12	8	SDI	Data Input of the SPI serial interface
13	9	$\overline{CS}$	Chip Select active low input
14	10	VCC	Positive power supply pin
	EPAD*		Exposed Die Pad internally connected to V-

* Note: PCB thermal land for QFN EPAD should be connected to V- plane or left floating. For more information refer to http://www.intersil.com/data/tb/TB389.pdf

Absolute Maximum Ratings

Storage Temperature . . . . . .-65°C to +150°C
Voltage at any Digital Interface Pin
with Respect to GND . . . . . -0.3V to V_{CC} +0.3
V_{CC} . . . . . .-0.3V to +6V
V- . . . . . .-6V to 0.3V
Voltage at any DCP pin with Respect to GND . . . . . V- to V_{CC}
I_W (10s) . . . . . ±6mA
Latchup . . . . . Class II, Level A @ +125°C
ESD
Human Body Model 3.5kV
Machine Model. 350V

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
14 Lead TSSOP. 105
16 Lead QFN 39
Maximum Junction Temperature (Plastic Package). . . . . +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range (Full Industrial) . . . . . .-40°C to +125°C
Power Rating 15mW
V_{CC} . . . . . 2.25V to 5.5V
V- . . . . . .-2.25V to -5.5V
Max Wiper Current Iw . . . . . .±3.0mA

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNIT
R_{TOTAL}	RHi to RLi resistance	W option		10		kΩ
		U option		50		kΩ
		T option		100		kΩ
	RHi to RLi resistance tolerance		-20		+20	%
	End-to-End Temperature Coefficient	W option		±85		ppm/°C
		U, T option		±45		ppm/°C
V_{RH}, V_{RL}	DCP terminal voltage	V_{RHi} and V_{RLi} to GND	V-		V_{CC}	V
R_W	Wiper resistance	RH - floating, V_{RL} = V-, force Iw current to the wiper, $I_W = (V_{CC} - V_{RL})/R_{TOTAL}$		70	250	Ω
$C_H/C_L/C_W$ (Note 20)	Potentiometer capacitance	See Macro Model below.		10/10/25		pF
I_{LkgDCP}	Leakage on DCP pins	Voltage at pin from V- to V_{CC}		0.1	1	µA
VOLTAGE DIVIDER MODE (V- @ RLi; V_{CC} @ RHi; measured at RWi, unloaded)						
INL (Note 9)	Integral non-linearity	W option	-1.5	±0.5	1.5	LSB (Note 5)
		U, T option	-1.0	±0.2	1.0	LSB (Note 5)
DNL (Note 8)	Differential non-linearity Monotonic over all tap positions	W option	-1.0	±0.4	1.0	LSB (Note 5)
		U, T option	-0.5	±0.15	0.5	LSB (Note 5)
ZSerror (Note 6)	Zero-scale error	W option	0	1	5	LSB (Note 5)
		U, T option	0	0.5	2	
FSerror (Note 7)	Full-scale error	W option	-5	-1	0	LSB (Note 5)
		U, T option	-2	-1	0	
V_{MATCH} (Note 10)	DCP to DCP matching	Wipers at the same tap position, the same voltage at all RH terminals and the same voltage at all RL terminals	-2		2	LSB (Note 5)
TC_V (Note 11, 20)	Ratiometric temperature coefficient	DCP register set to 80 hex		±4		ppm/°C

Analog Specifications Over recommended operating conditions unless otherwise stated. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNIT
f_{cutoff} (Note 20)	-3dB cut off frequency	Wiper at midpoint (80hex) W option (10k)		1000		kHz
		Wiper at midpoint (80hex) U option (50k)		250		kHz
		Wiper at midpoint (80hex) T option (100k)		120		kHz
RESISTOR MODE (Measurements between R_W and R_L with R_H not connected, or between R_W and R_H with R_L not connected)						
RINL (Note 15)	Integral non-linearity	W option	-3	±1.5	3	MI (Note 12)
		U, T option	-1	±0.4	1	MI (Note 12)
RDNL (Note 14)	Differential non-linearity	W option	-1.5	±0.5	1.5	MI (Note 12)
		U, T option	-0.5	±0.15	0.5	MI (Note 12)
Roffset (Note 13)	Offset	W option	0	1	5	MI (Note 12)
		U, T option	0	0.5	2	MI (Note 12)
R_{MATCH} (Note 16)	DCP to DCP matching	Wipers at the same tap position with the same terminal voltages	-2		2	MI (Note 12)
TC_R (Note 17, 20)	Resistance temperature coefficient	DCP register set between 32hex and FF hex		±40		ppm/°C

Operating Specifications Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNIT
I_{CC1}	V_{CC} Supply Current (volatile write/read)	V_{CC} = 5.5V, V- = 5.5V, f_{SCK} = 5MHz; (for SPI Active, Read and Volatile Write states only)		0.6	1.0	mA
		V_{CC} = 2.25V, V- = -2.25V, f_{SCK} = 5MHz; (for SPI Active, Read and Volatile Write states only)		0.25	0.5	mA
I_{V-1}	V- Supply Current (volatile write/read)	V- = -5.5V, V_{CC} = 5.5V, f_{SCK} = 5MHz; (for SPI Active, Read and Volatile Write states only)	-1.0	-0.3		mA
		V- = -2.25V, V_{CC} = 2.25V, f_{SCK} = 5MHz; (for SPI Active, Read and Volatile Write states only)	-0.5	-0.1		mA
I_{CC2}	V_{CC} Supply Current (non-volatile write/read)	V_{CC} = 5.5V, V- = 5.5V, f_{SCK} = 5MHz; (for SPI Active, Read and Non-volatile Write states only)		1.0	2.0	mA
		V_{CC} = 2.25V, V- = -2.25V, f_{SCK} = 5MHz; (for SPI Active, Read and Non-volatile Write states only)		0.3	1.0	mA
I_{V-2}	V- Supply Current (non-volatile write/read)	V- = -5.5V, V_{CC} = 5.5V, f_{SCK} = 5MHz; (for SPI Active, Read and Non-volatile Write states only)	-2.0	-1.2		mA
	V- Supply Current (non-volatile write/read)	V- = -2.25V, V_{CC} = 2.25V, f_{SCK} = 5MHz; (for SPI Active, Read and Non-volatile Write states only)	-1.0	-0.4		mA
I_{SB}	V_{CC} Current (standby)	V_{CC} = +5.5V, V- = -5.5V @ +85°C, SPI interface in standby state		0.5	2.0	µA
		V_{CC} = +5.5V, V- = -5.5V @ +125°C, SPI interface in standby state		1.0	4.0	µA
		V_{CC} = +2.25V, V- = -2.25V @ +85°C, SPI interface in standby state		0.2	1.0	µA
		V_{CC} = +2.25V, V- = -2.25V @ +125°C, SPI interface in standby state		0.5	2.0	µA

Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNIT
I_{V-SB}	V- Current (standby)	V- = -5.5V, V_{CC} = +5.5V @ +85°C, SPI interface in standby state	-3.0	-0.7		µA
		V- = -5.5V, V_{CC} = +5.5V @ +125°C, SPI interface in standby state	-5.0	-1.5		µA
		V- = -2.25V, V_{CC} = +2.25V @ +85°C, SPI interface in standby state	-2.0	-0.3		µA
		V- = -2.25V, V_{CC} = +2.25V @ +125°C, SPI interface in standby state	-3.0	-0.4		µA
I_{SD}	V_{CC} Current (shutdown)	V_{CC} = +5.5V, V- = -5.5V @ +85°C, SPI interface in standby state		0.5	2.0	µA
		V_{CC} = +5.5V, V- = -5.5V @ +125°C, SPI interface in standby state		1.0	4.0	µA
		V_{CC} = +2.25V, V- = -2.25V @ +85°C, SPI interface in standby state		0.2	1.0	µA
		V_{CC} = +2.25V, V- = -2.25V @ +125°C, SPI interface in standby state		0.5	2.0	µA
I_{V-SD}	V- Current (shutdown)	V- = -5.5V, V_{CC} = +5.5V @ +85°C, SPI interface in standby state	-3.0	-0.7		µA
		V- = -5.5V, V_{CC} = +5.5V @ +125°C, SPI interface in standby state	-5.0	-1.5		µA
		V- = -2.25V, V_{CC} = +2.25V @ +85°C, SPI interface in standby state	-2.0	-0.3		µA
		V- = -2.25V, V_{CC} = +2.25V @ +125°C, SPI interface in standby state	-3.0	-0.4		µA
I_{LkgDig}	Leakage current, at pins SCK, SDI, SDO and $\overline{CS}$	Voltage at pin from GND to V_{CC}	-1		1	µA
t_{WRT} (Note 20)	DCP wiper response time	$\overline{CS}$ rising edge to wiper new position		1.5		µs
$t_{ShdnRec}$ (Note 20)	DCP recall time from shutdown mode	$\overline{CS}$ rising edge to wiper stored position and RH connection		1.5		µs
Vpor	Power-on recall voltage	Minimum Vcc at which memory recall occurs	1.9		2.1	V
VccRamp	V_{CC} ramp rate		0.2			V/ms
t_D	Power-up delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and SPI Interface in standby state			5	ms
EEPROM SPECIFICATION						
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	Temperature T ≤ +55ºC	50			Years
t_{WC} (Note 18)	Non-volatile Write Cycle time			12	20	ms
SERIAL INTERFACE SPECIFICATIONS						
V_{IL}	SCK, SDI, and $\overline{CS}$ input buffer LOW voltage				0.3 * V_{CC}	V
V_{IH}	SCK, SDI, and $\overline{CS}$ input buffer HIGH voltage		0.7 * V_{CC}			V
Hysteresis	SCK, SDI, and $\overline{CS}$ input buffer hysteresis		0.05 * V_{CC}			V
V_{OL}	SDO output buffer LOW voltage	I_{OL} = 4mA for Open Drain output, pull-up voltage Vpu = Vcc	0		0.4	V
R_{pu} (Note 19)	SDO pull-up resistor off-chip	Maximum is determined by t_{RO} and t_{FO} with maximum bus load Cb = 30pF, f_{SCK} = 5MHz			2	kΩ

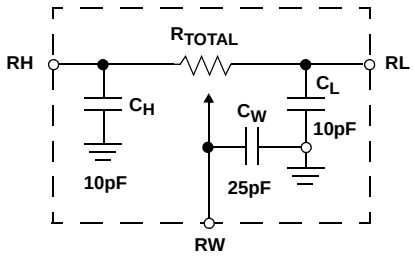
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 4)	MAX	UNIT
Cpin (Note 20)	SCK, SDI, SDO and $\overline{CS}$ pin capacitance			10		pF
f_{SCK}	SPI frequency				5	MHz
t_{CYC}	SPI clock cycle time		200			ns
t_{WH}	SPI clock high time		100			ns
t_{WL}	SPI clock low time		100			ns
t_{LEAD}	Lead time		250			ns
t_{LAG}	Lag time		250			ns
t_{SU}	SDI, SCK and $\overline{CS}$ input setup time		50			ns
t_H	SDI, SCK and $\overline{CS}$ input hold time		50			ns
t_{RI}	SDI, SCK and $\overline{CS}$ input rise time		10			ns
t_{FI}	SDI, SCK and $\overline{CS}$ input fall time		10		20	ns
t_{DIS}	SDO output Disable time		0		100	ns
t_{SO}	SDO output setup time		50			ns
t_V	SDO output valid time		150			ns
t_{HO}	SDO output hold time		0			ns
t_{RO}	SDO output rise time	R_{pu} = 2k, Cbus = 30pF			60	ns
t_{FO}	SDO output fall time	R_{pu} = 2k, Cbus = 30pF			60	ns
t_{CS}	CS deselect time		2			µs

NOTES:

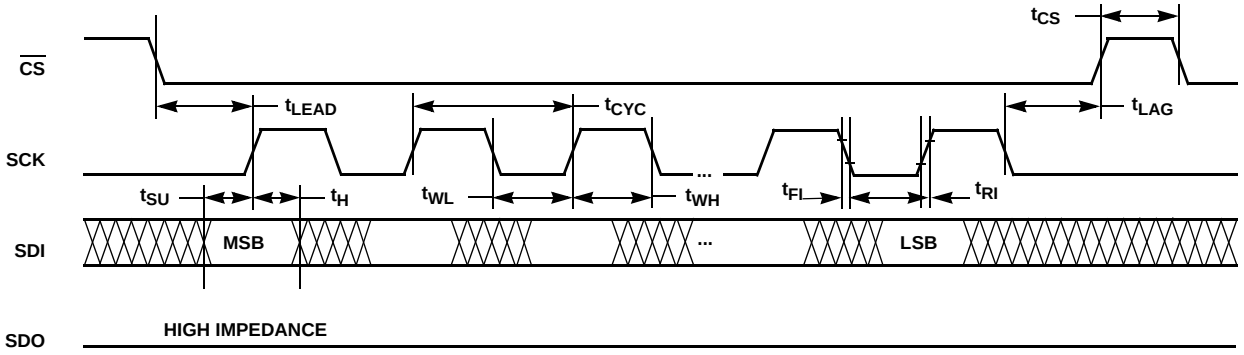
4. Typical values are for T_A = +25°C and 3.3V supply voltage.
5. LSB: $[V(RW)_{255} – V(RW)_0]/255$. $V(RW)_{255}$ and $V(RW)_0$ are V(RW) for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
6. ZS error = $V(RW)_0$/LSB.
7. FS error = $[V(RW)_{255} – V_{CC}]$/LSB.
8. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB-1, for i = 1 to 255. i is the DCP register setting.
9. INL = $[V(RW)_i – i • LSB – V(RW)]$/LSB for i = 1 to 255.
10. V_{MATCH}= [V(RWx)i -V(RWy)i]/LSB, for i = 0 to 255, x = 0 to 1, y = 0 to 1.
11. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{+165°C}$ for i = 16 to 240 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
12. MI = $|RW_{255} – RW_0|/255$. MI is a minimum increment. RW_{255} and RW_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively.
13. Roffset = RW_0/MI, when measuring between RW and RL.
    Roffset = RW_{255}/MI, when measuring between RW and RH.
14. RDNL = $(RW_i – RW_{i-1})$/MI -1, for i = 1 to 255.
15. RINL = $[RW_i – (MI • i) – RW_0]$/MI, for i = 1 to 255.
16. R_{MATCH}= [(Rx)i -(Ry)i]/MI, for i = 0 to 255, x = 0 to 1, y = 0 to 1.
17. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{+165°C}$ for i = 16 to 240, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
18. t_{WC} is the time from the end of a Write sequence of SPI serial interface, to the end of the self-timed internal non-volatile write cycle.
19. R_{pu} is specified for the highest data rate transfer for the device. Higher value pull-up can be used at lower data rates.
20. This parameter is not 100% tested.

DCP Macro Model

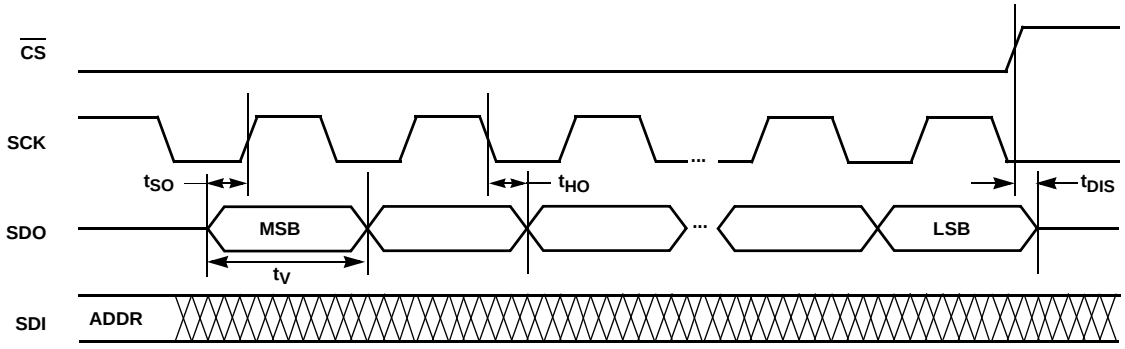


Timing Diagrams

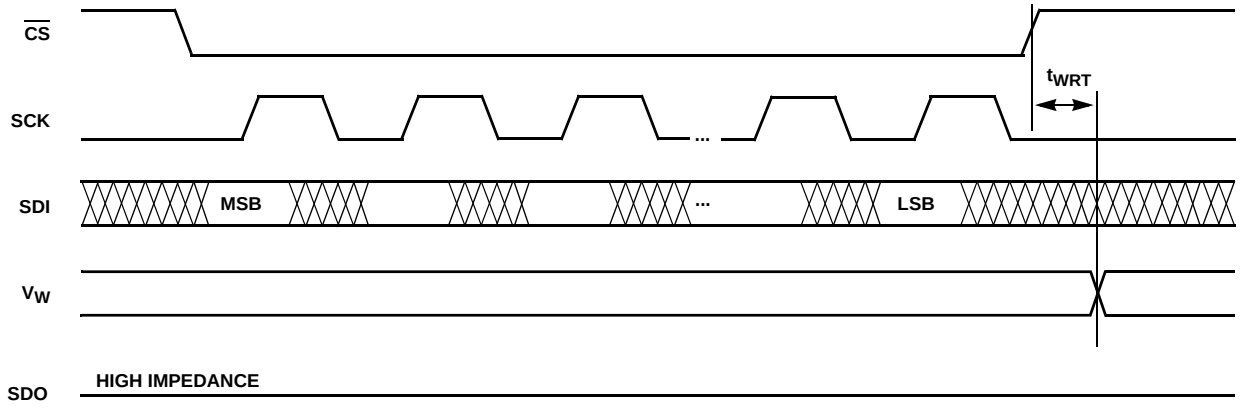
Input Timing



Output Timing



XDCP Timing (for All Load Instructions)



Typical Performance Curves

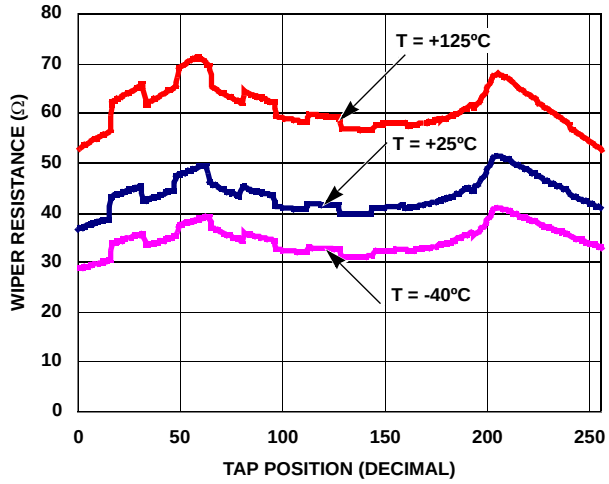


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

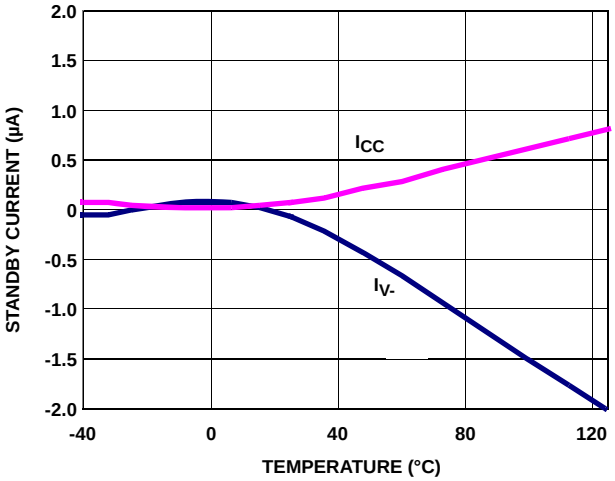


FIGURE 2. STANDBY I_{CC} and I_{V-} vs TEMPERATURE

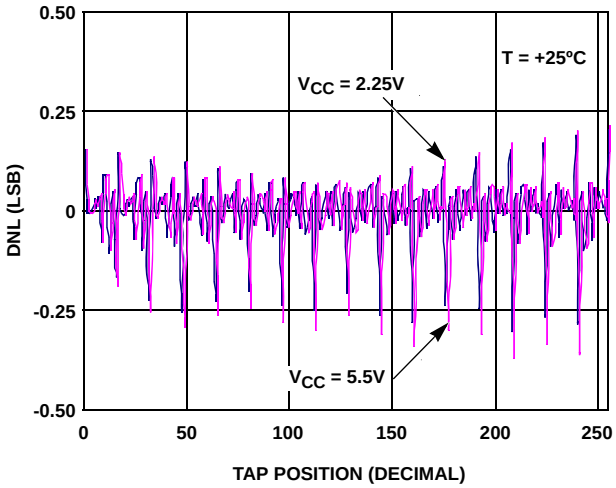


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

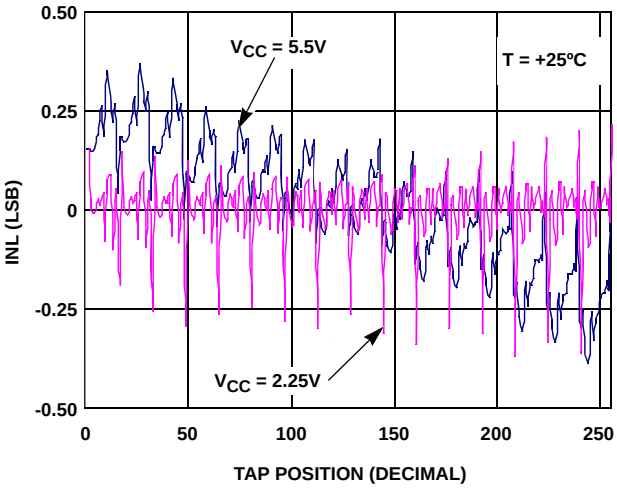


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

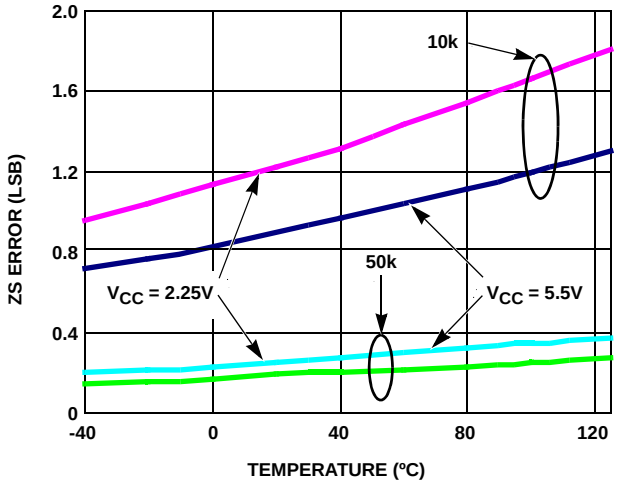


FIGURE 5. ZS ERROR vs TEMPERATURE

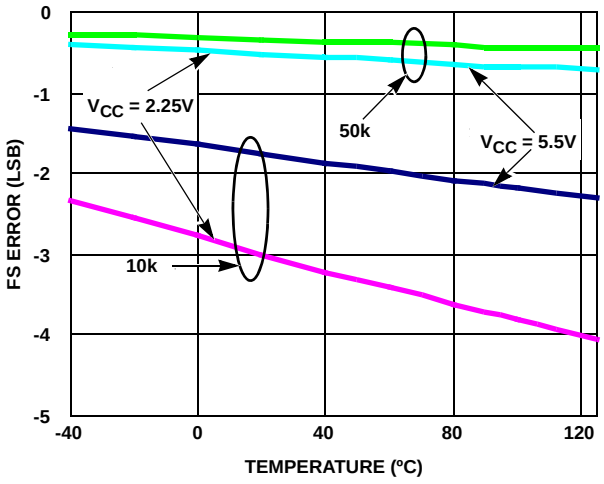


FIGURE 6. FS ERROR vs TEMPERATURE

Typical Performance Curves (Continued)

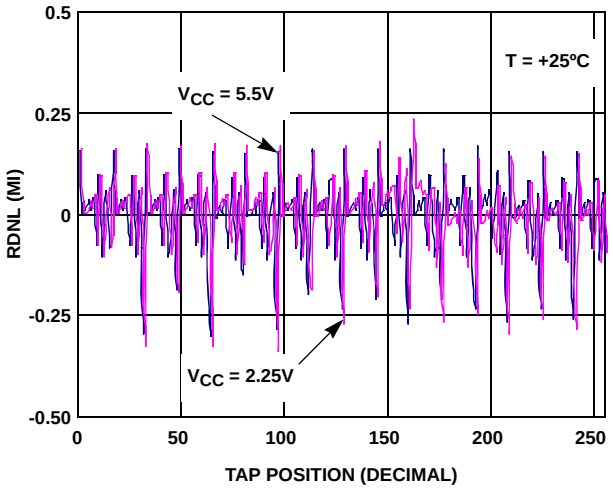


FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

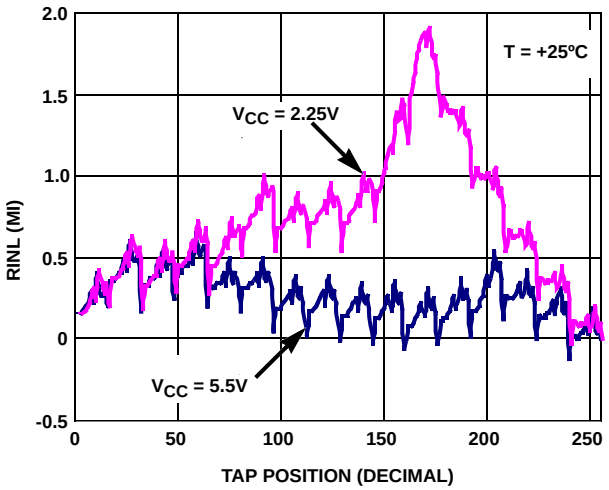


FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

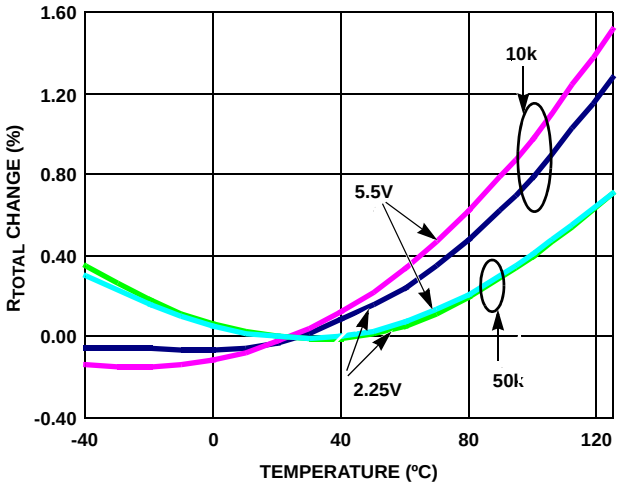


FIGURE 9. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

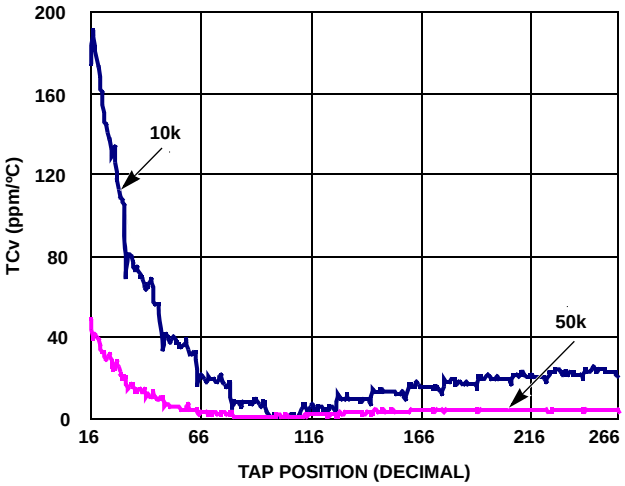


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

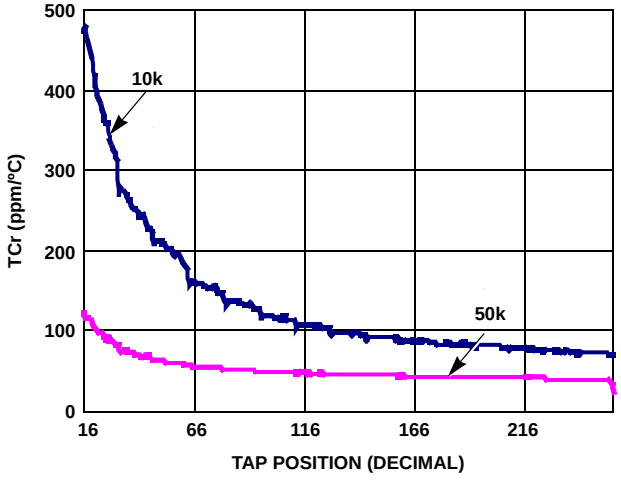


FIGURE 11. TC FOR RHEOSTAT MODE IN ppm

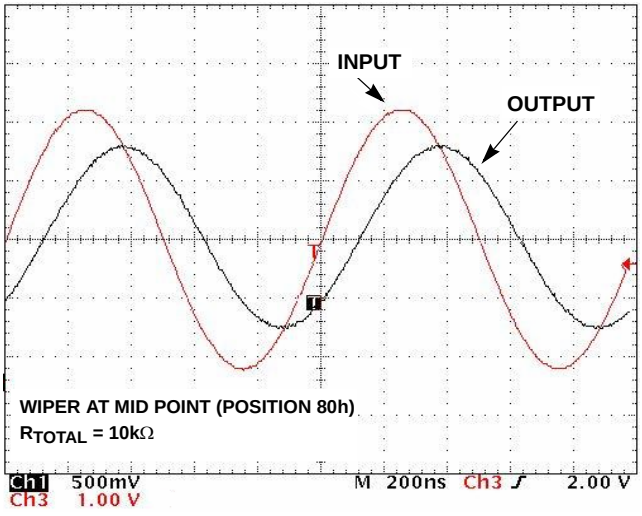


FIGURE 12. FREQUENCY RESPONSE (1MHz)

Typical Performance Curves (Continued)

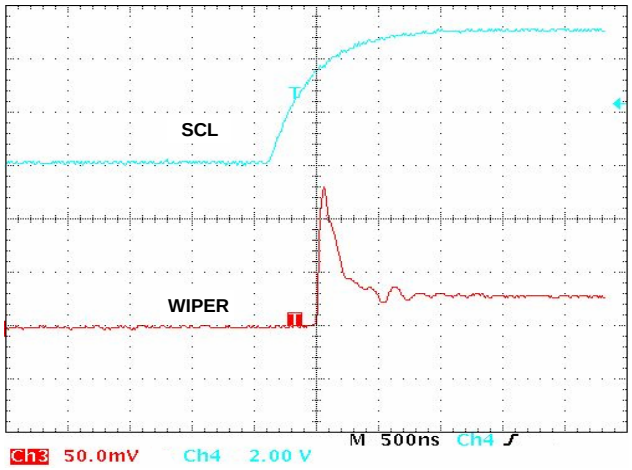


FIGURE 13. MIDSCALE GLITCH, CODE 7Fh TO 80h

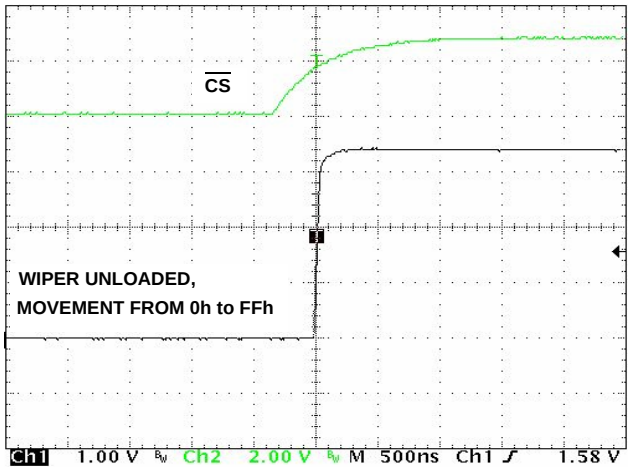


FIGURE 14. LARGE SIGNAL SETTLING TIME

Pin Description

Potentiometer Pins

RHI AND RLI

The high (RHi) and low (RLi) terminals of the ISL22424 are equivalent to the fixed terminals of a mechanical potentiometer. RHi and RLi are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WRi set to 255 decimal, the wiper will be closest to RHi, and with the WRi set to 0, the wiper is closest to RLi.

RWI

RWi is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WRi register.

Bus Interface Pins

SERIAL CLOCK (SCK)

This is the serial clock input of the SPI serial interface.

SERIAL DATA OUTPUT (SDO)

The SDO is a serial data output pin. During a read cycle, the data bits are shifted out on the falling edge of the serial clock SCK and will be available to the master on the following rising edge of SCK.

The output type is configured through ACR[1] bit for Push - Pull or Open Drain operation. Default setting for this pin is Push - Pull. An external pull up resistor is required for Open Drain output operation. Note: the external pull up voltage not allowed beyond V_{CC}.

SERIAL DATA INPUT (SDI)

The SDI is the serial data input pin for the SPI interface. It receives device address, operation code, wiper address and data from the SPI remote host device. The data bits are shifted in at the rising edge of the serial clock SCK, while the $\overline{CS}$ input is low.

CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ LOW enables the ISL22424, placing it in the active power mode. A HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation after power up. When $\overline{CS}$ is HIGH, the ISL22424 is deselected and the SDO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state.

Principles of Operation

The ISL22424 is an integrated circuit incorporating two DCPs with their associated registers, non-volatile memory and the SPI serial interface providing direct communication between host, potentiometers and memory. The resistor arrays are comprised of individual resistors connected in a series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVRi will be maintained in the non-volatile memory. When power is restored, the content of the IVRi is recalled and loaded into the corresponding WRi to set the wiper to the initial position.

DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RHi and RLi pins). The RWi pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WRi). When the WRi of a DCP

contains all zeroes (WRi[7:0]= 00h), its wiper terminal (RWi) is closest to its “Low” terminal (RLi). When the WRi register of a DCP contains all ones (WRi[7:0]= FFh), its wiper terminal (RWi) is closest to its “High” terminal (RHi). As the value of the WRi increases from all zeroes (0) to all ones (255 decimal), the wiper moves monotonically from the position closest to RLi to the closest to RHi. At the same time, the resistance between RWi and RLi increases monotonically, while the resistance between RHi and RWi decreases monotonically.

While the ISL22424 is being powered up, the WRi is reset to 80h (128 decimal), which locates RWi roughly at the center between RLi and RHi. After the power supply voltage becomes large enough for reliable non-volatile memory reading, the WRi will be reloaded with the value stored in a corresponding non-volatile Initial Value Register (IVRi).

The WRi and IVRi can be read or written to directly using the SPI serial interface as described in the following sections.

Memory Description

The ISL22424 contains two non-volatile 8-bit Initial Value Registers (IVRi), thirteen non-volatile 8-bit General Purpose (GP) registers, two volatile 8-bit Wiper Registers (WRi), and volatile 8-bit Access Control Register (ACR). The memory map of ISL22424 is in Table 1.

TABLE 1. MEMORY MAP

ADDRESS (hex)	NON-VOLATILE	VOLATILE
10	N/A	ACR
F	Reserved	
E	General Purpose	N/A
D	General Purpose	N/A
C	General Purpose	N/A
B	General Purpose	N/A
A	General Purpose	N/A
9	General Purpose	N/A
8	General Purpose	N/A
7	General Purpose	N/A
6	General Purpose	N/A
5	General Purpose	N/A
4	General Purpose	N/A
3	General Purpose	N/A
2	General Purpose	N/A
1	IVR1	WR1
0	IVR0	WR0

The non-volatile registers (IVRi) at address 0 and 1, contain initial wiper position and volatile registers (WRi) contain current wiper position.

The register at address 0Fh is a read-only reserved register. Information read from this register should be ignored.

The non-volatile IVRi and volatile WRi registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described below in Table 2.

The VOL bit (ACR[7]) determines whether the access to wiper registers WRi or initial value registers IVRi.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

BIT #	7	6	5	4	3	2	1	0
BIT NAME	VOL	SHDN	WIP	0	0	0	SDO	0

If VOL bit is 0, the non-volatile IVRi and General Purpose registers are accessible. If VOL bit is 1, only the volatile WRi are accessible. Note: value that is written to IVRi register also is written to the corresponding WRi. The default value of this bit is 0.

The $\overline{SHDN}$ bit (ACR[6]) disables or enables Shutdown mode. When this bit is 0, DCP is in Shutdown mode, i.e. each DCP is forced to end-to-end open circuit and RWi is shorted to RLi as shown on Figure 15. Default value of $\overline{SHDN}$ bit is 1.

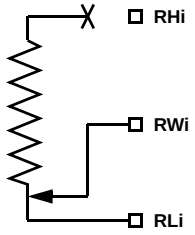


FIGURE 15. DCP CONNECTION IN SHUTDOWN MODE

Setting $\overline{SHDN}$ bit to 1 is returned wipers to prior to Shutdown Mode position.

The WIP bit (ACR[5]) is a read-only bit. It indicates that non-volatile write operation is in progress. The WIP bit can be read repeatedly after a non-volatile write to determine if the write has been completed. It is impossible to write or read to the WRi or ACR while WIP bit is 1.

The SDO bit (ACR[1]) configures type of SDO output pin. The default value of SDO bit is 0 for Push - Pull output. SDO pin can be configured as Open Drain output for some application. In this case, an external pull up resistor is required. See “Applications Information” on page 14.

SPI Serial Interface

The ISL22424 supports an SPI serial protocol, mode 0. The device is accessed via the SDI input and SDO output with data clocked in on the rising edge of SCK, and clocked out on the falling edge of SCK. $\overline{CS}$ must be LOW during communication with the ISL22424. SCK and $\overline{CS}$ lines are

controlled by the host or master. The ISL22424 operates only as a slave device.

All communication over the SPI interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

The SPI protocol contains Instruction Byte followed by one or more Data Bytes. A valid Instruction Byte contains instruction as the three MSBs, with the following five register address bits (see Table 3).

The next byte sent to the ISL22424 is the Data Byte.

TABLE 3. INSTRUCTION BYTE FORMAT

BIT #	7	6	5	4	3	2	1	0
	I2	I1	I0	R4	R3	R2	R1	R0

Table 4 contains a valid instruction set for ISL22424.

There are only sixteen register addresses possible for this DCP. If the [R4:R0] bits are 00000 or 00001, then the read or write is to either the IVRi or the WRi registers (depends of VOL bit at ACR). If the [R4:R0] are 10000, then the operation is on the ACR.

Write Operation

A Write operation to the ISL22424 is a two or more bytes operation. First, It requires, the $\overline{CS}$ transition from HIGH to LOW. Then host must send a valid Instruction Byte followed by one or more Data Bytes to SDI pin. The host terminates the write operation by pulling the $\overline{CS}$ pin from LOW to HIGH. Instruction is executed on rising edge of $\overline{CS}$. For a write-to address 0 or 1, the MSB of the byte at address 10h (ACR[7]) determines if the Data Byte is to be written to volatile or both volatile and non-volatile registers. Refer to “Memory Description” and Figure 16. Note: the internal non-volatile write cycle starts with the rising edge of $\overline{CS}$ and requires up to 20ms. During non-volatile write cycle the read operation to ACR register is allowed to check WIP bit.

Read Operation

A Read operation to the ISL22424 is a four byte operation. It requires first, the $\overline{CS}$ transition from HIGH to LOW. Then the host must send a valid Instruction Byte followed by “dummy” Data Byte, a NOP Instruction Byte and another “dummy” Data Byte to SDI pin. The SPI host receives the Instruction Byte (instruction code + register address) and requested Data Byte from SDO pin on rising edge of SCK during third and fourth bytes respectively. The host terminates the read operation by pulling the $\overline{CS}$ pin from LOW to HIGH (see Figure 17). Reading from the IVRi will not change the WRi, if its contents are different.

TABLE 4. INSTRUCTION SET

INSTRUCTION SET								OPERATION
I2	I1	I0	R4	R3	R2	R1	R0	
0	0	0	X	X	X	X	X	NOP
0	0	1	X	X	X	X	X	ACR READ
0	1	1	X	X	X	X	X	ACR WRITE
1	0	0	R4	R3	R2	R1	R0	WR, IVR, GP or ACR READ
1	1	0	R4	R3	R2	R1	R0	WR, IVR, GP or ACR WRITE

where X means “do not care”.

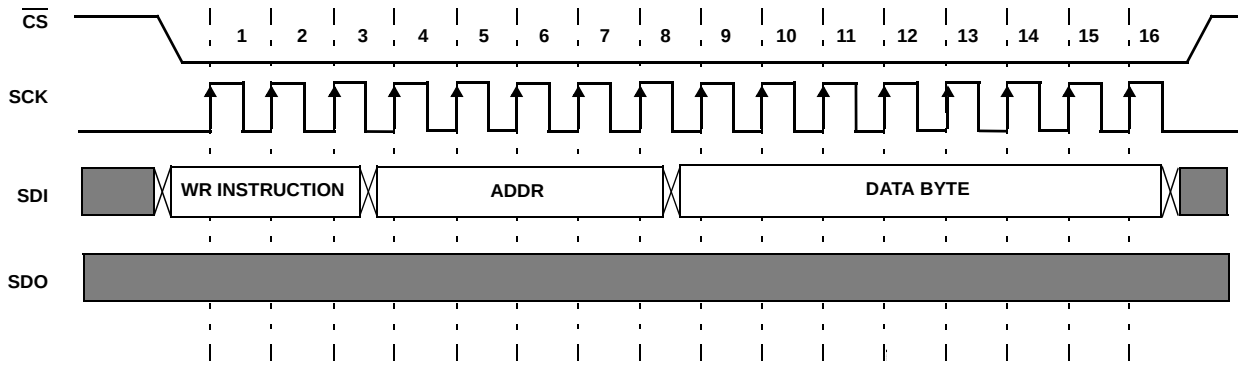


FIGURE 16. TWO BYTE WRITE SEQUENCE

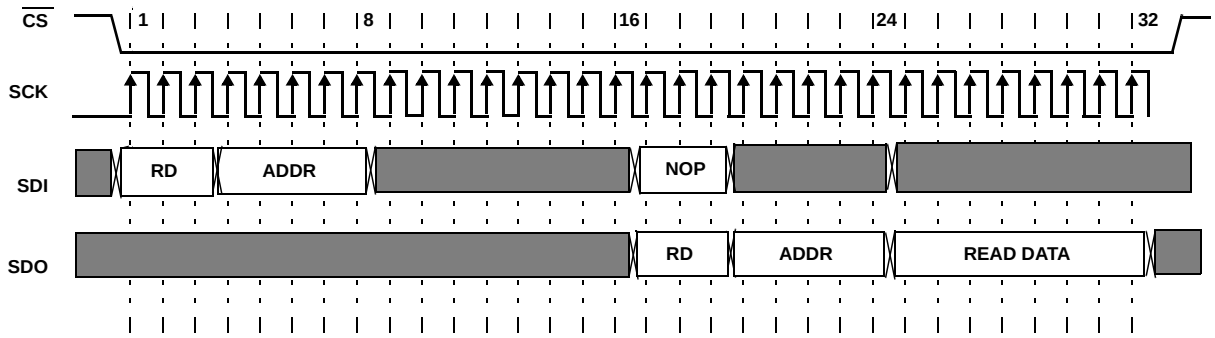


FIGURE 17. FOUR BYTE READ SEQUENCE

Applications Information

Communicating with ISL22424

Communication with ISL22424 proceeds using SPI interface through the ACR (address 10000b), IVRi (address 00000b, 00001b), WRi (addresses 00000b, 00001b) and General Purpose registers (addresses from 00010b to 01110b).

The wiper position of each potentiometer is controlled by the corresponding WRi register. Writes and reads can be made directly to these registers to control and monitor the wiper position without any non-volatile memory changes. This is done by setting MSB bit at address 10000b to 1 (ACR[7] = 1).

The non-volatile IVRi stores the power up position of the wiper. IVRi is accessible when MSB bit at address 10000b is set to 0 (ACR[7] = 0). Writing a new value to the IVRi register will set a new power up position for the wiper. Also, writing to this registers will load the same value into the corresponding WRi as the IVRi. Reading from the IVRi will not change the WRi, if its contents are different.

Daisy Chain Configuration

When application needs more then one ISL22424, it can communicate with all of them without additional $\overline{CS}$ lines by daisy chaining the DCPs as shown on Figure 18. In Daisy Chain configuration the SDO pin of previous chip is connected to SDI pin of the following chip, and each $\overline{CS}$ and SCK pins are connected to the corresponding microcontroller pins in parallel, like regular SPI interface implementation. The Daisy Chain configuration can also be used for simultaneous setting of multiple DCPs. Note, the number of daisy chained DCPs is limited only by the driving capabilities of SCK and $\overline{CS}$ pins of microcontroller; for larger number of SPI devices buffering of SCK and $\overline{CS}$ lines is required.

Daisy Chain Write Operation

The write operation starts by HIGH to LOW transition on $\overline{CS}$ line, followed by N two bytes write instructions on SDI line with reversed chain access sequence: the instruction byte + data byte for the last DCP in chain is going first, as shown on Figure 19. The serial data is going through DCPs from DCP0 to DCP(N-1) as follow: DCP0 --> DCP1 --> DCP2 --> ... --> DCP(N-1). The write instruction is executed on the rising edge of $\overline{CS}$ for all N DCPs simultaneously.

Daisy Chain Read Operation

The read operation consists of two parts: first, send read instructions (N two bytes operation) with valid address; second, read the requested data while sending NOP instructions (N two bytes operation) as shown on Figure 20 and Figure 21.

The first part starts by HIGH to LOW transition on $\overline{CS}$ line, followed by N two bytes read instruction on SDI line with reversed chain access sequence: the instruction byte + dummy data byte for the last DCP in chain is going first, followed by LOW to HIGH transition on $\overline{CS}$ line. The read instructions are executed during second part of read sequence. It also starts by HIGH to LOW transition on $\overline{CS}$ line, followed by N two bytes NOP instructions on SDI line and LOW to HIGH transition of $\overline{CS}$. The data is read on every even byte during second part of read sequence while every odd byte contains instruction code + address from which the data is being read.

Wiper Transition

When stepping up through each tap in voltage divider mode, some tap transition points can result in noticeable voltage transients, or overshoot/undershoot, resulting from the sudden transition from a very low impedance “make” to a much higher impedance “break within an extremely short period of time (<50ns). Two such code transitions are EFh to F0h, and 0Fh to 10h. Note, that all switching transients will settle well within the settling time as stated on the datasheet. A small capacitor can be added externally to reduce the amplitude of these voltage transients, but that will also reduce the useful bandwidth of the circuit, thus may not be a good solution for some applications. It may be a good idea, in that case, to use fast amplifiers in a signal chain for fast recovery.

Application Example

Figure 22 shows an example of using ISL22424 for gain setting and offset correction in high side current measurement application. DCP0 applies a programmable offset voltage of ±25mV to the FB+ pin of the Instrumentation Amplifier EL8173 to adjust output offset to zero voltages. DCP1 programs the gain of the EL8173 from 90 to 110 with 5V output for 10A current through current sense resistor.

More application examples can be found at http://www.intersil.com/data/an/AN1145.pdf

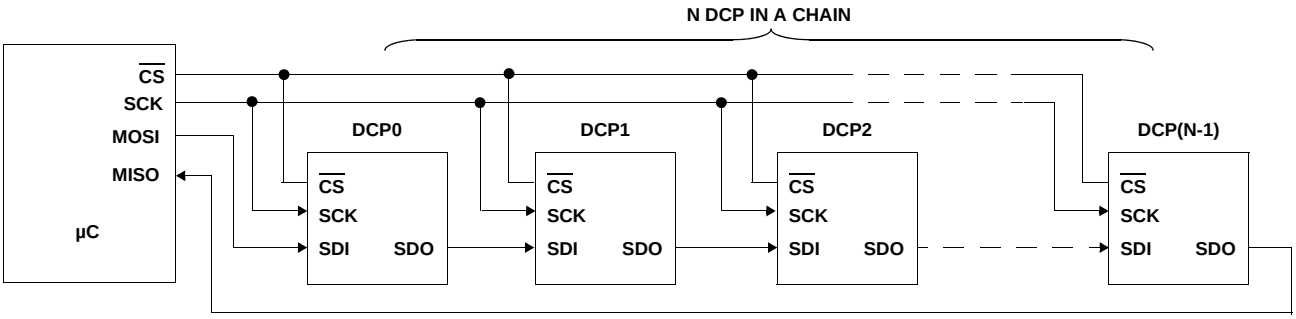


FIGURE 18. DAISY CHAIN CONFIGURATION

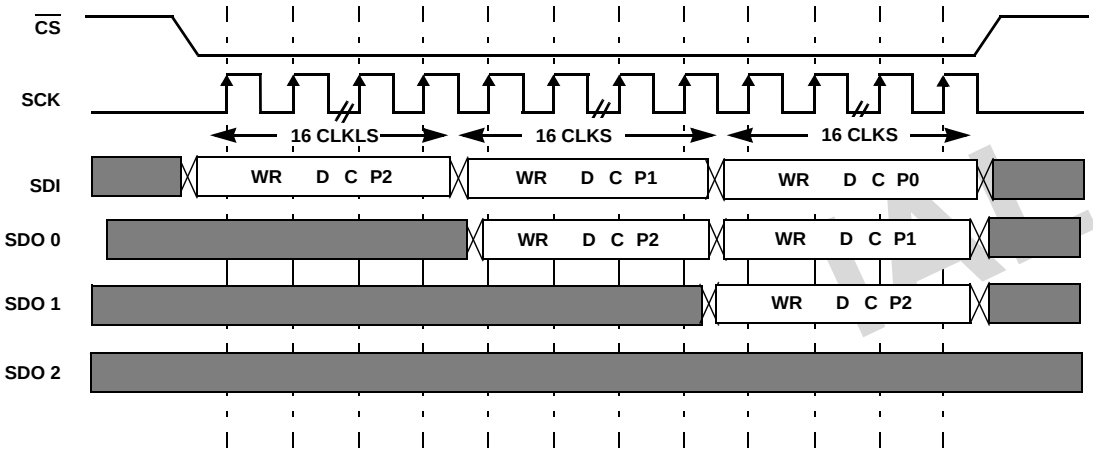


FIGURE 19. DAISY CHAIN WRITE SEQUENCE OF N = 3 DCP

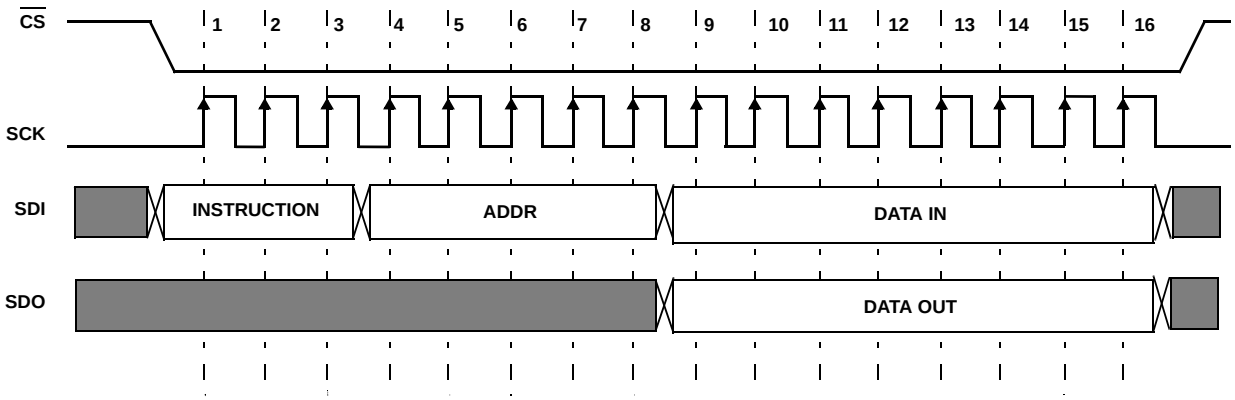


FIGURE 20. TWO BYTE OPERATION

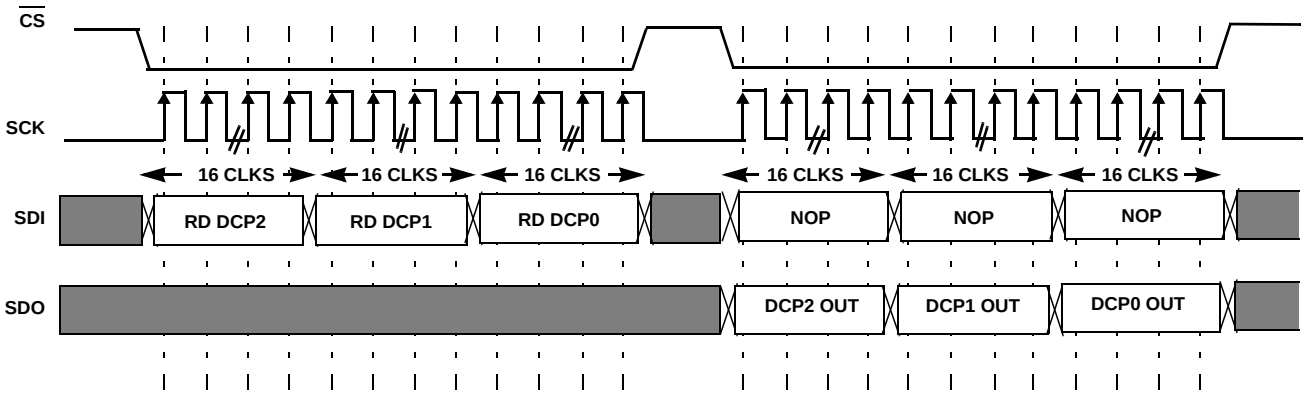


FIGURE 21. DAISY CHAIN READ SEQUENCE OF N = 3 DCP

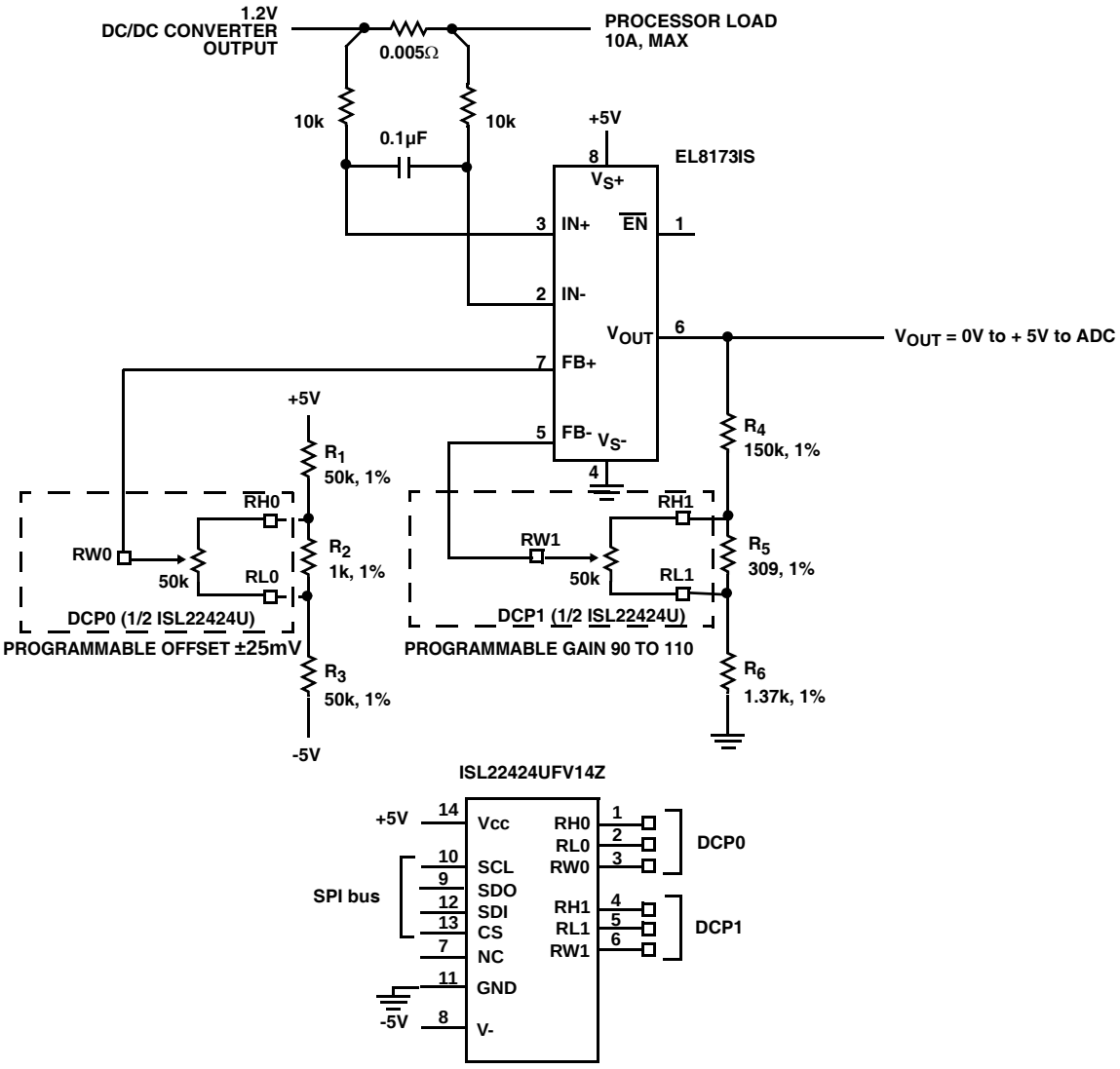
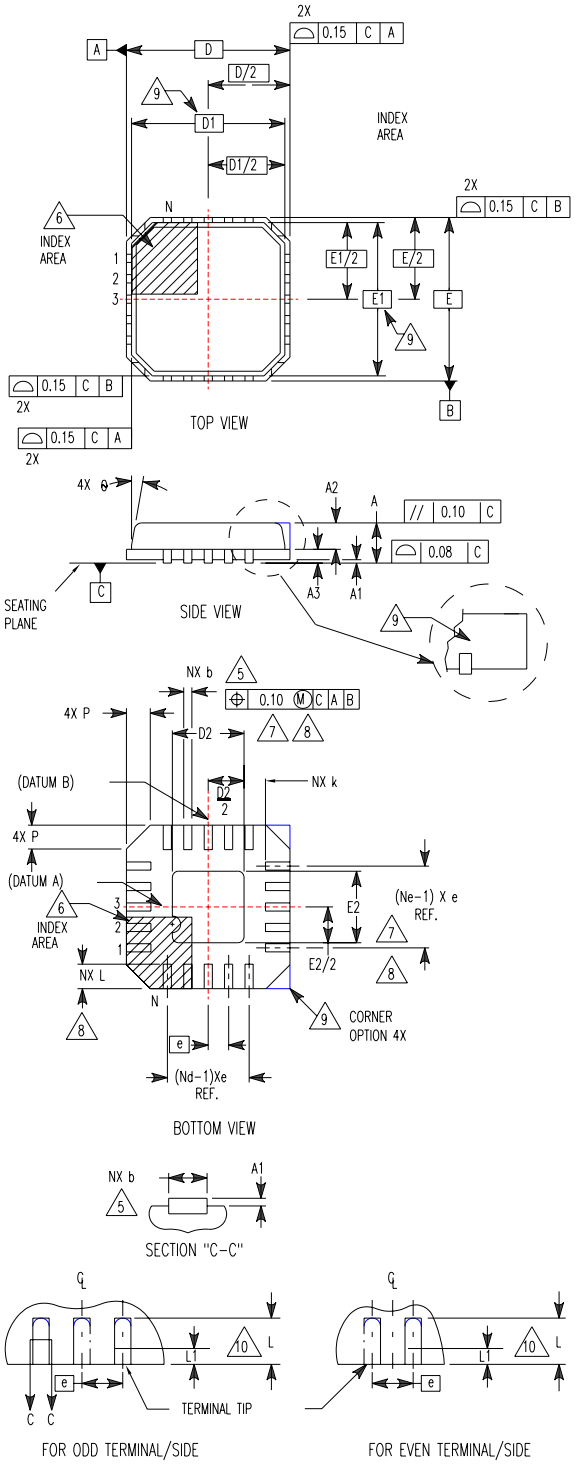


FIGURE 22. CURRENT SENSING WITH GAIN AND OFFSET CONTROL

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4A

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGD-10)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.25	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	2.30	2.40	2.55	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	2.30	2.40	2.55	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

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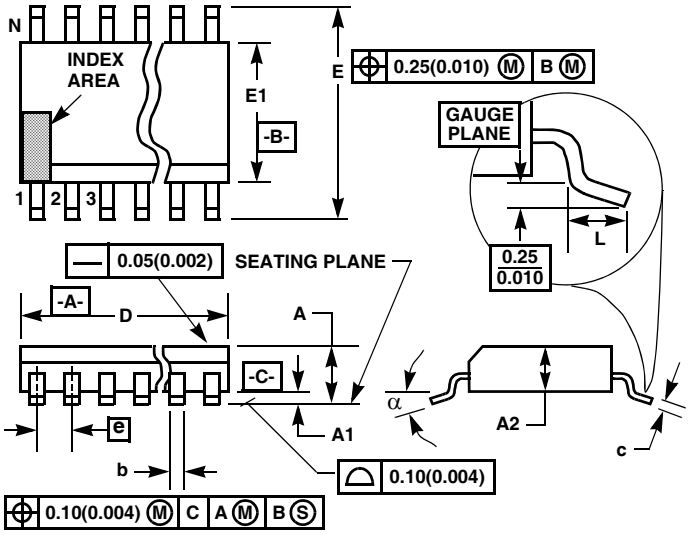
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

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