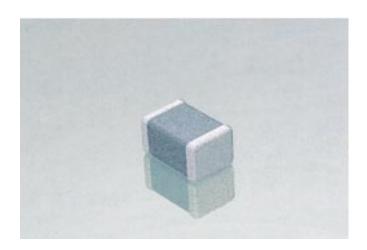


## **General Specifications**

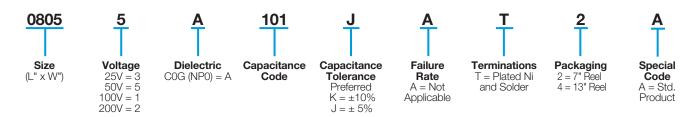


COG (NP0) is the most popular formulation of the "temperature-compensating," EIA Class I ceramic materials. Modern COG (NP0) formulations contain neodymium, samarium and other rare earth oxides.

COG (NP0) ceramics offer one of the most stable capacitor dielectrics available. Capacitance change with temperature is 0 ±30ppm/°C which is less than ±0.3%  $\Delta$  C from -55°C to +125°C. Capacitance drift or hysteresis for COG (NP0) ceramics is negligible at less than ±0.05% versus up to ±2% for films. Typical capacitance change with life is less than ±0.1% for COG (NP0), one-fifth that shown by most other dielectrics. COG (NP0) formulations show no aging characteristics.

The COG (NP0) formulation usually has a "Q" in excess of 1000 and shows little capacitance or "Q" changes with frequency. Their dielectric absorption is typically less than 0.6% which is similar to mica and most films.

### PART NUMBER (see page 3 for complete part number explanation)



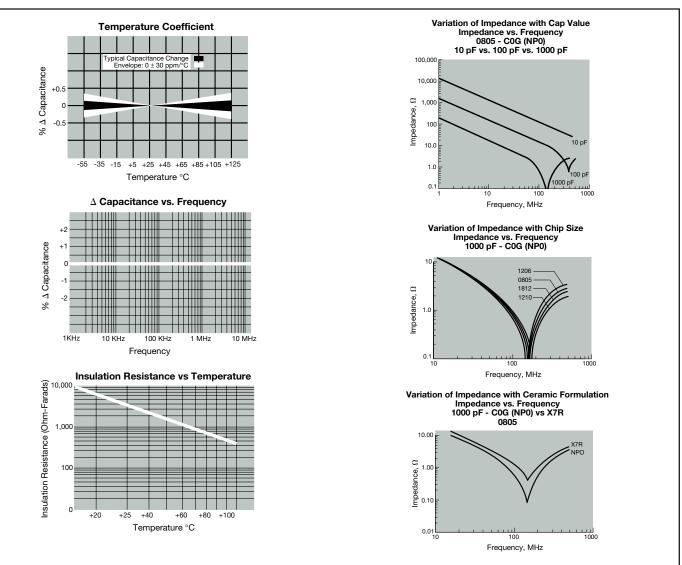
## **PERFORMANCE CHARACTERISTICS**

Capacitance Range	0.5 pF to .1 μF (1.0 ±0.2 Vrms, 1kHz, for ≤100 pF use 1 MHz)
Capacitance Tolerances	Preferred $\pm$ 5%, $\pm$ 10% others available: $\pm$ .25 pF, $\pm$ .5 pF, $\pm$ 1% ( $\geq$ 25pF), $\pm$ 2%( $\geq$ 13pF), $\pm$ 20% For values $\leq$ 10 pF preferred tolerance is $\pm$ .5 pF, also available $\pm$ .25 pF.
Operating Temperature Range	-55°C to +125°C
Temperature Characteristic	$0 \pm 30 \text{ ppm/°C}$ (EIA COG)
Voltage Ratings	25, 50, 100 & 200 VDC (+125°C)
Dissipation Factor and "Q"	For values >30 pF: 0.1% max. (+25°C and +125°C) For values ≤30 pF: "Q" = 400 + 20 x C (C in pF)
Insulation Resistance (+25°C, RVDC)	100,000 megohms min. or 1000 M $\Omega$ - $\mu$ F min., whichever is less
Insulation Resistance (+125°C, RVDC)	10,000 megohms min. or 100 M $\Omega$ - $\mu$ F min., whichever is less
Dielectric Strength	250% of rated voltage for 5 seconds at 50 mamp max. current
Test Voltage	1 ± 0.2 Vrms
Test Frequency	For values ≤100 pF: 1 MHz For values >100 pF: 1 KHz



## **Typical Characteristic Curves\*\***





### SUMMARY OF CAPACITANCE RANGES VS. CHIP SIZE

Style	25V	50V	100V	200V
0402*	0.5pF - 220pF	0.5pF - 120pF	—	—
0504	0.5pF - 330pF	0.5pF - 150pF	0.5pF - 68pF	—
0603*	0.5pF - 1nF	0.5pF - 1nF	0.5pF - 330pF	—
0805*	0.5pF - 4.7nF	0.5pF - 2.2nF	0.5pF - 1nF	0.5pF - 470pF
1206*	0.5pF - 10nF	0.5pF - 4.7nF	0.5pF - 2.2nF	0.5pF - 1nF
1210*	560pF - 10nF	560pF - 10nF	560pF - 3.9nF	560pF - 1.5nF
1505	—	10pF - 1.5nF	10pF - 820pF	10pF - 560pF
1808	$\rightarrow$	1nF - 4.7nF	1nF - 3.9nF	1nF - 2.2nF
1812*	1nF - 15nF	1nF - 10nF	1nF - 4.7nF	1nF - 3.3nF
1825*	$\rightarrow$	1nF - 22nF	1nF - 12nF	1nF - 6.8nF
2220	$\rightarrow$	4.7nF - 47nF	4.7nF - 39nF	3.3nF - 27nF
2225	$\rightarrow$	1nF - 100nF	1nF - 39nF	1nF - 39nF

Standard Sizes For additional information on performance changes with operating conditions consult AVX's software SpiCap. \*\*



## **Capacitance Range**

## **PREFERRED SIZES ARE SHADED**

	•								Œ	ם			Œ												
SIZE	0402*		0504*			0603*			08	05			120	)6			1505								
Standard Reel Packaging	All Paper	A	II Embossed			All Paper	r	P	aper/Er	nbosse	ed	Pa	Paper/Embossed		Paper/Embossed		Paper/Embossed		Paper/Embossed		Paper/Embossed		All	Embos	sed
(L) Length MM (in.)	1.00 ± .10 (.040 ± .004)		1.27 ± .25 (.050 ± .010)			1.60 ± .15 (.063 ± .006			2.01 (.079 :	± .20 ± .008)			3.20 ± (.126 ±	.20 .008)			3.81 ± .2 150 ± .01								
(W) Width MM (in.)	.50 ± .10 (.020 ± .004)		1.02 ± .25 (.040 ± .010)			.81 ± .15 (.032 ± .000			1.25	± .20 ± .008)			1.60 ± (.063 ±	.20			1.27 ± .2 050 ± .01	5							
(T) Max. Thickness MM (in.)	.60 (.024)		1.02 (.040)			.90 (.035)	,			30			1.50	) )			1.27 (.050)	,							
(t) Terminal MM (in.)	.25 ± .15 (.010 ± .006)		.38 ± .13 (.015 ± .005)			.35 ± .15 (.014 ± .006			.50 :	± .25 ± .010)			.50 ± (.020 ±	.25		(.	.50 ± .25 020 ± .01	5							
WVDC		50 25	1	00	25	50	100	25	50	100	200	25	50	100	200	50	100	200							
Cap 0.5 (pF) 1.0 1.2 1.5 1.8 2.2 2.7 3.3 3.9 4.7 5.6 6.8 8.2 10 12 15 18 22 27 33 39 4.7 5.6 6.8 8.2 10 12 15 18 22 27 33 39 47 56 6.8 8.2 10 12 15 18 22 27 33 39 47 10 12 15 18 22 27 33 39 47 10 12 15 18 8 22 27 33 39 47 10 12 15 18 8 22 27 33 39 47 10 12 15 18 22 27 33 39 47 10 12 15 18 22 27 33 39 47 10 12 15 18 22 27 33 39 47 10 12 15 18 22 27 33 39 47 47 56 68 82 27 27 33 39 47 47 56 68 82 27 33 39 47 47 56 68 82 27 33 39 47 47 56 68 82 27 27 33 39 47 47 56 68 82 27 33 39 47 47 56 68 82 27 33 39 47 47 56 68 82 27 27 33 39 47 50 50 68 82 27 70 30 39 47 50 68 82 20 270 330 390 470 560 680 820 270 270 270 270 270 270 270 2													×												
1000 1200 1500																									
1800 2200 2700								////	////																
3300 3900 4700																									
5600 6800 8200																									
10000																									

\*Reflow soldering only.

 $\ensuremath{\mathsf{NOTES}}\xspace$  For higher voltage chips, see pages 20 and 21.



= Paper Tape

6

## **Capacitance Range**

## **PREFERRED SIZES ARE SHADED**

		Π								$\square$										
SIZE		1:	210			1808*			18	12*			1825*			2220*			2225*	,
Standard Reel Packaging	F	Paper/E	mbos	sed	All	Emboss	ed		All Eml	oosse	d	Al	Emboss	ed	All	Emboss	ed	All	Embos	sed
(L) Length MM (in.)			) ± .20 ± .008)			l.57 ± .25 80 ± .010	)		4.50 ±				4.50 ± .30			5.7 ± .40 225 ± .010			5.72 ± .2	
(W) Width MM (in.)			) ± .20 ± .008)			2.03 ± .25 80 ± .010	)		3.20 ±				6.40 ± .40 252 ± .016			5.0 ± .40 197 ± .016			6.35 ± .2	
(T) Max. Thickness MM (in.)		1.70 (.067)		1.52 1.70 (.060) (.067)			1.70 (.067)			2.30 (.090)			1.70 (.067)							
(t) Terminal MM (in.)			± .25 ± .010)			.64 ± .39 )25 ± .015	)		.61 ± (.024 ±			(	.61 ± .36 024 ± .014	4)	(.	.64 ± .39 025 ± .01		(	.64 ± .39	
WVDC	25	50	100	200	50	100	200	25	50	100	200	50	100	200	50	100	200	50	100	200
Cap 560 (pF) 680 820																			× v	
1000 1200 1500																	$\sum$	$\sum_{n}$		
1800 2200 2700																				
3300 3900 4700																				
5600 6800 8200																				
Cap010 (μF) .012 .015																				
.018 .022 .027																				
.033 .039 .047																				
.068 .082 .1																				

#### \*Reflow soldering only.

NOTES: For higher voltage chips, see pages 20 and 21.

= Paper Tape = Embossed Tape

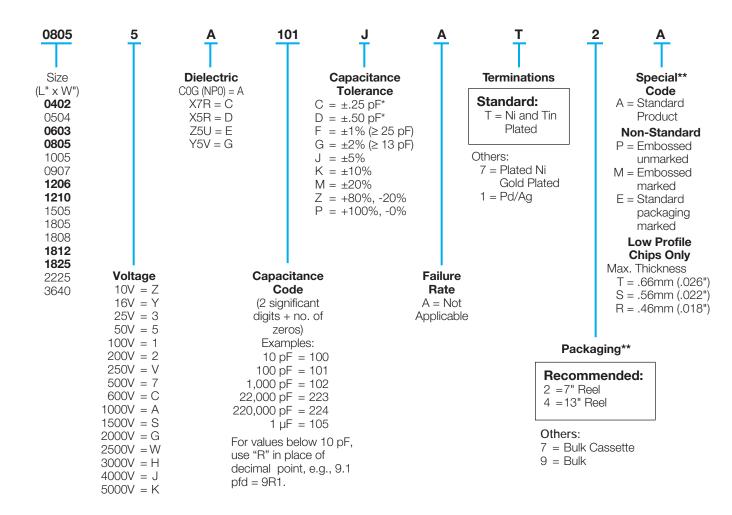


# How to Order





### **EXAMPLE: 08055A101JAT2A**



\*C&D tolerances for  $\leq 10 \text{ pF}$  values.

\*\* Standard Tape and Reel material depends upon chip size and thickness. See individual part tables for tape material type for each capacitance value.

Note: Unmarked product is standard. Marked product is available on special request, please contact AVX. Standard packaging is shown in the individual tables.

Non-standard packaging is available on special request, please contact AVX.



# **Surface Mounting Guide**

## **MLC Chip Capacitors**



#### **Component Pad Design**

Component pads should be designed to achieve good solder filets and minimize component movement during reflow soldering. Pad designs are given below for the most common sizes of multilayer ceramic capacitors for both wave and reflow soldering. The basis of these designs is:

- Pad width equal to component width. It is permissible to decrease this to as low as 85% of component width but it is not advisable to go below this.
- Pad overlap 0.5mm beneath component.
- Pad extension 0.5mm beyond components for reflow and 1.0mm for wave soldering.

	Case Size	D1	D2	D3	D4	D5
D2	0402	1.70 (0.07)	0.60 (0.02)	0.50 (0.02)	0.60 (0.02)	0.50 (0.02)
	0603	2.30 (0.09)	0.80 (0.03)	0.70 (0.03)	0.80 (0.03)	0.75 (0.03)
1 D3	0805	3.00 (0.12)	1.00 (0.04)	1.00 (0.04)	1.00 (0.04)	1.25 (0.05)
	1206	4.00 (0.16)	1.00 (0.04)	2.00 (0.09)	1.00 (0.04)	1.60 (0.06)
<b>≜</b>	1210	4.00 (0.16)	1.00 (0.04)	2.00 (0.09)	1.00 (0.04)	2.50 (0.10)
D4	1808	5.60 (0.22)	1.00 (0.04)	3.60 (0.14)	1.00 (0.04)	2.00 (0.08)
▼	1812	5.60 (0.22)	1.00 (0.04))	3.60 (0.14)	1.00 (0.04)	3.00 (0.12)
→ D5 -	1825	5.60 (0.22)	1.00 (0.04)	3.60 (0.14)	1.00 (0.04)	6.35 (0.25)
	2220	6.60 (0.26)	1.00 (0.04)	4.60 (0.18)	1.00 (0.04)	5.00 (0.20)
ensions in millimeters (inches)	2225	6.60 (0.26)	1.00 (0.04)	4.60 (0.18)	1.00 (0.04)	6.35 (0.25)

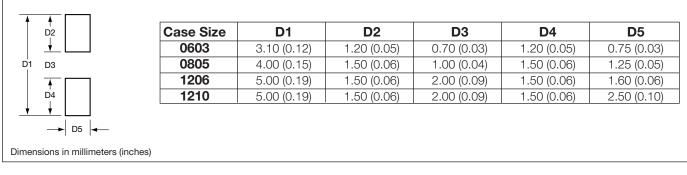
### **REFLOW SOLDERING**

# **Surface Mounting Guide**

**MLC Chip Capacitors** 

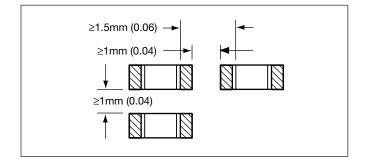


## **WAVE SOLDERING**



#### **Component Spacing**

For wave soldering components, must be spaced sufficiently far apart to avoid bridging or shadowing (inability of solder to penetrate properly into small spaces). This is less important for reflow soldering but sufficient space must be allowed to enable rework should it be required.



#### **Preheat & Soldering**

The rate of preheat should not exceed 4°C/second to prevent thermal shock. A better maximum figure is about 2°C/second.

For capacitors size 1206 and below, with a maximum thickness of 1.25mm, it is generally permissible to allow a temperature differential from preheat to soldering of 150°C. In all other cases this differential should not exceed 100°C.

For further specific application or process advice, please consult AVX.

#### Cleaning

Care should be taken to ensure that the capacitors are thoroughly cleaned of flux residues especially the space beneath the capacitor. Such residues may otherwise become conductive and effectively offer a low resistance bypass to the capacitor.

Ultrasonic cleaning is permissible, the recommended conditions being 8 Watts/litre at 20-45 kHz, with a process cycle of 2 minutes vapor rinse, 2 minutes immersion in the ultrasonic solvent bath and finally 2 minutes vapor rinse.

# **Surface Mounting Guide**



## **MLC Chip Capacitors**

## **APPLICATION NOTES**

#### Storage

Good solderability is maintained for at least twelve months, provided the components are stored in their "as received" packaging at less than 40°C and 70% RH.

#### Solderability

Terminations to be well soldered after immersion in a 60/40 tin/lead solder bath at  $235 \pm 5^{\circ}$ C for  $2\pm 1$  seconds.

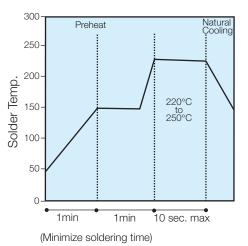
#### Leaching

Terminations will resist leaching for at least the immersion times and conditions shown below.

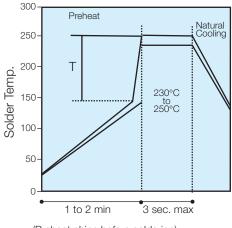
Termination Type	Solder	Solder	Immersion Time
	Tin/Lead/Silver	Temp. °C	Seconds
Nickel Barrier	60/40/0	260±5	30±1

#### **Recommended Soldering Profiles**





#### Wave



(Preheat chips before soldering) T/maximum 150°C

#### General

Surface mounting chip multilayer ceramic capacitors are designed for soldering to printed circuit boards or other substrates. The construction of the components is such that they will withstand the time/temperature profiles used in both wave and reflow soldering methods.

#### Handling

Chip multilayer ceramic capacitors should be handled with care to avoid damage or contamination from perspiration and skin oils. The use of tweezers or vacuum pick ups is strongly recommended for individual components. Bulk handling should ensure that abrasion and mechanical shock are minimized. Taped and reeled components provides the ideal medium for direct presentation to the placement machine. Any mechanical shock should be minimized during handling chip multilayer ceramic capacitors.

#### Preheat

It is important to avoid the possibility of thermal shock during soldering and carefully controlled preheat is therefore required. The rate of preheat should not exceed 4°C/second and a target figure 2°C/second is recommended. Although an 80°C to 120°C temperature differential is preferred, recent developments allow a temperature differential between the component surface and the soldering temperature of 150°C (Maximum) for capacitors of 1210 size and below with a maximum thickness of 1.25mm. The user is cautioned that the risk of thermal shock increases as chip size or temperature differential increases.

#### Soldering

Mildly activated rosin fluxes are preferred. The minimum amount of solder to give a good joint should be used. Excessive solder can lead to damage from the stresses caused by the difference in coefficients of expansion between solder, chip and substrate. AVX terminations are suitable for all wave and reflow soldering systems. If hand soldering cannot be avoided, the preferred technique is the utilization of hot air soldering tools.

#### Cooling

Natural cooling in air is preferred, as this minimizes stresses within the soldered joint. When forced air cooling is used, cooling rate should not exceed 4°C/second. Quenching is not recommended but if used, maximum temperature differentials should be observed according to the preheat conditions above.

#### Cleaning

Flux residues may be hygroscopic or acidic and must be removed. AVX MLC capacitors are acceptable for use with all of the solvents described in the specifications MIL-STD-202 and EIA-RS-198. Alcohol based solvents are acceptable and properly controlled water cleaning systems are also acceptable. Many other solvents have been proven successful, and most solvents that are acceptable to other components on circuit assemblies are equally acceptable for use with ceramic capacitors.

# **Packaging of Chip Components**



## **Automatic Insertion Packaging**

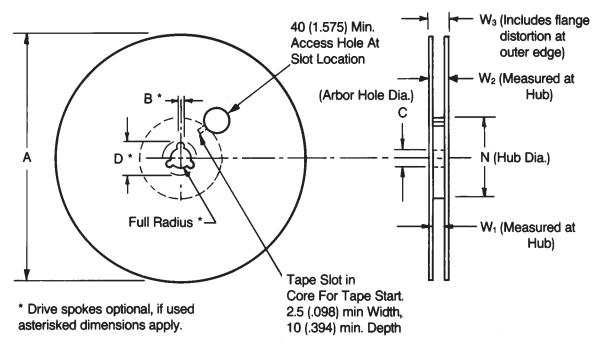
## **TAPE & REEL QUANTITIES**

All tape and reel specifications are in compliance with RS481.

	8mm	12n	nm
Paper or Embossed Carrier	0805, 1005, 1206, 1210		
Embossed Only	0504, 0907	1505, 1805, 1808	1812, 1825 2220, 2225
Paper Only	0402, 0603		
Qty. per Reel/7" Reel	2,000 or 4,000 <sup>(1)</sup>	3,000	1,000
Qty. per Reel/13" Reel	10,000	10,000	4,000

<sup>(1)</sup> Dependent on chip thickness. Low profile chips shown on page 27 are 5,000 per reel for 7" reel. 0402 size chips are 10,000 per 7" reels and are not available on 13" reels. For 3640 size chip contact factory for quantity per reel.

## **REEL DIMENSIONS**



Tape Size <sup>(1)</sup>	A Max.	B* Min.	С	D* Min.	N Min.	W <sub>1</sub>	W <sub>2</sub> Max.	W <sub>3</sub>
8mm	330	1.5	13.0±0.20	20.2	50	$\begin{array}{c} 8.4\substack{+1.0\\-0.0}\\(.331\substack{\pm0.0\\-0.0}^{+0.0})\end{array}$	14.4 (.567)	7.9 Min. (.311) 10.9 Max. (.429)
12mm	(12.992)	(.059)	(.512±.008)	(.795)	(1.969)	$12.4^{\pm 2.9}_{-0.0} \\ (.488^{+.076}_{-0.0})$	18.4 (.724)	11.9 Min. (.469) 15.4 Max. (.607)

Metric dimensions will govern.

English measurements rounded and for reference only.

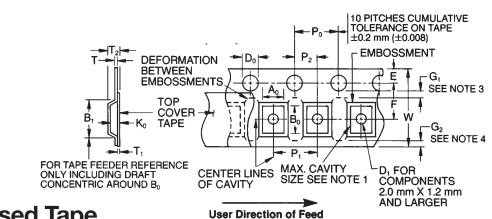
(1) For tape sizes 16mm and 24mm (used with chip size 3640) consult EIA RS-481 latest revision.



# **Embossed Carrier Configuration**



## 8 & 12mm Tape Only



## 8 & 12mm Embossed Tape Metric Dimensions Will Govern

### **CONSTANT DIMENSIONS**

Tape Size	D <sub>0</sub>	E	Po	P <sub>2</sub>	T Max.	T <sub>1</sub>	G <sub>1</sub>	G <sub>2</sub>
8mm and 12mm	$\begin{array}{c} 8.4 \substack{+0.10 \\ -0.0} \\ (.059 \substack{+.004 \\ -0.0}) \end{array}$	1.75 ± 0.10 (.069 ± .004)	4.0 ± 0.10 (.157 ± .004)	2.0 ± 0.05 (.079 ± .002)	0.600 (.024)	0.10 (.004) Max.	0.75 (.030) Min. See Note 3	0.75 (.030) Min. See Note 4

### **VARIABLE DIMENSIONS**

Tape Size	B <sub>1</sub> Max. See Note 6	D <sub>1</sub> Min. See Note 5	F	P <sub>1</sub>	R Min. See Note 2	T <sub>2</sub>	W	A <sub>0</sub> B <sub>0</sub> K <sub>0</sub>
8mm	4.55 (.179)	1.0 (.039)	3.5 ± 0.05 (.138 ± .002)	4.0 ± 0.10 (.157 ± .004)	25 (.984)	2.5 Max (.098)	8.0 <sup>+0.3</sup> (.315 <sup>+.012</sup> 004)	See Note 1
12mm	8.2 (.323)	1.5 (.059)	5.5 ± 0.05 (.217 ± .002)	4.0 ± 0.10 (.157 ± .004)	30 (1.181)	6.5 Max. (.256)	12.0 ± .30 (.472 ± .012)	See Note 1
8mm 1/2 Pitch	4.55 (.179)	1.0 (.039)	3.5 ± 0.05 (.138 ± .002)	2.0 ± 0.10 0.79 ± .004	25 (.984)	2.5 Max. (.098)	8.0 <sup>+0.3</sup> -0.1 (.315 <sup>+.012</sup> 004)	See Note 1
12mm Double Pitch	8.2 (.323)	1.5 (.059)	5.5 ± 0.05 (.217 ± .002)	8.0 ± 0.10 (.315 ± .004)	30 (1.181)	6.5 Max. (.256)	12.0 ± .30 (.472 ± .012)	See Note 1

#### NOTES:

1. A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by the max. dimensions to the ends of the terminals extending from the component body and/or the body dimensions of the component. The clearance between the end of the terminals or body of the component to the sides and depth of the cavity (A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub>) must be within 0.05 mm (.002) min. and 0.50 mm (.020) max. The clearance allowed must also prevent rotation of the component within the cavity of not more than 20 degrees (see sketches C & D).

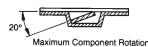
2. Tape with components shall pass around radius "R" without damage. The minimum trailer length (Note 2 Fig. 3) may require additional length to provide R min. for 12 mm embossed tape for reels with hub diameters approaching N min. (Table 4).

3. G, dimension is the flat area from the edge of the sprocket hole to either the outward deformation of the carrier tape between the embossed cavities or to the edge of the cavity whichever is less.

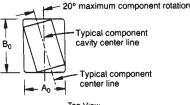
4. G<sub>2</sub> dimension is the flat area from the edge of the carrier tape opposite the sprocket holes to either the outward deformation of the carrier tape between the embossed cavity or to the edge of the cavity whichever is less.

5. The embossment hole location shall be measured from the sprocket hole controlling the location of the embossment. Dimensions of embossment location and hole location shall be applied independent of each other.

6.  $B_1$  dimension is a reference dimension for tape feeder clearance only.



Side or Front Sectional View Sketch "C"

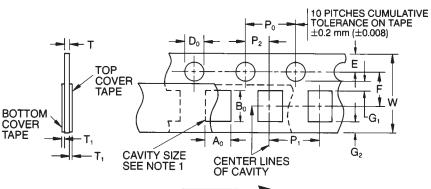


Top View Sketch "D

# **Paper Carrier Configuration**



## 8 & 12mm Tape Only



## 8 & 12mm Paper Tape Metric Dimensions Will Govern

User Direction of Feed

### **CONSTANT DIMENSIONS**

Tape Siz	e D <sub>0</sub>	E	Po	P <sub>2</sub>	T <sub>1</sub>	G <sub>1</sub>	G <sub>2</sub>	R MIN.
8mm and 12mm	1.5 <sup>+0.1</sup> (.059 <sup>+.004</sup> 000	1.75 ± 0.10 (.069 ± .004)	4.0 ± 0.10 (.157 ± .004)	2.0 ± 0.05 (.079 ± .002)	0.10 (.004) Max.	0.75 (.030) Min.	0.75 (.030) Min.	25 (.984) See Note 2

### **VARIABLE DIMENSIONS**

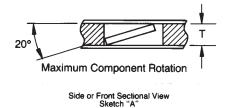
Tape Size	P <sub>1</sub>	F	w	A <sub>0</sub> B <sub>0</sub>	Т
8mm	4.0 ± 0.10 (.157 ± .004)	3.5 ± 0.05 (.138 ± .002)	8.0 <sup>+0.3</sup> (.315 <sup>+.012</sup> )	See Note 1	See Note 3
12mm	4.0 ± .010 (.157 ± .004)	5.5 ± 0.05 (.217 ± .002)	12.0 ± 0.3 (.472 ± .012)		
8mm 1/2 Pitch	2.0 ± 0.10 (.079 ± .004)	3.5 ± 0.05 (.138 ± .002)	8.0 <sup>+0.3</sup> (.315 <sup>+.012</sup> )		
12mm Double Pitch	8.0 ± 0.10 (.315 ± .004)	5.5 ± 0.05 (.217 ± .002)	12.0 ± 0.3 (.472 ± .012)		

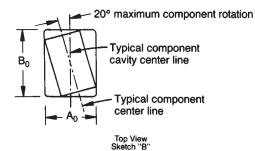
#### NOTES:

1. A<sub>0</sub>, B<sub>0</sub>, and T are determined by the max. dimensions to the ends of the terminals extending from the component body and/or the body dimensions of the component. The clearance between the ends of the terminals or body of the component to the sides and depth of the cavity (A<sub>0</sub>, B<sub>0</sub>, and T) must be within 0.05 mm (.002) min. and 0.50 mm (.020) max. The clearance allowed must also prevent rotation of the component within the cavity of not more than 20 degrees (see sketches A & B).

2. Tape with components shall pass around radius "R" without damage.

3. 1.1 mm (.043) Base Tape and 1.6 mm (.063) Max. for Non-Paper Base Compositions.





## **Bar Code Labeling Standard**

AVX bar code labeling is available and follows latest version of EIA-556-A.



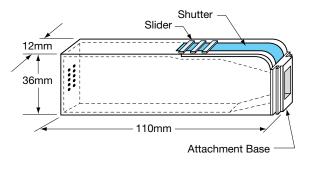
# **Bulk Case Packaging**



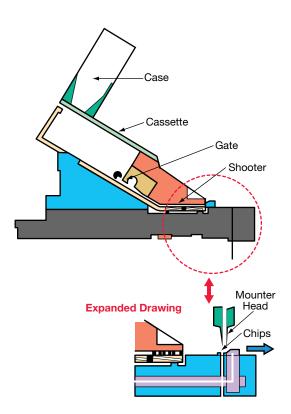
### **BENEFITS**

- Easier handling
- Smaller packaging volume (1/20 of T/R packaging)
- Easier inventory control
- Flexibility
- Recyclable

## **CASE DIMENSIONS**







## **CASE QUANTITIES**

Part Size	0402	0603	0805
Qty. (pcs / cassette)	80,000	15,000	10,000 (T=0.6mm) 5,000 (T≥0.6mm)