12-V/3.3-V Hot Swap and ORing Controller with I²C™ and Load Current Monitor for AdvancedMC™

Check for Samples: TPS2459

FEATURES

- ATCA AdvancedMC™ Compliant
- Full Power Control for an AdvancedMC™ Module
- Independently Programmable 12-V Current Limit and Fast Trip
- 3.3-V and 12-V FET ORing Control for MicroTCA™
- 12-V Output Shuts Off If 3.3-V Output Shuts Off
- Internal 3.3-V Current Limit and ORing
- I²C™ Power Good and Fault Reporting
- I²C™ Programmable Fault Times and Limits
- FET Status Bits for 3.3-V and 12-V Channels
- Load Current Monitors for 12-V and 3.3-V
- 32-Pin QFN Package

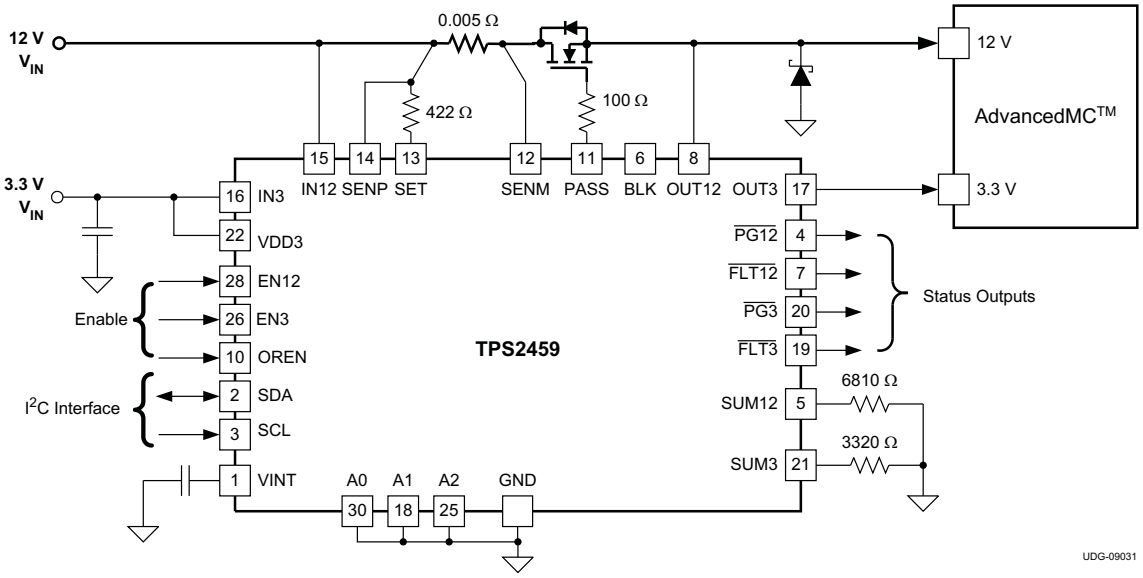
APPLICATIONS

- ATCA Carrier Boards
- MicroTCA™Power Modules
- AdvancedMC™ Slots
- Systems Using 12-V and 3.3-V Channels
- Base Stations

DESCRIPTION

The TPS2459 hot-plug controller performs all necessary power interface functions for an AdvancedMC™ (Advanced Mezzanine Card). A fully integrated 3.3-V channel provides inrush control, over-current protection, and FET ORing. A 12-V channel provides the same functions using external FETs and sense resistors. The 3.3-V current limit is factory set to AdvancedMC™ compliant levels while the 12-V current limit is programmed using external sense resistors. The accurate current sense comparators of the TPS2459 satisfy the narrow ATCA™ AdvancedMC™ current limit requirements.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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I²C is a trademark of Phillips.

ORDERING INFORMATION

DEVICE	TEMPERATURE	PACKAGE	ORDERING CODE	MARKING
TPS2459	-40°C to 85°C	QFN-32	TPS2459RHB	TPS2459

ABSOLUTE MAXIMUM RATINGS(1)

over –40°C ≤ T_J ≤ 85°C (unless otherwise noted)

		VALUE	UNIT
	BLK, PASS	0 to 30	V
	IN12, OUT12, SENM, SENP, SET, EN12	0 to 17	
	EN3 , IN3, OUT3, OREN, SCL, SDA, SUM, VDD,	0 to 5	
	AGND, GND	–0.3 to 0.3	
	A0, A1, A2	0 to V_{INT}	
ESD	Human Body Model	2	kV
	Charged Device Model	0.5	
	SUMx	5	mA
	VINT	–1 to 1	
	OUT3 continuous current	250	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device under any conditions beyond those indicated under recommended operating conditions is neither implied nor guaranteed. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

DISSIPATION RATINGS

PACKAGE	θJ_A HIGH-K (°C/W)	θJ_A LOW-K (°C/W)
QFN32 - RHB	34	93

RECOMMENDED OPERATING CONDITIONS

over –40°C ≤ T_J ≤ 85°C (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
VIN12	12-V input supply	8.5	12	15	V
VIN3	3.3-V input supply	3	3.3	4	
VVDD3		3	3.3	4	
IOUT3	3.3-V output current			165	mA
ISUMx	Summing pin current		100	1000	µA
	PASS pin board leakage current	-1		1	
	VINT bypass capacitance	1	10	250	nF
T_J	Operating junction temperature range	-40		125	°C

ELECTRICAL CHARACTERISTICS

over –40°C ≤ T_J ≤ 85°C, V_{IN3} =V_{VDD3} = 3.3 V, V_{IN12} = V_{SENP} = V_{SENM} = V_{SETP} = 12 V, V_{EN3}=V_{EN12}=logic 1 or open, V_{AGND} = V_{GNDA} = V_{GNDB} = 0 V, V_{SUM12} = 6.8 kΩ to GND, , V_{SUM3} = 3.3 kΩ to GND. All other pins OPEN, all I²C™ bits at different values, all voltages referenced to GND. (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE INPUTS					
Threshold voltage, falling edge		1.2	1.3	1.4	V
Hysteresis		20	50	80	mV
Pullup current	V_{EN} =V_{OREN} = 0 V	5	8	15	µA
Input bias current	V_{EN12} =V_{OREN} = 17 V		6	15	µA
	V_{EN3} = 5 V		1	5	µA
3.3-V Turn off time	EN3 deasserts to V_{VOUT3} < 1.0 V, C_{OUT} = 0 µF			10	µs
12-V Turn off time	EN12 deasserts to V_{VOUT12} < 1.0 V, C_{OUT} = 0 µF, C_{QGATE} = 35 nF			20	µs
POWER GOOD COMPARATORS					
Threshold voltage	$\overline{PG12}$, falling OUT12	10.2	10.5	10.8	V
	$\overline{PG3}$, falling OUT3	2.7	2.8	2.9	V
Hysteresis	$\overline{PG12}$, measured at OUT12		130		mV
	$\overline{PG3}$, measured at OUT3		50		mV
INTERNAL 2.35-V RAIL					
Output voltage	0 V < I_{VINT} < 50 µA	2.0	2.3	2.8	V
FAULT TIMER					
Minimum fault time	3FT[4:0] = 12FT[4:0] = 00001B		1		ms
Fault time bit weight			0.5		ms
Retry duty cycle	D = t_{FAULT}/t_{DELAY}	1.4%	1.5	1.6%	
12-V SUMMING NODE					
Input referred offset	10.8 V ≤ V_{SENM} ≤ 13.2 V, V_{SENP} = (V_{SENM} + 50 mV), measure V_{SET}– V_{SENM}	–1.5		1.5	mV
Summing threshold	12CL[3:0] = 1111B, V_{PASS} = 15 V	0.66	0.675	0.69	V
Leakage current	V_{SET} =(V_{SENM} – 10 mV)			1	µA
12-V CURRENT LIMIT					
Current limit threshold	R_{SUM} = 6.8 kΩ, R_{SET} = 422 Ω, increase I_{LOAD} and measure V_{SENP} – V_{SENM} when V_{PASS} = 15 V	47.5	50	52.5	mV
Sink current in current limit	I_{PASS} measured at V_{SUM} = 1 V and V_{PASS} = 12 V	20		40	µA
Fast trip threshold	Measure V_{SENP} – V_{SENM}	80	100	120	mV
Fast turn-off delay	20 mV overdrive, C_{PASS} = 0 pF, tp50-50		200	300	ns
Bleed-down resistance	V_{OUT} = 6 V	1.1	1.6	2.1	kΩ
Bleed-down threshold		75	100	130	mV
Timer start threshold	V_{PASS} - V_{IN} when timer starts, while V_{PASS} falling due to overcurrent	5	6	7	V

ELECTRICAL CHARACTERISTICS (continued)

over –40°C ≤ T_J ≤ 85°C, V_{IN3} =V_{VDD3} = 3.3 V, V_{IN12} = V_{SENP} = V_{SENM} = V_{SETP} = 12 V, V_{EN3}=V_{EN12}=logic 1 or open, V_{AGND} = V_{GNDA} = V_{GNDB} = 0 V, V_{SUM12} = 6.8 kΩ to GND, , V_{SUM3} = 3.3 kΩ to GND. All other pins OPEN, all I²C™ bits at different values, all voltages referenced to GND. (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
12-V UVLO					
UVLO rising	IN12 rising	8.1	8.5	8.9	V
UVLO hysteresis	IN12 falling	0.44	0.5	0.59	
12-V BLOCKING					
Turn-on threshold	Measure V_{SENP} – V_{VOUT}	5	10	15	mV
Turn-off threshold	Measure V_{SENP} – V_{VOUT}	–6	–3	0	
Turn-off delay	20-mV overdrive, C_{BLK} = 0 pF, t_{P50-50}		200	300	ns
12-V GATE DRIVERS (PASS, BLK)					
Output voltage	V_{VIN12} = V_{VOUT12} = 10 V	21.5	23	24.5	V
Sourcing current	V_{VIN12} = V_{VOUT12} = 10 V, V_{PASS}= V_{BLK} = 17 V	20	30	40	µA
Sinking current	Fast turnoff, V_{PASS} = V_{BLK} = 14 V	0.5	1		A
	4 V ≤ V_{PASS} = V_{BLK} ≤ 25 V	6	14	25	mA
Pulldown resistance	In OTSD (at 150°C)	14	20	26	kΩ
Fast turn-off duration		5	10	15	µs
Startup time	IN12 rising to PASS and BLK sourcing			0.25	ms
3.3-V SUMMING NODE					
Summing threshold		655	675	695	mV
3.3-V CURRENT LIMIT					
On-resistance	I_{OUT3} = 150 mA		290	500	mΩ
Current limit	R_{SUM3} = 3.3 kΩ , V_{VOUT3} = 0 V	170	195	225	mA
Fast trip threshold		240	300	400	
Fast turn-off delay	I_{OUT3}= 400 mA, t_{P50-50}		750	1300	ns
Bleed-down resistance	V_{OUT3}= 1.65 V	280	400	500	Ω
Bleed-down threshold		75	100	130	mV
3.3-V UVLO					
UVLO rising	IN3 rising	2.65	2.75	2.85	V
UVLO hysteresis	IN3 falling	200	240	300	mV
3.3-V BLOCKING					
Turn-on threshold	Measure V_{IN3} – V_{OUT3}	5	10	15	mV
Turn-off threshold	Measure V_{IN3} – V_{OUT3}	–5	–3	0	mV
ORing turn-on delay time	V_{IN3} = 3.3 V, V_{OUT3} = 3.5 V, R_{OUT3} = 100 Ω to GND, V_{ORON} = 1. Remove 3.5 V from OUT3. Measure time from V_{OUT3} decreasing thru 2.9 V to V_{OUT3} = 3.2 V		300	350	µs
Fast turnoff delay time	20 mV overdrive, t_{P50-50}		250	350	ns
Safety gate pulldown current (1)	Slew IN3x, Out3x, 5-V in 1 µs			15	mA
SUPPLY CURRENTS (I_{IN}+I_{SENP}+I_{SENM}+I_{SET}+I_{VDD})					
Both channels enabled	I_{OUT3A} = I_{OUT3B}= 0		3.1	4	mA
Both channels disabled			2.0	2.8	
THERMAL SHUTDOWN					
Whole-chip shutdown temperature	T_J rising, I_{OUT3A} = I_{OUT3B}= 0 A	140	150		°C
3.3-V channel shutdown temperature	T_J rising, I_{OUT3A} or I_{OUT3B} in current limit	130	140		
Hysteresis	Whole chip or 3.3-V channel		10		

(1) When setting an address bit to a logic 1 the pin should be connected to VINT.

ELECTRICAL CHARACTERISTICS (continued)

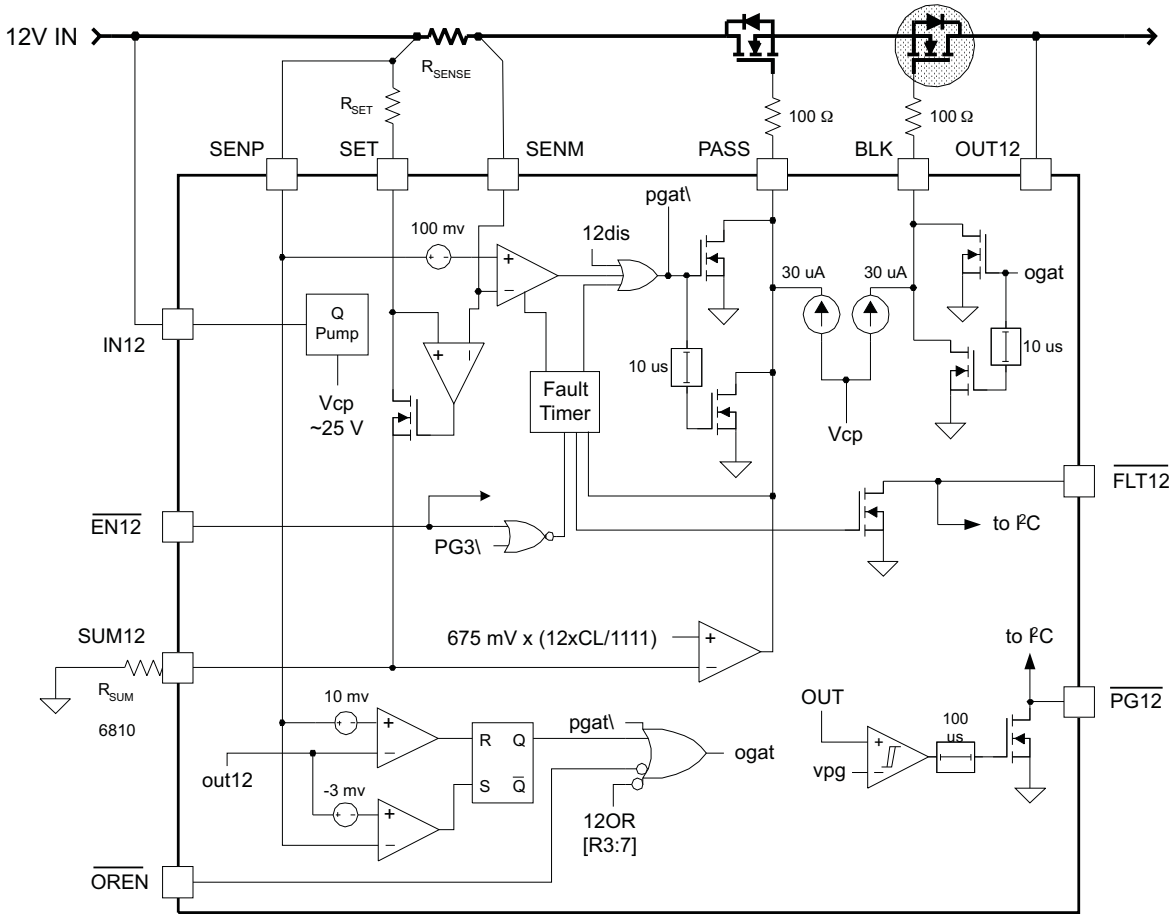
over –40°C ≤ T_J ≤ 85°C, V_{IN3} =V_{VDD3} = 3.3 V, V_{IN12} = V_{SENP} = V_{SENM} = V_{SETP} = 12 V, V_{EN3}=V_{EN12}=logic 1 or open, V_{AGND} = V_{GNDA} = V_{GNDB} = 0 V, V_{SUM12} = 6.8 kΩ to GND, , V_{SUM3} = 3.3 kΩ to GND. All other pins OPEN, all I²C™ bits at different values, all voltages referenced to GND. (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I²C™ SERIAL INTERFACE (SDA, SCL, A0, A1, A2)					
Lower logic threshold	A0, A1, A2	0.33	0.35	0.37	V
Upper logic threshold	A0, A1, A2	1.32	1.35	1.38	V
Input pullup resistance	A0, A1, A2, (V_{Ax} – 0 V)	400	700	1000	kΩ
Input pulldown resistance	A0, A1, A2, (V_{Ax} – V_{VINT})(2)	200	350	550	kΩ
Input open-circuit voltage	I_A = 0 V	0.5	0.8	1.0	V
Threshold voltage, rising	SDA, SCL			2.3	V
Threshold voltage, falling	SDA, SCL	1.0			V
Hysteresis	SDA, SCL	165			mV
Leakage	SDA, SCL			1	μA
Input clock frequency	SCL			400	kHz
Low-level output voltage	I_{SDA} = 3 mA			0.4	V
Input clock low duration	SCL	1.3			μs
Input clock high duration	SCL	0.6			μs
Data setup time	SDA	100			ns
Data hold time	SDA	300		900	ns
Output fall time	SDA, 2.3 V–1.0 V, C_{BUS} = 10 pF	21		250	ns
	SDA, 2.3 V–1.0 V, C_{BUS} = 400 pF	60		250	
Deglitch time	SDA, pulse width suppressed	0		50	ns
Capacitance	C_{SDA}, C_{SCL}			10	pF

(2) When setting an address bit to a logic 1 the pin should be connected to VINT.

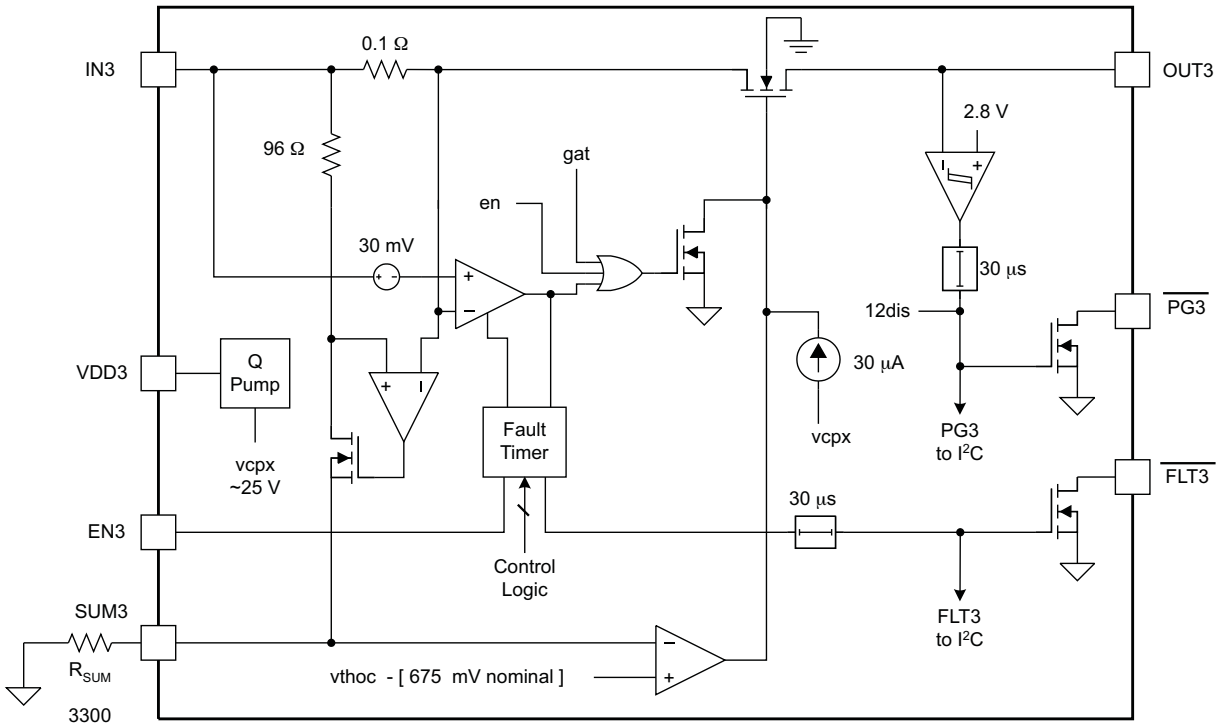
TPS2459 FUNCTIONAL BLOCK DIAGRAMS

12-V Channel Circuitry

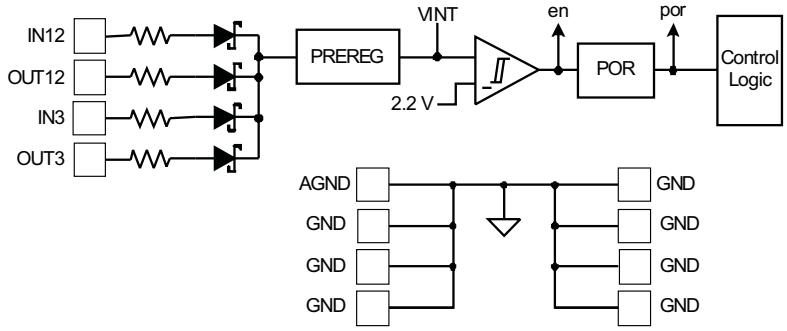


Optional Oring FET for Redundant Power Feed Systems

3.3-V Channel Circuitry



Circuitry Common to Both Channels



DEVICE INFORMATION

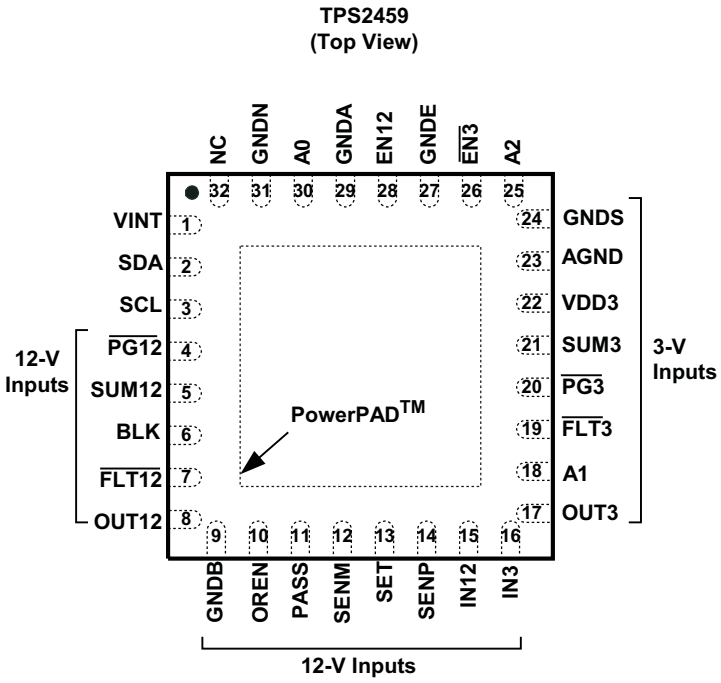


Figure 1.

TERMINAL FUNCTIONS

NAME	PIN NO.	I/O	DESCRIPTION
A0	30	I	I²C™ address programming bit, LSB
A1	18	I	I²C™ address programming bit, LSB+1
A2	25	I	I²C™ address programming bit, LSB+2
AGND	23	—	Analog ground. Ground pin for the analog circuitry insideBypass capacitor connection point for internal supply the TPS2459.
BLK	6	O	12-V blocking transistor gate drive. Gate drive pin for the 12-V channel BLK FET. This pin sources 30 μA to turn the FET on. An internal clam prevents this pin from rising more than 14.5 V above OUT12. Setting the $\overline{\text{OREN}}$ pin high holds the BLK pin low.
EN12	28	I	12-V enable. (active high). Pulling this pin low turns off the 12-V channel by pulling both BLK and PASS low. An internal 200-kΩ resistor pulls this pin up to VINT when disconnected.
EN3	26	I	3-V enable. (active high) Pulling this pin low turns off the 3-V channel by pulling the gate of the internal pass FET to GND. An internal 200-kΩ resistor pulls this pin up to VINT when disconnected.
$\overline{\text{FLT12}}$	7	O	12-V fault output (active low) Open-drain output indicating that channel 12 has remained in current limit long enough to time out the fault timer and shut the channel down. asserted when 12-V fault timer runs out
$\overline{\text{FLT3}}$	19	O	3-V fault output (active low) Open-drain output indicating that channel 3 has remained in current limit long enough to time out the fault timer and shut the channel down. asserted when 3-V fault timer runs out
GNDA	29	—	12-V power ground.
GNDB	9		
GNDE	27	—	Ground.
GNDN	31		
GNDS	24		
IN3	16	I	3-V input. Supply pin for the 3-V channel internal pass FET.
IN12	15	I	12-V input. Supply pin for 12-V channel internal circuitry.
NC	32	—	No connection.

TERMINAL FUNCTIONS (continued)

NAME	PIN NO.	I/O	DESCRIPTION
OREN	10	I	12-V blocking transistor enable. (active high). Pulling this pin high (or allowing it to float high) allows the 12-V channel ORing function to operate normally. Pulling this pin low disables the 12-V ORing function by pulling the BLK pin low. An internal 200-kΩ resistor pulls this pin up to VINT when disconnected.
OUT12	8	I/O	12-V output. Senses the output voltage of the 12-V channel.
OUT3	17	I/O	3-V output. Output of the 3-V channel internal pass FET.
PASS	11	O	12-V pass transistor gate drive. This pin sources 30 μA to turn the FET on. An internal clamp prevents this pin from rising more than 14.5 V above IN12.
$\overline{PG12}$	4	O	12-V power good output,asserts when $V_{OUT12} > V_{\overline{PG12}}$ (active low) . Open-drain output indicating that channel 12 output voltage has dropped below the PG threshold, which nominally equals 10.5 V.
$\overline{PG3}$	20	O	3-V power good output, asserts when $V_{OUT3} > 2.8$ V (active low) . Open-drain output indicating that channel 3 output voltage has dropped below the PG threshold, which nominally equals 2.85 V.
SCL	3	I	Serial clock input for the I²C™ data line. (See TPS2459 *I²C™ Interface* section for details.)
SDA	2	I/O	Bidirectional I²C™ data line. (See TPS2459 *I²C™ Interface* section for details.)
SENM	12	I	12-V current limit sense. Senses the voltage on the low side of the 12-V channel current sense resistor.
SENP	14	I	12-V input sense. Senses the voltage on the high side of the 12-V channel current sense resistor.
SET	13	I	12-V current limit set. A resistor connected from this pin to SENP sets the current limit level in conjunction with the current sense resistor and the resistor connected to the SUM12 pin, as described in 12-V thresholds, setting current limit and fast overcurrent trip section.
SUM12	5	I/O	12-V summing node. A resistor connected from this pin to ground forms part of the channel x current limit. As the current delivered to the load increases, so does the voltage on this pin. When the voltage on this pin reaches 675 mV, the current limit amplifier acts to prevent the current from further increasing.
SUM3	21	I/O	3-V summing node. A resistor connected from this pin to ground forms part of the channel x current limit. As the current delivered to the load increases, so does the voltage on this pin. When the voltage on this pin reaches 675 mV, the current limit amplifier acts to prevent the current from further increasing.
VDD3	22	I	3-V charge pump input
VINT	1	I/O	Bypass capacitor connection point for internal supply. This pin connects to the internal 2.35-V rail. A 0.1-μF capacitor must be connected from this pin to ground. **Do not connect other external circuitry to this pin except the address programming pins,** as required.

TYPICAL CHARACTERISTICS

ORING TURN-OFF THRESHOLD vs JUNCTION TEMPERATURE

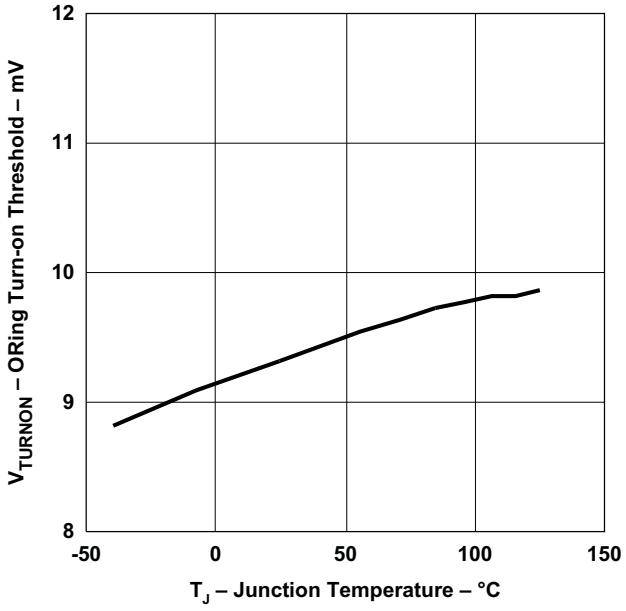


Figure 2.

ORING TURN-ON THRESHOLD vs JUNCTION TEMPERATURE

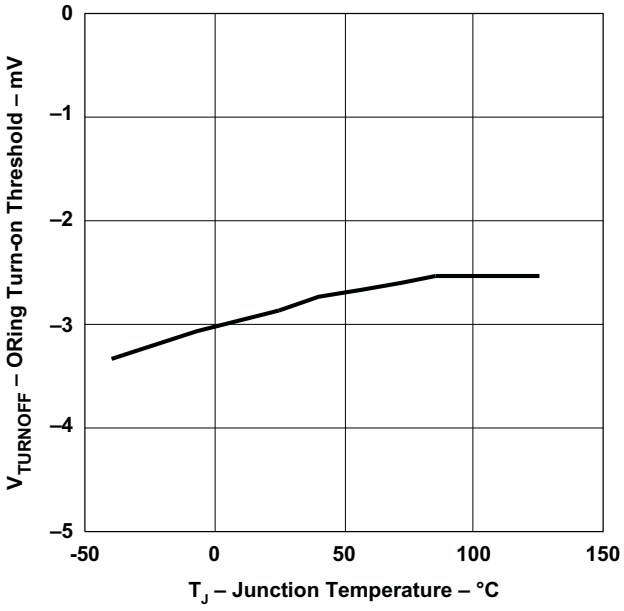


Figure 3.

12-V TURN OFF VOLTAGE THRESHOLD vs JUNCTION TEMPERATURE

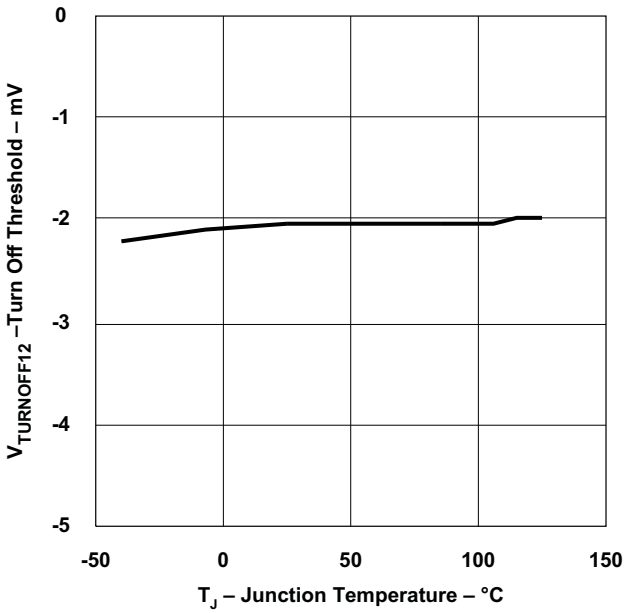


Figure 4.

12-V TURN ON THRESHOLD vs JUNCTION TEMPERATURE

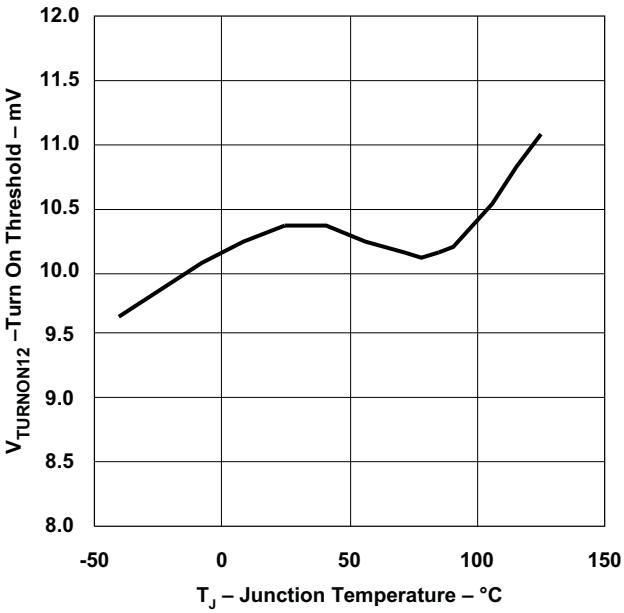


Figure 5.

TYPICAL CHARACTERISTICS (continued)

12-V INPUT CURRENT vs JUNCTION TEMPERATURE

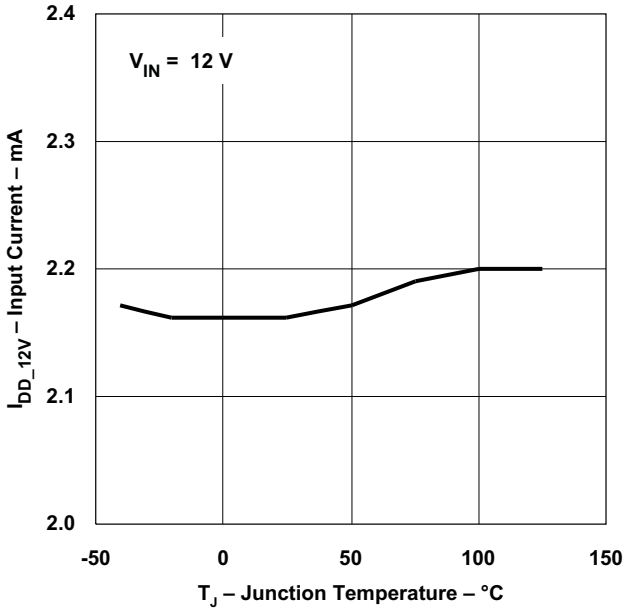


Figure 6.

3-V INPUT CURRENT vs JUNCTION TEMPERATURE

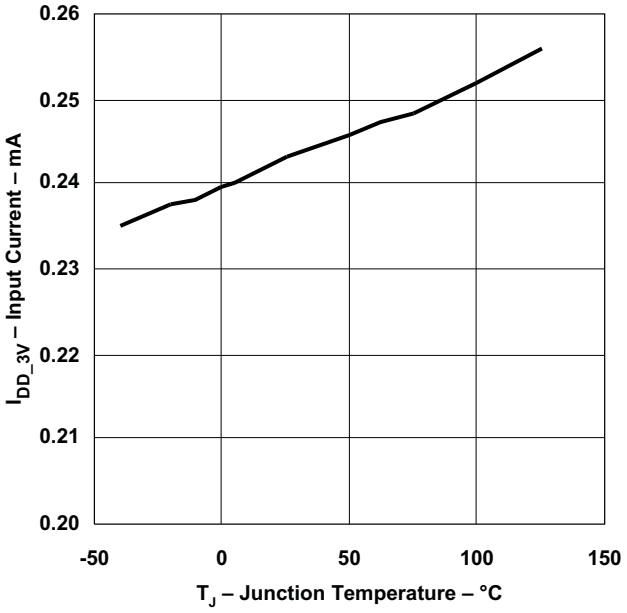


Figure 7.

12-V INPUT CURRENT vs INPUT VOLTAGE

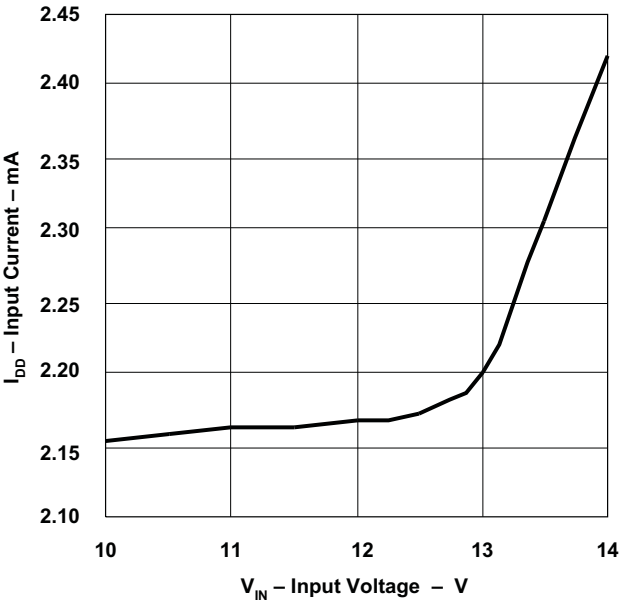


Figure 8.

12-V CURRENT LIMIT THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

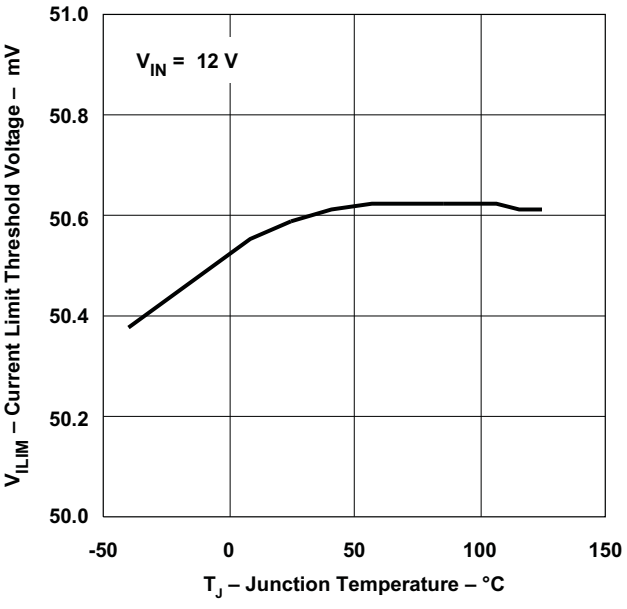


Figure 9.

TYPICAL WAVEFORMS

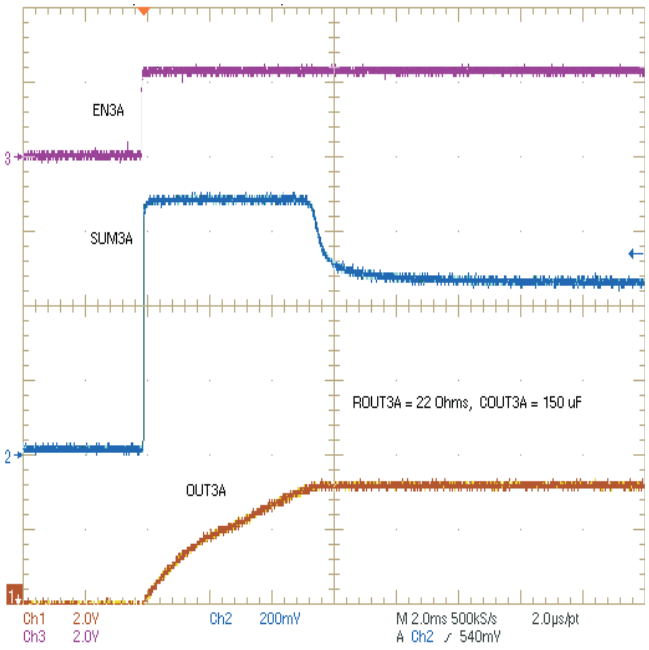


Figure 10. OUT3 Startup Into 22-Ω, (150 mA), 150-µF Load

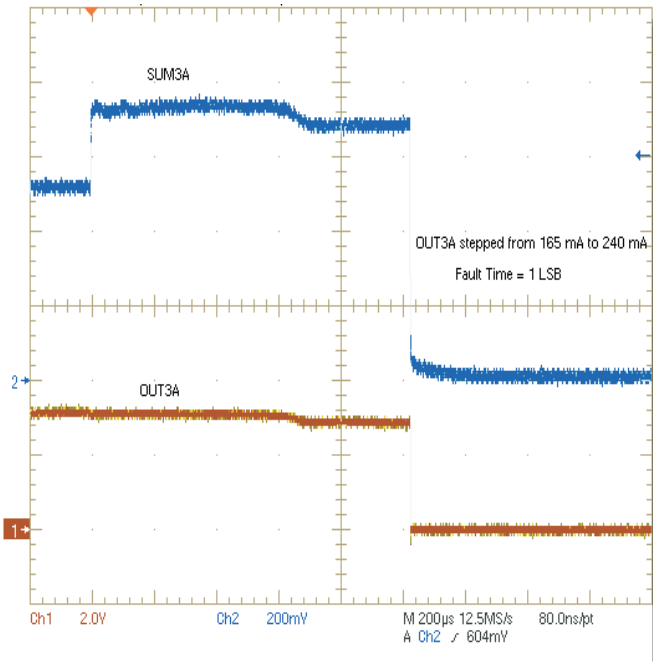


Figure 11. OUT3 Load Stepped from 165 mA to 240 mA

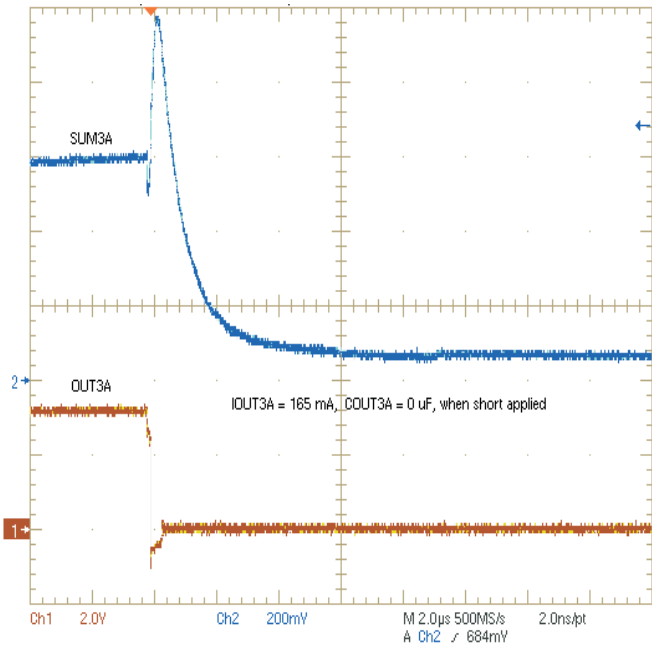


Figure 12. OUT3 Short Circuit Under Full Load, (165 mA), Zoom View

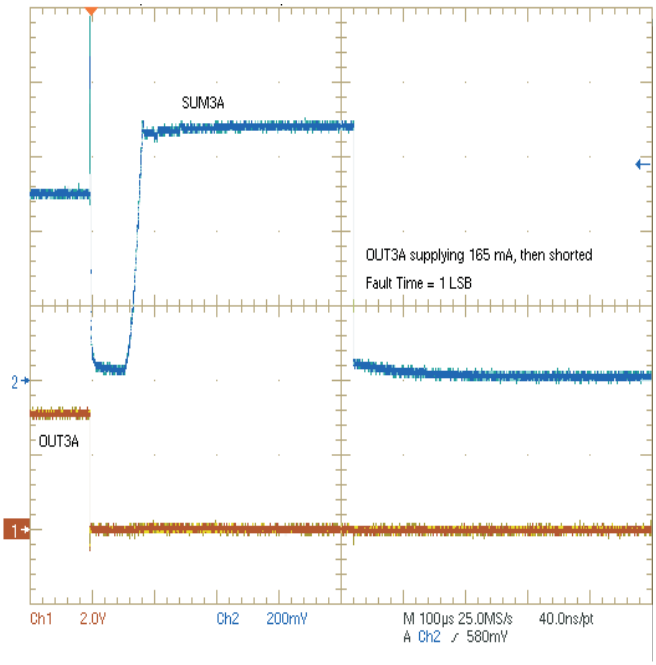


Figure 13. OUT3 Short Circuit Under Full Load, (165 mA), Wide View

TYPICAL WAVEFORMS (continued)

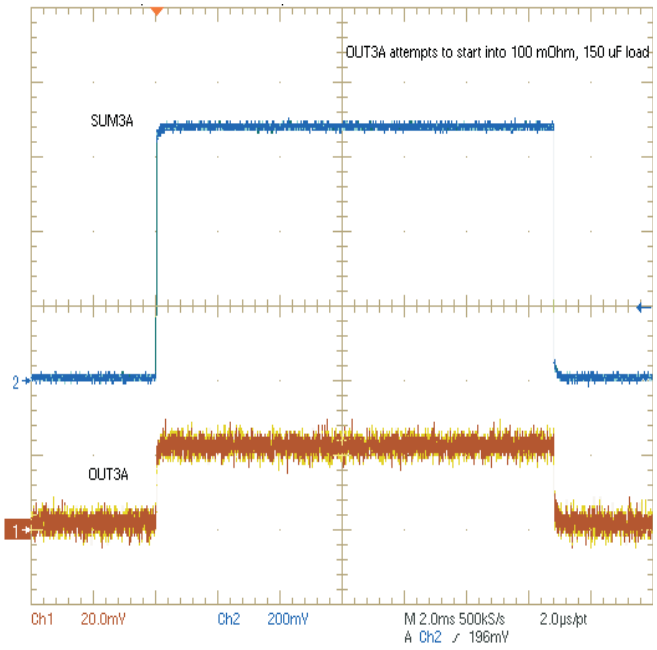


Figure 14. OUT3 Startup Into Short Circuit

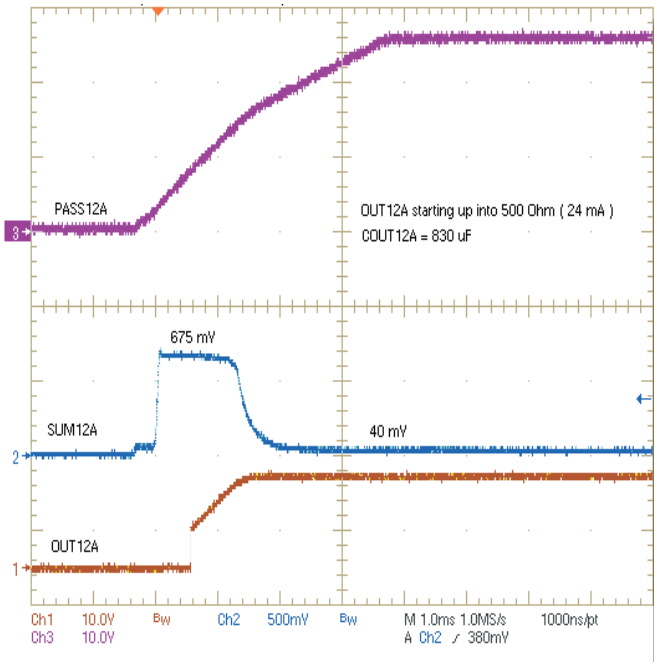


Figure 15. OUT12 Startup Into 500-Ω, 830-µF Load

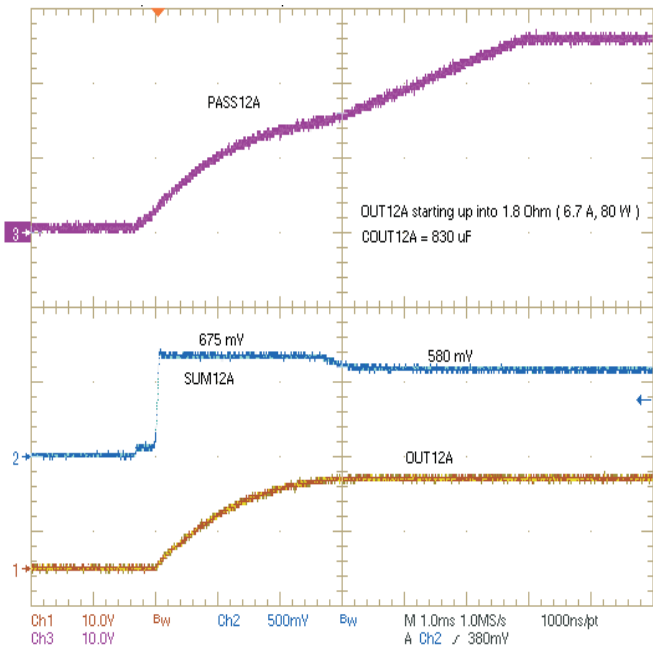


Figure 16. OUT12 Startup Into 80-W, 830-µF Load

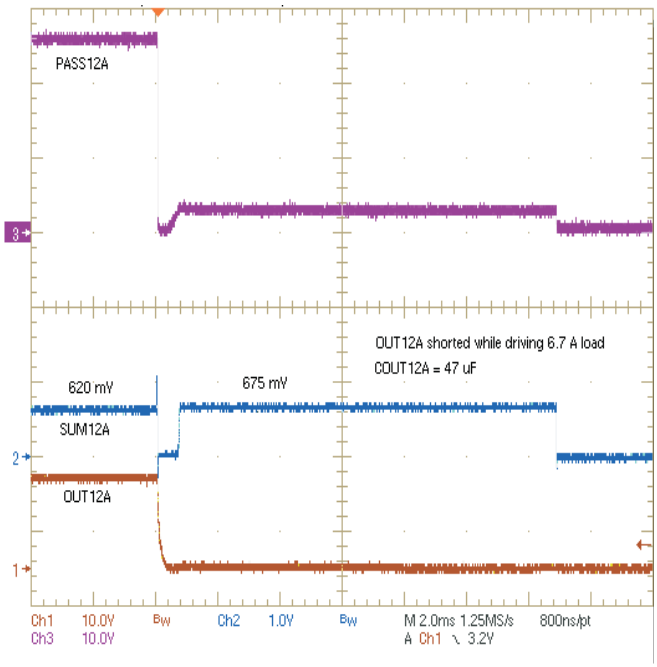


Figure 17. OUT12 Short Circuit Under Full Load, (6.7 A), Wide View

TYPICAL WAVEFORMS (continued)

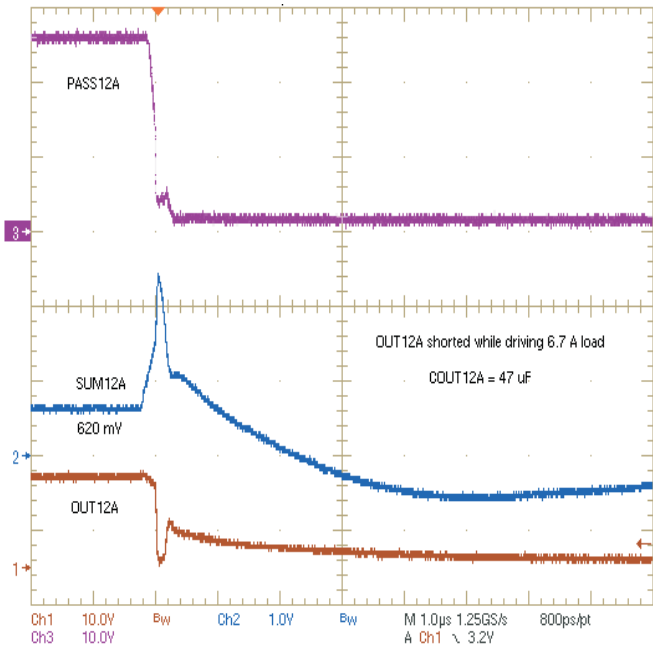


Figure 18. OUT12 Short Circuit Under Full Load, (6.7 A), Zoom View

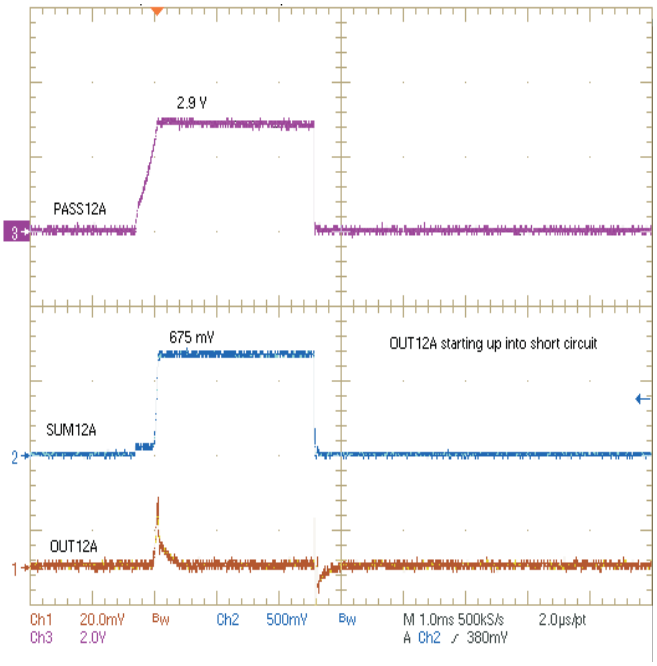


Figure 19. OUT12 Startup Into Short Circuit

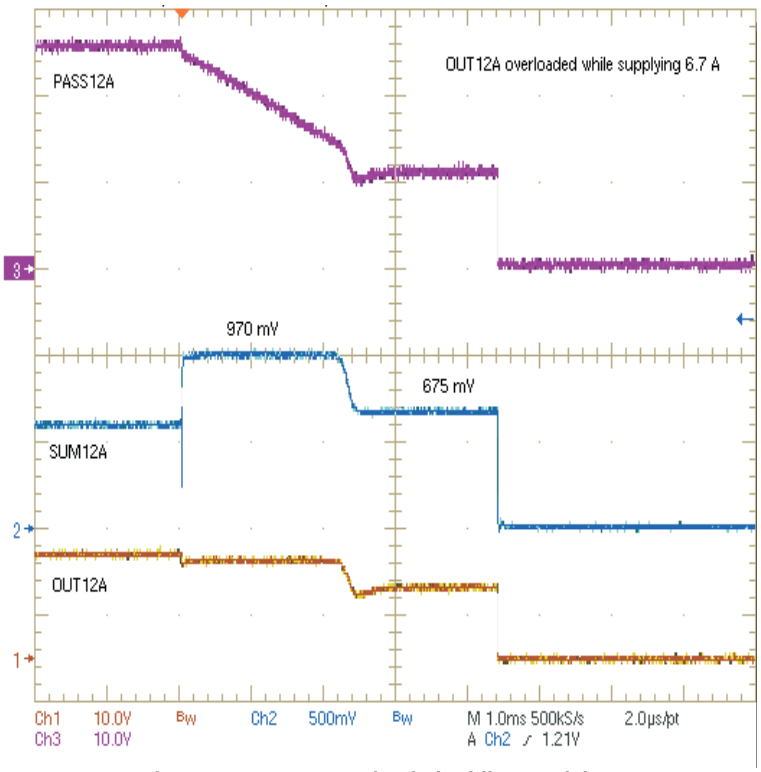


Figure 20. OUT12 Overloaded While Supplying 6.7 A

Control and Status Registers

Seven 8-bit registers are used to control and read the status of the TPS2459. Registers 3 and 4 control the 12-V channel. Rregister 5 controls the 3-V channel. Register 6 contains eight general configuration bits. Read-only registers 7, 8, and 9 report back system status to the I^{2}C™ controller. All ten registers use the I^{2}C™ protocol and are organized as follows shown in Table 1.

Table 1. Top Level Register Functions

REGISTER	FUNCTION		VOLTAGE (V)		DESCRIPTION
	READ	WRITE	3.3	12	
3	√	√		√	Set 12-V current limit, power good level, and OR functions
4	√	√			Set 12-V fault time, enable, and bleed-down functions
5		√	√		Set 3-V fault time, enable, and bleed-down functions
6	√	√	√	√	System configuration controls
7		√	√	√	Fault and PG outputs
8		√		√	Overcurrent and fast trip indicators are latched
9		√	√	√	Channel status indicators

Summary of Registers

Table 2. Summary of Registers

BIT	NAME	DEFAULT	DESCRIPTION
REGISTER 3 READ/WRITE			**12-V CHANNEL CONFIGURATION**
0	12CL0	1	Clearing bit reduces 12-V current limit and fast threshold by 5%.
1	12CL1	1	Clearing bit reduces 12-V current limit and fast threshold by 10%.
2	12CL2	1	Clearing bit reduces 12-V current limit and fast threshold by 20%.
3	12CL3	1	Clearing bit reduces 12-V current limit and fast threshold by 40%.
4	12PG0	1	Clearing bit reduces 12-V power good threshold by 600 mV.
5	12PG1	1	Clearing bit reduces 12-V power good threshold by 1.2 V.
6	12HP	0	Setting bit shifts 12 OR $V_{TURNOFF}$ from –3 mV to +3 mV nominal.
7	12OR	1	Clearing bit turns off 12-V ORing FET by pulling BLK low.
REGISTER 4 READ/WRITE			**12-V CHANNEL CONFIGURATION**
0	12FT0	1	Setting bit increases 12-V fault time by 0.5 ms.
1	12FT1	0	Setting bit increases 12-V fault time by 1 ms.
2	12FT2	0	Setting bit increases 12-V fault time by 2 ms.
3	12FT3	0	Setting bit increases 12-V fault time by 4 ms.
4	12FT4	0	Setting bit increases 12-V fault time by 8 ms.
5	12EN	0	Clearing bit disables 12-V by pulling PASSB and BLKB to 0 V.
6	12UV	0	Setting bit prevents enabling unless OUT12 < bleed-down threshold.
7	12DS	0	Clearing bit disconnects OUT12 bleed-down resistor.
REGISTER 5 READ/WRITE			**3.3-V CHANNEL CONFIGURATION**
0	3FT0	1	Setting bit increases 3 V fault time by 0.5 ms.
1	3FT1	0	Setting bit increases 3 V fault time by 1 ms.
2	3FT2	0	Setting bit increases 3 V fault time by 2 ms.
3	3FT3	0	Setting bit increases 3 V fault time by 4 ms.
4	3FT4	0	Setting bit increases 3 V fault time by 8 ms.
5	3EN	0	Clearing bit disables 3 V.
6	3UV	0	Setting bit prevents enabling unless OUT3B < bleed-down threshold.
7	3DS	0	Clearing bit disconnects OUT3B bleed-down resistor.
REGISTER 6 READ/WRITE			**SYSTEM CONFIGURATION**
0	PPTEST	0	12-V pulldown test pin. Setting pin pulls the PASS and BLK pins to 0 V.
1	FLTMODE	0	Clearing bit latchs off channels after over-current fault. Setting bit allows channels to automatically attempt restart after fault.
2	ENPOL	0	This bit must be 0.
3	3ORON	0	Setting bit enables 3-V channel to prevent reverse current flow.
4	12VNRS	0	Non Redundant System in rush control bit. Setting bit allows increased inrush current in 12-V channel .
5	DISA	0	This bit must be set to 1
6	spare	0	
7	DCC	0	Setting bit allows the 12-V channels to operate despite loss of 3.3-V. This bit should be low for μTCA and AMC applications

Table 2. Summary of Registers (continued)

BIT	NAME	DEFAULT	DESCRIPTION
REGISTER 7 READ ONLY			**LATCHED CHANNEL STATUS INDICATORS, CLEARED ON READ**
0	spare	—	
1			
2			
3			
4	$\overline{12PG}$	0	Latches high when OUT12 goes from above VTH_PG to below VTH_PG.
5	12FLT	0	Latches high when 12 fault timer has run out.
6	$\overline{3PG}$	0	Latches high when OUT3 goes from above VTH_PG to below VTH_PG.
7	3FLT	0	Latches high when 3-V fault timer has run out.
REGISTER 8 READ ONLY			**LATCHED OVERCURRENT INDICATORS, CLEARED ON READ**
0	spare	—	
1			
2			
3			
4	12OC	0	Latches high when 12-V channel goes into over-current.
5	12FTR	0	Latches high if 12-V fast trip threshold exceeded.
6	3OC	0	Latches high when 3-V enters over-current.
7	3FTR	0	Latches high if 3-V fast trip threshold exceeded.
REGISTER 9 READ ONLY			**UNLATCHED FET STATUS INDICATORS**
0	spare	–	
1	spare		
2	spare		
3	12BS	–	High indicates BLK commanded high.
4	$\overline{12PS}$	–	Low indicates (V_{PASS} > V_{OUT} + 6 V).
5	$\overline{3BS}$	–	Low indicates V_{IN3} > V_{OUT3}.
6	spare		
7	3GS	–	Low indicates 3 V channel gate is driven on V_{GATE} > (V_{IN} + 1.75 V).

DETAILED DESCRIPTION OF REGISTERS

Table 3. Register 3: 12-V Channel Configuration (Read/Write)

BIT	NAME	DEFAULT	DESCRIPTION
0	12CL0	1	Clearing bit reduces 12-V current limit and fast threshold by 5%.
1	12CL1	1	Clearing bit reduces 12-V current limit and fast threshold by 10%.
2	12CL2	1	Clearing bit reduces 12-V current limit and fast threshold by 20%.
3	12CL3	1	Clearing bit reduces 12-V current limit and fast threshold by 40%.
4	12PG0	1	Clearing bit reduces 12-V power good threshold by 600 mV.
5	12PG1	1	Clearing bit reduces 12-V power good threshold by 1.2 V.
6	12HP	0	Setting bit shifts 12-V OR VTURNOFF from –3 mV to +3 mV nominal.
7	12OR	1	Clearing bit turns off 12-V ORing FET by pulling BLK low.

12CL[3:0] These four bits adjust the 12-V current limit and fast trip threshold using the I2CTM interface. Setting the bits to 1111B places the 12-V current limit at its maximum level, corresponding to 675 mV at SUM12. The fast trip threshold then equals 100 mV. Clearing all bits reduces the current limit and fast trip threshold to 25% of these maximums.

12PG[1:0] These two bits adjust the 12-V power good threshold. Setting the bits to 11B places the power good threshold at its maximum level of 10.5 V . Setting the bits to 00B places the threshold at its minimum level of 8.7 V. The lower thresholds may prove desirable in systems that routinely experience large voltage droops.

12HP Setting this bit moves the 12-V ORing turn off threshold from –3 mV to +3 mV. A positive threshold prevents reverse current from flowing through the channel, but it may cause the ORing FET to repeatedly cycle on-and-off if the load is too light to maintain the required positive voltage drop across the combined resistance of the external FETs and the sense resistor. For further information, see *Adjusting ORing Turn Off Threshold For High Power Loads* section.

12OR Clearing this bit forces the BLK pin low, keeping the 12-V ORing FET off. Clearing this bit does not prevent current from flowing through the FET's body diode.

Table 4. Register 4: 12-V Channel Configuration (Read/Write)

BIT	NAME	DEFAULT	DESCRIPTION
0	12FT0	1	Setting bit increases 12-V fault time by 0.5 ms.
1	12FT1	0	Setting bit increases 12-V fault time by 1 ms.
2	12FT2	0	Setting bit increases 12-V fault time by 2 ms.
3	12FT3	0	Setting bit increases 12-V fault time by 4 ms.
4	12FT4	0	Setting bit increases 12-V fault time by 8 ms.
5	12EN	0	Clearing bit disables 12-V by pulling PASS and BLK to 0 V.
6	12UV	0	Setting bit prevents enabling unless OUT12 < bleed-down threshold.
7	12DS	0	Clearing bit disconnects OUT12 bleed-down resistor.

12FT[4:0] These five bits adjust the 12-V channel fault time. The least-significant bit has a nominal weight of 0.5 ms, so fault times ranging from 0.5 ms (for code 00001B) to 15.5 ms (for code 11111B) can be programmed. In general the shortest fault time that fully charges downstream bulk capacitors without generating a fault should be used. Once the load capacitors have fully charged, the fault time can be reduced to provide faster short circuit protection. See *Setting Fault Time* section.

12EN This bit serves as a master enable for the 12-V channel. Setting the bit allows the 12-V channel to operate normally. Clearing the bit disables the channel by pulling PASS and BLK low.

12UV Setting this bit prevents 12-V channel from turning on until VOUT12 falls below the bleed-down threshold of 100 mV. This feature ensures that downstream devices reset by requiring their supply voltage to fall to nearly zero before the channel can enable them.

12DS Clearing this bit disconnects the bleed-down resistor that otherwise connects from OUT12 to ground. Systems using redundant power supplies should clear 12DS to prevent the bleed-down resistor from continuously sinking current.

Table 5. Register 5: 3.3-V Channel Configuration (Read/Write)

BIT	NAME	DEFAULT	DESCRIPTION
0	3FT0	1	Setting bit increases 3-V fault time by 0.5 ms.
1	3FT1	0	Setting bit increases 3-V fault time by 1 ms.
2	3FT2	0	Setting bit increases 3-V fault time by 2 ms.
3	3FT3	0	Setting bit increases 3-V fault time by 4 ms.
4	3FT4	0	Setting bit increases 3-V fault time by 8 ms.
5	3EN	0	Clearing bit disables 3-V.
6	3UV	0	Setting bit prevents enabling unless OUT3 < bleed-down threshold.
7	3DS	0	Clearing bit disconnects OUT3 bleed-down resistor.

3FT[4:0] These five bits adjust the 3-V channel fault time. The least-significant bit has a nominal weight of 0.5 ms, so fault times ranging from 0.5 ms (for code 00001B) to 15.5 ms (for code 11111B) can be programmed. In general the shortest fault time that fully charges downstream bulk capacitors without generating a fault should be used. See the *Setting Fault Time* section.

3EN This bit serves as a master enable for the 3-V channel. Setting this bit allows the 3-V channel to operate normally, provided the EN3 pin is also asserted. Clearing this bit disables the channel by removing gate drive to the internal pass FET, regardless of the state of the EN3 pin.

3UV Setting this bit prevents the 3-V channel from turning on until VOUT3 falls below the bleed-down threshold of 100 mV. This feature ensures that downstream devices reset by requiring their supply voltage to fall to nearly zero before the channel can enable them.

3DS Clearing this bit disconnects the bleed-down resistor that otherwise connects from OUT3 to ground. Systems using redundant power supplies should clear 3DS to prevent the bleed-down resistor from continuously sinking current.

Table 6. Register 6: System Configuration (Read/Write)

BIT	NAME	DEFAULT	DESCRIPTION
0	PPTEST	0	12V pulldown test pin. Asserting this pulls the PASS and BLK pins to 0 V.
1	FLTMODE	0	Clearing bit forces channels to latch off after over-current fault. Setting bit allows channels to automatically attempt restart after fault.
2	ENPOL ENP	0	This bit must be 0.
3	3ORON	0	Setting bit enables 3.3-V channel to prevent reverse current flow.Clearing bit disables 3A and 3B ORing.
4	12VNRS	0	Non-redundant system inrush control bit. Setting bit allows increased inrush current in 12-V channel
5	DISA	0	This bit must be set to 1.
6	spare	0	
7	DCC	0	Setting bit allows the 12-V channel to operate despite loss of 3.3 V. For μTCA and AMC applications this bit should be low.

PPTEST This bit is used for testing the fast turnoff feature of the PASS and BLK pins. Setting this bit enables the fast turnoff drivers for all four pins. Clearing this bit restores normal operation. PPTEST allows the fast turnoff drivers to operate at full current indefinitely, whereas they would normally operate for only approximately 15 μs. While using PPTEST the energy dissipated in the fast turnoff drivers must be externally limited to 1 mJ per driver to prevent damage to the TPS2459.

FLTMODE Setting this bit allows a channel to attempt an automatic restart after an overcurrent condition has caused it to time out and shut off. The retry period equals approximately 100 times the programmed fault time. The FLTMODE bit affects all four channels. If cross-connection is enabled (DCC = 0), a fault on the 3.3-V channel turns off the 12-V channel. If the 3.3-V channel automatically restarts because FLTMODE = 1, the 12-V channel remains disabled until its enable bit (12EN) is cycled off and on.

ENPOL This bit must be 0.

3ORON Setting this bit allows the 3.3-V ORing function to operate normally. Clearing this bit prevents a VOUT3 > VIN3 condition from turning off the 3 V channel and forces 3A / 3B ORing to behave as if IN3A >> OUT3A, and IN3B >> OUT3B... This bit is typically cleared for non-redundant systems.

12VNRS Setting this bit increases the current limit for the 12-V channel to its maximum value during the initial inrush period that immediately follows the enabling of the channel. During inrush, the current limit behaves as if 12CL[3:0] = 1111B. After the current drops below this limit, signifying the end of the inrush period, the current limit returns to normal operation. This function is intended for use in non-redundant systems with capacitive loads. Setting this bit forces the 12-V current limiters to behave as though the current limit adjust bits R0[3:0], R3[3:0] are set to 1111 right after EN asserts and will persist until the channel comes out of current limit or the fault timer times out, whichever comes first.

DISA This bit must be set to 1.

DCC Setting this bit disables cross-connection. If DCC = 0, when the 3.3-V channel experiences a fault, both it and the 12-V channel turn off. If DCC = 1, then the 12-V channel continues to operate even if the 3.3-V channel experiences a fault.

Table 7. Register 7: Latched Channel Status Indicators (Read-only, cleared on read)

BIT	NAME	DEFAULT	DESCRIPTION
0	spare	–	
1	spare		
2	spare		
3	spare		
4	$\overline{12PG}$	0	Latches high when OUT12 goes from above VTH_PG to below VTH_PG. This bit is set each time channel is turned on. A second read cycle will indicate true status.
5	12FLT	0	Latches high when 12-V fault timer has run out.
6	$\overline{3PG}$	0	Latches high when OUT3 goes from above VTH_PG to below VTH_PG. This bit is set each time channel is turned on. A second read cycle will indicate true status.
7	3FLT	0	Latches high when 3 V fault timer has run out.

$\overline{12PG}$ This bit is set if the voltage on OUT12 drops below the power-good threshold set by the 12PG[1:0] bits, and it remains set until Register 7 is read.

12FLT This bit is set if the fault timer on the 12-V channel has run out, and it remains set until Register 7 is read.

$\overline{3PG}$ This bit is set if the voltage on OUT3 drops below the power-good threshold, and it remains set until Register 7 is read.

3FLT This bit is set if the fault timer on the 3.3-V channel runs out, and it remains set until Register 7 is read.

Table 8. Register 8: Latched Status Indicators (Read-only, cleared on read)

BIT	NAME	DEFAULT	DESCRIPTION
0	spare	–	
1	spare		
2	spare		
3	spare		
4	12OC	0	Latches high when 12-V channel enters overcurrent.
5	12FTR	0	Latches high if 12-V fast trip threshold exceeded.
6	3BOC	0	Latches high when 3 V channel enters over-current.
7	3BFTR	0	Latches high if 3 fV ast trip threshold exceeded.

12OC This bit is set if the voltage on the PASS pin drops below the timer start threshold, signifying a current limit condition. This bit remains set until Register 8 is read. This bit is set each time channel is turned on. A second read cycle after turn on is required to determine true status.

12FTR This bit is set if the voltage across the sense resistor for the 12-V channel exceeds the fast trip threshold. This bit remains set until Register 8 is read. This bit remains set until Register 8 is read. This bit is set each time channel is turned on. A second read cycle after turn on is required to determine true status.

3OC This bit is set if the gate-to-source voltage on the 3 V channel pass FET drops low enough to start the fault timer. This bit remains set until Register 8 is read. This bit remains set until Register 8 is read. This bit is set each time channel is turned on. A second read cycle after turn on is required to determine true status.

3FTR This bit is set if the current through the 3 V channel exceeds the fast trip threshold. This bit remains set until Register 8 is read.

Table 9. Register 9: Unlatched Status Indicators (Read-only)

BIT	NAME	DEFAULT	DESCRIPTION
0	spare	–	
1	spare		
2	spare		
3	12BS	–	High indicates BLK commanded high.
4	$\overline{12PS}$	–	Low indicates $V_{PASS} > V_{OUT} + 6$ V.
5	$\overline{3BS}$	–	Low indicates $V_{IN3} > V_{OUT3}$.
6	spare		
7	$\overline{3GS}$	–	Low indicates channel 3 gate is driven on ($V_{GATE} > V_{IN} + 1.75$ V).

12BS This bit goes high when the 12-V ORing logic commands the BLK pin high (25 V) and the BLK FET should be on.

$\overline{12PS}$ This bit goes low when the 12-V PASS pin is above the timer start threshold (OUT12 + 7 V), indicating that the 12-V PASS FET should be on.

$\overline{3BS}$ This bit goes low when the 3 V ORing logic commands the 3 V pass FET on, indicating that a reverse blocking condition does not exist.

$\overline{3GS}$ This bit goes low when the 3 V FET gate-to-source voltage exceeds 1.75 V, indicating that the 3 V FET should be on.

APPLICATION INFORMATION

The TPS2459 has been designed to simplify compliance with the PICMG-AMC.R2.0 and PICMG-MTCA.0 specifications. These specifications were developed by the PCI Industrial Computer Manufacturers Group (PICMG). These two specifications are derivations of the PICMG-ATCA (Advanced Telecommunication Computing Architecture) specification originally released in December, 2002.

PICMG-AMC Highlights

- AMC – Advanced Mezzanine Cards
- Designed to Plug into ATCA Carrier Boards
- AdvancedMC™ Focuses on Low Cost
- 1 to 8 AdvancedMC™ per ATCA Carrier Board
- 3.3-V Management Power – Maximum Current Draw of 150 mA
- 12-V Payload Power – Converted to Required Voltages on AMC
- Maximum 80 W Dissipation per AdvancedMC™
- Hotswap and Current Limiting and must be Present on Carrier Board
- For details, see www.picmg.org/

PICMG-MTCA Highlights

- MTCA – MicroTelecommunications Computing Architecture
- Architecture for Using AMCs without an ATCA Carrier Board
- Up to 12 AMCs per System, plus Two MicroTCA Carrier Hub (MCH)s, plus Two Cooling Units (CU)s
- Focuses on Low Cost – Commoditizes the Hardware
- All Functions of ATCA Carrier Board must be Provided
- MicroTCA is also known as MTCA, mTCA, μTCA or uTCA
- For details, see www.picmg.org/

Introduction

The TPS2459 controls a 12-V power path and a 3.3-V power path in a 32-pin QFN package. An I^2C™ interface enables the implementation using one small integrated circuit, but it also provides many opportunities for design customization. The following sections describe the main functions of the TPS2459 and provide guidance for designing systems around this device.

Control Logic and Power-On Reset

The TPS2459 circuitry, including the I^2C™ interface, draws power from an internal bus fed by a preregulator. A capacitor attached to the VINT pin provides decoupling and output filtering for this preregulator. It can draw power from either of the two inputs (IN12, IN3) or from either of two outputs (OUT12, OUT3). This feature allows the internal circuitry to function regardless of which channels receive power, or from what source. The two external FET drive pins (PASS, BLK) are held low during startup to ensure that the 12-V channel remains off. The internal 3.3-V channel is also held off. When the voltage on the internal VINT rail exceeds approximately 1 V, the power-on reset circuit loads the internal registers with the default values listed in *Detailed Description of Registers* section.

Enable Functions

Table 10 lists the specific conditions required to enable the two channels of the TPS2459. The 3.3-V channel has an active-high enable pin with a 200-kΩ internal pullup resistor. The enable pin must be pulled high, or allowed to float high, to enable the channel. The I²C™ interface includes an enable bit for each of the two channels. The bit corresponding to a channel must be set to enable the channel. Both channels also include bleed-down threshold comparators. Setting the bleed-down control bit ensures that a channel cannot turn on until its output voltage drops below about 100 mV. This feature supports applications in which removal and restoration of power re-initializes the state of downstream loads. The 12-V channel also includes a cross-connection feature to support PICMG.AMC™ and MicroTCA™ requirements. When enabled, this feature ensures that when the 3.3-V output drops below 2.85 V, the 12-V channel automatically shuts off. This feature can be disabled by setting the DCC bit in Register 6.

Table 10. Enable Requirements

CHANNEL (V)	ENABLE PINS	ENABLE BITS	BLEED DOWN	CROSS CONNECTION
3.3	EN3 > 1.4 V	3EN = 1	OUT3 > 0.1 V or 3UV = 0	
12	EN12 > 1.4 V	12EN = 1	OUT12 > 0.1 V or 12UV = 0	$\overline{3PG}$ = 0 or DCC = 1

Fault, Powergood, Overcurrent and FET Status Bits

The TPS2459 I²C™ interface includes six status bits for each channel, for a total of 12 bits. These status bits occupy registers 7, 8, and 9. Table 11 summarizes the locations of these bits.

Table 11. Location

NAME	FUNCTION	REGISTER[BIT]	
		12-V CHANNEL	3-V CHANNEL
$\overline{PG}$	Powergood	R7[4]	R7[6]
$\overline{FLT}$	Overcurrent time-out fault	R7[5]	R7[7]
OC	Momentary overcurrent	R8[4]	R8[6]
FTR	Overcurrent fast trip	R8[5]	R8[7]
12BS	12-V block FET status	R9[3]	–
$\overline{12PS}$	12-V pass FET status	R9[4]	
$\overline{3BS}$	3-V block status	–	R9[5]
$\overline{3GS}$	3-V gate status	R9[7]	

Current Limit and Fast Trip Thresholds

Both channels monitor current by sensing the voltage across a resistor. The 3.3-V channel uses an internal sense resistor with a nominal value of 290 mΩ. The 12-V channel uses an external sense resistor that typically lies in the range of 4 mΩ to 10 mΩ. Each channel features two distinct thresholds: a current limit threshold and a fast trip threshold.

The current limit threshold sets the regulation point of a feedback loop. If the current flowing through the channel exceeds the current limit threshold, then this feedback loop reduces the gate-to-source voltage imposed on the pass FET. This causes the current flowing through the channel to settle to the value determined by the current limit threshold. For example, when a module first powers up, it draws an inrush current to charge its load capacitance. The current limit feedback loop ensures that this inrush current does not exceed the current limit threshold.

The current limit feedback loop has a finite response time. Serious faults such as shorted loads require a faster response in order to prevent damage to the pass FETs or voltage sags on the supply rails. A comparator monitors the current flowing through the sense resistor, and if it ever exceeds the fast trip threshold it immediately shuts off the channel. Then it will immediately attempt a normal turn on which allows the current limit feedback loop time to respond. The fast trip threshold is normally set 2 to 5 times higher than the current limit.

3.3-V Current Limiting

The 3.3-V management power channel includes an internal pass FET and current sense resistor. The on-resistance of the management channel (including pass FET, sense resistor, metallization resistance, and bond wires) typically equals 290 mΩ and never exceeds 500 mΩ. The AdvancedMC™ specification allows a total of 1 Ω between the power source and the load. The TPS2459 never consumes more than half of this requirement.

3.3-V Fast Trip Function

The 3.3-V fast trip function protects the channel against short-circuit events. If the current through the channel exceeds a nominal value of 300 mA, then the TPS2459 immediately disables the internal pass transistor and then allows it to slowly turn back on into current limiting.

3.3-V Current Limit Function

The 3.3-V current limit function internally limits the current to comply with the AdvancedMC™ and MicroTCA™ specifications. External resistor R_{SUM3} allows the user to adjust the current limit threshold. The nominal current limit threshold I_{LIMIT} is shown in Equation 1.

$$I_{LIMIT} = \frac{650\,V}{R_{SUM3}} \quad (1)$$

A 3320-Ω resistor gives a nominal current limit of I_{LIMIT} = 195 mA which complies with AdvancedMC™ and MicroTCA™ specifications. This resistance corresponds to an EIA 1% value. Alternatively, a 3.3-kΩ resistor also suffices. Whenever the 3.3-V channel enters current limit, its fault timer begins to operate (see *Fault Timer Programming* section).

3.3-V Over-Temperature Shutdown

The 3.3-V over-temperature shutdown is enabled if the 3.3 V channel remains in current limit while the die temperature exceeds approximately 140°C. When this occurs, the channel operating in current limit turns off until the chip cools by approximately 10°C.

3.3-V ORing

The 3.3-V channel limits reverse current flow by sensing the input-to-output voltage differential and turning off the internal pass FET when this differential drops below –3 mV. This corresponds to a nominal reverse current flow of 10 mA. The pass FET turns back on when the differential exceeds +10 mV. These thresholds provide a nominal 13 mV of hysteresis to help prevent false triggering. This feature allows the implementation of redundant power supplies (also known as supply ORing).

If the 3.3-V channel does not use redundant supplies, the 3ORON bit can be cleared to disable the ORing circuitry. This precaution eliminates the chance that transients might trigger the ORing circuitry and upset system operation.

12-V Fast Trip and Current Limiting

Figure 21 shows a simplified block diagram of the circuitry associated with the fast trip and current limit circuitry in the 12-V channel, which requires an external N-channel pass FET and three external resistors. These resistors allow the user to independently set the fast trip threshold and the current limit threshold, as described below.

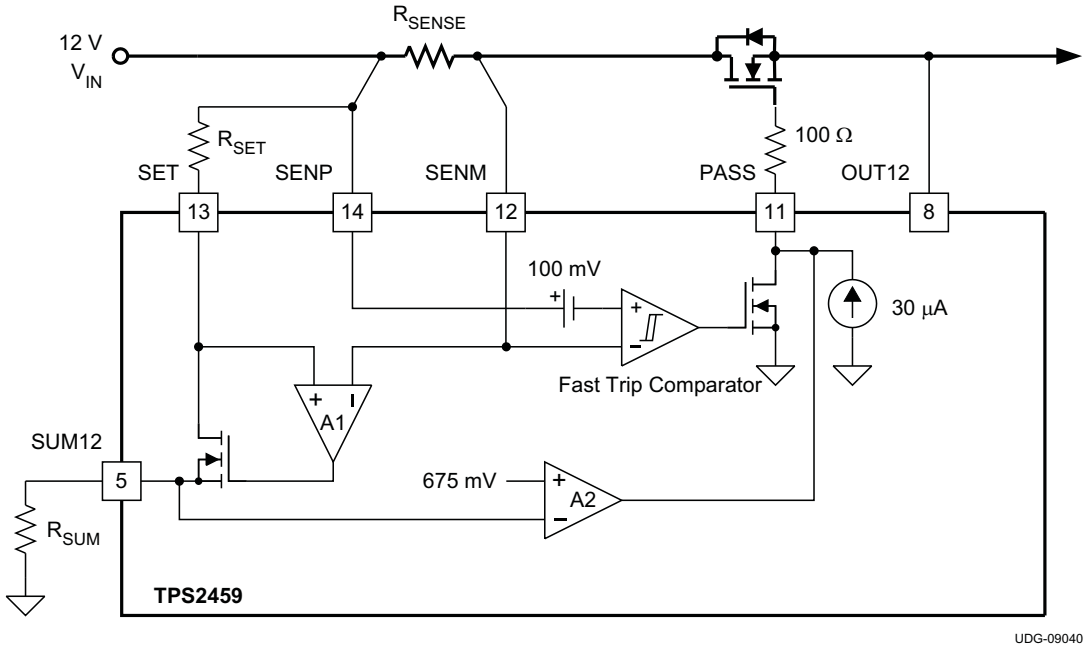


Figure 21. 12-V Channel Threshold Circuitry

12-V Fast Trip Function

The 12-V fast trip function protects the channel against short-circuit events. If the voltage across external resistor R_{SENSE} exceeds the fast trip threshold, then the TPS2459 immediately disables the pass transistor. The 12CL bits set the magnitude of the fast trip threshold. When 12CL = 1111B, the fast trip threshold nominally equals 100 mV. The fast trip current I_{FT} corresponding to this threshold is shown in Equation 2.

$$I_{FT} = \frac{100\,mV}{R_{SENSE}} \tag{2}$$

The recommended value of (R_{SENSE} = 5 mΩ) sets the fast trip threshold at 20 A for 12CL = 1111B. This choice of sense resistor corresponds to the maximum 19.4 A inrush current allowed by the MicroTCA™ specification.

12-V Current Limit Function

The 12-V current limit function regulates the PASS pin voltage to prevent the current through the channel from exceeding I_{LIMIT}. The current limit circuitry includes two amplifiers, A_1 and A_2, as shown in Figure 21. Amplifier A_1 forces the voltage across external resistor R_{SET} to equal the voltage across external resistor R_{SENSE}. The current that flows through R_{SET} also flows through external resistor R_{SUM}, generating a voltage on the 12SUM pin is shown in Equation 3.

$$V_{12SUM} = \left(\frac{R_{SENSE} \times R_{SUM}}{R_{SET}} \right) \times I_{SENSE} \tag{3}$$

Amplifier A2 senses the voltage on the 12SUM pin. As long as this voltage is less than the reference voltage on its positive input (nominally 0.675 V for 12CL = 1111B), the amplifier sources current to PASS. When the voltage on the 12SUM pin exceeds the reference voltage, amplifier A2 begins to sink current from PASS. The gate-to-source voltage of pass FET MPASS drops until the voltages on the two inputs of amplifier A2 balance. The current flowing through the channel then nominally is shown in Equation 4.

$$I_{LIMIT} = \left(\frac{R_{SET}}{R_{SUM} \times R_{SENSE}} \right) \times 0.675\,V \quad (4)$$

The recommended value of R_{SUM} is 6810 Ω. This resistor should never equal less than 675 Ω to prevent excessive currents from flowing through the internal circuitry. Using the recommended values of R_{SENSE} = 5 mΩ and R_{SUM} = 6810 Ω gives Equation 5.

$$I_{LIMIT} = \left(\frac{0.0198\,A}{\Omega} \right) \times R_{SET} \quad (5)$$

A system capable of powering an 80-W AdvancedMC™ module consumes a maximum of 8.25 A according to MicroTCA™ specifications. The above equation suggests R_{SET} = 417 Ω. The nearest 1% EIA value equals 422 Ω. The selection of R_{SET} for MicroTCA™ power modules is described in the *Redundant vs. Non-redundant Inrush Current Limiting* section.

12-V Inrush Slew Rate Control

Although it is possible to slow the gate slew rate, it is very unlikely that would be necessary since the TPS2459 limits inrush current at turn on. The limit level is programmed by the user.

As normally configured, the turn-on slew rate of the 12-V channel output voltage V_{OUT} is shown in Equation 6.

$$\frac{\Delta V_{OUT}}{\Delta t} \cong \frac{I_{SRC}}{C_g} \quad (6)$$

where

- I_{SRC} equals the current sourced by the PASS pin (nominally 30 μA)
- C_g equals the effective gate capacitance

For purposes of this computation, the effective gate capacitance approximately equals the reverse transfer capacitance, C_{RSS}. To reduce the slew rate, increase C_g by connecting additional capacitance from PASS to ground. Place a resistor of at least 1000 Ω in series with the additional capacitance to prevent it from interfering with the fast turn off of the FET.

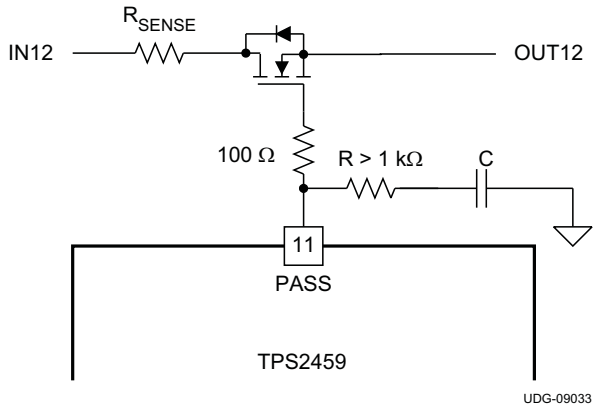


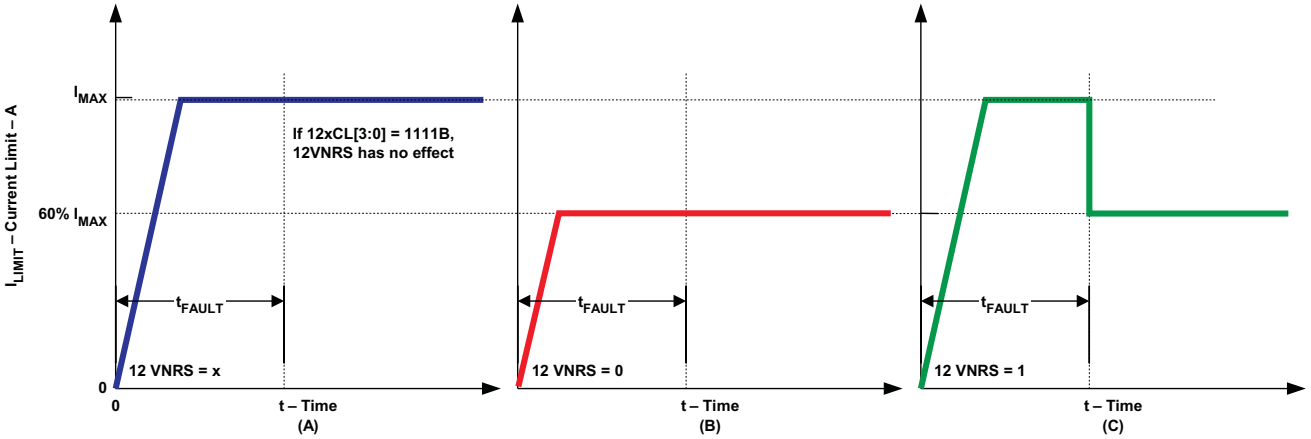
Figure 22. RC Slew Rate Control

Redundant vs. Non-Redundant Inrush Current Limiting

The TPS2459 can support redundant and non-redundant systems. Redundant systems generally use a single fixed current limit, as described above. Non-redundant systems often allow a higher current limit during inrush to compensate for the lack of a redundant supply. The MicroTCA™ standard allows up to 19.4 A for up to 200 ms in non-redundant systems, while limiting individual supplies in redundant systems to 9.1 A at all times. Designers can optimize the performance of the system for either application by properly setting the 12VNRS bit that controls inrush limiting. The ability to change the inrush profile using 12VNRS makes it possible to reconfigure a controller for redundant or non-redundant operation with a single bit. This is particularly useful for MicroTCA Power Modules which may be deployed in redundant or non-redundamnt systems.

The 12VNRS bit affects the value of the 12CL bits during inrush. Setting 12VNRS causes the current limit threshold and fast trip threshold to behave as if 12CL = 1111B during inrush. Once the current flowing through the channel falls below the current limit threshold, the current limit threshold and fast trip threshold correspond to the actual values of the 12CL bits.

Figure 23 illustrates the behavior of the 12VNRS bit. Figure A shows that setting the 12CL bits to 1111B results in a current limit equal to I_{MAX}. Figure 6B shows how the 12CL bits affect the current limit when the 12VNRS bit is cleared. Setting 12CL = 0111B reduces the current limit to 60% of I_{MAX}. Figure C shows how the 12CL bits affect the current limit when the 12VNRS bit is set. The current limit initially equals I_{MAX}, but as soon as the current drops below this level, the current limit resets to 60% of I_{MAX} and remains there so long as the channel remains enabled.



A. 12xCL[3:0] = 111B

B. The characteristics shown represent the current *limit* level versus time. It is not a representation of current versus time.

Figure 23. Current Limits in Redundant and Non-Redundant Systems

Current Limiting Design Examples

Example One

Set up a 12-V channel input voltage to start into an 80-W load and charge a 1600-μF capacitor in less than 3 ms. Set an operational I_{LIMIT} of 8.25 A ±10%.

Equation 7 calculate how much current is needed for capacitor charging and powering the load.

$$I_{STARTUP} = I_{CHARGE} + I_{LOAD} = 6.4\,A + 6.67\,A = 13.7\,A$$

where

- $I_{CHARGE} = \frac{C \times V}{t} = \frac{1600\,\mu F \times 12\,V}{0.003\,s} = 6.4\,A$
- $I_{LOAD} = \frac{P_{LOAD}}{V_{LOAD}} = \frac{80\,W}{12\,V} = 6.67\,A$ (7)

Next, use Equation 8 to calculate R_{SET} for an I_{LIMIT} of 13.7 A.

$$R_{SET} = \frac{(I_{LIMIT} \times R_{SENSE} \times R_{SUM})}{0.675} = 691\,\Omega$$

where

- R_{SUM} = 6810 Ω
- R_{SENSE} = 5 Ω (8)

The closest 1% value is 698 Ω. The I_{LIMIT} can be calculated in Equation 9.

$$I_{LIMIT} = \frac{0.675 \times R_{SET}}{R_{SENSE} \times R_{SUM}} = 13.83\,A \quad (9)$$

If R3[3:0] are set to 0111 and R6[4] = 1 the current limit drops to 60% of the programmed maximum after dropping out of current limit following inrush. The operational current limit is calcualted in Equation 10.

$$I_{LIMIT} = 0.6 \times I_{INRUSH} = 0.6 \times 13.83\,A = 8.3\,A \quad (10)$$

The new 8.38-A current limit is within the specification of 8.25 A ±10 %. Note. These calculations use all nominal values and neglect di/dt rates at turn on.

Example Two

Set up 12-A to startup into an 80-W load and charge a 1600 μF at not more than 17-A nominal. Then drop to an operational I_{LIMIT} of 8.25 A ±10%.

$I_{STARTUP}$ = 17 A

The correct R_{SET} must be found to set maximum I_{LIMIT} to less than 17 A.

$$R_{SET} = \frac{(I_{LIMIT} \times R_{SENSE} \times R_{SUM})}{0.675} = 857\,\Omega$$

where

- R_{SUM} = 6810 Ω
- R_{SENSE} = 5 Ω (11)

The closest 1% value is 845 Ω.

$$I_{LIMIT} = \frac{0.675 \times R_{SET}}{R_{SENSE} \times R_{SUM}} = 16.75\,A \quad (12)$$

Neglecting the current slew time, charge the 1600-μF capacitor in 1.9 ms.

If R3[3:0] are set to 0101 and R6[4] = 1 the current limit drops to 50% of the programmed maximum after dropping out of current limit following inrush. The operational current limit is calculated in Equation 13.

$$I_{LIMIT} = 0.5 \times I_{INRUSH} = 0.5 \times 16.75\,A = 8.38\,A \quad (13)$$

The new 8.38-A current limit is within the specification of 8.25 A ±10 %.

Note. These calculations use all nominal values.

Table 12. Configuring 12-V Current Limits in Non-Redundant Systems

R_{SET}	12CLx [3:0]	I_{LIMIT} (A) – INRUSH 12VNRS		I_{LIMIT} (A) OPERATIONAL 12VNRS = 1	P_{LOAD} (W)	C_{BULK} CHARGE TIME (ms)		FAULT TIME (ms)	
		R6[4]=0	R6[4]=1			800 µF	1600 µF	800 µF	1600 µF
412	1111	8.17	8.17	8.17	80	6.4	12.8	8.5	17
698	111	13.84	8.3	8.3	80	1.34	2.68	2	3.5
845	101	16.75	8.38	8.38	80	0.95	1.9	1.5	3

12-V ORing Operation for Redundant Systems

The 12-V channels use external pass FETs to provide reverse blocking. The TPS2459 pulls the BLK pin high when the input-to-output differential voltage $V_{IN12–OUT12}$ exceeds a nominal value of 10 mV, and it pulls the pin low when this differential falls below a nominal value of –3 mV. These thresholds provide a nominal 13 mV of hysteresis to help prevent false triggering.

The source of the blocking FET connects to the source of the pass FET, and the drain of the blocking FET connects to the load. This orients the body diode of the blocking FET such that it conducts forward current and blocks reverse current. The body diode of the blocking FET does not normally conduct current because the FET turns on when the voltage differential across it exceeds 10 mV.

Applications that do not use the blocking FET should clear the associated 12OR bit to turn off the internal circuitry that drives the BLK pin. (See Figure 24).

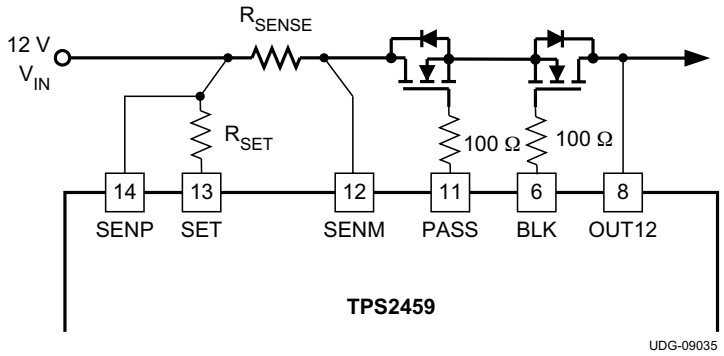


Figure 24. 12-V Path

12-V ORing for High-Power Loads

The 12HP bit adjusts the ORing turn-off threshold of the 12-V channel. Clearing the bit sets the ORing turn-off threshold to the default nominal value of -3 mV. Setting the bit shifts the threshold up by 6 mV to a nominal value of +3 mV (Figure 8). Shifting the turn-off threshold to a positive value ensures that the blocking FET shuts off before any reverse current flows.

A light load may not draw sufficient current to keep the input-to-output differential VIN12-OUT12 above 3 mV. When this happens, the blocking FET shuts off and then the differential voltage increases until it turns back on. This process endlessly repeats, wasting power and generating noise. Therefore 12HP should only be set for high-power loads that satisfy the relationship.

$$I_{LOAD} > \frac{10\,mV}{R_{SENSE} + R_{DS(on)PASS} + R_{DS(on)BLK}} \quad (14)$$

where

- I_{LOAD} is the current drawn by the load
- R_{SENSE} is the value of the sense resistor
- $R_{DS(on)PASS}$ is the maximum on-resistance of the pass FET
- $R_{DS(on)BLK}$ equals the maximum on-resistance of the blocking FET

For example, if R_{SENSE} = R_{HSFET} = R_{ORFET} = 5 mΩ, then a high-power load must always draw at least 667 mA. Most, although not all, AdvancedMC™ loads can benefit from using the high-power bit 12HP.

Figure 25 shows the different ORing thresholds in high power and low power applications.

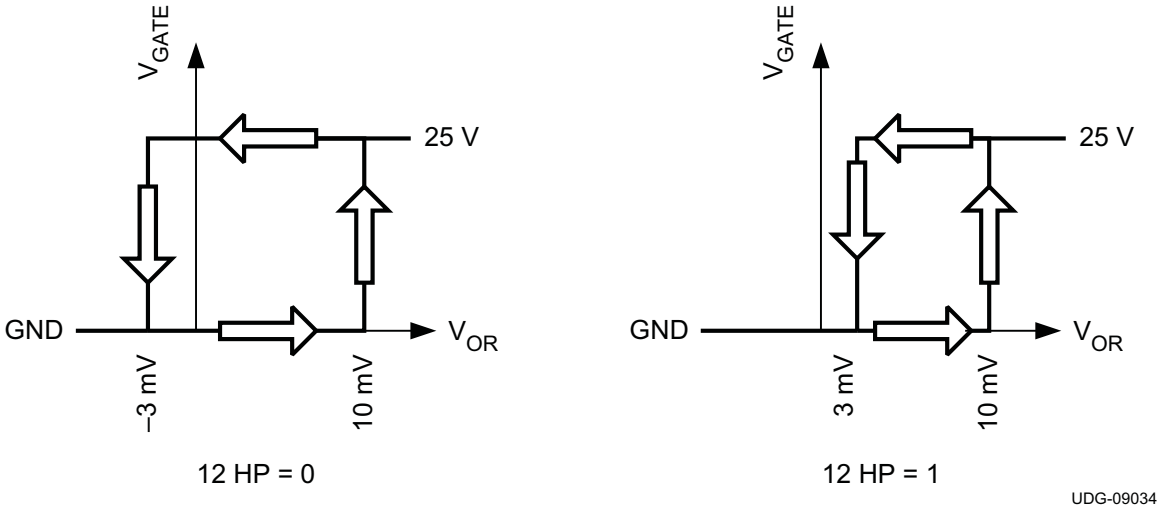


Figure 25. ORing Thresholds High Power vs. Low Power

Internal Bleed-Down Resistors and Bleed-Down Thresholds

The TPS2459 includes two features intended to support downstream loads that require removal and reapplication of power to properly reset their internal circuitry. Disabling and re-enabling a channel of the TPS2459 does not necessarily reset such a load because the capacitance attached to the output bus may not fully discharge.

The TPS2459 includes two bleed-down comparators that monitor the OUT12 and OUT3 pins. The I^2C™ interface includes two bits (3DS and 12DS) that enable these comparators. Enabling a bleed-down comparator prevents the corresponding channel from turning on until the output voltage drops below about 100 mV. This precaution ensures that the output rail drops so low that all downstream loads properly reset.

In case the downstream load cannot quickly bleed-off charge from the output capacitance, the TPS2459 also includes bleed-down resistors connected to each output rail through pins OUT12 and OUT3. Internal switches connect these resistors from their corresponding rails to ground when the channels are disabled, providing that one sets the appropriate bit in the I^2C™ interface. These bits are named 12UV and 3UV. Clearing these bits ensures that the corresponding resistors never connect to their buses.

If redundant supplies connect to an output, clear the corresponding bleed-down threshold and bleed-down resistor bits. Failing to clear the bleed-down threshold bit prevents the channel from enabling, while the redundant supply continues to hold up the output rail. Failing to clear the bleed-down resistor bit causes current to continually flow through the resistor when the TPS2459 is disabled and the redundant supply holds up the output bus.

Multiswap Operation in Redundant Systems

TheTPS2459 features an additional mode of operation called Multiswap redundancy. This technique does not require a microcontroller, making it simpler and faster than the redundancy schemes described in the MicroTCA™standard. Multiswap is especially attractive for AdvancedMC™ applications that require redundancy but need not comply with the MicroTCA™ power module standard.

To implement Multiswap redundancy, connect the SUM pins of the redundant channels together and tie a single R_{SUM} resistor from this node to ground. The current limit thresholds now apply to the sum of the currents delivered by the redundant supplies. When implementing Multiswap redundancy on 12-V channels, all of the channels must use the same values of resistors for R_{SENSE} and R_{SET}.

Figure 26 and Figure 27 compare the redundancy technique advocated by the MicroTCA™ specification with Multiswap redundancy. MicroTCA™ redundancy independently limits the current delivered by each power source. The current drawn by the load cannot exceed the sum of the current limits of the individual power sources. Multiswap redundancy limits the current drawn by the load to a fixed value regardless of the number of operational power sources. Removing or inserting power sources within a Multiswap system does not affect the current limit seen by the load.

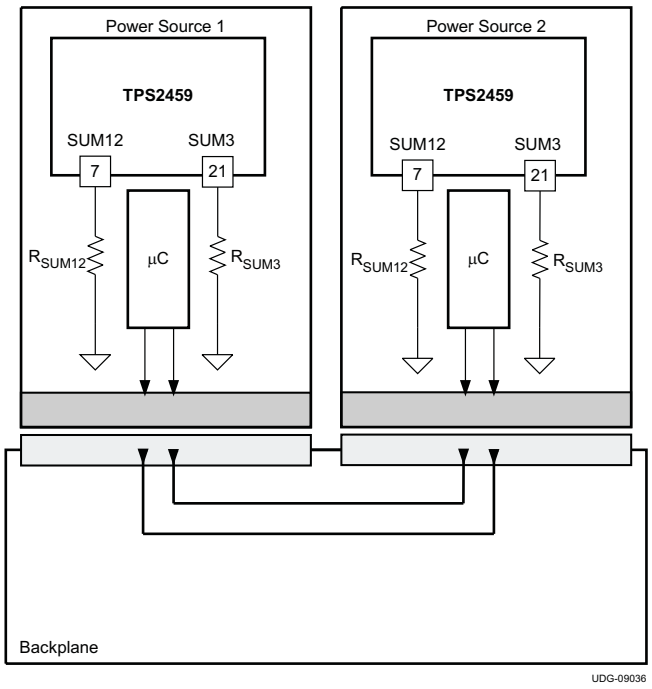


Figure 26. μTCA Redundancy

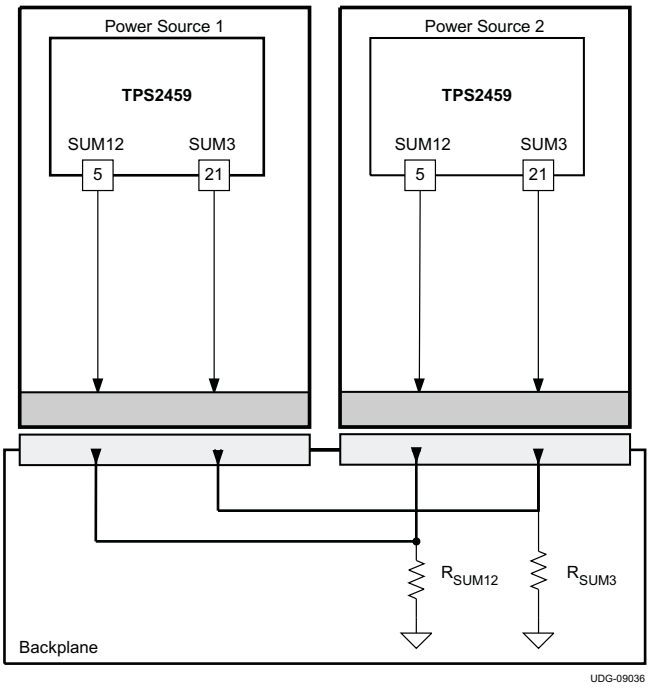


Figure 27. Multiswap Redundancy

Fault Timer Programming

Both of the TPS2459 channels include a fault timer. The timer begins operating whenever the channel enters current limit. If the channel remains in current limit so long that the fault timer runs out, then the channel turns off the pass FET and reports a fault condition by means of the xFLT bit in the I²C™ interface.

The fault timers are independently programmable from 0.5 to 15.5 ms in steps of 0.5 ms using the appropriate xFT bits. A code of xFT = 00001B corresponds to the minimum programmable time of 0.5 ms. The code xFT = 00000B corresponds to an extremely short time interval of no practical use. The locations of the fault timer programming bits are shown in Table 13.

Table 13. Fault Time Control Bits

	CHANNEL VOLTAGE (V)	FAULT TIME (ms)				
		8	4	2	1	0.5
REGISTER[BIT]	12	R4[4]	R4[3]	R4[2]	R4[1]	R4[0]
	3.3	R5[4]	R5[3]	R5[2]	R5[1]	R5[0]

Select the shortest fault times sufficient to allow down-stream loads and bulk capacitors to charge. Shorter fault times reduce the stresses imposed on the pass FETs under fault conditions. This consideration may allow the use of smaller and less expensive pass FETs for the 12-V channels.

The TPS2459 supports two modes of fault timer operation. Clearing the FLTMODE bit causes a channel to latch off whenever its fault timer runs out. The channel remains off until it has been disabled and re-enabled (see *Enable Functions* section). The TPS2459 operates in this manner by default. Setting the FLTMODE bit causes a faulted channel to automatically attempt to turn back on after a delay roughly one hundred times the fault time. This process repeats until either the fault disappears or the user disables the channel. The pass FET for a 12-V channel with a shorted output must therefore continuously dissipate the following power;

$$P_{FAULT} \cong 0.01 \times V_{IN12} \times I_{CL} \quad (15)$$

where

- V_{IN12} equals the voltage present at the input of the 12-V channel
- I_{CL} equals the current limit setting for this channel (the inrush current if 12VNRS is set)

When used in MicroTCA Power Modules it is very important to protect the OUT12 pin by connecting a Schottky diode from the OUT12 pin to GND. The relatively long and uncontrolled load line lengths to the AdvancedMC modules make it quite likely that shutting off while under load causes an inductive transient to pull the OUT12 pin below -0.3 V. Pulling OUT12 below this level can disrupt proper device operation.

TPS2459 I²C™ Interface

The TPS2459 digital interface meets the specifications for an I²C™ bus operating in the high-speed mode. The interface to recognize any one of 27 separate I²C™ addresses can be configured using the A0, A1, and A2 pins (Table 14 I²C™ Addressing). These pins accept any of three distinct voltage levels. Connecting a pin to ground generates a low level (L). Connecting a pin to VINT generates a high level (H). Leaving a pin floating generates a no-connect level (NC).

Table 14. I²C™ Addressing

EXTERNAL PINS			I²C™ (DEVICE) ADDRESS		
A2	A1	A0	DEC	HEX	BINARY
L	L	L	8	8	1000
L	L	NC	9	9	1001
L	L	H	10	0A	1010
L	NC	L	11	0B	1011
L	NC	NC	12	0C	1100
L	NC	H	13	0D	1101
L	H	L	14	0E	1110
L	H	NC	15	0F	1111
L	H	H	16	10	10000
NC	L	L	17	11	10001
NC	L	NC	18	12	10010
NC	L	H	19	13	10011
NC	NC	L	20	14	10100
NC	NC	NC	21	15	10101
NC	NC	H	22	16	10110
NC	H	L	23	17	10111
NC	H	NC	24	18	11000
NC	H	H	25	19	11001
H	L	L	26	1A	11010
H	L	NC	27	1B	11011
H	L	H	28	1C	11100
H	NC	L	29	1D	11101
H	NC	NC	30	1E	11110
H	NC	H	31	1F	11111
H	H	L	32	20	100000
H	H	NC	33	21	100001
H	H	H	34	22	100010

The I²C™ hardware interface consists of two wires known as serial data (SDA) and serial clock (SCL). The interface is designed to operate from a nominal 3.3-V supply. SDA is a bidirectional wired-OR bus that requires an external pullup resistor, typically a 2.2-kΩ resistor connected from SDA to the 3.3-V supply.

The I²C™ protocol assumes one device on the bus acts as a master and another device acts as a slave. The TPS2459 supports only slave operation with two basic functions called register write and register read.

Register Write

Figure 28 shows the format of a register write. First, the master issues a start condition, followed by a seven-bit I²C™ address. Next, the master writes a zero to signify that it wishes to conduct a write operation. Upon receiving an acknowledge from the slave, the master writes the eight-bit register number across the bus. Following a second acknowledge, the master writes the eight-bit data value for the register across the bus. Upon receiving a third acknowledge, the master issues a stop condition. This action concludes the register write.

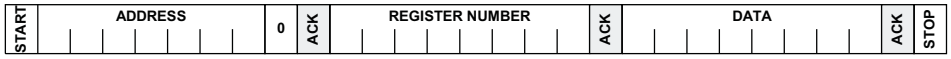


Figure 28. Register Write Format

Register Read

Figure 29 shows the format of a register read. First, the master issues a start condition followed by a seven-bit I²C™ address. Next, the master writes a zero to signify that it conducts a write operation. Upon receiving an acknowledge from the slave, the master writes the eight-bit register number across the bus. Following a second acknowledge, the master issues a repeat start condition. Then the master issues a seven-bit I²C™ address followed by a one to signify that it conducts a read operation. Upon receiving a third acknowledge, the master releases the bus to the TPS2459. The TPS2459 then writes the eight-bit data value from the register across the bus. The master acknowledges receiving this byte and issues a stop condition. This action concludes the register read.

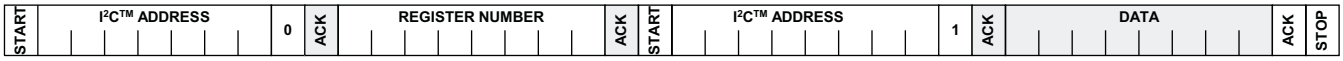


Figure 29. Register Read Format

Using the TPS2459 to Control an AdvancedMC™ Slot

The TPS2459 has been designed for use in systems under I²C™ control. Figure 30 shows the TPS2459 in a typical system implementing redundant power sources. A non-redundant application would omit the blocking FET and leave the BLK pin unconnected.

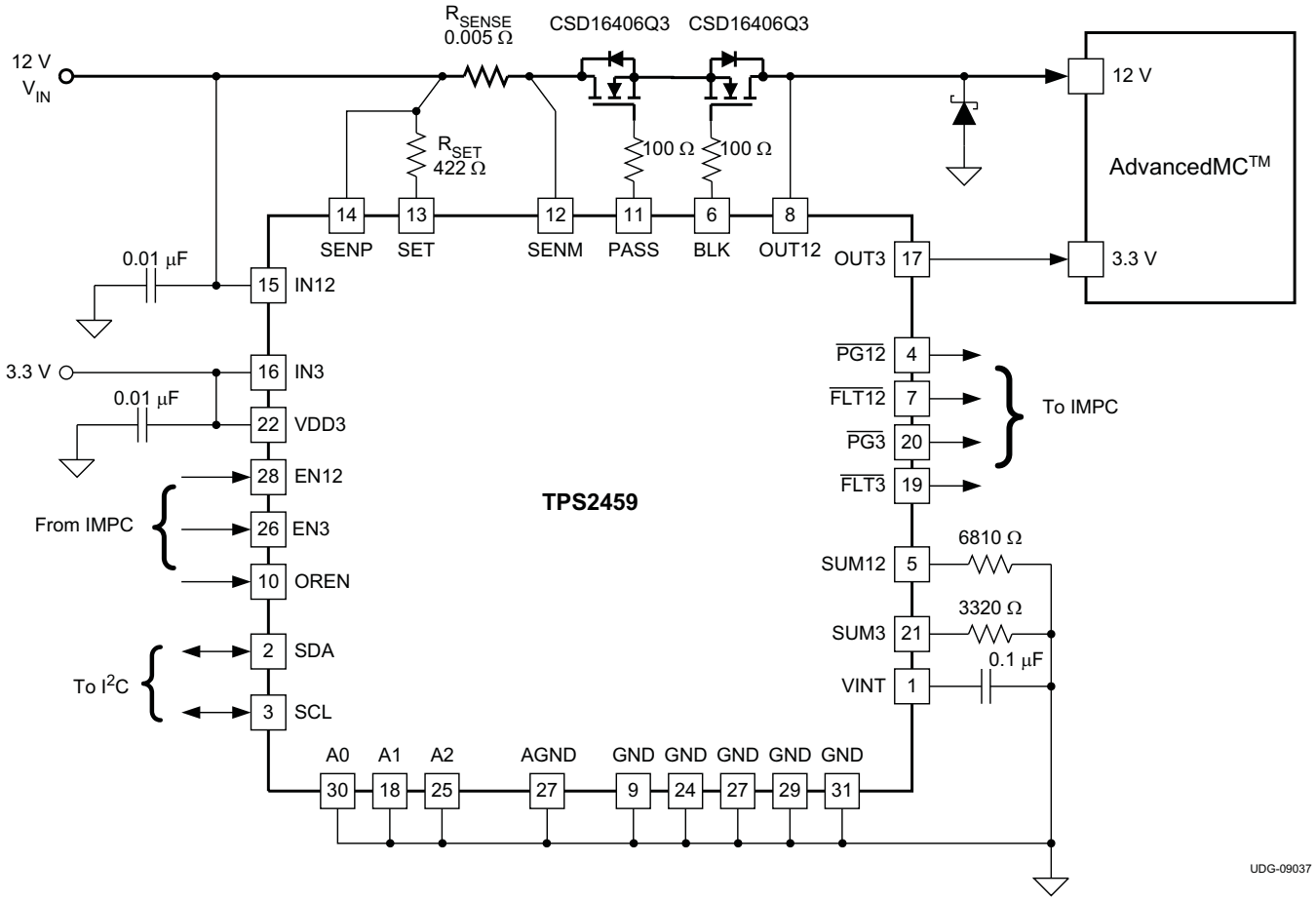


Figure 30. TPS2459 Redundant System Schematic

Layout Considerations

TPS2459 applications require careful attention to layout to ensure proper performance and minimize susceptibility to transients and noise. IImportant points to consider include:

- Connect AGND and all GND pins to a ground plane.
- Place a 0.01-μF or larger ceramic bypass capacitors on IN12 and VDD3.
- Minimize the loop area created by the leads running to these devices.
- Minimize the loop area between the SENM and SENP leads by running them side-by-side.
- Use Kelvin connections at the points of contact with R_{SENSE} Figure 31
- Minimize the loop area between the SET and SENP leads.
- Connect the SET leads to the same Kelvin points as the SENP leads, or as close to these points as possible.
- Size the following runs to carry at least 20 A:
  - Runs on both sides of R_{SENSE}
  - Runs from the drains and sources of the external FETs
- Minimize the loop area between the OUT12 and SENP leads.
- Size the runs to IN3 and OUT3 to carry at least 1 A.
- Soldering the powerpad of the TPS2459 to the board will improve thermal performance.

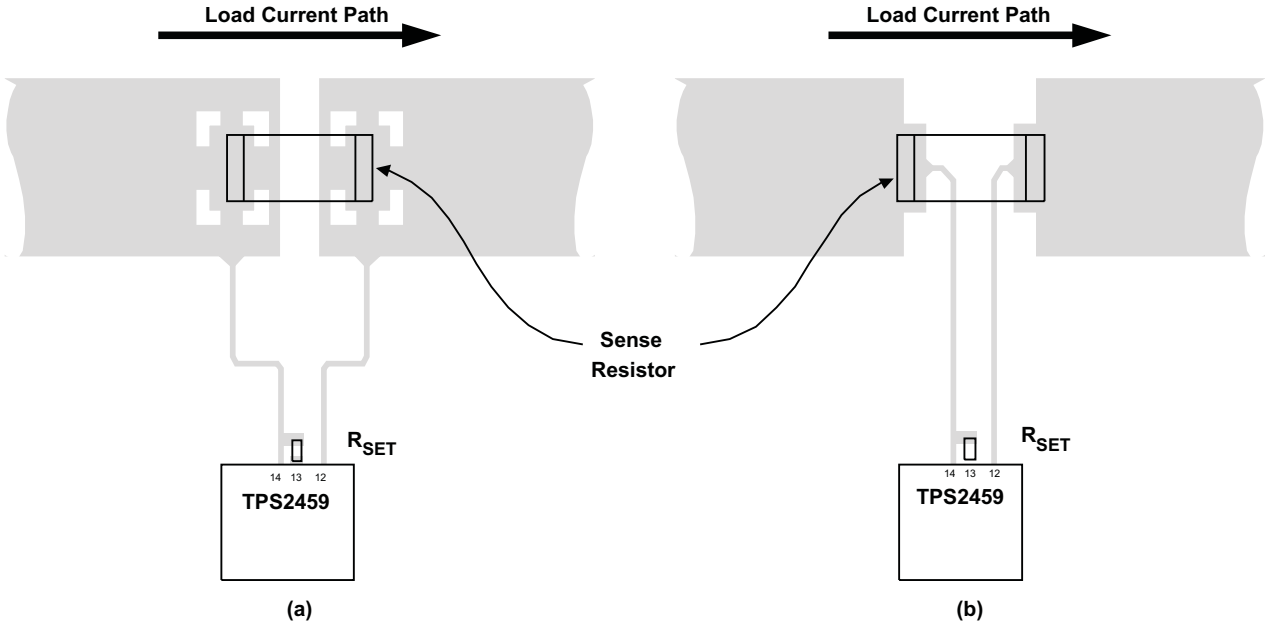


Figure 31. Recommended R_{SENSE} Layout

Transient Protection

The need for transient protection in conjunction with hot-swap controllers should always be considered. When the TPS2459 interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. Such transients can easily exceed twice the supply voltage if steps are not taken to address the issue. Typical methods for addressing transients include :

- minimizing lead length/inductance into and out of the device
- transient voltage suppressors (TVS) on the input to absorb inductive spikes
- Shottky diode and/or capacitors across the output to absorb negative spikes
- a combination of ceramic and electrolytic capacitors on the input and output to absorb energy.

Equation 16 estimates the magnitude of these voltage spikes.

$$V_{SPIKE} = V_{NOM} + I_{LOAD} \times \sqrt{L/C} \quad (16)$$

where

- V_{NOM} is the nominal voltage at terminal being analyzed
- L is the combined inductance of feed to RTN lines.
- C is the capacitance at point of disconnect.
- I_{LOAD} is the current through terminal at $T_{DISCONNECT}$

The inductance due to a straight length of wire is described in Equation 17.

$$L_{STRAIGHTWIRE} \cong \left(0.2 \times length \times \left(\ln\left(\frac{4 \times length}{diameter}\right) - 0.75\right)\right) \quad (17)$$

where

- L is the length of the wire
- D is the diameter

If sufficient capacitance to prevent transients from exceeding the absolute ratings of the TPS2459 cannot be included the application requires the addition of transient protectors.

Output Protection Considerations for MicroTCA Power Systems

MicroTCA Power systems have particular transient protection requirements because of the basic power architecture. Traditional protection methods must be adjusted to accommodate these systems where the supplies are OR'ed together after the inrush control and current limit circuits. However, minor changes to some standard techniques will yield very good results.

Unlike systems which have hotswap/inrush control at the load, uTCA power modules and their hot-swap circuitry are often a significant distance (up to 1 m of trace length, two way) from the load module. Even with the best designed backplanes this distance results in stray inductance which will store energy while current is being delivered to the load. The inductive energy can cause large negative voltage spikes at the power module output when the current is switched off under load. The spikes become especially severe when the channel shuts off due to a short circuit, which drives the current well above normal levels just before shut off.

The lowest voltage allowed on the device pins is -0.3 V. If a transient makes a pin more negative than -0.3 V the internal ESD Zener diode attached to the pin will become forward biased and current will be conducted across the substrate to the ground pins. This current may disrupt normal operation or, if large enough, damage the silicon. Typical protection solutions involve capacitors, TVSs (Transient Voltage Suppressors) and/or a Schottky diode to absorb the energy which appears at the power module output in the form of a large negative voltage spike.

The Risk With Output Capacitors

Putting transient filter capacitors at the output of a uTCA power module can cause nuisance trips when that power module is plugged into an active bus. If there is no series resistance with the capacitor and the bus is low impedance an inrush surge can cause the active supply to "detect" a short circuit and shut down. One possible solution is to put a few Ohms of resistance in series with the cap to limit inrush below the fast trip level. A better solution is to put a Schottky diode across the output to clamp the transient energy and shunt it to ground as shown in Figure 32. Although the Schottky diode will absorb most of the energy, the extremely fast di/dt at shutoff allows some of the leading edge energy to couple through the parasitic capacitances of the hotswap FET and the ORing FET, (C_{DS}, C_{GS}, C_{GD}) and into the BLK and GATE pins. Protection for these pins is provided by 100-Ω GATE resistors which have little effect on normal operation but provide good isolation during transient events.

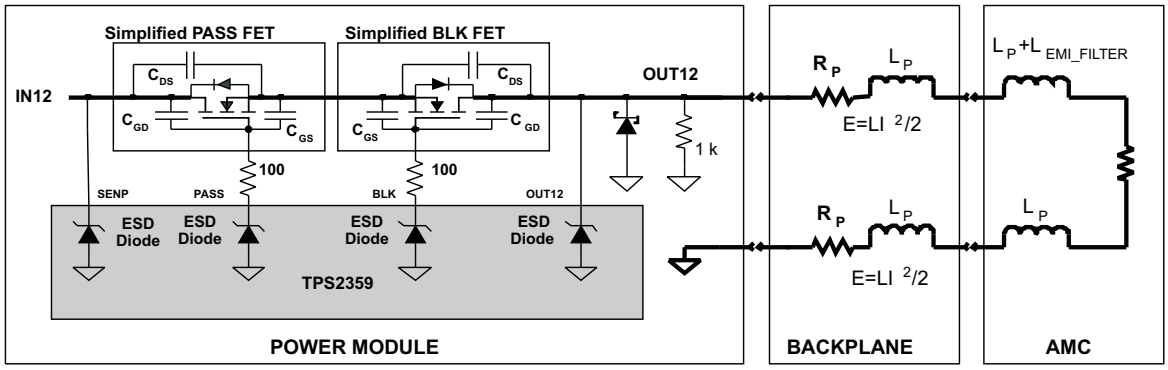


Figure 32. Parasitic Inductance and Transient Protection

Output Bleed Down Resistance

When the TPS2359 commands the 12-V channel off there is a small leakage current sourced by the OUT12 pin. If this leakage is ignored it can eventually charge any external capacitance to approximately 6 V. In some systems this may be acceptable but, if not, the leakage can be bled to GND by commanding the internal bleed down resistor on by setting 12xDS high.

- 12ADS = R1[7]
- 12DSB = R4[7]

If a hardware solution is preferred then a 1k resistor from OUT12 to GND will suffice. Maximum leakage is around 23 uA and can be modeled as a 6-V source in series with a 280-kΩ resistor.

REVISION HISTORY

Changes from Revision A (August 2009) to Revision B **Page**

- Added New Typical Application Diagram 1
- Added EN12 2
- Deleted EN12 2
- Deleted m 3
- Added µ 3
- Deleted m 3
- Added µ 3
- Added New Block Diagram 6
- Changed 3.3-V Channel Circuitry Block Diagram 7
- Deleted Setting bit makes EN3 and EN12 pins active low. 16
- Added This bit must be 0. 16
- Added This bit must be 0. 16
- Deleted Setting bit makes EN3 and EN12 pins active low.Setting bit makes external ENx pins active low; clearing bit makes pins active high. (Actually, setting this bit reverses polarity of ENPOL R14[5] which will nominally be set as active low). 20
- Added This bit must be 0. 20
- Deleted Setting this bit makes the EN12 and EN3 pins active low. 20
- Added This bit must be 0. 20
- Deleted Latches high when OUT12 goes from above VTH_PG to below VTH_PG. 21
- Added This bit is set each time channel is turned on. A second read cycle will indicate true status. 21
- Deleted Latches high when OUT3 goes from above VTH_PG to below VTH_PG. 21
- Added This bit is set each time channel is turned on. A second read cycle will indicate true status. 21
- Added This bit remains set until Register 8 is read. This bit is set each time channel is turned on. A second read cycle after turn on is required to determine true status. 21
- Added This bit remains set until Register 8 is read. This bit is set each time channel is turned on. A second read cycle after turn on is required to determine true status. 21
- Added This bit remains set until Register 8 is read. This bit is set each time channel is turned on. A second read cycle after turn on is required to determine true status. 21
- Added New 12-V Channel Threshold Circuitry Diagram 26
- Added New RC Slew Rate Control Diagram 27
- Added New 12-V Path Diagram, replaced ORing Thresholds Diagram 30
- Deleted ORing Thresholds 30
- Added 12-V Path 30
- Added ORing Thresholds High Power vs. Low Power 31
- Changed 32 ms 34
- Added 15.5 ms 34
- Added the following power; 34
- Added New TPS3459 Redundant System Schematic Diagram 37

REVISION HISTORY (CONT.)

Changes from Revision B (February 2010) to Revision C **Page**

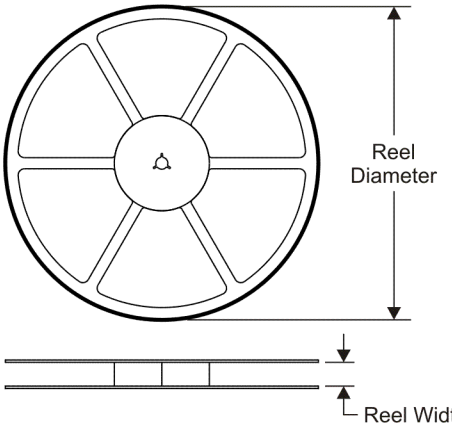
- Added Latches high when OUT12 goes from above VTH_PG to below VTH_PG. 21
- Added Latches high when OUT3 goes from above VTH_PG to below VTH_PG. 21

Changes from Revision C (March 2010) to Revision D **Page**

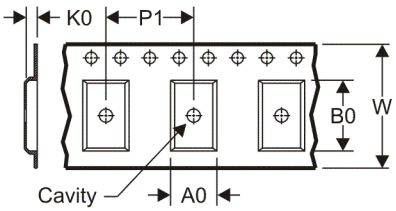
- Deleted µS 3
- Added µs 3
- Deleted m 3
- Added µ 3
- Deleted m 4
- Added µ 4

TAPE AND REEL INFORMATION

REEL DIMENSIONS

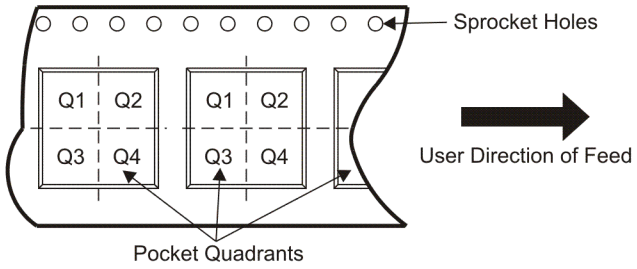


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

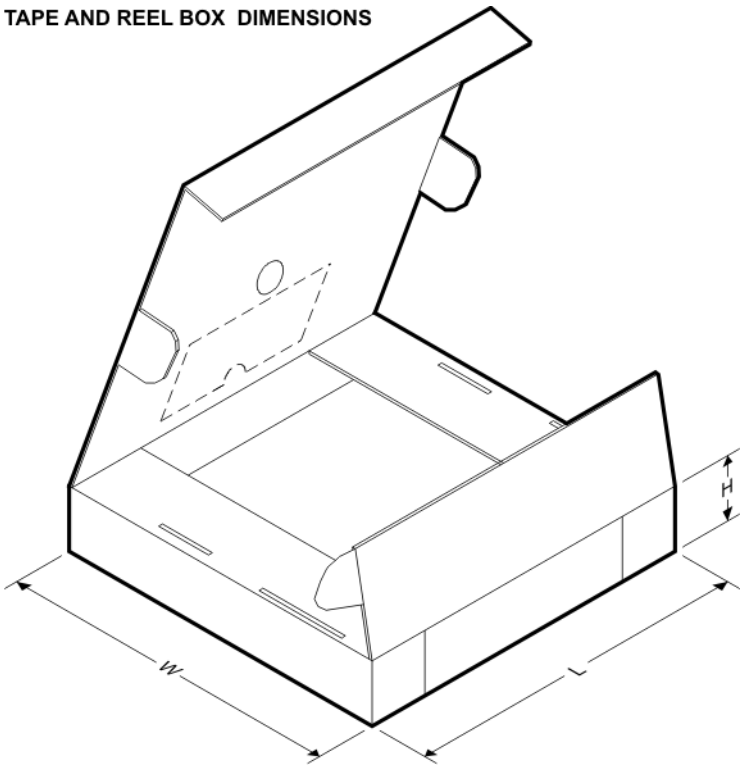
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2459RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS2459RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

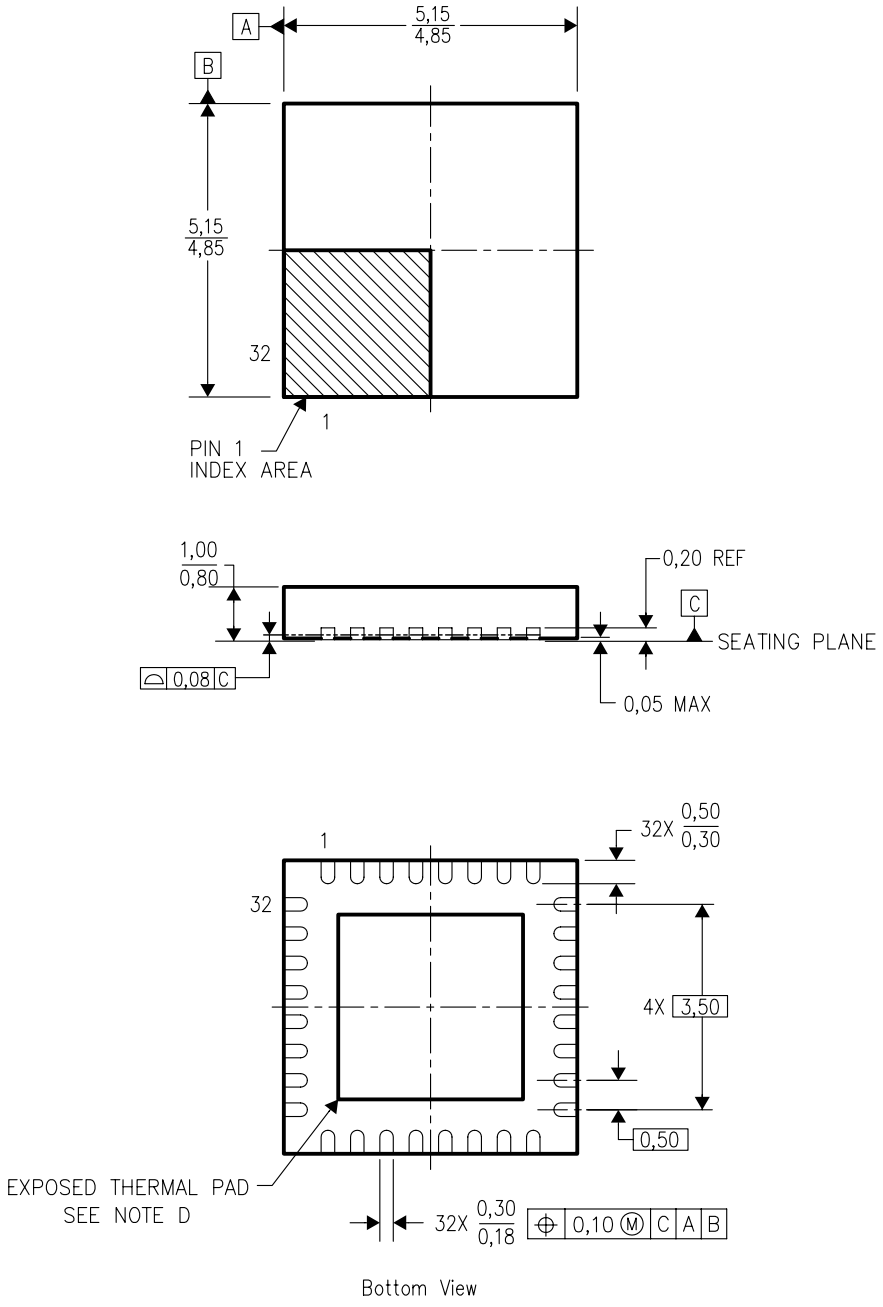
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2459RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TPS2459RHBT	QFN	RHB	32	250	190.5	212.7	31.8

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



4204326/C xx/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

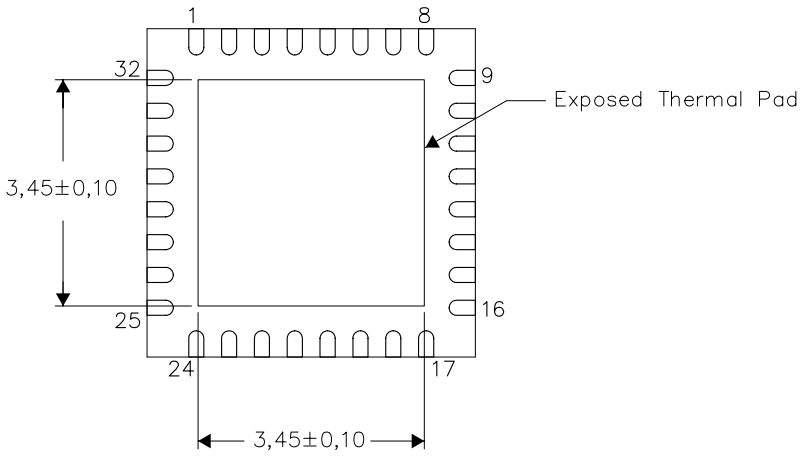
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

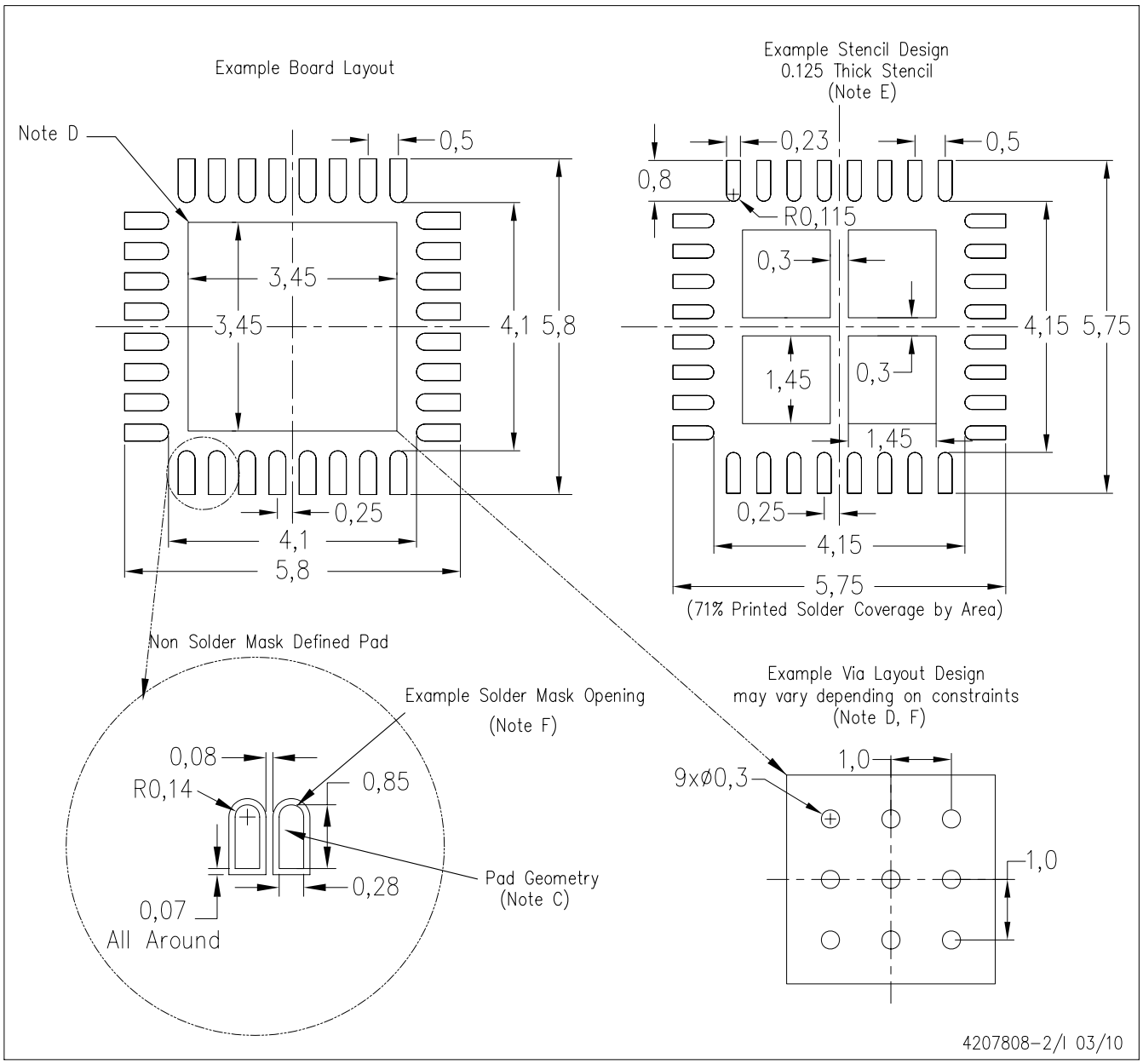


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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