Title	***Engineering Prototype Report (EPR-000008)*** ***1.2 W, Universal Input, Non-isolated, TNY254 (EP8)***
Customer	Home Appliance Market
Author	S.L.
Document Number	EPR-000008
Date	08-May-2001
Revision	10

Abstract

This document presents the specification, schematic & BOM, inductor calculation, test data and wave forms for a low cost, non-isolated, converter for a home appliance application (triac driving).

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1 Introduction

There are three specific requirements for this power supply:

1. To provide power for driving a trial requires that the output power be referenced to the input line (L), with no series impedance, therefore only ½ wave rectification is allowed and the switch must be in the return side of the primary switching circuit. EMI filtering, if necessary, has to be implemented at the system level.
2. The unit has to operate at 85 °C ambient.
3. The unit has to withstand 2 kV (configuration "1", page 4) and 6 kV (configuration "2", page 5) input surge voltage as defined by IEC 1000-4-5 (1.2/50 μs). The surge protection added to satisfy these requirements reduces the converter efficiency. It would be more beneficial (lower cost, improved efficiency) if the surge protection were implemented at the system (appliance) level.

2 Power Supply Specification

The specification below is for the worst case (6 kV configuration "2")

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Input Voltage	V_{AC}	85		265	V_{AC}	50/60 Hz
Input frequency	f_{LINE}	47		63	Hz	
Output						
Output Voltage	V_{OUT}	10.8	12	13.2	V	12 V+/-10%*
Output Ripple Voltage	V_{RIPPLE}		80	120	MV	of V_{OUT} @ full load
Output Current	I_{OUT}	0		100	MA	~200 mA short
Load Regulation						0-100% load
Line Regulation						85-265 V_{AC}, full load
Power Output						
Continuous Output power	P_{OUT}	0		1.2	W	0-85 °C internal ambient**
Power supply efficiency	η	50			%	@low line, full load
Environmental						
Temperature	T_{AMB}	0		85	C	6" x 6" x 4" enclosure
EMI – conducted						Designed to meet CISPRR 22B (FCCB)
Safety						Designed to meet IEC950
Input Surge Voltage	Config. "1"	2			kV	IEC1000-4-5
Input Surge Voltage	Config. "2"	6			kV	IEC1000-4-5

* +/-5% with 2% Zener.

**The unit was placed in a 6" x 6" x 4" enclosure inside the temperature chamber.

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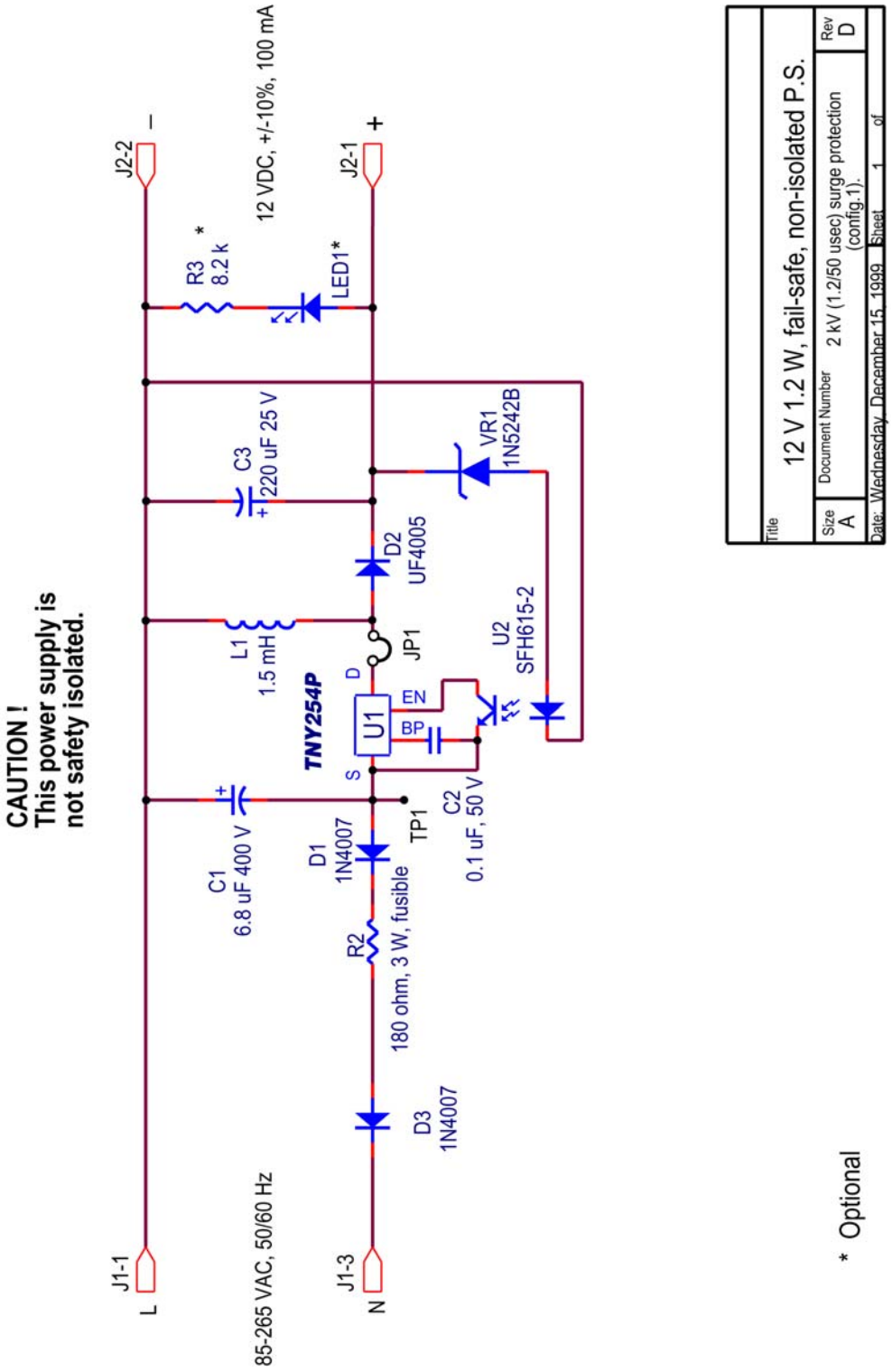
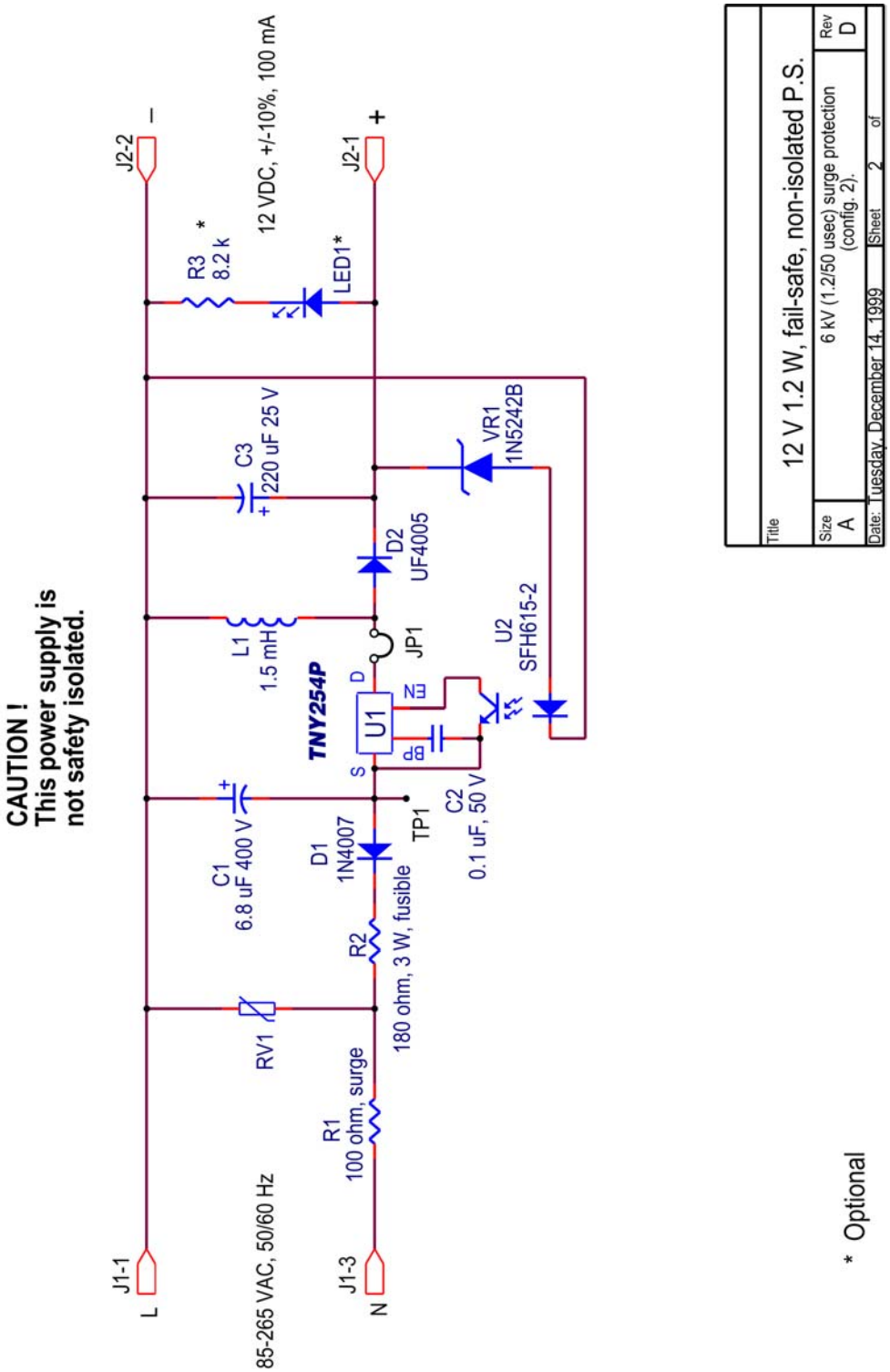
3 Schematic

3.1 Configuration "1" – 2 kV (1.2/50 μs) Surge Withstand



3.2 Configuration "2" – 6 kV (1.2/50 μs) Surge Withstand



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4 Circuit Description

The circuit is a fail-safe, non-isolated fly-back topology. Fail-safe means that the output is not subjected to high voltage DC if the switch (U1) fails, since the diode D2 blocks the voltage.
During the ON time (U1 conducting), L1 is charged up to $\mathbf{I}_{LIMIT}$ of the TNY254 (0.25 A type.), from the energy stored in C1. During the OFF time (U1 blocking), the energy stored in L1 is transferred to C3 and the load via D2.

The device switching frequency is 44 kHz. The surge protection circuit has to prevent the *TinySwitch* V_{DSMAX} from exceeding 700 V. The surge protection for configuration ”1” (2 kV) and configuration ”2” (6 kV) is illustrated in the schematics (pages 4, 5).

Configuration ”1” relies on the current/energy-limiting resistor R2 to keep the maximum charging voltage of C1 during a +2 kV surge below 700 V. For the -2 kV surge the diodes D1+D3 block the voltage.

Configuration ”2” relies on the current/energy-limiting resistor R1 to limit the current in the MOV (RV1) to approximately 50 A peak, such that the RV1 clamping voltage is kept well under 1 kV (~700 V). During the +6 kV surge, R2 limits C1 charging current so that the maximum voltage does not exceed 700 V. During the -6 kV surge, D1 blocks the RV1 clamping voltage from reaching C1.
In both configurations, the fusible resistor R2 provides protection for component failure.

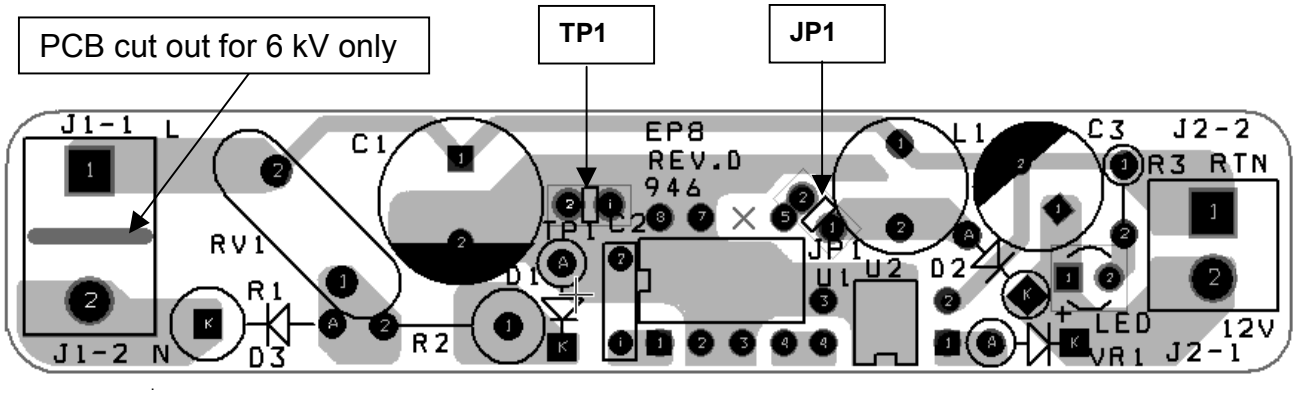
5 Layout

CAUTION!

This is a non-isolated power supply with the low voltage return referenced to the input line (85-265 V_{AC}). Do not touch the unit while it is powered. Power the board using a safety isolation transformer so the high voltage probe return is not referenced to the neutral of the input line.

For the drain-to-source voltage waveforms connect the high voltage probe tip to jumper JP1 and the probe ground to test point TP1.

For switching current waveforms replace jumper JP1 with a wire loop and use a Tektronix A6302 current probe and AM503 current probe amplifier (with TM501 power module) or equivalent.



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6 Bill of Materials

6.1 Configuration ”1”, 2 kV

Item	Qty.	Ref.	Description	Manufacturer	Part Number
1	1	C1	6.8 μF, 400 V, 105 C	Rubycon	400BXA6R8M10x16
2	1	C2	0.1 μF, 50 V, ceramic	Panasonic	ECU-S1H104KBB
3	1	C3	220 μF 25 V (0.12 Ω)	Panasonic	
4	2	D1, D3	Glass Passivated Diode	Vishay/Lite On	1N4007GP
5	1	D2	600 V, 1 A, 75 ns	General Instrument	UF4005
6	1	**J1	Header, 3 pos., 0.156 spacing	Molex	26-48-1035
7	1	J2	Header, 2 pos., 0.156 spacing	Molex	26-48-1025
8	1	*LED1	low current	Siemens/HP	LG3369/HLMP1790
9	1	L1	1.5 mH, 0.4 A_{DC}, 0.2 A_{AC}, 600 V_{DC},	Chilisin	
10	1	R2	180 Ω, flame proof, fusible, 3 W;	Vitrohm (Farnell Components.)	(08WX7849)
11	1	*R3	8.2 kΩ, ¼ W		
12	1	U1	Off-line Switcher	Power Integrations	TNY254P
13	1	U2	Optocoupler	Siemens/NEC	SFH615-2/PS2501-1
14	1	VR1	Zener, 12 V ±5%	Diodes Incorporated	1N5242B

*Optional

**Remove middle pin

6.2 Configuration ”2”, 6 kV

(Add the following items to Configuration "1" and subtract D3)

Item	Qty.	Ref.	Description	Manufacturer	Part Number
15	1	RV1	Varistor, 275 V_{AC}, 14 mm	Harris/Littlefuse	V275LA20A
16	1	R1	100 Ω, 15 J, 500 V_{AC}	Ohmite	OX 101

7 Inductor

7.1 Calculation

The inductor value can be determined using the TNY253-255 flyback transformer spreadsheet with the following considerations:

1) the frequency value (f_L) is ½ the line frequency, 25 Hz for 50 Hz, 30 Hz for 60 Hz, to account for half wave rectification.

2) Z factor, the ratio between the secondary losses and the total losses, has to reflect the dominance of the primary losses, as the *TinySwitch* losses (high R_{dson}) overshadow the output diode losses. Z factor does not reflect the extra power loss due to R1 and R2.
The efficiency used in the spreadsheet is only the efficiency of the converter portion of the supply, it does not include the losses in the input resistor.

3) the output diode rating can be calculated from the formula ($V_R \geq P_{IVS/0.8}$), where $P_{IVS}=V_{MAX}+V_O-V_{DS}$. The inductor can be looked at as a transformer with 1:1 turns ratio, therefore $V_{OR}=V_O+V_D$.

4) the output capacitor minimum value is dictated by the output RMS ripple current and the maximum value by the specified maximum output voltage ripple.

Select the next higher standard “L” value (for the rated “I”) from a qualified vendor (min. 400 V_{DC} voltage rated inductor) like Chilisin, and the smallest DC resistance.

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7.2 Spreadsheet

ACDC_TNY_Rev1.8_072699 Copyright Power Integrations, Inc. 1999	INPUT		OUTPUT	UNIT	ACDC_TNY_REV1_8_072699.xls: *TinySwitch* Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					Customer
VACMIN	77			V	Minimum AC Input Voltage
VACMAX	265			V	Maximum AC Input Voltage
fL	**25**			Hz	AC Mains Frequency
VO	12			V	Output Voltage
PO	1.2			W	Output Power
n	0.65				Efficiency Estimate
Z	**0.1**				Loss Allocation Factor
tC	3			mS	Bridge Rectifier Conduction Time Estimate
CIN	6.8			µF	Input Filter Capacitor
MODE OF OPERATION					
Continuous ('c') or Discontinuous ('d')?	c				Continuous Mode Operation or Discontinuous Mode Operation?
	n	Continuous			
ENTER TinySwitch Parameters		*Universal*		115/230 V_{AC}	
TinySwitch	TNY254	*4 W*	*5 W*		
ILIMITMIN		*0.23*		A	Minimum Current Limit
ILIMITMAX		*0.28*		A	Maximum Current Limit
fSmin		*40000*		Hz	Minimum Frequency
VDS	10			V	Voltage Drop Between Drain to Source
ENTER Output Diode Parameters					
Output Diode					
VR	**500**			V	Diode Maximum Peak Repetitive Reverse Voltage
ID	1			A	Diode Average Forward Current
VD	1			V	Diode Forward Voltage Drop
k	0.8				Diode Peak to RMS Current Factor (k=0.9 for Schottky, k=0.8 for PN Diode)
Design Parameters					
VMIN			**51**	V	Minimum DC Input Voltage
VMAX			375	V	Maximum DC Input Voltage
IP			0.21	A	Peak Primary Current
DMAX			0.252		Duty Cycle at Minimum DC Input Voltage
KRP			0.62		Ripple to Peak Current Ratio (0.6<KRP<1.0)
VOR			13.91	V	Reflected Output Voltage
VDRAIN			445.63	V	Maximum Drain Voltage Estimate
PIVS			362	V	Output Rectifier Peak Inverse Voltage
LP			**1552**	µH	**Minimum Primary Inductance**
CURRENT WAVEFORM SHAPE PARAMETERS					
IAVGmax			0.04	A	Maximum Average Primary Current
IAVGmin			0.00	A	Minimum Average Primary Current
IRMS			0.07	A	Primary RMS Current
IR			0.13	A	Primary Ripple Current
ISP			0.22	A	Maximum Peak Secondary Current
ISRMS			0.14	A	Secondary RMS current
IO			**0.10**	A	Power Supply Output Current
IRIPPLE			**0.09**	A	Output Capacitor RMS Ripple Current
IOS			**0.24**	A	Estimated Short Circuit Current

8.0 Performance Data

8.1 Efficiency

TEST EQUIPMENT
INPUT: AC POWER ANALYZER PM1000 (VOLTECH).
OUTPUT: ELECTRONIC LOAD PLZ 153 W (KIKUSUI).

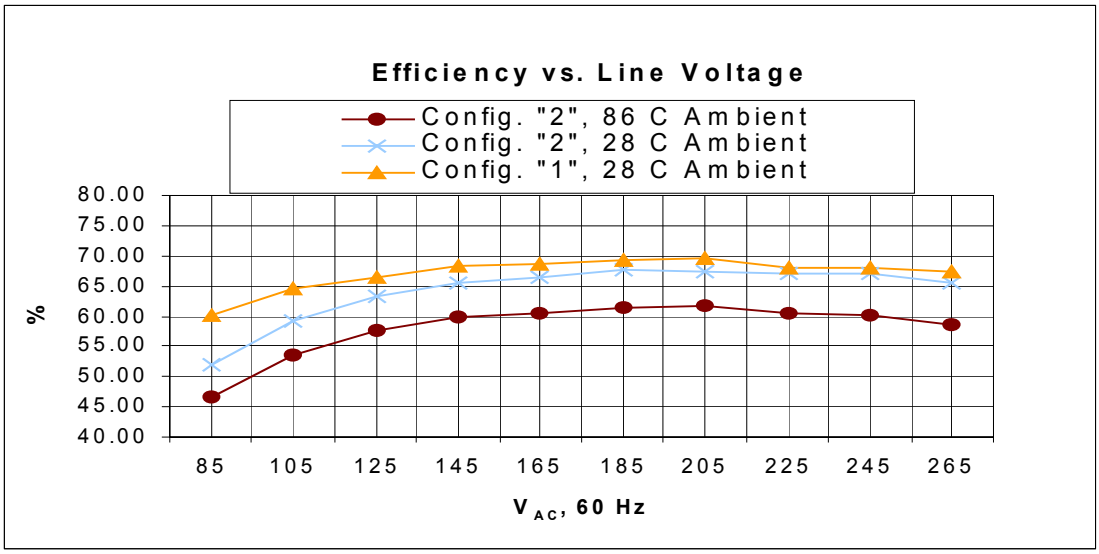

Figure 8.1.1 - Efficiency vs. Input Voltage.

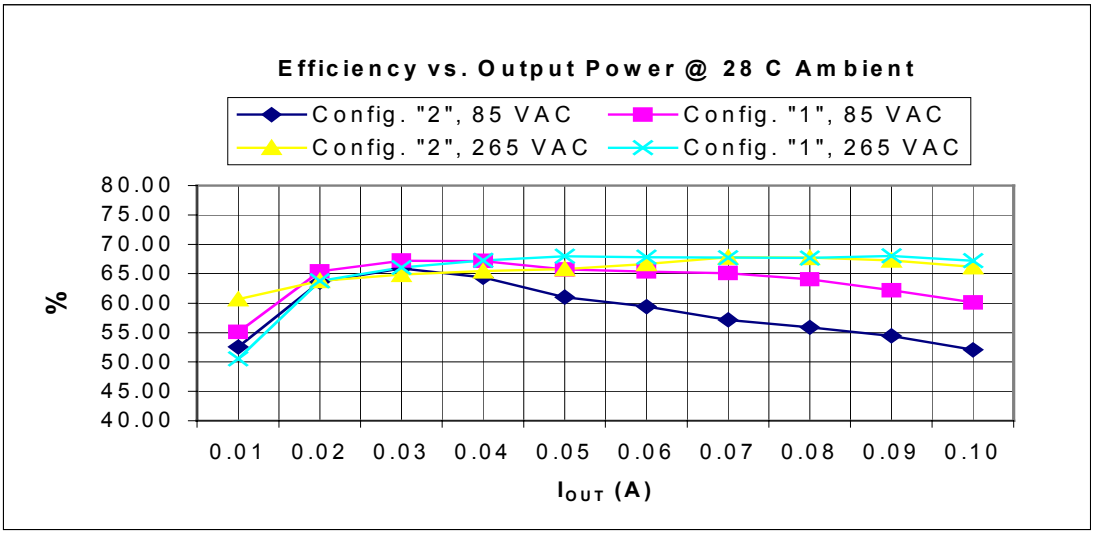

Figure 8.1.2 - Efficiency vs. Output Power.

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8.2 Regulation

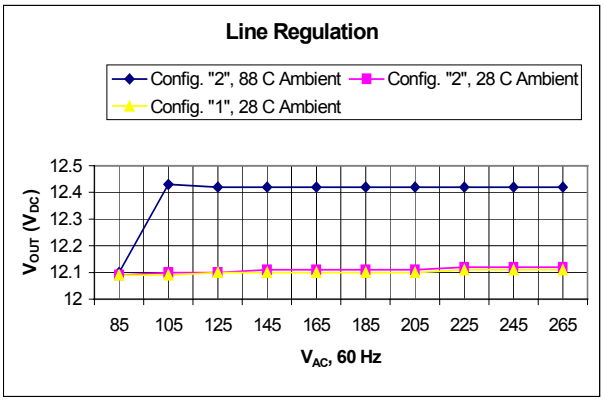

Figure 5.2.1 – Line Regulation at Full Load, 28 °C Ambient.

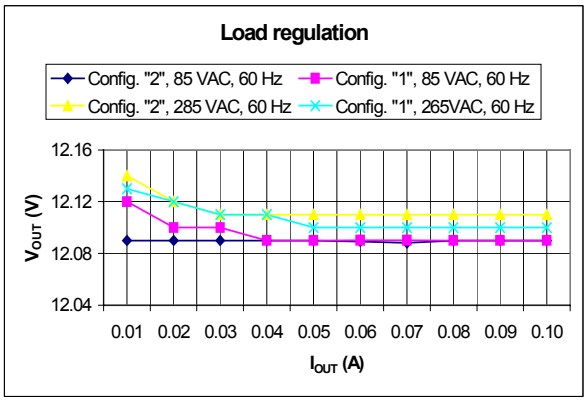

Figure 5.2.2 – Load Regulation, at 28 °C Ambient.

8.3 Temperature

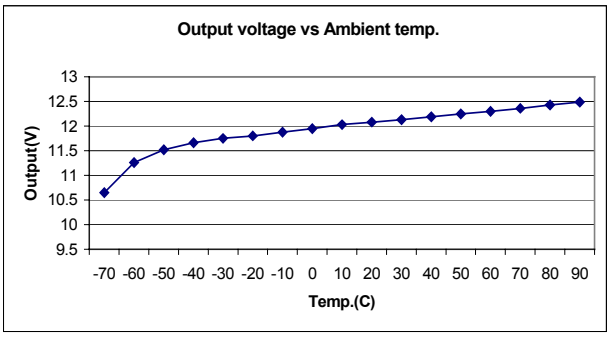

Figure 8.3.1 – Output Voltage at Full Load (0.1 A) Over -70° C to 90° C Ambient.

Thermocouple location	**Low T_{AMB} (°C)** 265 V_{AC}, full load	**High T_{AMB} (°C)** 85 V_{AC}, full load
External Ambient	0	84
Internal Enclosure	2.3	85.4
TNYSwitch (U 1)	26	100
R2	39	102
Output Diode (D2)	15	90
Input Cap (C1)	17	91

Table 8.1 – Components Temperature at Low and High Ambient

Worst case input voltage was selected for the two temperature extremes, 265 V_{AC} (minimum losses) for “Low T” and 85 V_{AC} (maximum losses) for “High T”.
The temperature dependence of the output voltage can be reduced by using two, lower voltage Zener diodes in series.
The unit shut down at 96 °C inside internal enclosure.

8.4 Waveforms

8.4.1 Turn-on delay/hold-up time

8.4.1.1 2 kV config.”1” 85 V_{AC}

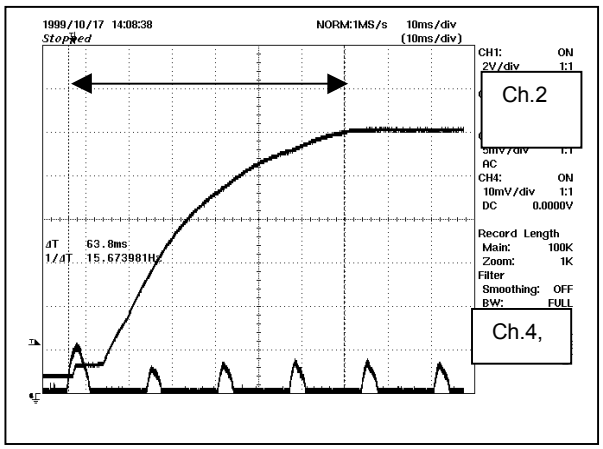

Figure 8.4.1.1 - Output Voltage Turn On Delay at Full Load.
CH2: V_{OUT} (2 V/div),
CH4: I_{IN_MAINS} (0.1 A/div)

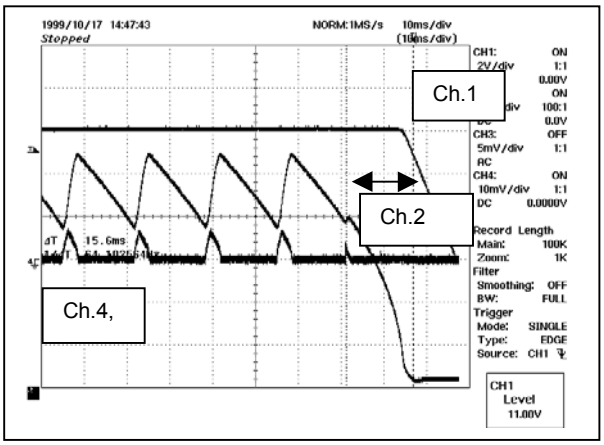

Figure 8.4.1.2 - Output Voltage Hold Up Time.
CH1: V_{OUT} (2 V/div),
CH2: V_{OUT} (2 V/div),
CH4: I_{IN_MAINS} (0.1 A/div)

8.4.1.2 6 kV config.”1” 85 V_{AC}

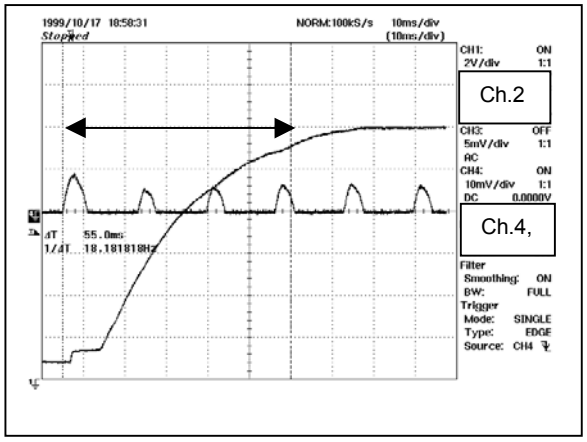

Figure 8.4.1.3 - Output Voltage Turn-on Delay at Full Load.
CH2: V_{OUT} (2 V/div),
CH4: I_{IN_MAINS} (0.1 A/div)

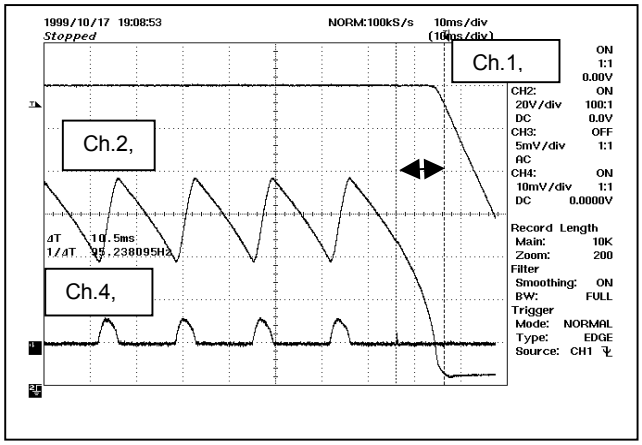

Figure 8.4.1.4 - Output Voltage Hold-up Time at Full Load. CH1: V_{OUT} (2 V/div),
CH2: V_{OUT} (2 V/div),
CH4: I_{IN_MAINS} (0.1 A/div)

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8.4.2 Switch Current and Drain-to-Source Voltage

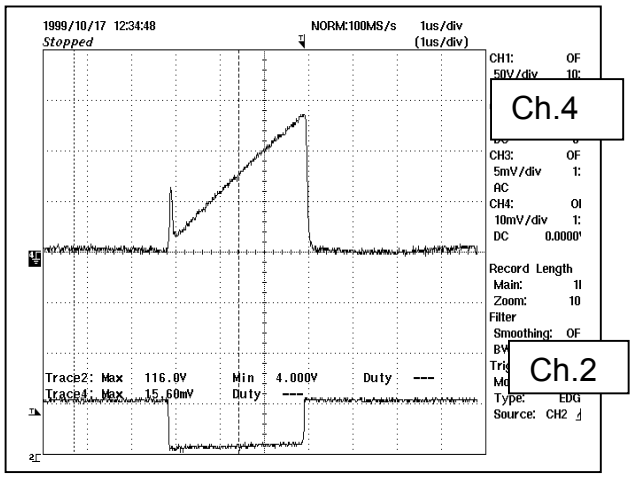

Figure 8.4.2.1 - Full Load at 85 V_{AC}.
CH4: I_{DRAIN}, (100 mA/div),
CH2: V_{DS} (100 V/Div)

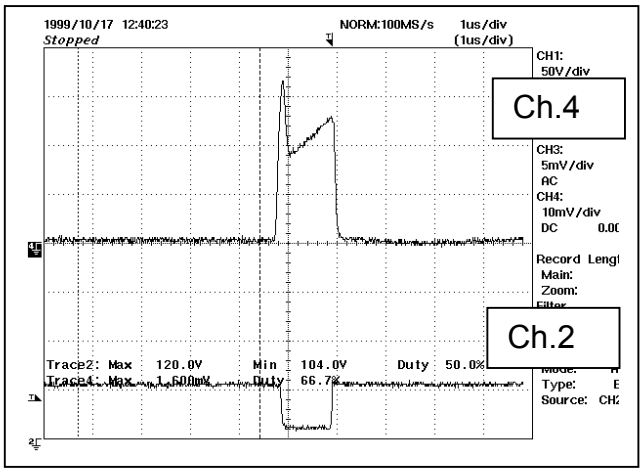

Figure 8.4.2.2 - Short Circuit at 85 V_{AC}.
CH4: I_{DRAIN}, (100 mA/div),
CH2: V_{DS} (100 V/Div)

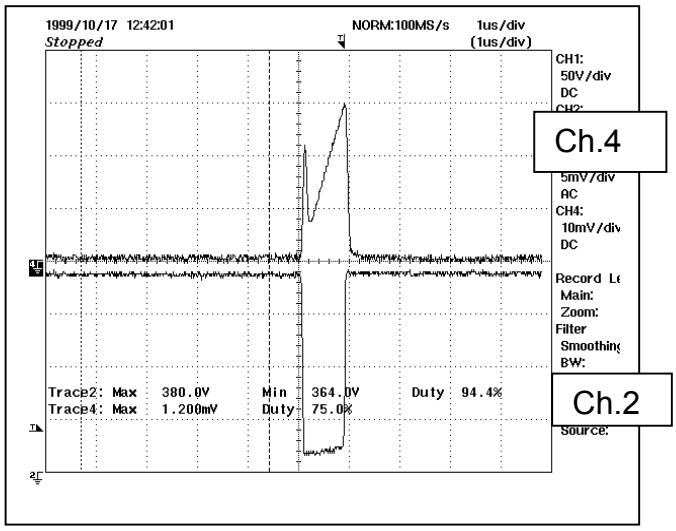

Figure 8.4.2.3 - Full Load at 265 V_{AC}.
CH4: I_{DRAIN}, (100 mA/div),
CH2: V_{DS} (100 V/Div)

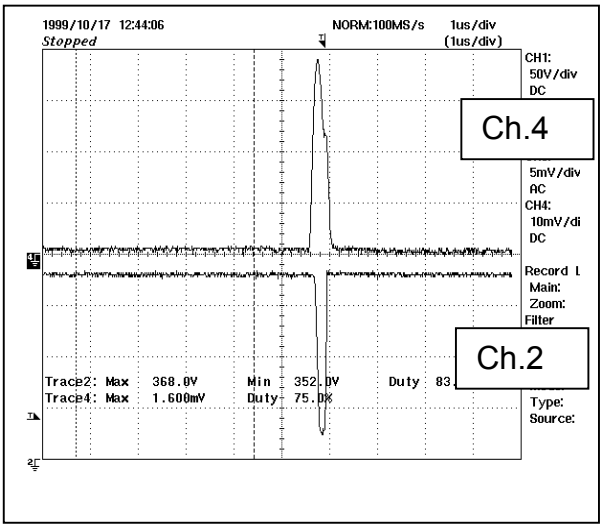

Figure 8.4.2.4 - Short Circuit at 265 V_{AC}.
CH4: I_{DRAIN}, (100 mA/div),
CH2: V_{DS} (100 V/Div)

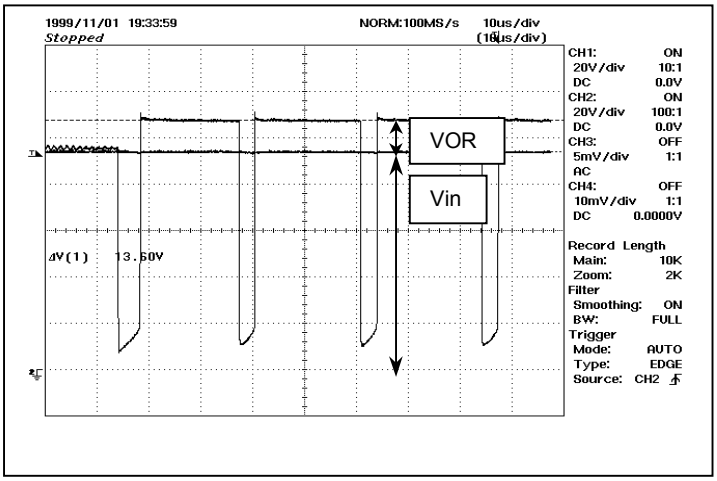

Figure 8.4.2.5 - Drain-Source Voltage (V_{DS}). CH2 (20 V/div). $V_{OR}=V_O+V_D=13.6$ V

8.4.3 Output Voltage Ripple

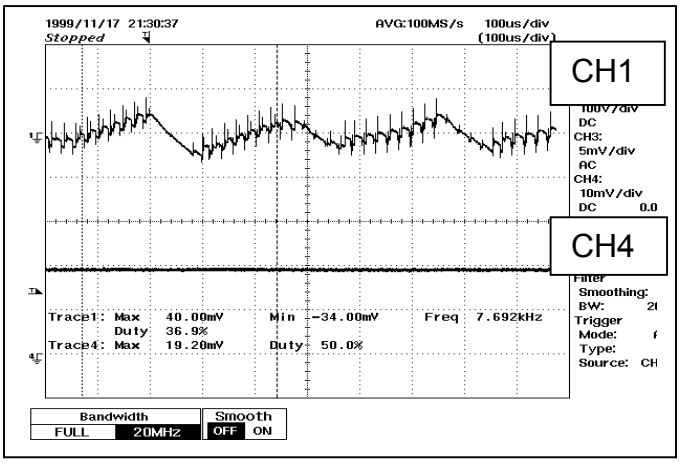

Figure 8.4.3.1 - Switching Ripple at Full Load.
CH1: V_{OUT} (50 mV/div),
CH4: I_{OUT} (50 mA/div)

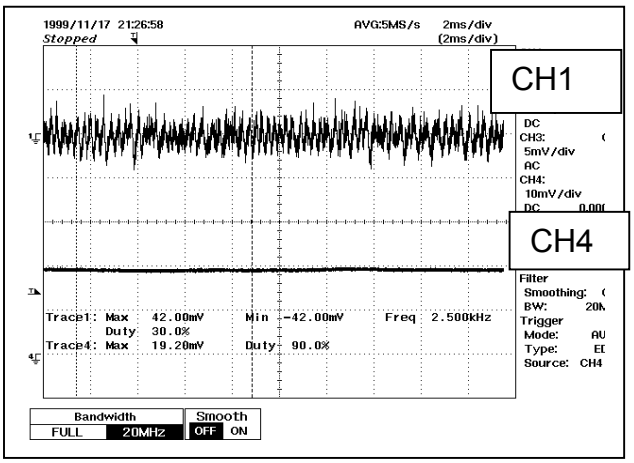

Figure 8.4.3.2 - Switching Frequency Ripple at Full Load.
CH1: V_{OUT} (50 mV/div),
CH4: I_{OUT} (50 mA/div)

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8.5 Transient Response

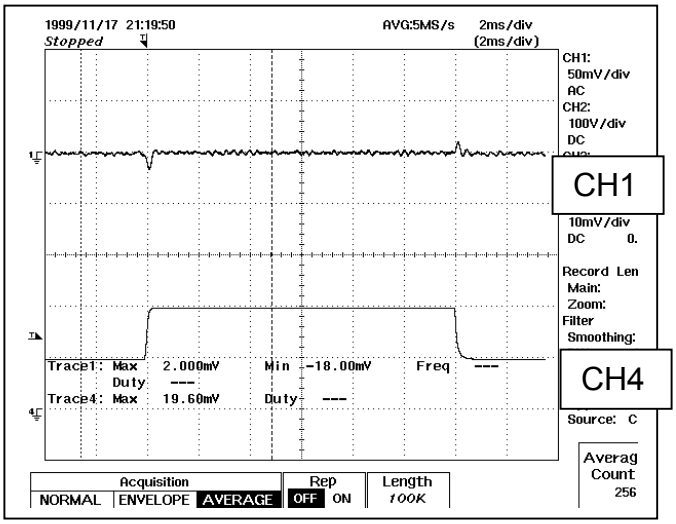

Figure 8.5.1 - Output Voltage Transient Response at 115 V_{AC} 50-100% Load Change. CH1: V_{OUT} (50 mV/div), CH2: I_{OUT} (50 mA/div)

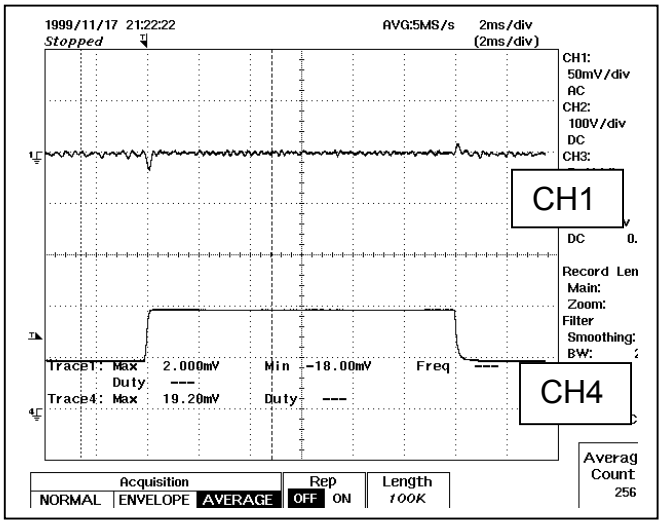

Figure 8.5.2 - Output Voltage Transient Response at 230 V_{AC} 50-100% Load Change. CH1: V_{OUT} (50 mV/div), CH2: I_{OUT} (50 mA/div)

8.6 Surge Voltage Immunity (2 kV and 6 kV, 1.2/50 μs per IEC1000-4-5)

Two series of surge tests were performed:
Configuration “1” (2 kV), Fig. 8.6.1 and configuration “2” (6 kV), Fig. 8.6.2 passed 20 surges each at 45 seconds apart; 10 surges with positive (Fig. 8.6.3) and 10 with negative polarity (Fig. 8.6.4), all at high input line and full load. The 45 seconds delay between surges allows the energy rated components (R1, R2 and RV1) to cool down.

High input line is the worst case condition as the input capacitor (C1) reaches highest voltage therefore minimizing margin for *TinySwitch* breakdown voltage.

R2 limits the charging current during a +voltage surge such that C1 peak voltage does not exceed the TNY254 breakdown voltage.

R1 limits the maximum surge current to approximately 50 A, the value at which the clamping voltage of the varistor is characterized (<700 V). The 6 kV, 1.2/50 μs pulse at 700 V clipping level is approximately 100 μs (see Fig. 8.7.2). From the graph in Fig. 8.6.5, it can be inferred that the unit will survive 10 k surges of -6 kV (more of +6 kV as C1 can divert ~0.3 J).
Reducing the value of R1 would reduce the total number of 6 kV pulses the unit can survive.

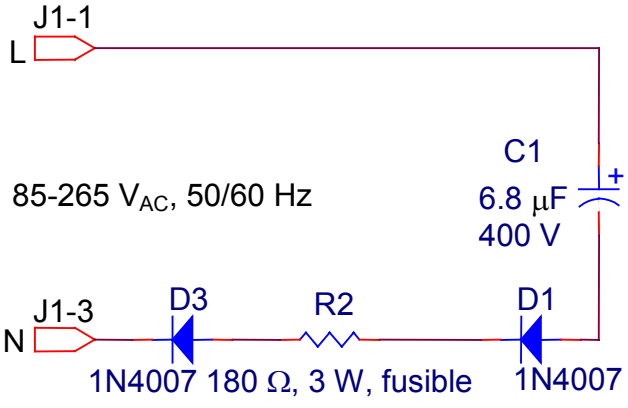

Figure 8.6.1 - Configuration “1”, 2 kV.

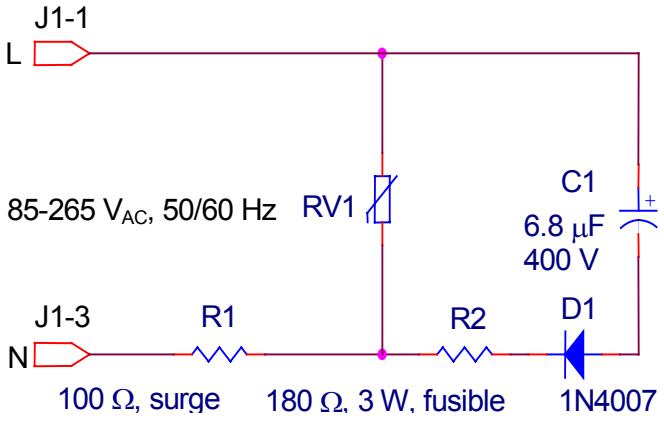

Figure 8.6.2 - Configuration “2”, 6 kV.

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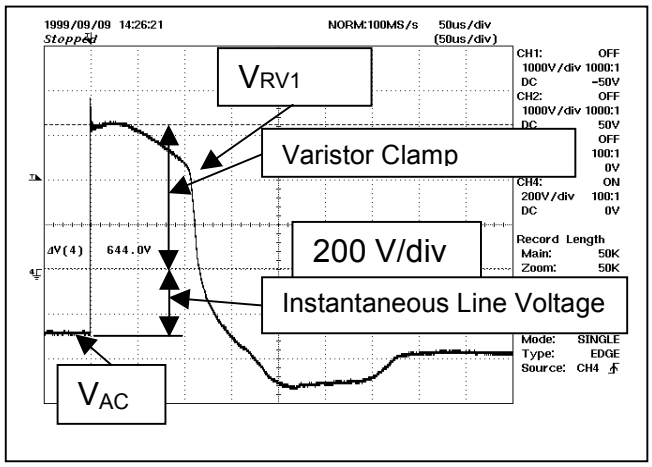

Figure 8.6.3 - RV1 Voltage During +6 kV, 1.2/50 μs Surge.

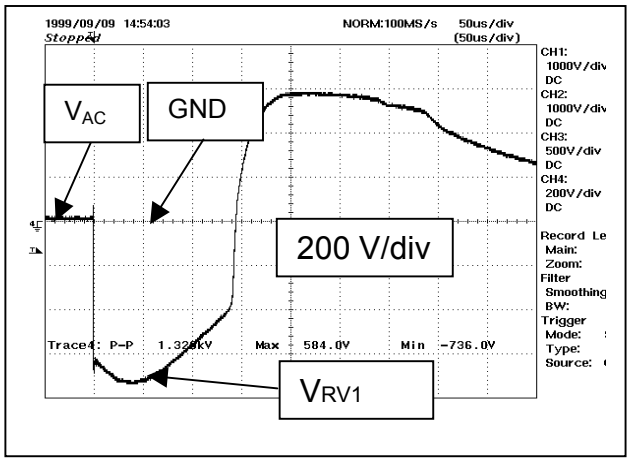

Figure 8.6.4 - RV1 Voltage During -6 kV, 1.2/50 μs Surge.

The pre-trigger voltage is the instantaneous line voltage.
The RV1 voltage is post-trigger and is referenced to the ground.

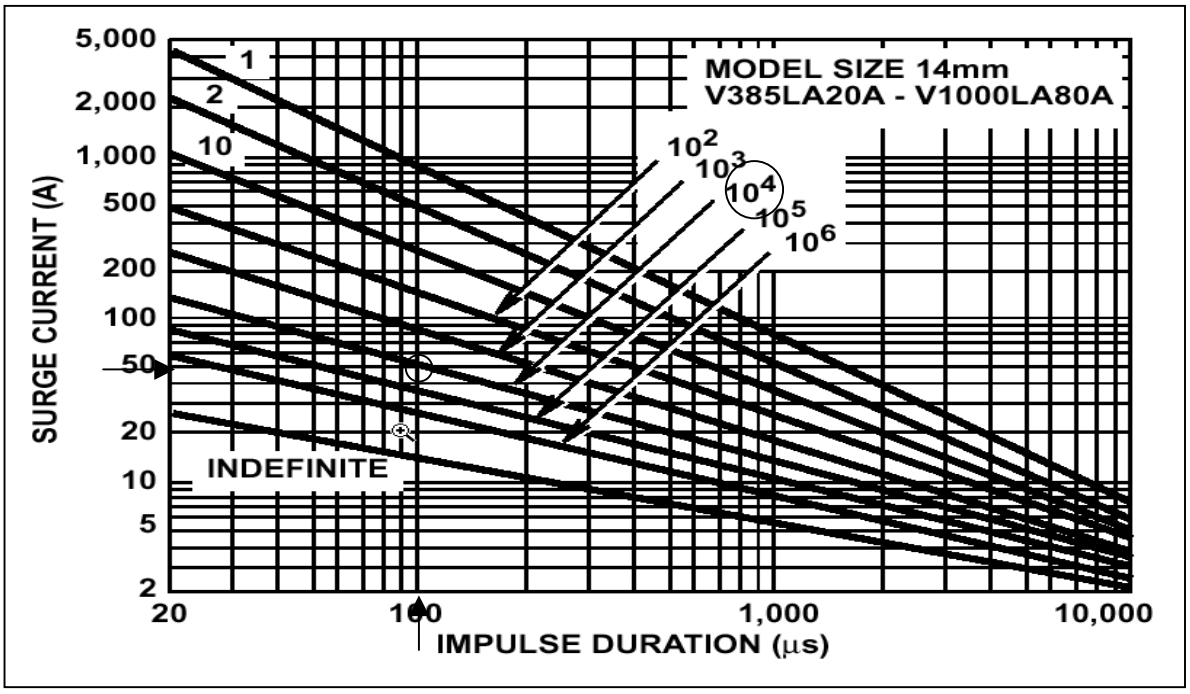

Figure 8.6.5 - Varistor Life (Number of Surges) as a Function of the Rectangular Pulse Amplitude and its Duration.

Revision History

Date	Author	Rev	Description
5-Aug-1999	S. L.	1	First Draft
30-Aug-1999	S. L	2	Second Draft
7-Sep-1999	S. L	3	Third Draft
16-Oct-1999	S. L	4	Fourth Draft
18-Nov-1999	S. L	5	Fifth Draft
24-Nov-1999	S. L	6	Sixth Draft
23-Feb-2000	S. L	7	Seventh Draft
23-Mar-2000	S. L	8	Release
9-Oct-2000	S. L	9	Pg.6, D1+D2 to D1+D3
23-Apr-2001	S. L	10	Pg.8, 6.2 Config. Items 4 and 10

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