DATA SHEET

C-Array: Class 2, Y5V 25 V
Surface mount ceramic multilayer capacitors

Product specification
Supersedes data of 10th February 1999
File under Discrete Ceramics, ACM2

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Philips Components

PHILIPS

Surface mount ceramic multilayer capacitors

C-Array: Class 2, Y5V 25 V

FEATURES

- 4 × 0603 capacitors (of the same capacitance value) per array
- Less than 50% board space of an equivalent discrete component
- High volumetric efficiency
- Dense dielectric layers
- Supplied in tape on reel or loose in bag
- Increased throughput, by time saved in mounting
- Cost savings on manufacturing time.

APPLICATIONS

- Professional electronics
- High density consumer electronics
- Automotive.

DESCRIPTION

Each capacitor element consists of a rectangular block of ceramic dielectric in which a number of interleaved precious metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two terminations, copper dipped with a barrier layer of plated nickel and finally covered with a layer of plated tin (NiSn). An outline of the structure is shown in Fig.1.

QUICK REFERENCE DATA

DESCRIPTION	VALUE
Rated voltage U_R (DC)	25 V (IEC)
Capacitance (E6 series)	10 nF to 100 nF
Tolerance on capacitance	–20 to +80% (Z)
Sectional specifications	IEC 60384-10, second edition 1989-04; also based on CECC 32 100
Detailed specification	based on CECC 32 101-801
Climatic category (IEC 6068)	25/85/21

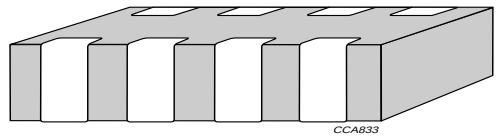
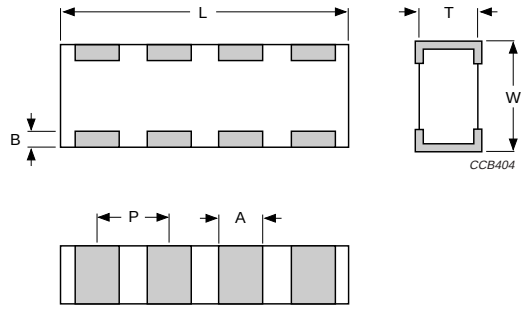


Fig.1 Simplified outline.

MECHANICAL DATA



For dimensions see Table 1.

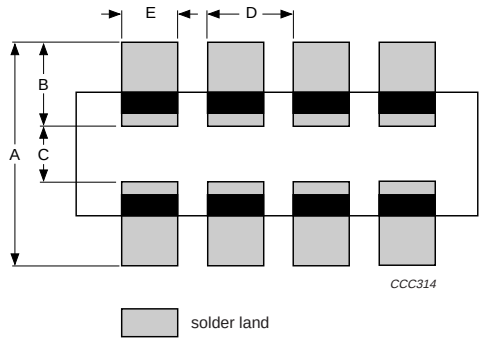
Fig.2 Dimensional outline.

Physical dimensions

Table 1 Capacitor dimensions for product size 0612 (4 × 0603)

CASE SIZE	L	W	T		A	B	P
			MIN.	MAX.			
Dimensions in millimetres							
0612 (4 × 0603)	3.20 ±0.15	1.60 ±0.15	0.50	1.20	0.40 ±0.1	0.30 ±0.2	0.80 ±0.1
Dimensions in inches							
0612 (4 × 0603)	0.125 ±0.006	0.063 ±0.006	0.020	0.047	0.016 ±0.006	0.012 ±0.006	0.031 ±0.004

DIMENSIONS OF SOLDER LANDS



For dimensions see Table 2.

Fig.3 Recommended dimensions of solder lands.

Table 2 Solder land dimensions; see Fig.3

CASE SIZE	FOOTPRINT DIMENSIONS (mm)				
	A	**B**	**C**	**D**	**E**
0612 (4 × 0603)	2.54 ±0.15	0.89 ±0.10	0.76 ±0.10	0.80 ±0.10	0.45 ±0.10

SELECTION CHART

C (nF)	LAST TWO DIGITS OF 12NC	25 V
		0612 (4 × 0603)
10	36	
12	37	
15	38	
18	39	
22	41	
27	42	
33	43	thickness classification: 0.6 ±0.1
39	44	
47	45	
56	46	
68	47	
82	48	
100	49	

Thickness classification and packaging quantities

THICKNESS CLASSIFICATION (mm)	8 mm TAPE WIDTH AMOUNT PER REEL			
	∅180 mm; 7"		∅330 mm; 13"	
	PAPER	BLISTER	PAPER	BLISTER
0.6 ±0.1	4000	4000	10000	10000

ORDERING INFORMATION

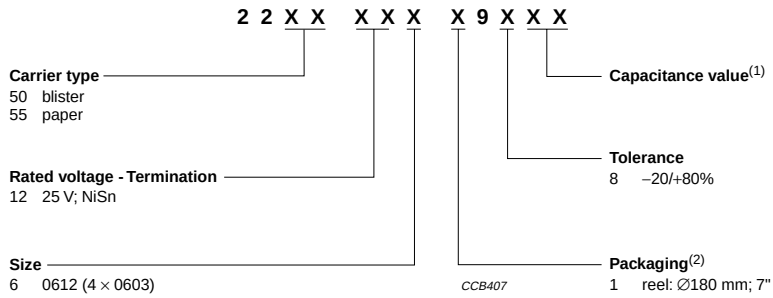
Components may be ordered by using either a simple 15-digit clear text code or Philips unique 12NC.

Clear text code

EXAMPLE: 06122F104K7B20D

SIZE CODE	TEMP. CHAR.	CAPACITANCE	TOL.	VOLTAGE	TERMINATION	PACKAGING	MARKING	SERIES
0612 (4 × 0603)	2F = Y5V	104 = 100000 pF; the third digit signifies the number of zeros	Z = −20/+80%	8 = 25 V	B = NiSn	2 = 180 mm; 7" paper B = 180 mm; 7" blister	0 = no marking	D = BME

Ordering code 12NC



(1) Refer to chapter “Selection chart”.

(2) Amount on reel depends on thickness classification, see section “Thickness classification and packaging quantities”.

ELECTRICAL CHARACTERISTICS FOR CLASS 2, CAPACITORS

Class 2 capacitors; Y5V dielectric; NiSn terminations

Unless otherwise stated all electrical values apply at an ambient temperature of 25 ±1 °C, an atmospheric pressure of 86 to 106 kPa, and a relative humidity of 63 to 67%.

DESCRIPTION	VALUE
Capacitance range (E6 series); note 1	10 nF to 100 nF
Tolerance on capacitance after 1000 hours	–20 to +80% (Z)
Tan δ; note 1	≤7%
Insulation resistance after 1 minute at U_R (DC)	$R_{ins} \times C \geq 500$ s
Ageing	typical 7% per time decade
Resistance to soldering heat	260 °C; 10 seconds

Note

1. Measured at 1 V, using a four-gauge method.

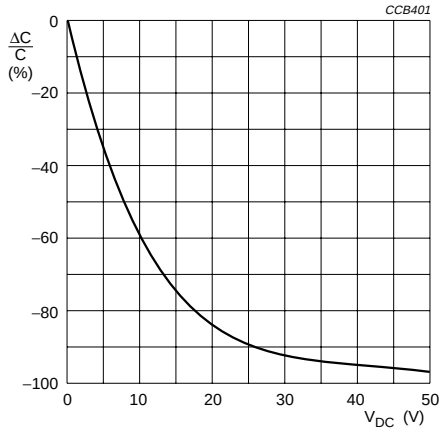


Fig.4 Typical capacitance change with respect to the capacitance at 1 V as a function of DC voltage at 25 °C.

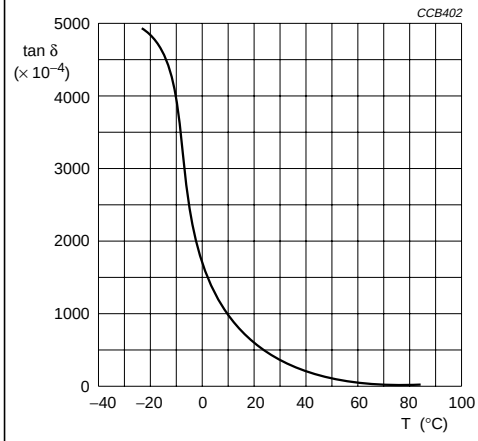


Fig.5 Typical tan δ as a function of temperature.

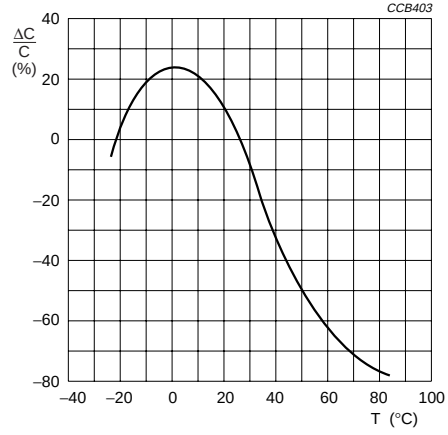


Fig.6 Typical capacitance change as a function of temperature.

TESTS AND REQUIREMENTS

Table 3 Test procedures and requirements

IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.4		mounting	the capacitors may be mounted on printed-circuit boards or ceramic substrates by applying wave soldering, reflow soldering (including vapour phase soldering) or conductive adhesive	no visible damage
4.5		visual inspection and dimension check	any applicable method using ×10 magnification	in accordance with specification
4.6.1		capacitance	f = 1 kHz; measuring voltage 1 V_{rms} at 25 °C	within specified tolerance
4.6.2		tan δ	f = 1 kHz; measuring voltage 1 V_{rms} at 25 °C	in accordance with specification
4.6.3		insulation resistance	at U_R (DC) for 1 minute	$R_i C_R \geq 500$ s
4.6.4		voltage proof	$2.5 \times U_R$ for 1 minutes	no breakdown or flashover
4.7.1		temperature characteristic	between minimum and maximum temperature	in accordance with specification
4.8		adhesion	a force of 5 N applied for 10 s to the line joining the terminations and in a plane parallel to the substrate	no visible damage
4.9		bond strength of plating on end face	mounted in accordance with CECC 32 100, paragraph 4.4	no visible damage
			conditions: bending 1 mm at a rate of 1 mm/s, radius jig 340 mm	ΔC/C: ±30%
4.10	Tb	resistance to soldering heat	preconditioning: 120 to 150 °C during 1 minute; 260 ±5 °C for 10 ±0.5 s in a static solder bath	the terminations shall be well tinned after recovery ΔC/C: ±20% tan δ: original specification R_{ins}: original specification
		resistance to leaching	260 ±5 °C for 30 ±1 s in a static solder bath	using visual enlargement of ×10, dissolution of the terminations shall not exceed 10%
4.11	Ta	solderability	zero hour test, and test after storage (20 to 24 months) in original packing in normal atmosphere; unmounted chips completely immersed for 2 ±0.5 s in a solder bath at 235 ±5 °C	the terminations shall be well tinned

IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.12	Na	rapid change of temperature	preconditioning: between minimum and maximum temperature, 5 cycles	no visual damage after 48 hours recovery: $\Delta C/C$: ±20%
4.14	Ca	damp heat	preconditioning (for initial value measurement): 500 ±12 hours at 40 °C; 90 to 95% RH; U_R applied	pretreatment: $\Delta C/C$: +30%/–40% tan δ: ≤9% R_{ins}: 500 MΩ or $R_i C_R \geq 25$ s, whichever is less
4.15		endurance	initialization: $2 \times U_R$ at 85 °C for 1 hour (initial value is measured after 48 ±4 hours); $2 \times U_R$ at 85 °C for 1000 hours, recovery 48 ±4 hours at room temperature	after 48 hours recovery: $\Delta C/C$: +30%/–40% tan δ: ≤9% R_{ins}: 1000 MΩ or $R_i C_R \geq 50$ s, whichever is less