

OLED DISPLAY MODULE

Product Specification

CUSTOMER	Standard	
PRODUCT NUMBER	DD-12864WE-1A	
CUSTOMER APPROVAL		Date

INTERNAL APPROVALS			
Product Mgr Doc. Control Electr. Eng			
Bruno Anthony Recaldini Perkins		Bazile	
		Peter	



TABLE OF CONTENTS

I	IVI /	AIN FEATURES	4
2	M	ECHANICAL SPECIFICATION	5
	2.1	MECHANICAL CHARACTERISTICS	5
	2.2	MECHANICAL DRAWING	6
3	EL	LECTRICAL SPECIFICATION	7
	3.1	ABSOLUTE MAXIMUM RATINGS	7
	3.2	ELECTRICAL CHARACTERISTICS	8
	3.3	INTERFACE PIN ASSIGNMENT	
	3.4	BLOCK DIAGRAM	
	3.5	TIMING CHARACTERISTICS	
4	OI	PTICAL SPECIFICATION	15
	4.1	OPTICAL CHARACTERISTICS	15
5	FU	UNCTIONAL SPECIFICATION	16
	5.1	COMMANDS	16
	5.2	POWER UP/DOWN SEQUENCE	
	5.3	RESET CIRCUIT	
	5.4	ACTUAL APPLICATION EXAMPLE	17
6	PA	ACKAGING AND LABELLING SPECIFICATION	18
7	QU	UALITY ASSURANCE SPECIFICATION	19
	7.1	CONFORMITY	19
	7.2	DELIVERY ASSURANCE	
	7.3	DEALING WITH CUSTOMER COMPLAINTS	23
8	RF	ELIABILITY SPECIFICATION	24
	8.1	RELIABILITY TESTS	24
	8.2	LIFE TIME	24
9	HA	ANDLING PRECAUTIONS	25

Product No.	DD-12864WE-1A	REV. A
Troduct No.		

Page	2 / 25
------	--------



REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	27 Nov 06			First Issue	

Product No.	DD-12864WE-1A	REV. A
r roduct No.		

Page 3	3 / 25
--------	--------



1 MAIN FEATURES

ITEM	CONTENTS
Display Format	128 x 64 Dots
Overall Dimensions	Glass 26.70 x 19.26 x 2.10 mm
Colour	Monochrome White
Active Area	21.74 x 10.86 mm
Viewing Area	23.74 x 12.86 mm
Display Mode	Passive Matrix (0.96")
Driving Method	1/64 duty
Driver IC	SH1101A
Operating temperature	-30 ∼ +70
Storage temperature	-40 ∼ +80

Product No.	DD-12864WE-1A	REV. A
1 Toduct No.		

Page	4 / 25
- 4.00	.,



2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

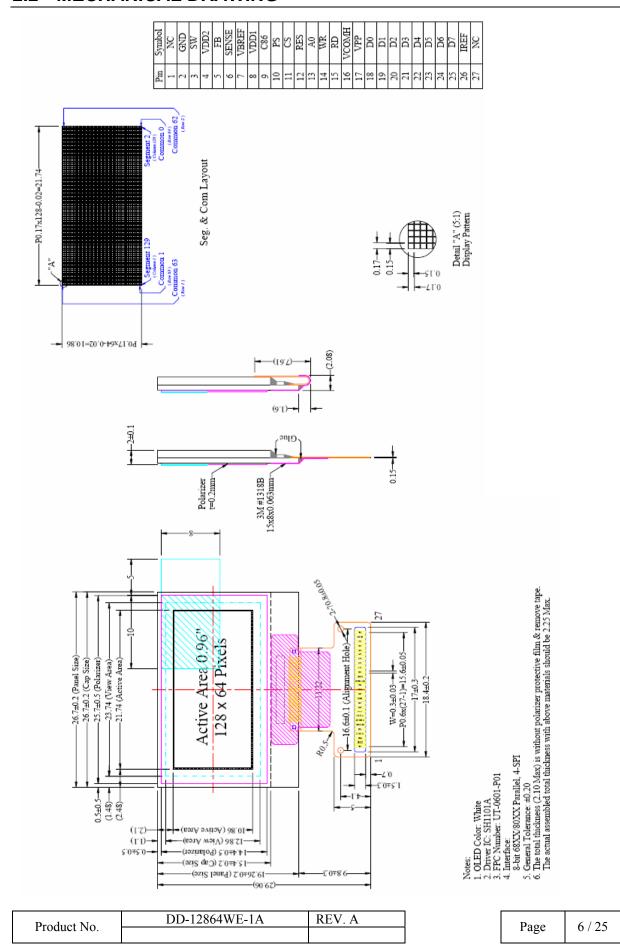
ITEM	CHARACTERISTIC	UNIT
Display Format	128 x 64 Dots	Dots
Overall Dimensions	Glass 26.70 x 19.26 x 2.10	mm
Viewing Area	23.74 x 12.86	mm
Active Area	21.74 x 10.86	mm
Dot Size	0.15 x 0.15	mm
Dot Pitch	0.17 x 0.17	mm
Weight	2	g
IC Controller/Driver	SH1101A	

Product No.	DD-12864WE-1A	REV. A
r roduct No.		

Page	5 / 25
------	--------



2.2 MECHANICAL DRAWING





3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD1}	-0.3	3.5	V	Note 1 2
Driver Supply Voltage	VPP	0	15	V	Note 1, 2
Operating Temperature	Тор	-30	70	°C	
Storage Temperature	Tst	-40	80	°C	
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of "GND=0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent damage to the module may occur. Also for normal operations it's desirable to use this module under the conditions according to Section 3.2 "Electrical Characteristics". If this module is used beyond these conditions the module may malfunction and the reliability could deteriorate.



3.2 ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Тур	Max	Unit
Supply Voltage	V_{DD1}		2.6	2.8	3.5	V
DC/DC Supply Voltage	V _{DD2}		2.6	-	3.5	V
Driver Supply Voltage	VPP		8	9	10	V
High Level Input	V _{IHC}		$0.8 \mathrm{xV}_{\mathrm{DD}_1}$	-	V_{DD1}	V
Low Level Input	V _{ILC}	IOUT=0.5mA,	0	-	0.2 x VDD1	V
High Level Output	V _{OHC}	3.3MHz	0.8 x V DD1	-	V _{DD1}	V
Low Level Output	V _{OLC}		0	-	0.2 x V _{DD} 1	V
Operating current for	I _{DD1}	Note 4	-	180	320	
VDD1	IDD1	Note 5	-	180	320	μA
Operating surrent for VDD	Inn	Note 4	-	5.6	8	A
Operating current for VPP	Ірр	Note 5	-	8	11	mA
Sleep mode current for VDD1	Idd1 Sleep		-	<1	1	μА
Sleep mode current for VCC	ICC SLEEP		-	<1	1	μΑ

Note 4 VDD1 = 2.8V, VPP = 9V, Frame rate = 150Hz, Contrast setting = 0x64, 50% display area turned on.

Note 5 VDD1 = 2.8V, VPP = 9V, Frame rate = 150Hz, Contrast setting = 0x64, 100% display area turned on.

Product No.	DD-12864WE-1A	REV. A

Page	8 / 25
------	--------



3.3 INTERFACE PIN ASSIGNMENT

No.	Symbol	Function		
1	N.C.	No Connection		
2	GND	Ground This is the ground pin. It also acts as a reference for the logic pins, the OLED driving voltages and the analogue circuits. It must be connected to external ground		
3	SW	Output for connected external NMOS This output pin drives the gate of the external NMOS of the booster circuit.		
4	VDD2	Power supply for DC/DC converter circuit This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to VDD when the converter is used. It must be floated when the converter is not used		
5	FB	Feedback Input for DC/DC converter circuit This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level (VCC)		
6	SENSE	Input for connected External NMOS This pin connects to the source current pin of the external NMOS of the booster circuit.		
7	VBREF	Voltage reference for DC/DC converter circuit This pin is the internal voltage reference of booster circuit. A Stabilization capacitor typ 1µF should be connected to VSS.		
8	VDD1	Power supply for logic circuit This is a voltage supply pin. It must be connected to external source.		
9	C86	Communicating protocol select		
10	PS	These pins are MCU interface selection input. See the following table: 6800-parallel 8080-parallel Serial C86 0 1 0 PS 1 1 0		
11	CS	Chip select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.		
12	RES	Power reset for controller and driver This pin is reset signal input. When the pin is low initialization of the chip is executed.		
13	A0	Data/Command Control This pin is data/command control pin. When the pin is pulled high, the input D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals please refer to the Timing Characteristics Diagrams		
14	WR	Read/Write select or write This pin is MCU interface input. When interfacing to a 6800-series microprocessor this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for Read mode and pull it to "Low" for Write mode. When 8080 interface mode is selcted this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.		

Product No	DD-12864WE-1A	REV. A
Product No.		

D	0./05
Page	9 / 25



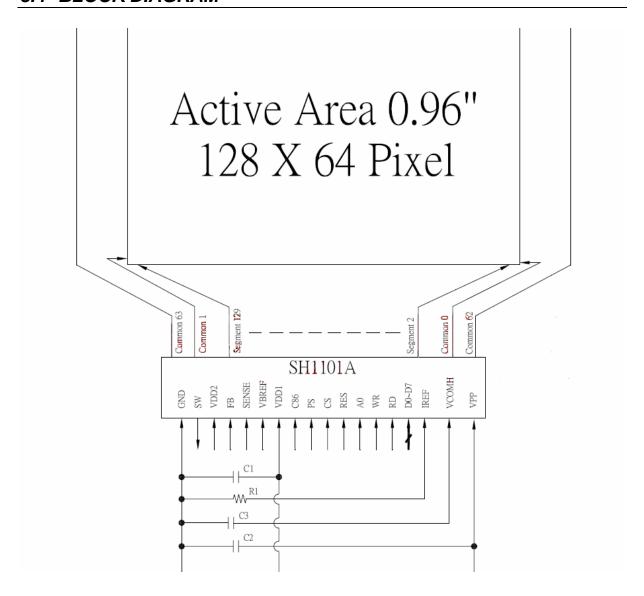
15	RD	Read/Write enable or Read This pin is MCU interface input. When interfacing to a 6800-series microprocessor this pin will be used as the Enable (E) signal. Read/Write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to a 8080-series microprocessor this pin receives the
		Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low
16	VCOMH	Voltage output high level for COM signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
17	VPP	Power Supply for OLED Panel This is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC/DC voltage converter
18		
19		
20		
21	D0 D7	Host data Input/Output bus These pins are 8-bit bi-directional data bus to be connected to the
22	D0~D7	microprocessors data bus. When serial mode is selected D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.
23		input SDIT and DO will be the Schal clock input SCEK.
24		
25		
26	IREF	Current reference for brightness adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10µA
27	N.C.	No Connection

Product No.	DD-12864WE-1A	REV. A
Flouuct No.		

Page	10 / 25
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3.4 BLOCK DIAGRAM



MCU Interface Selection: PS and C86

Pins connected to MCU interface: D7~D0, RD, WR, A0, RES and CS.

*VBREF, SENSE, FB, VDD2 and SW should be left float when using external DC/DC converter.

C1, C2, C3: 4.7µF

R1: $910 \text{ k}\Omega$, R1 = (Voltage at IREF – GND) / IREF

Droduct No	DD-12864WE-1A	REV. A	
Product No.			

Page	11 / 25
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3.5 TIMING CHARACTERISTICS

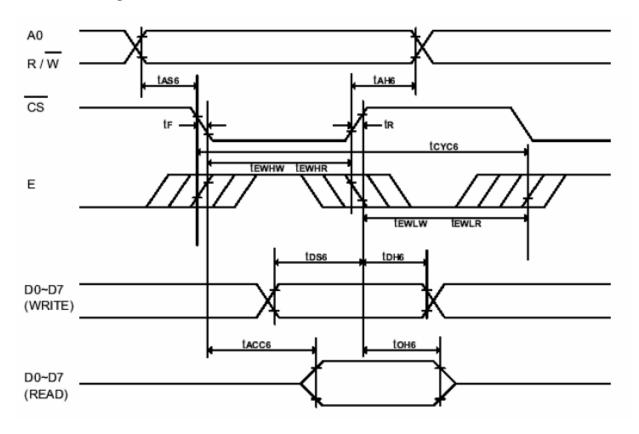
3.5.1 AC CHARACTERISTICS

3.5.1.1 6800-Series MPU Parallel Interface Timing Characteristics

VDD = 2.8V, Ta = 25°C

Characteristics	Symbol	Min	Max	Unit
System cycle time	tCYC6	300	•	
Address setup timing	tAS6	0	•	
Address hold time	tAH6	0	•	
Write Data Setup time	tDS6	40	-	
Write Data Hold time	tDH6	15		
Output Disable time	tOH6	10	70	nS
Access time	tACC6	1	140	113
Enable H pulse width (Write)	tEWHW	100	-	
Enable H pulse width (Read)	tEWHR	120	-	
Enable L pulse width (Write)	tEWLW	100	-	
Enable L pulse width (Read)	tEWLR	100		
Rise time	tR	-	15	
Fall time	tF	-	15	

All the timing should be based on 30% and 70% of V_{DD1} . VSS



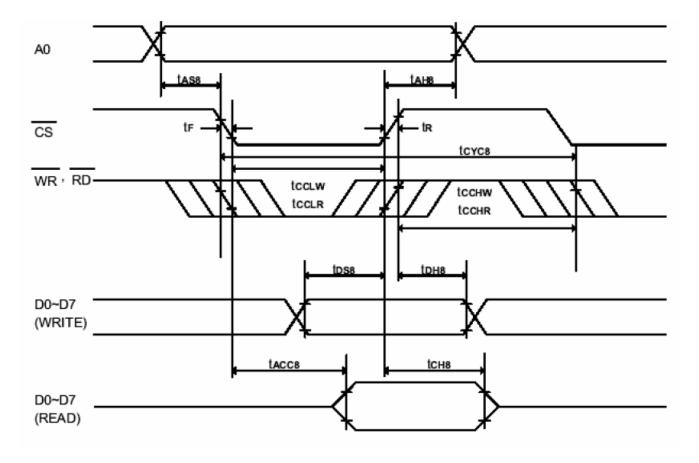
Product No	DD-12864WE-1A	REV. A	Раде	12 / 25
Product No.			rage	12 / 23



3.5.1.2 8080-Series MPU Parallel Interface Timing Characteristics

Characteristics	Symbol	Min	Max	Unit
System cycle time	tCYC8	300	•	
Address setup timing	tAS8	0	•	
Address hold time	tAH8	0	•	
Write Data Setup time	tDS8	40	-	
Write Data Hold time	tDH8	15	•	
Output Disable time	tCH8	10	70	nS
/RD Access time	tACC8	-	140	113
Control L pulse width (WR)	tCCLW	100	-	
Control L pulse width (RD)	tCCLR	120	-	
Control H pulse width (WR)	tCCHW	100	-	
Control H pulse width (RD)	tCCHR	100	-	
Rise time	tR	-	15	
Fall time	tF	-	15	

All the timing should be based on 30% and 70% of V_{DD1}. VSS



Product No.	DD-12864WE-1A	REV. A
Flouuct No.		

Page	13 / 25
------	---------

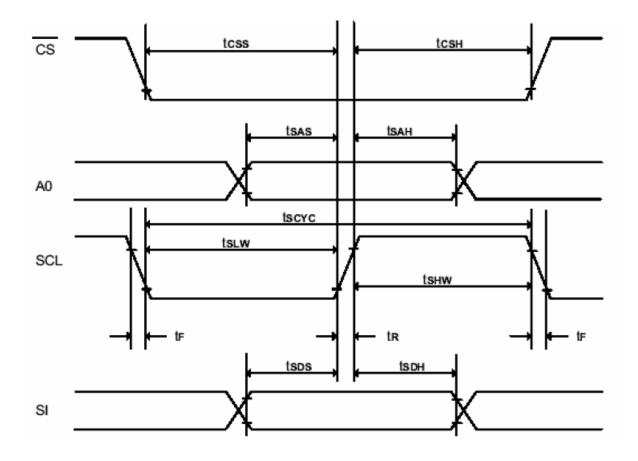


3.5.1.3 Serial Interface Timing Characteristics

VDD = 2.8V, $Ta = 25^{\circ}C$

Characteristics	Symbol	Min	Max	Unit
Serial Clock Cycle Time	Tscyc	250	•	
Address Setup Time	Tsas	150	•	
Address Hold Time	Tsah	150	•	
Data Setup Time	Tsds	100	-	
Data Hold Time	Tsdh	100	-	nS
/CS Setup Time	Tcss	120	-	113
/CS Hold Time	Tcsh	60	-	
Serial clock H pulse width	Tshw	100	-	
Serial clock L pulse width	Tslw	100	-	
Rise Time	tR	-	15	
Fall Time	tF	-	15	

^{*} All the timing should be based on 30% and 70% of $\ensuremath{V_{DD\,\text{-}}}\ensuremath{\text{VSS}}$



Product No.	DD-12864WE-1A	REV. A
Floduct No.		

Page	14 / 25



4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Тур	Max	Unit
Brightness(White)	L_{br}		40	60	-	cd/m ²
C I E (White)	(X)		0.28	0.32	0.36	
C.I.E.(White)	(Y)		0.29	0.33	0.37	-
Dark Room Contrast	CR		-	>100:1	-	-
Viewing Angle			>160	-	-	degree

Optical measurement with polarizer is taken at 1/64 duty, 150Hz Frame Rate, 0x64 Contrast setting.

Product No	DD-12864WE-1A	REV. A
Product No.		

Page	15 / 25



5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

Please refer to the Technical Manual for the SH1101A

5.2 POWER UP/DOWN SEQUENCE

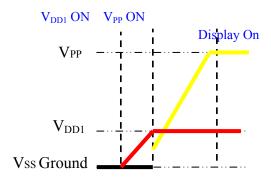
To protect panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

5.2.1 POWER UP SEQUENCE

- 1. Power up V_{DD1}
- 2. Delay 100ms at least (when reset is finished)
- 3. Send Display off command
- 4. Clear Screen
- 5.Power up VPP
- 6. Delay 100ms

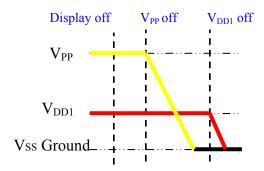
(when VDD1 is stable)

7. Send Display on command



5.2.2 POWER DOWN SEQUENCE

- 1. Send Display off command
- 2. Power down V_{PP}
- 3. Delay 100ms (When V_{PP} reach 0 and panel is completely discharges)
- 4. Power down V_{DD1}



5.3 RESET CIRCUIT

When RES# input is low, the chip is initialized with the following status:

- 1. Display is OFF
- 2. 132x64 Display mode
- 3. Normal segment and display data colume and row address mapping (SEG0 mapped to column address ooH and COM0 mapped to row address 00H)
- 4. Shift register data clear in serial interface
- 5. Display start line is set at display RAM address 0
- 6. Column address counter is set at 0
- 7. Normal scan direction of the COM outputs
- 8. Contrast control register is set at 80H
- 9. Internal booster is selected

Product No.	DD-12864WE-1A	REV. A
Floduct No.		



5.4 ACTUAL APPLICATION EXAMPLE

Command usage and explanation of an actual example

<Initialisation Setting>
Set Display Clock Divide Ratio / Oscillator Frequency (11010101 with XXXXXXXXX)

Set Display Offset (11010011 with **XXXXXX) Set Multiplex Ratio (10101000 with **XXXXXX)

Set DC/DC On/Off (10101101 with 1000101X) 10001010=>0x8A (Off)

Set Display Start Line
(01XXXXXX)
Set Segment Re-map
(1010000X)
Set COM Output Scan Direction
(1100X***)
Set COM Pins Hardware Configuration
(11011010 with 000X0010)
00010010=>0x12 (Alternative Mode)

Set Contrast Control Register (10000001 with XXXXXXXX)

Set Entire Display On/Off (1010010X) 10100100=>0xA4 (Normal) Set Normal/Inverse Display (1010011X) 10100110=>0xA6 (Normal) Set Display On/Off (1010111X) 10101111=> 0xAF (Turns On)

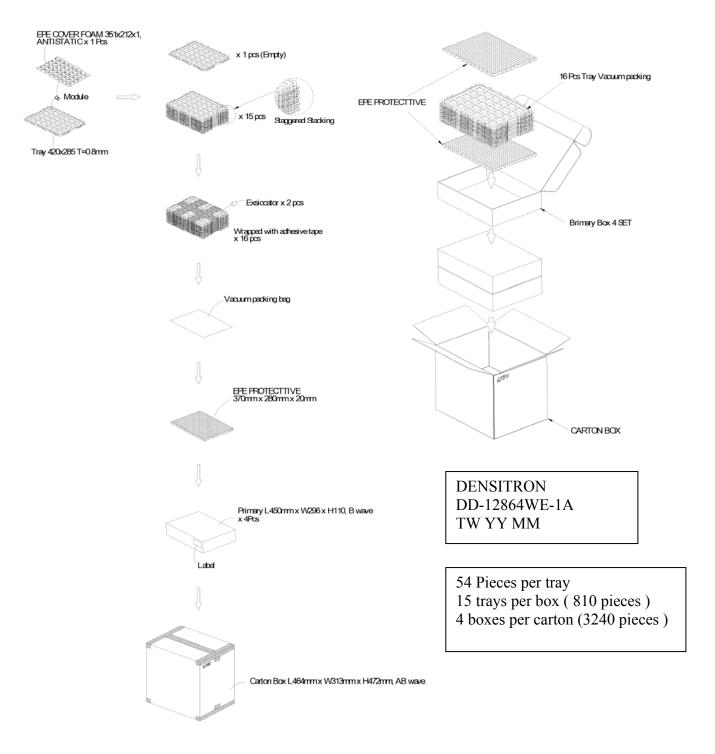
<Display Boundary Settings>
Set Page Address (1011XXXX)
10110000=>0xB0
Set Lower Column Address
(0000XXXX)
Set Higher Column Address
(0001XXXX)

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

Product No.	DD-12864WE-1A	REV. A	Do
Floduct No.			Pa



6 PACKAGING AND LABELLING SPECIFICATION



Product No.	DD-12864WE-1A	REV. A
Floduct No.		

Page	18 / 25
1 age	10/23



7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

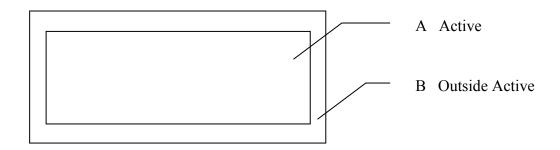
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assemblies standard

7.2.2 Zone definition



7.2.3 Visual inspection

Test and measurement to be conducted under following conditions

Temperature: 23 ± 5 °C

Humidity: 55 ± 15 %RH

Fluorescent lamp: 30 WDistance between the Panel & Eyes of the Inspector: $\ge 30 \text{ cm}$ Distance between the Panel & the lamp: $\ge 50 \text{ cm}$

Product No.	DD-12864WE-1A	REV. A
Flouuct No.		

Page	19 / 25
------	---------



7.2.4 Standard of appearance inspection

Units: mm

Class	Item	Criteria				
Minor	Packing &	Outside & inside package Presence of product no., lot no., quantity				
Critical	Label	Product mus	t not be mixe	d with others and	quantity must not	be different from
			d on the label			
Major	Dimension	Product dim	ensions must	be according to sp	pecification and di	rawing
Major	Electrical	Product elec	trical characte	eristics must be ac	cording to specifi	cation
Critical	OLED Display	Missing line allowed	s, short circui	its or wrong patter	ns on OLED disp	lay are not
Minor	Black spot, white spot,	Round type: $\emptyset = (X+Y)/2$	as per follow	ring drawing		
	dust			A	cceptable quantity	/
				Size	Zone A	Zone B
			<u> </u>	Ø<0.1	Any number	
			Y	0.1<Ø<0.2	3	A nyy nyymh an
		1	F	0.2<Ø<0.25	1	Any number
		X		0.25<Ø	0	1
			s per followin	Acceptal	ple quantity	
		V.W.	Length	Width	Zone A	Zone B
				W≤0.05	Any number	1
			L≤2.0	W≤0.1	3	Any number
		 	L>2.0		0	
			Total accept	table quantity: 3		
Minor	Polariser	Scratch on p	rotective film	is permitted		
	scratch	Scratch on p	olariser: same	e as No. 1		
Minor	Polariser	$\emptyset = (X+Y)/2$	2			
	bubble	Acceptable quantity				
				Size	Zone A	Zone B
			<u>k_</u>	Ø<0.5	Any number	Any number
			Y	Ø>0.5	0	This indicates
		X				

Product No.	DD-12864WE-1A	REV. A
Floduct No.		

Page	20 / 25
------	---------



Class	Item	Criteria		
Minor	Segment deformation	1b. Pin hole on dot matrix display	Acceptable Size $a,b<0.1$ $(a+b)/2\leq0.1$ $0.5<\varnothing<1.0$ Total acceptable	Any number Any number 3
		2. Segments / dots with different width	Accep <u>a≥b</u> a <b< td=""><td>table a/b≤4/3 a/b>4/3</td></b<>	table a/b≤4/3 a/b>4/3
		3. Alignment layer defect $\emptyset = (a+b)/2$	Acceptable Size $\emptyset \leq 0.4$ $0.4 < \emptyset \leq 1.0$ $1.0 < \emptyset \leq 1.5$ $1.5 < \emptyset \leq 2.0$ Total acceptable	Any number 5 3 2
Minor	Panel Chipping	$X \le 1/6$ Panel length $Y \le 1$ $Z \le T$		Z
Minor	Panel Cracking	Cracks not allowed		
Minor	Cupper exposed (pin or film)	Not allowed if visible by eye inspection		
Minor	Film or Trace Damage	Not allowed if affect electrical function		

Product No.	DD-12864WE-1A	REV. A

Page	21 / 25
------	---------



Class	Item		Crit	eria	
Minor	Contact Lead Twist	Not allowed		D. TVISTED LEAD	
Minor	Contact Lead Broken	Not allowed		A. BROKEN LEAD	
Minor	Contact Lead Bent	Not allowed if bent lead causes short circuit			
		Not allowed if bent extends horizontall more than 50% of its width	/ 11111111		
Minor	Colour uniformity	Level of sample for approval set as limit sample			
Major	PCB _	No unmelted solder paste should be present on PCB			
Critical		Cold solder joints, missing solder connections, or oxidation are not allowed			
Minor		No residue or solder balls on PCB are allowed			
Critical Minor	Trovi	Short circuits on components are not allowed			
IVIIIIOF	Tray particles	Size Quantity $\emptyset < 0.2$ Any number		Any number	
	rantito		On tray	Ø>0.25	4
			On display	Ø≥0.25	2
			On display	L = 3	1

Product No.	DD-12864WE-1A	REV. A
Product No.		



7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample. After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.

If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

Product No.	DD-12864WE-1A	REV. A
Floudet No.		

Page	23 / 25
------	---------



8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70°C±2, 120 hours	No abnormalities in function and appearance
Low Temperature Operation	-30°C±2, 120 hours	No abnormalities in function and appearance
High Temperature Storage	80°C±2, 120 hours	No abnormalities in function and appearance
Low Temperature Storage	-40°C±2, 120 hours	No abnormalities in function and appearance
High Temperature & High Humidity Storage(Operation)	60°C±2, 90%RH, 120 hours	No abnormalities in function and appearance
Thermal Shock	24 cycle of -40°C 1 Hour, 85°C 1 Hour. 60 Mins dwell	No abnormalities in function and appearance

- The brightness should be greater than 50% of the initial brightness.
- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 °C; 55±15% RH

8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration more than 10,000 hours under 70 cd/m² brightness and storage conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.

Product No.	DD-12864WE-1A	REV. A

Page	24 / 25
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9 HANDLING PRECAUTIONS

Safety

If the panel breaks, be careful not to get the organic substance in your mouth or in your eyes. If the organic substance touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design

Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.

Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during OLED cleaning

Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.

Do not wipe the display surface with dry or hard materials that will damage the polariser surface. Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge

As the display uses C-MOS LSI drivers, connect any unused input terminal to V_{DD} or V_{SS} . Do not input any signals before power is turned on.

Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging

Displays use OLED elements, and must be treated as such. Avoid strong shock and drop from a height.

To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation

It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.

Other Precautions

When a display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.

Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

Storage

Store the display in a dark place where the temperature is $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ and the humidity below 50%RH.

Store the display in a clean environment, free from dust, organic solvents and corrosive gases. Do not crash, shake or jolt the display (including accessories).

Product No.	DD-12864WE-1A	REV. A
Flouuct No.		

Page	25 / 25
------	---------