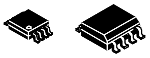


LOW-NOISE, HIGH-OUTPUT DRIVE, CURRENT-FEEDBACK, OPERATIONAL AMPLIFIERS

FEATURES

- **Low Noise**
  - **– 1 pA/√Hz Noninverting Current Noise**
  - **– 10 pA/√Hz Inverting Current Noise**
  - **– 2.5 nV/√Hz Voltage Noise**
- **High Output Current Drive: 475 mA**
- **High Slew Rate: 1700 V/μs (R_L = 50 Ω, V_O = 8 V_{PP})**
- **Wide Bandwidth: 120 MHz (G = 2, R_L = 50 Ω)**
- **Wide Supply Range: ±5 V to ±15 V**
- **Power-Down Feature: (THS3120 Only)**

APPLICATIONS

- **Video Distribution**
- **Power FET Driver**
- **Pin Driver**
- **Capacitive Load Driver**

DESCRIPTION

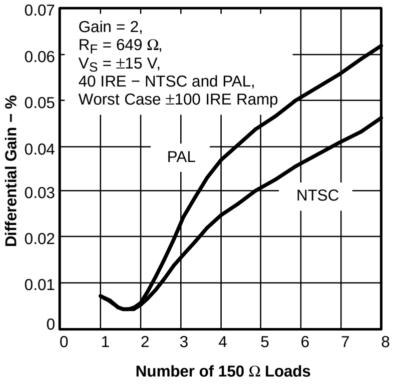
The THS3120 and THS3121 are low-noise, high-voltage, high output current drive, current-feedback amplifiers designed to operate over a wide supply range of ±5 V to ±15 V for today's high performance applications.

The THS3120 offers a power saving mode by providing a power-down pin for reducing the 7-mA quiescent current of the device, when the device is not active.

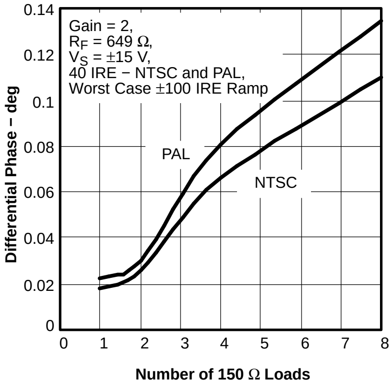
These amplifiers provide well-regulated ac performance characteristics. Most notably, the 0.1-dB flat bandwidth is exceedingly high, reaching beyond 90 MHz. The unity gain bandwidth of 130 MHz allows for good distortion characteristics at 10 MHz. Coupled with high 1700-V/μs slew rate, the THS3120 and THS3121 amplifiers allow for high output voltage swings at high frequencies.

The THS3120 and THS3121 are offered in a 8-pin SOIC (D), and the 8-pin MSOP (DGN) packages with PowerPAD™.

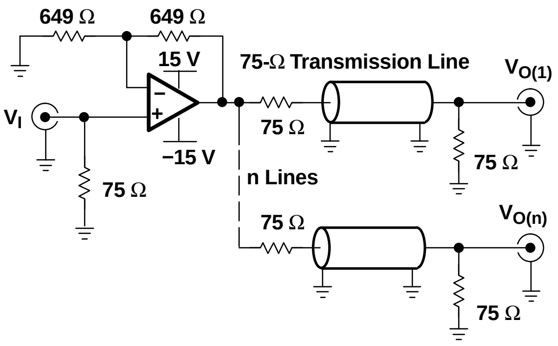
DIFFERENTIAL GAIN vs NUMBER OF LOADS



DIFFERENTIAL PHASE vs NUMBER OF LOADS

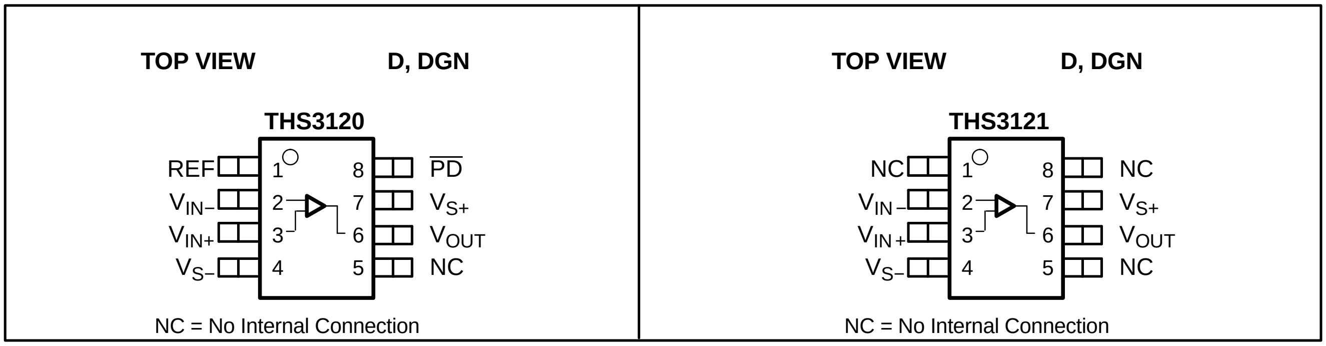


VIDEO DISTRIBUTION AMPLIFIER APPLICATION



PowerPAD is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling procedures and installation procedures can cause damage.



NC = No Internal Connection

NC = No Internal Connection

Note: The device with the power down option defaults to the ON state if no signal is applied to the $\overline{PD}$ pin. Additionallly, the REF pin functional range is from V_{S-} to (V_{S+} − 4 V).

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE		
	PLASTIC SMALL OUTLINE SOIC (D)	PLASTIC MSOP (DGN)(1)(2)	SYMBOL
0°C to 70°C	THS3120CD	THS3120CDGN	AQA
	THS3120CDR	THS3120CDGNR	
-40°C to 85°C	THS3120ID	THS3120IDGN	APN
	THS3120IDR	THS3120IDGNR	
0°C to 70°C	THS3121CD	THS3121CDGN	AQO
	THS3121CDR	THS3121CDGNR	
-40°C to 85°C	THS3121ID	THS3121IDGN	APO
	THS3121IDR	THS3121IDGNR	

(1) Available in tape and reel. The R suffix standard quantity is 2500 (e.g. THS3120CDGNR).
(2) The PowerPAD is electrically isolated from all other pins.

DISSIPATION RATING TABLE

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)	POWER RATING T_J = 125°C	
			T_A = 25°C	T_A = 85°C
D-8(1)	38.3	95	1.05 W	421 mW
DGN-8(2)	4.7	58.4	1.71 W	685 W

(1) This data was taken using the JEDEC standard low-K test PCB. For the JEDEC proposed high-K test PCB, the Θ_{JA} is 95°C/W with power rating at T_A = 25°C of 1.05 W.
(2) This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 inch x 3 inch PCB. For further information, refer to the *Application Information* section of this data sheet.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage	Dual supply	±5		±15	V
	Single supply	10		30	
Operating free-air temperature, T_A	Commercial	0		70	°C
	Industrial	-40		85	
Operating junction temperature, continuous operating, T_J		-40		125	°C
Normal storage temperature, T_{stg}		-40		85	°C

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)(1)

		UNIT
Supply voltage, V_{S-} to V_{S+}		33 V
Input voltage, V_I		± V_S
Differential input voltage, V_{ID}		± 4 V
Output current, I_O(2)		550 mA
Continuous power dissipation		See Dissipation Ratings Table
Maximum junction temperature, T_J(3)		150°C
Maximum junction temperature, continuous operation, long term reliability, T_J(4)		125°C
Operating free-air temperature, T_A	Commercial	0°C to 70°C
	Industrial	-40°C to 85°C
Storage temperature, T_{stg}		-65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C
ESD ratings:		
HBM		1000
CDM		1500
MM		200

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under„ recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The THS3120 and THS3121 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

(3) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.

(4) The maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

ELECTRICAL CHARACTERISTICS

V_S = ±15 V, R_F = 649 Ω,R_L = 50 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TYP	OVER TEMPERATURE				
			25°C	25°C	0°C to 70°C	-40°C to 85°C	UNIT	MIN/TYP/MAX
AC PERFORMANCE								
Small-signal bandwidth, -3 dB	G = 1, R_F = 806 Ω, V_O = 200 mV_{PP}		130				MHz	TYP
	G = 2, R_F = 649 Ω, V_O = 200 mV_{PP}		120					
	G = 5, R_F = 499 Ω, V_O = 200 mV_{PP}		105					
	G = 10, R_F = 301 Ω, V_O = 200 mV_{PP}		66					
0.1 dB bandwidth flatness	G = 2, R_F = 649 Ω, V_O = 200 mV_{PP}		90					
Large-signal bandwidth	G = 5, R_F = 499 Ω , V_O = 2 V_{PP}		80					
Slew rate (25% to 75% level)	G = 1, V_O = 4-V step, R_F = 806 Ω		1500				V/µs	TYP
	G = 2, V_O = 8-V step, R_F = 649 Ω		1700					
Slew rate	Recommended maximum SR for repetitive signals(1)		900				V/µs	MAX
Rise and fall time	G = -5, V_O = 10-V step, R_F = 499Ω		10				ns	TYP
Settling time to 0.1%	G = -2, V_O = 2 V_{PP} step		11				ns	TYP
Settling time to 0.01%	G = -2, V_O = 2 V_{PP} step		52					
Harmonic distortion								
2nd Harmonic distortion	G = 2, R_F = 649 Ω, V_O = 2 V_{PP}, f = 10 MHz	R_L = 50 Ω	51				dBc	TYP
		R_L = 499 Ω	53					
3rd Harmonic distortion		R_L = 50 Ω	50					
		R_L = 499 Ω	65					
Input voltage noise	f > 20 kHz		2.5				nV / √Hz	TYP
Noninverting input current noise	f > 20 kHz		1				pA / √Hz	TYP
Inverting input current noise	f > 20 kHz		10				pA / √Hz	TYP
Differential gain	G = 2, R_L = 150 Ω, R_F = 649 Ω	NTSC	0.007%					TYP
		PAL	0.007%					
Differential phase		NTSC	0.018°					
		PAL	0.022°					
DC PERFORMANCE								
Transimpedance	V_O = ±3.75 V, Gain = 1		1.9	1.3	1	1	MΩ	MIN
Input offset voltage	V_{CM} = 0 V		2	6	8	8	mV	MAX
Average offset voltage drift					±10	±10	µV/°C	TYP
Noninverting input bias current	V_{CM} = 0 V		1	4	6	6	µA	MAX
Average bias current drift					±10	±10	nA/°C	TYP
Inverting input bias current	V_{CM} = 0 V		3	15	20	20	µA	MAX
Average bias current drift					±10	±10	nA/°C	TYP
Input offset current	V_{CM} = 0 V		4	15	20	20	µA	MAX
Average offset current drift					±30	±30	nA/°C	TYP
INPUT CHARACTERISTICS								
Input common-mode voltage range			±13.3	±13	±12.8	±12.8	V	MIN
Common-mode rejection ratio	V_{CM} = ±12.5 V		70	63	60	60	dB	MIN
Noninverting input resistance			41				MΩ	TYP
Noninverting input capacitance			0.4				pF	TYP
OUTPUT CHARACTERISTICS								
Output voltage swing	R_L = 1 kΩ		±14	±13.5	±13	±13	V	MIN
	R_L = 50 Ω		±13.5	±12.5	±12	±12		
Output current (sourcing)	R_L = 25 Ω		475	425	400	400	mA	MIN
Output current (sinking)	R_L = 25 Ω		490	425	400	400	mA	MIN
Output impedance	f = 1 MHz, Closed loop		0.04				Ω	TYP

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(1) For more information, see the *Application Information* section of this data sheet.

ELECTRICAL CHARACTERISTICS (continued)

V_S = ±15 V, R_F = 649 Ω,R_L = 50 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNIT	MIN/TYP/MAX
POWER SUPPLY							
Specified operating voltage		±15	±16	±16	±16	V	MAX
Maximum quiescent current		7	8.5	11	11	mA	MAX
Minimum quiescent current		7	5.5	4	4	mA	MIN
Power supply rejection (+PSRR)	V_{S+} = 15.5 V to 14.5 V, V_{S-} = 15 V	83	75	70	70	dB	MIN
Power supply rejection (-PSRR)	V_{S+} = 15 V, V_{S-} = -15.5 V to -14.5 V	78	70	65	65	dB	MIN
POWER-DOWN CHARACTERISTICS							
Power-down voltage level	Enable, REF = 0 V	≤ 0.8				V	MAX
	Power-down , REF = 0 V	≥ 2					
Power-down quiescent current	PD = 0V	300	450	500	500	µA	MAX
V_{PD} quiescent current	V_{PD} = 0 V, REF = 0 V,	11				µA	TYP
	V_{PD} = 3.3 V, REF = 0 V	11					
Turnon time delay	90% of final value	4				µs	TYP
Turnoff time delay	10% of final value	6					
Input impedance		3.4 || 1.7				kΩ || pF	TYP

ELECTRICAL CHARACTERISTICS

$V_S = \pm5$ V, $R_F = 750\ \Omega$, $R_L = 50\ \Omega$, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TYP	OVER TEMPERATURE				
			25°C	25°C	0°C to 70°C	-40°C to 85°C	UNIT	MIN/TYP/MAX
AC PERFORMANCE								
Small-signal bandwidth, -3 dB	G = 1, $R_F = 909\ \Omega$, $V_O = 200\ mV_{PP}$		105				MHz	TYP
	G = 2, $R_F = 750\ \Omega$, $V_O = 200\ mV_{PP}$		100					
	G = 5, $R_F = 499\ \Omega$, $V_O = 200\ mV_{PP}$		95					
	G = 10, $R_F = 301\ \Omega$, $V_O = 200\ mV_{PP}$		70					
0.1 dB bandwidth flatness	G = 2, $R_F = 750\ \Omega$, $V_O = 200\ mV_{PP}$		70					
Large-signal bandwidth	G = 2, $R_F = 750\ \Omega$, $V_O = 2\ V_{PP}$		85					
Slew rate (25% to 75% level)	G = 1, V_O= 2-V step, $R_F = 909\ \Omega$		560				V/µs	TYP
	G = 2, V_O= 2-V step, $R_F = 750\ \Omega$		620					
Slew rate	Recommended maximum SR for repetitive signals[1]		900				V/µs	MAX
Rise and fall time	G = -5, V_O = 5-V step, $R_F = 499\Omega$		10				ns	TYP
Settling time to 0.1%	G = -2, $V_O = 2\ V_{PP}$ step		7				ns	TYP
Settling time to 0.01%	G = -2, $V_O = 2\ V_{PP}$ step		42					
Harmonic distortion								
2nd Harmonic distortion	G = 2, $R_F = 649\ \Omega$, $V_O = 2\ V_{PP}$, f = 10 MHz	$R_L = 50\Omega$	51				dBc	TYP
		$R_L = 499\ \Omega$	53					
3rd Harmonic distortion		$R_L = 50\Omega$	48					
		$R_L = 499\ \Omega$	60					
Input voltage noise	f > 20 kHz		2.5				nV / √Hz	TYP
Noninverting input current noise	f > 20 kHz		1				pA / √Hz	TYP
Inverting input current noise	f > 20 kHz		10				pA / √Hz	TYP
Differential gain	G = 2, $R_L = 150\ \Omega$, $R_F = 806\ \Omega$	NTSC	0.008%					TYP
		PAL	0.008%					
Differential phase		NTSC	0.014°					
		PAL	0.018°					
DC PERFORMANCE								
Transimpedance	$V_O = \pm1.25$ V, Gain = 1		1.2	0.9	0.7	0.7	MΩ	MIN
Input offset voltage	$V_{CM} = 0$ V		3	6	8	8	mV	MAX
Average offset voltage drift					±10	±10	µV/°C	TYP
Noninverting input bias current	$V_{CM} = 0$ V		1	4	6	6	µA	MAX
Average bias current drift					±10	±10	nA/°C	TYP
Inverting input bias current	$V_{CM} = 0$ V		2	15	20	20	µA	MAX
Average bias current drift					±10	±10	nA/°C	TYP
Input offset current	$V_{CM} = 0$ V		2	15	20	20	µA	MAX
Average offset current drift					±30	±30	nA/°C	TYP
INPUT CHARACTERISTICS								
Input common-mode voltage range			±3.2	±2.9	±2.8	±2.8	V	MIN
Common-mode rejection ratio	$V_{CM} = \pm2.5$ V		66	62	58	58	dB	MIN
Noninverting input resistance			35				MΩ	TYP
Noninverting input capacitance			0.5				pF	TYP
OUTPUT CHARACTERISTICS								
Output voltage swing	$R_L = 1\ k\Omega$		±4	±3.8	±3.7	±3.7	V	MIN
	$R_L = 50\ \Omega$		±3.9	±3.7	±3.6	±3.6		
Output current (sourcing)	$R_L = 10\ \Omega$		310	250	200	200	mA	MIN
Output current (sinking)	$R_L = 10\ \Omega$		325	250	200	200	mA	MIN
Output impedance	f = 1 MHz		0.05				Ω	TYP

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(1) For more information, see the *Application Information* section of this data sheet.

ELECTRICAL CHARACTERISTICS (continued)

V_S = ±5 V, R_F = 750 Ω, R_L = 50 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNIT	MIN/TYP/ MAX
POWER SUPPLY							
Specified operating voltage		±5	±4.5	±4.5	±4.5	V	MIN
Maximum quiescent current		6.5	8	10	10	mA	MAX
Minimum quiescent current		6.5	4	3.5	3.5	mA	MIN
Power supply rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, V_{S-} = 5 V	80	72	67	67	dB	MIN
Power supply rejection (-PSRR)	V_{S+} = 5 V, V_{S-} = -5.5 V to -4.5 V	75	67	62	62	dB	MIN
POWER-DOWN CHARACTERISTICS							
Power-down voltage level	Enable, REF = 0 V	≤ 0.8				V	MAX
	Power-down , REF = 0 V	≥ 0.2					
Power-down quiescent current	PD = 0 V	200	450	500	500	µA	MAX
V_{PD} quiescent current	V_{PD} = 0 V, REF = 0 V,	11				µA	TYP
	V_{PD} = 3.3 V, REF = 0 V	11					
Turnon time delay	90% of final value	4				µs	TYP
Turnoff time delay	10% of final value	6					
Input impedance		3.4 || 1.7				kΩ || pF	TYP

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE
±15-V graphs		
Noninverting small signal gain frequency response		1, 2
Inverting small signal gain frequency response		3
0.1 dB flatness		4
Noninverting large signal gain frequency response		5
Inverting large signal gain frequency response		6
Frequency response capacitive load		7
Recommended R_{ISO}	vs Capacitive load	8
2nd Harmonic distortion	vs Frequency	9
3rd Harmonic distortion	vs Frequency	10
Harmonic distortion	vs Output voltage swing	11, 12
Slew rate	vs Output voltage step	13, 14
Noise	vs Frequency	15
Settling time		16, 17
Quiescent current	vs Supply voltage	18
Output voltage	vs Load resistance	19
Input bias and offset current	vs Case temperature	20
Input offset voltage	vs Case temperature	21
Transimpedance	vs Frequency	22
Rejection ratio	vs Frequency	23
Noninverting small signal transient response		24
Inverting large signal transient response		25
Overdrive recovery time		26
Differential gain	vs Number of loads	27
Differential phase	vs Number of loads	28
Closed loop output impedance	vs Frequency	29
Power-down quiescent current	vs Supply voltage	30
Turnon and turnoff time delay		31
±5-V graphs		
Noninverting small signal gain frequency response		32
Inverting small signal gain frequency response		33
0.1 dB flatness		34
Slew rate	vs Output voltage step	35, 36
2nd Harmonic distortion	vs Frequency	37
3rd Harmonic distortion	vs Frequency	38
Harmonic distortion	vs Output voltage swing	39, 40
Noninverting small signal transient response		41
Inverting small signal transient response		42
Input bias and offset current	vs Case temperature	43
Overdrive recovery time		44
Settling time		45
Rejection ratio	vs Frequency	46

TYPICAL CHARACTERISTICS (±15 V)

NONINVERTING SMALL SIGNAL FREQUENCY RESPONSE

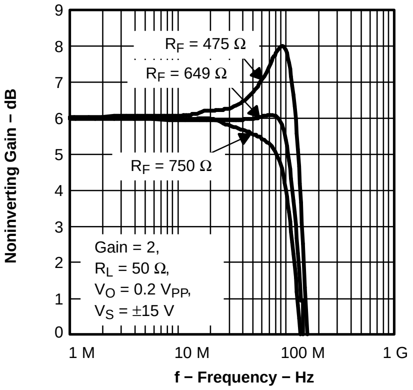


Figure 1.

NONINVERTING SMALL SIGNAL FREQUENCY RESPONSE

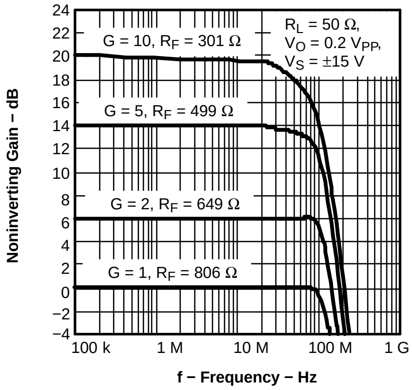


Figure 2.

INVERTING SMALL SIGNAL FREQUENCY RESPONSE

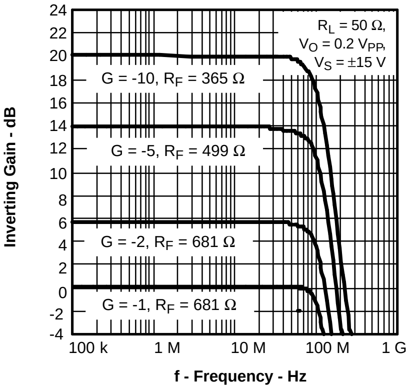


Figure 3.

0.1 dB FLATNESS

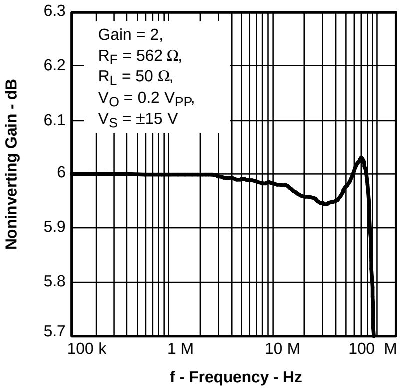


Figure 4.

NONINVERTING LARGE SIGNAL FREQUENCY RESPONSE

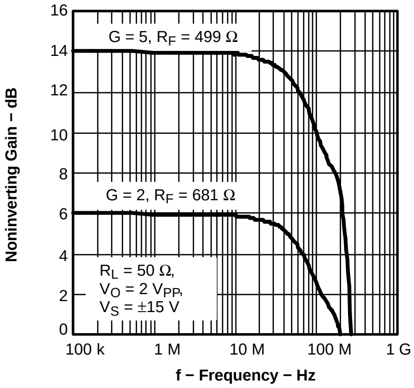


Figure 5.

INVERTING LARGE SIGNAL FREQUENCY RESPONSE

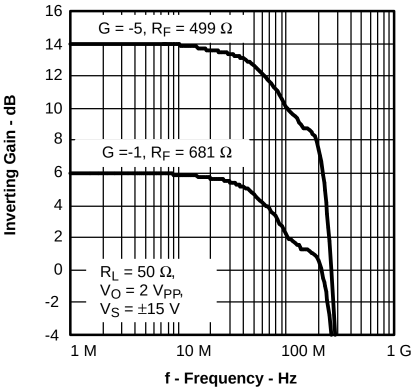


Figure 6.

FREQUENCY RESPONSE CAPACITIVE LOAD

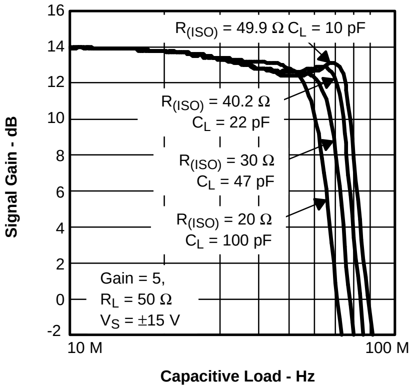


Figure 7.

RECOMMENDED R_{ISO} vs CAPACITIVE LOAD

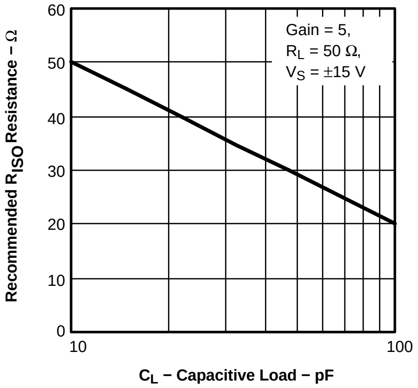


Figure 8.

2nd HARMONIC DISTORTION vs FREQUENCY

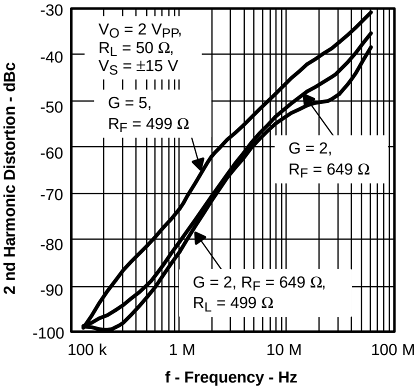


Figure 9.

TYPICAL CHARACTERISTICS (±15 V) (continued)

3rd HARMONIC DISTORTION
vs
FREQUENCY

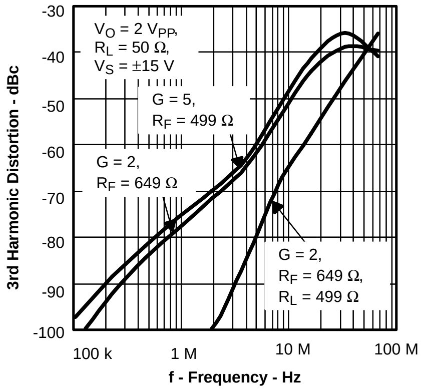


Figure 10.

HARMONIC DISTORTION
vs
OUTPUT VOLTAGE SWING

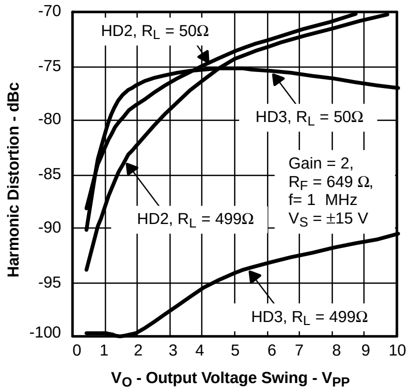


Figure 11.

HARMONIC DISTORTION
vs
OUTPUT VOLTAGE SWING

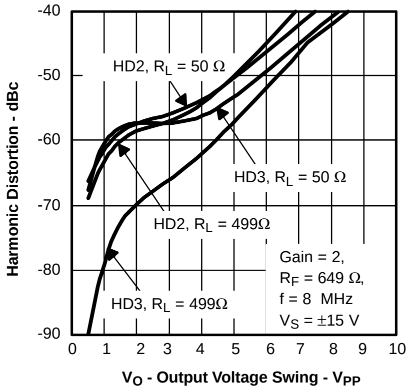


Figure 12.

SLEW RATE
vs
OUTPUT VOLTAGE STEP

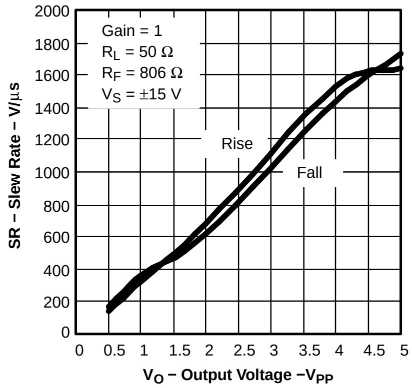


Figure 13.

SLEW RATE
vs
OUTPUT VOLTAGE STEP

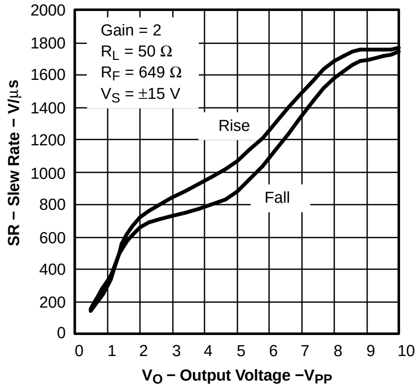


Figure 14.

NOISE
vs
FREQUENCY

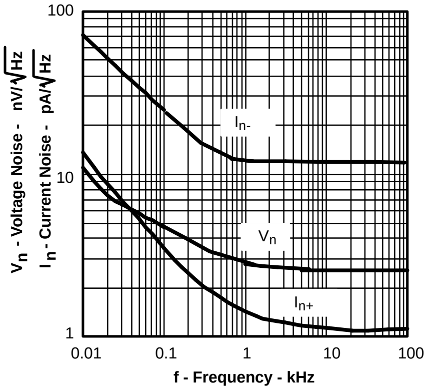


Figure 15.

SETTLING TIME

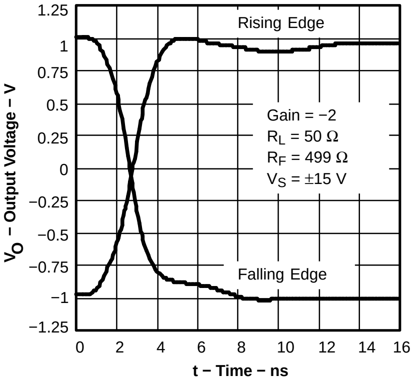


Figure 16.

SETTLING TIME

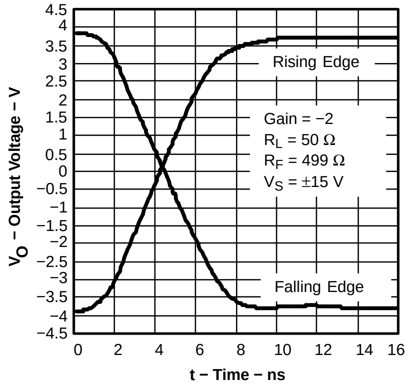
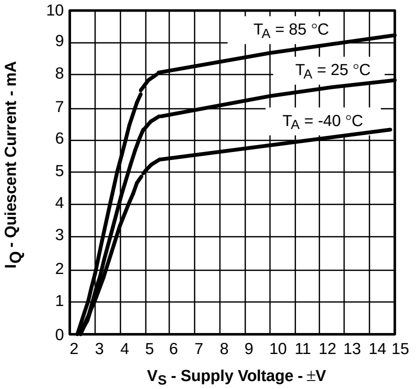


Figure 17.

QUIESCENT CURRENT
vs
SUPPLY VOLTAGE



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TYPICAL CHARACTERISTICS (±15 V) (continued)

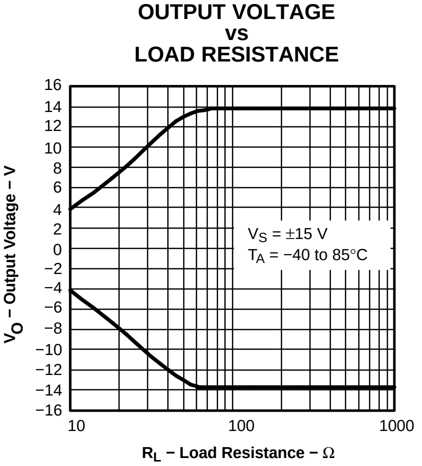

OUTPUT VOLTAGE vs LOAD RESISTANCE

Figure 18.

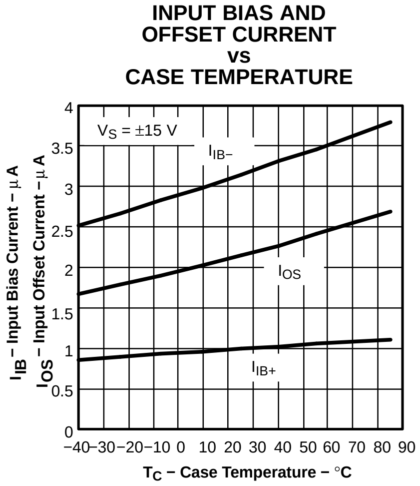

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

Figure 19.

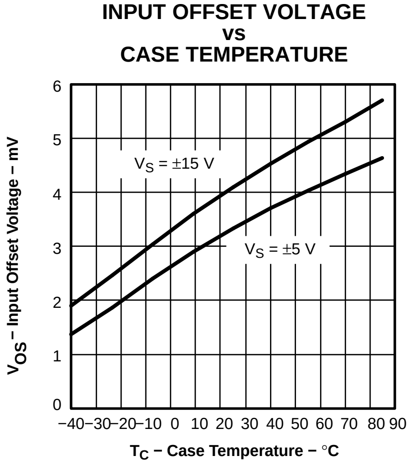

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

Figure 20.

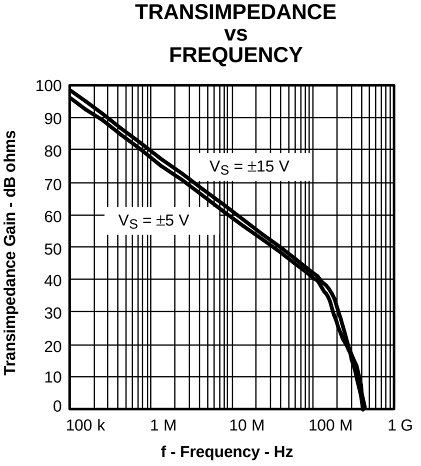

TRANSIMPEDANCE vs FREQUENCY

Figure 21.

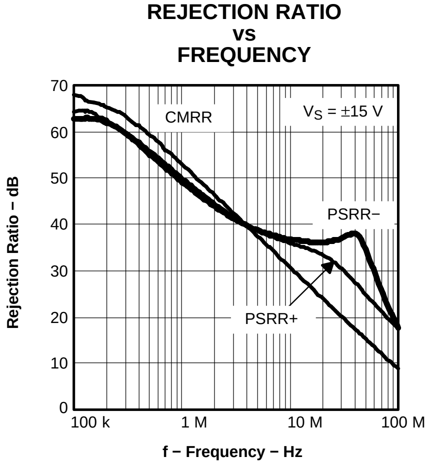

REJECTION RATIO vs FREQUENCY

Figure 22.

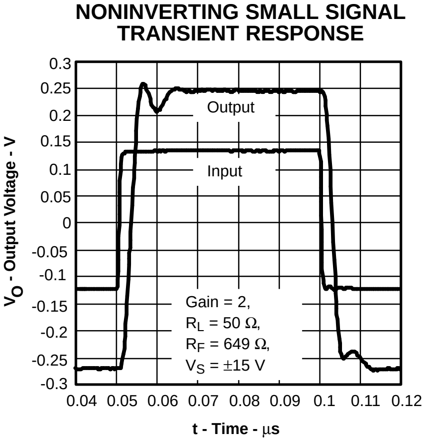

NONINVERTING SMALL SIGNAL TRANSIENT RESPONSE

Figure 23.

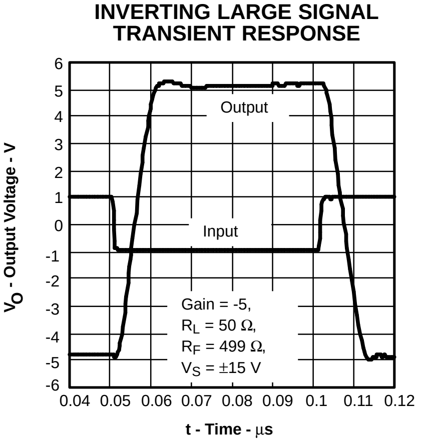

INVERTING LARGE SIGNAL TRANSIENT RESPONSE

Figure 24.

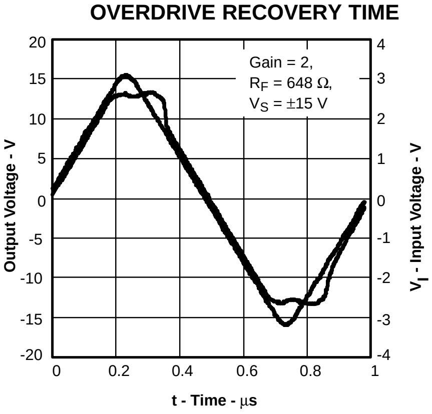

OVERDRIVE RECOVERY TIME

Figure 25.

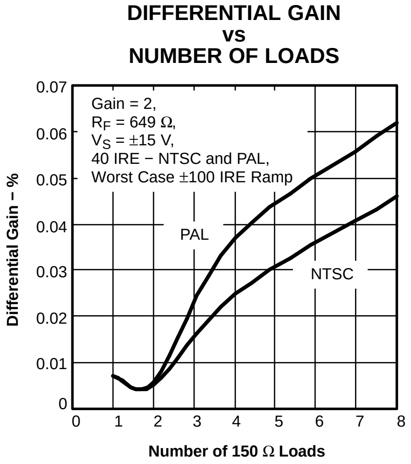

DIFFERENTIAL GAIN vs NUMBER OF LOADS

Figure 26.

TYPICAL CHARACTERISTICS (±15 V) (continued)

DIFFERENTIAL PHASE vs NUMBER OF LOADS

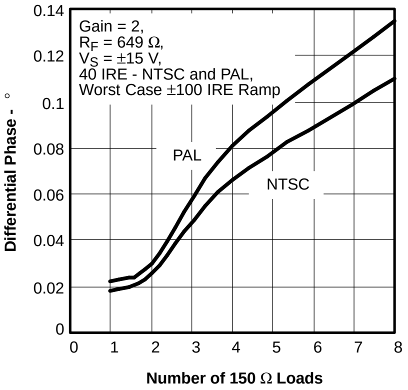
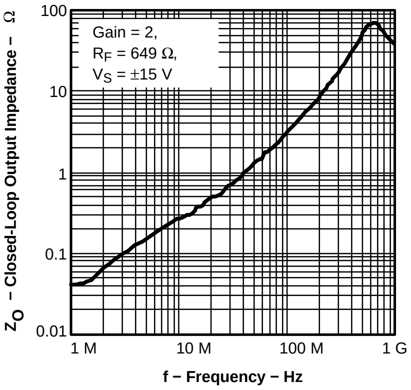


Figure 27.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



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POWER-DOWN QUIESCENT CURRENT vs SUPPLY VOLTAGE

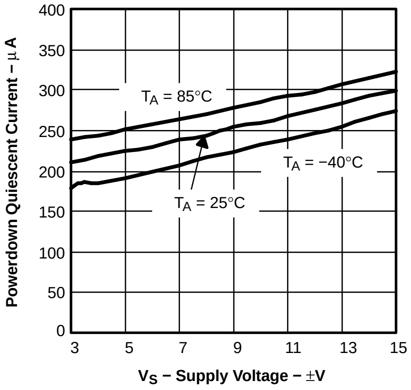


Figure 28.

TURNON AND TURNOFF TIME DELAY

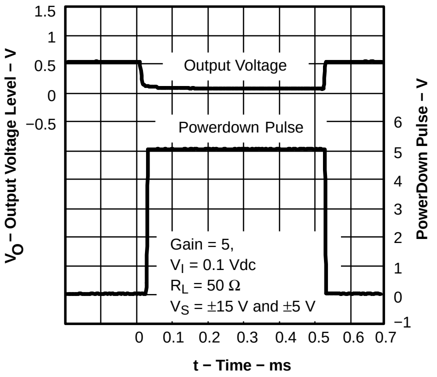


Figure 29.

TYPICAL CHARACTERISTICS (±5 V)

NONINVERTING SMALL SIGNAL FREQUENCY RESPONSE

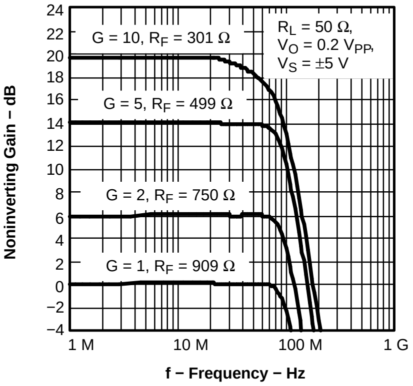


Figure 30.

INVERTING SMALL SIGNAL FREQUENCY RESPONSE

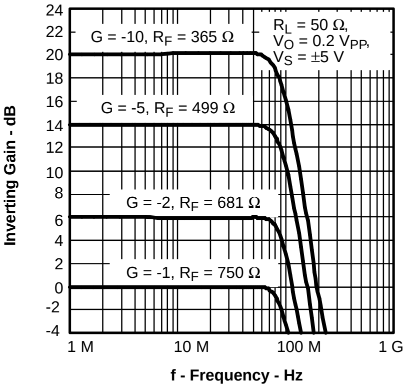


Figure 31.

0.1 dB FLATNESS

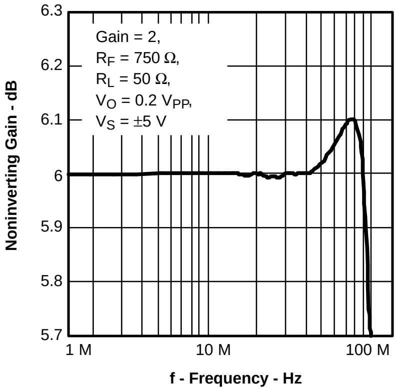


Figure 32.

SLEW RATE vs OUTPUT VOLTAGE STEP

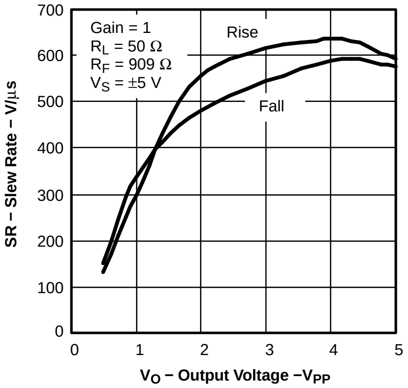


Figure 33.

SLEW RATE vs OUTPUT VOLTAGE STEP

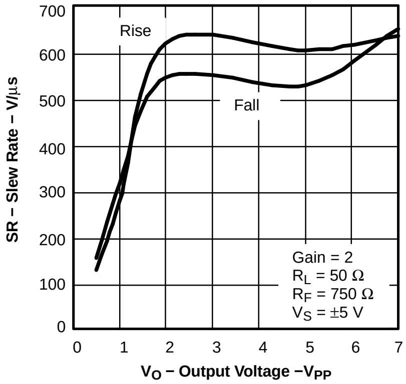


Figure 34.

2nd HARMONIC DISTORTION vs FREQUENCY

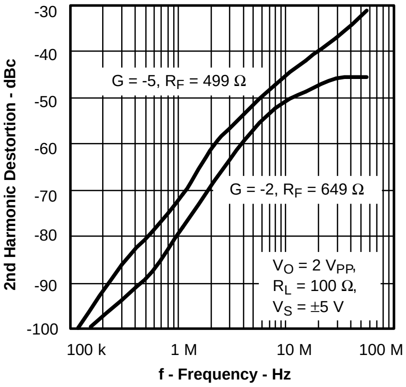


Figure 35.

3rd HARMONIC DISTORTION vs FREQUENCY

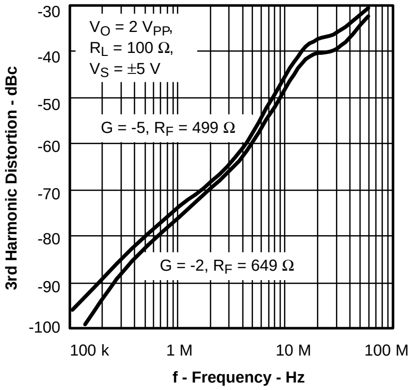


Figure 36.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

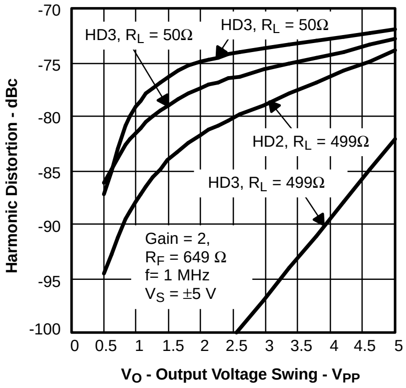


Figure 37.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

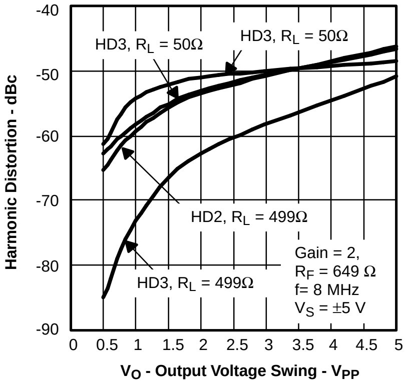


Figure 38.

TYPICAL CHARACTERISTICS (±5 V) (continued)

NONINVERTING SMALL SIGNAL TRANSIENT RESPONSE

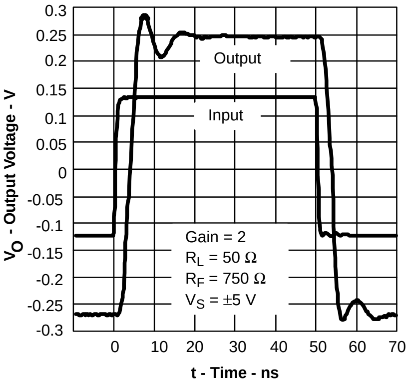


Figure 39.

INVERTING LARGE SIGNAL TRANSIENT RESPONSE

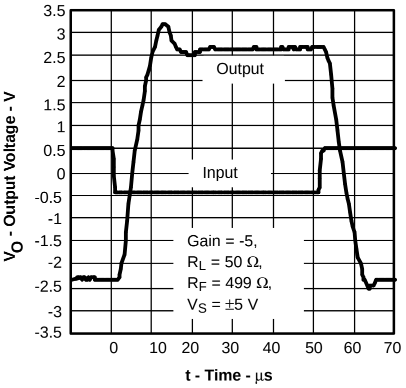


Figure 40.

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

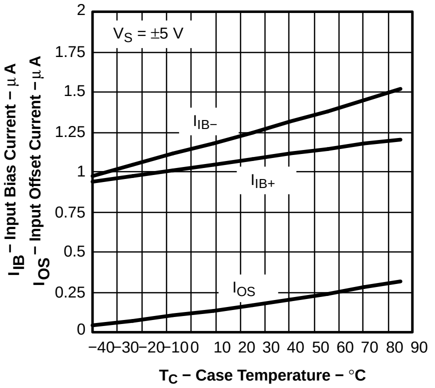


Figure 41.

OVERDRIVE RECOVERY TIME

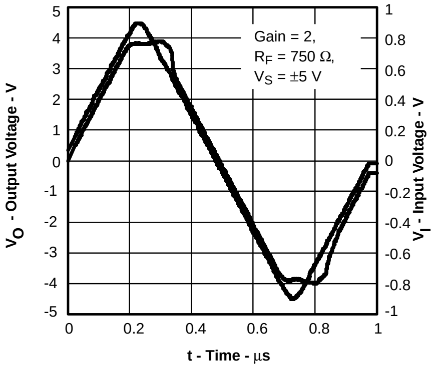


Figure 42.

SETTLING TIME

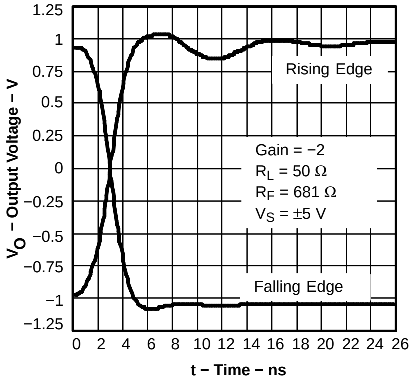


Figure 43.

REJECTION RATIO vs FREQUENCY

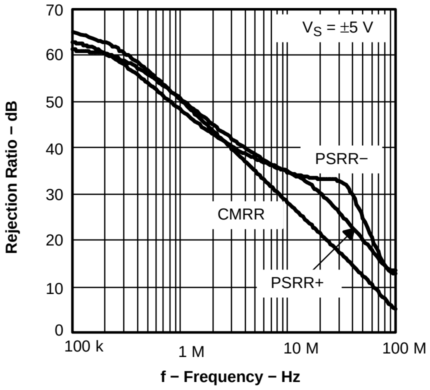


Figure 44.

APPLICATION INFORMATION

Maximum Slew Rate for Repetitive Signals

The THS3120 and THS3121 are recommended for high slew rate pulsed applications where the internal nodes of the amplifier have time to stabilize between pulses. It is recommended to have at least 20-ns delay between pulses.

The THS3120 and THS3121 are not recommended for applications with repetitive signals (sine, square, sawtooth, or other) that exceed 900 V/μs. Using the part in these applications results in excessive current draw from the power supply and possible device damage.

For applications with high slew rate, repetitive signals, the THS3091 and THS3095 (single), or THS3092 and THS3096 (dual) are recommended.

WIDEBAND, NONINVERTING OPERATION

The THS3120 and THS3121 are unity gain stable 130-MHz current-feedback operational amplifiers, designed to operate from a ±5-V to ±15-V power supply.

Figure 45 shows the THS3121 in a noninverting gain of 2-V/V configuration typically used to generate the performance curves. Most of the curves were characterized using signal sources with 50-Ω source impedance, and with measurement equipment presenting a 50-Ω load impedance.

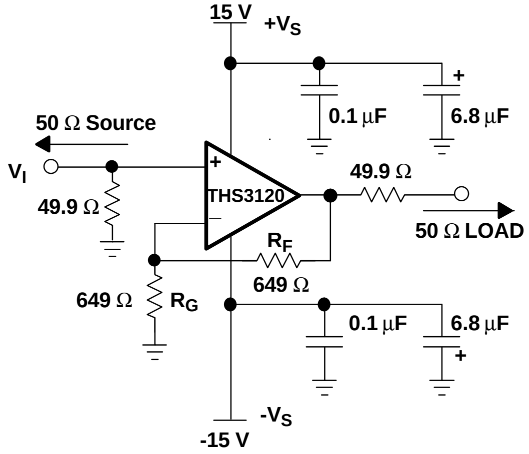


Figure 45. Wideband, Noninverting Gain Configuration

Current-feedback amplifiers are highly dependent on the feedback resistor R_F for maximum performance and stability. Table 1 shows the optimal gain setting resistors R_F and R_G at different gains to give maximum bandwidth with minimal peaking in the frequency response. Higher bandwidths can be achieved, at the expense of added peaking in the frequency response, by using even lower values for R_F. Conversely, increasing R_F decreases the bandwidth, but stability is improved.

Table 1. Recommended Resistor Values for Optimum Frequency Response

THS3120 and THS3121 R_F and R_G values for minimal peaking with R_L = 50 Ω			
GAIN (V/V)	SUPPLY VOLTAGE (V)	R_G (Ω)	R_F (Ω)
1	±15	--	806
	±5	--	909
2	±15	649	649
	±5	750	750
5	±15	124	499
	±5	124	499
10	±15	33.2	301
	±5	33.2	301
-1	±15	681	681
	±5	750	750
-2	±15 and ±5	340	681
-5	±15 and ±5	100	499
-10	±15 and ±5	36.5	365

WIDEBAND, INVERTING OPERATION

Figure 46 shows the THS3121 in a typical inverting gain configuration where the input and output impedances and signal gain from Figure 45 are retained in an inverting circuit configuration.

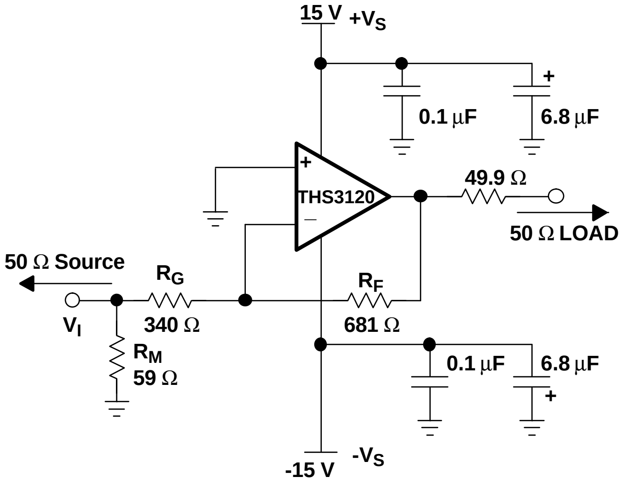


Figure 46. Wideband, Inverting Gain Configuration

SINGLE SUPPLY OPERATION

The THS3120 and THS3121 have the capability to operate from a single supply voltage ranging from 10 V to 30 V. When operating from a single power supply, biasing the input and output at mid-supply allows for the maximum output voltage swing. The circuits shown in Figure 47 shows inverting and noninverting amplifiers configured for single supply operations.

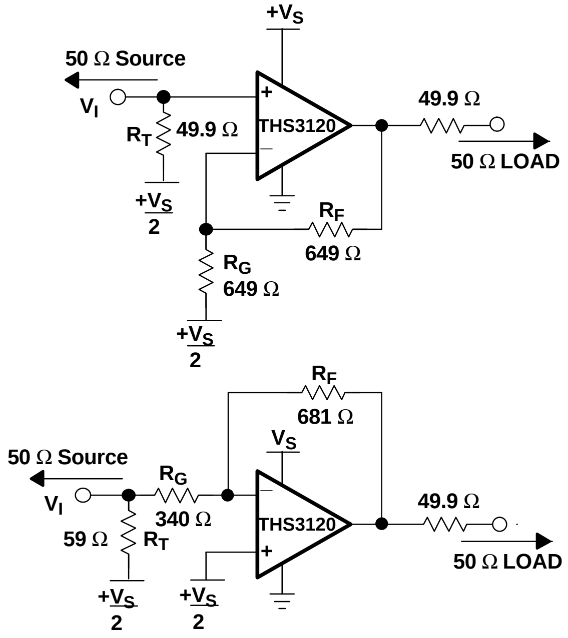


Figure 47. DC-Coupled, Single-Supply Operation

Video Distribution

The wide bandwidth, high slew rate, and high output drive current of the THS3120 and THS3121 matches the demands for video distribution for delivering video signals down multiple cables. To ensure high signal quality with minimal degradation of performance, a 0.1-dB gain flatness should be at least 7x the passband frequency to minimize group delay variations from the amplifier. A high slew rate minimizes distortion of the video signal, and supports component video and RGB video signals that require fast transition times and fast settling times for high signal quality.

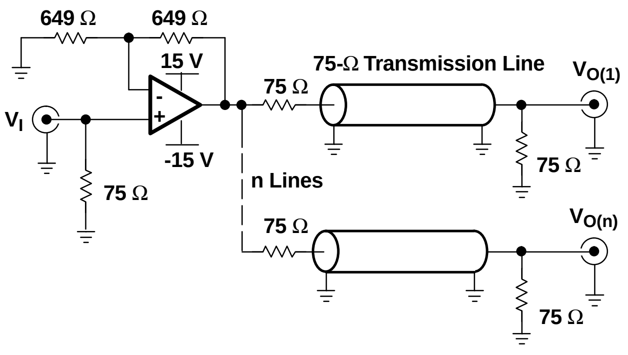


Figure 48. Video Distribution Amplifier Application

Driving Capacitive Loads

Applications, such as FET drivers and line drivers can be highly capacitive and cause stability problems for high-speed amplifiers.

Figure 49 through Figure 55 show recommended methods for driving capacitive loads. The basic idea is to use a resistor or ferrite chip to isolate the phase shift at high frequency caused by the capacitive load from the amplifier's feedback path. See Figure 49 for recommended resistor values versus capacitive load.

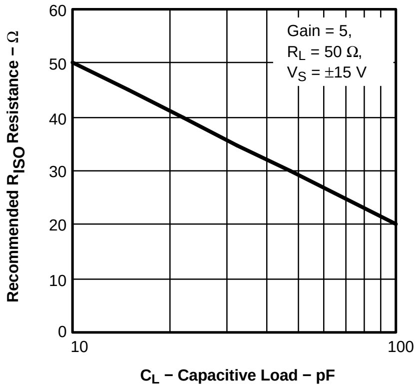


Figure 49. Recommended R_{ISO} vs Capacitive Load

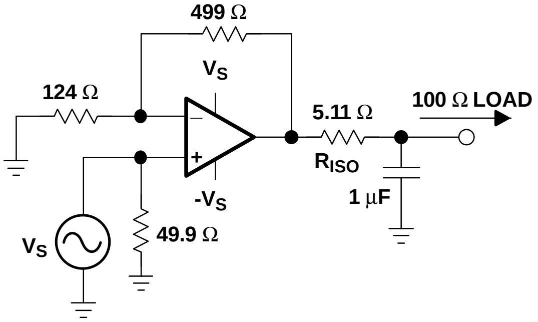


Figure 50.

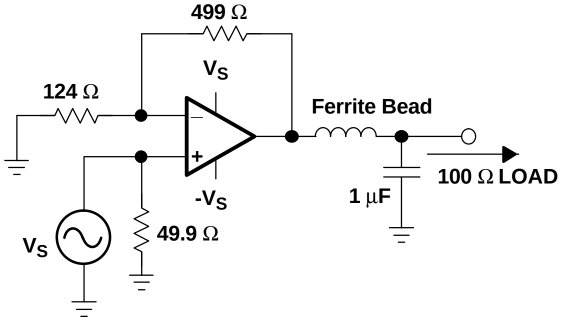


Figure 51.

Placing a small series resistor, R_{ISO}, between the amplifier's output and the capacitive load, as shown in Figure 50, is an easy way of isolating the load capacitance.

Using a ferrite chip in place of R_{ISO}, as shown in Figure 51, is another approach of isolating the output of the amplifier. The ferrite's impedance characteristic versus frequency is useful to maintain the low frequency load independence of the amplifier while isolating the phase shift caused by the capacitance at high frequency. Use a ferrite with similar impedance to R_{ISO}, 20 Ω - 50 Ω, at 100 MHz and low impedance at dc.

Figure 52 shows another method used to maintain the low frequency load independence of the amplifier while isolating the phase shift caused by the capacitance at high frequency. At low frequency, feedback is mainly from the load side of R_{ISO}. At high frequency, the feedback is mainly via the 27-pF capacitor. The resistor R_{IN} in series with the negative input is used to stabilize the amplifier and should be equal to the recommended value of R_F at unity gain. Replacing R_{IN} with a ferrite of similar impedance at about 100 MHz as shown in Figure 53 gives similar results with reduced dc offset and low frequency noise. (See the *ADDITIONAL REFERENCE MATERIAL* section for expanding the usability of current-feedback amplifiers.)

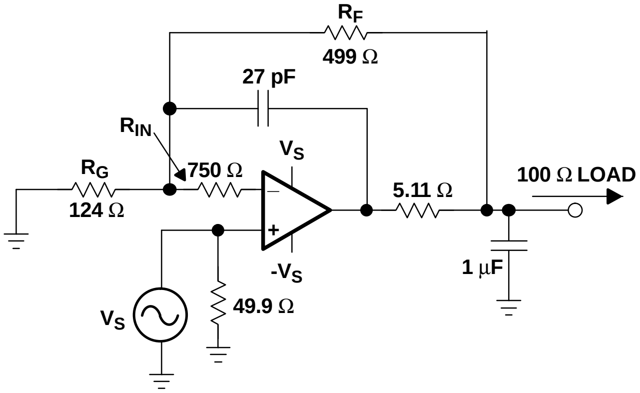


Figure 52.

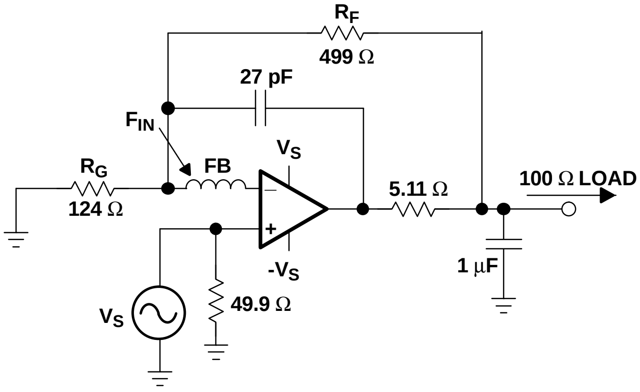


Figure 53.

Figure 54 is shown using two amplifiers in parallel to double the output drive current to larger capacitive loads. This technique is used when more output current is needed to charge and discharge the load faster as when driving large FET transistors.

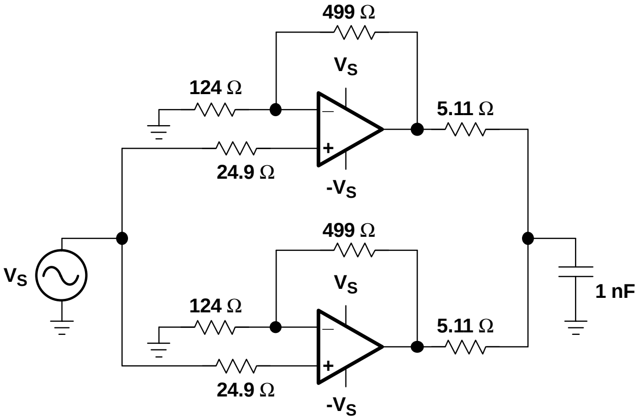


Figure 54.

Figure 55 shows a push-pull FET driver circuit typical of ultrasound applications with isolation resistors to isolate the gate capacitance from the amplifier.

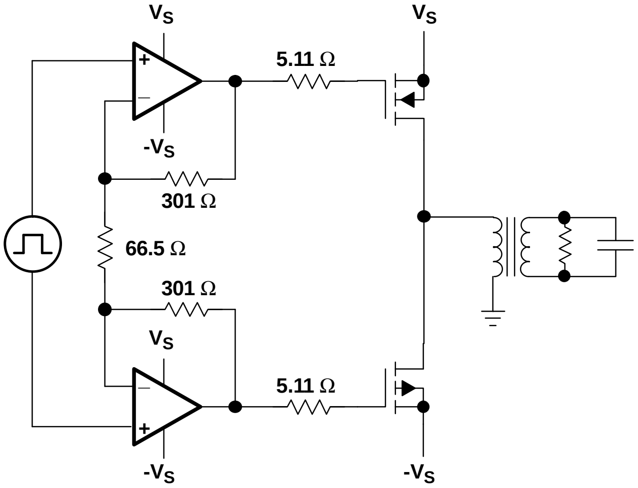


Figure 55. PowerFET Drive Circuit

SAVING POWER WITH POWER-DOWN FUNCTIONALITY AND SETTING THRESHOLD LEVELS WITH THE REFERENCE PIN

The THS3120 features a power-down pin (PD) which lowers the quiescent current from 7 mA down to 300 µA, ideal for reducing system power.

The power-down pin of the amplifier defaults to the negative supply voltage in the absence of an applied voltage, putting the amplifier in the power-on mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be driven towards the positive rail. The threshold voltages for power-on and power-down are relative to the supply rails and are given in the specification tables. Below the *Enable Threshold Voltage*, the device is on. Above the *Disable Threshold Voltage*, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high-impedance output. In other words, the power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

Figure 56 shows the total system output impedance which includes the amplifier output impedance in parallel with the feedback plus gain resistors, which cumulate to 1298 Ω. Figure 45 shows this circuit configuration for reference.

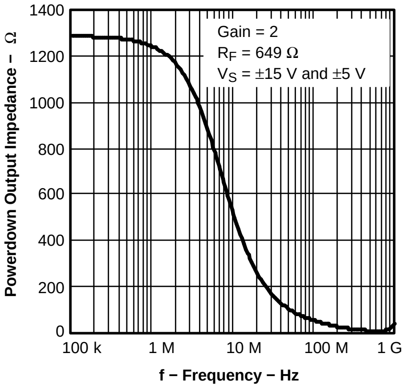


Figure 56. Power-down Output Impedance vs Frequency

As with most current feedback amplifiers, the internal architecture places some limitations on the system when in power-down mode. Most notably is the fact that the amplifier actually turns *ON* if there is a ±0.7 V or greater difference between the two input nodes (V+ and V-) of the amplifier. If this difference exceeds ±0.7 V, the output of the amplifier creates an output voltage equal to approximately [(V+ - V-) -0.7 V]×Gain. This also implies that if a voltage is applied to the output while in power-down mode, the V- node voltage is equal to $V_{O(applied)} \times R_G/(R_F + R_G)$. For low gain configurations and a large applied voltage at the output, the amplifier may actually turn *ON* due to the aforementioned behavior.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach either 10% or 90% of the final output voltage. The time delays are in the order of microseconds because the amplifier moves in and out of the linear mode of operation in these transitions.

POWER-DOWN REFERENCE PIN OPERATION

In addition to the power-down pin, the THS3120 also features a reference pin (REF) which allows the user to control the enable or disable power-down voltage levels applied to the PD pin. In most split-supply applications, the reference pin is connected to ground. In either case, the user needs to be aware of voltage level thresholds that apply to the power-down pin. The usable range at the REF pin is from V_{S-} to (V_{S+} - 4 V).

PRINTED-CIRCUIT BOARD LAYOUT TECHNIQUES FOR OPTIMAL PERFORMANCE

Achieving optimum performance with high frequency amplifiers, like the THS3120 and THS3121, requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance (< 0.25”) from the power supply pins to high frequency 0.1-µF and 100-pF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (6.8 µF or more) tantalum decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.
- Careful selection and placement of external components preserve the high frequency performance of the THS3120 and THS3121. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep their leads and PC board trace length as short as possible. Never use wirebound type resistors in a high frequency application. Since the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2.0 kΩ, this parasitic capacitance can add a pole and/or a zero that can effect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations.

- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (< 4 pF) may not need an R_S since the THS3120 and THS3121 are nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an RS are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS3120 / THS3121 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.
- Socketing a high speed part like the THS3120 and THS3121 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS3120 / THS3121 parts directly onto the board.

PowerPAD™ DESIGN CONSIDERATIONS

The THS3120 and THS3121 are available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 57(a) and Figure 57(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 57(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad. Note that devices such as the THS312x have no electrical connection between the PowerPAD and the die.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

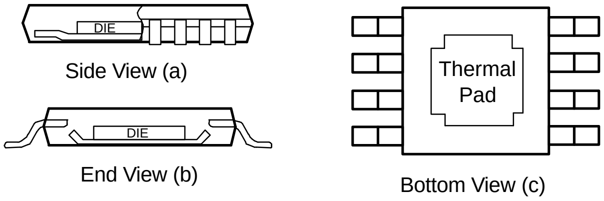


Figure 57. Views of Thermal Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

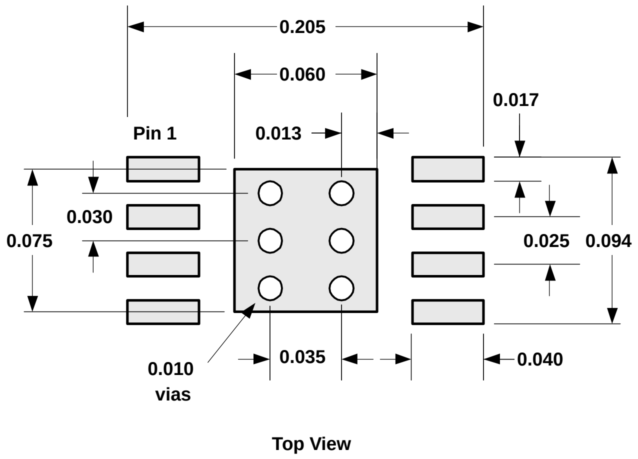


Figure 58. DGN PowerPAD PCB Etch and Via Pattern

PowerPAD™ LAYOUT CONSIDERATIONS

1. PCB with a top side etch pattern as shown in Figure 58. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 10 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS3120 / THS3121 IC. These additional vias may be larger than the 10-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane. Note that the PowerPAD is electrically isolated from the silicon and all leads. Connecting the PowerPAD to any potential voltage such as V_{S-}, is acceptable as there is no electrical connection to the silicon.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS3120 / THS3121 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The THS3120 and THS3121 incorporates automatic thermal shutoff protection. This protection circuitry shuts down the amplifier if the junction temperature exceeds approximately 160°C. When the junction temperature reduces to approximately 140°C, the amplifier turns on again. But, for maximum performance and reliability, the designer must take care to ensure that the design does not exeed a junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade and long term reliability suffers. The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where:

P_{Dmax} is the maximum power dissipation in the amplifier (W).

T_{max} is the absolute maximum junction temperature (°C).

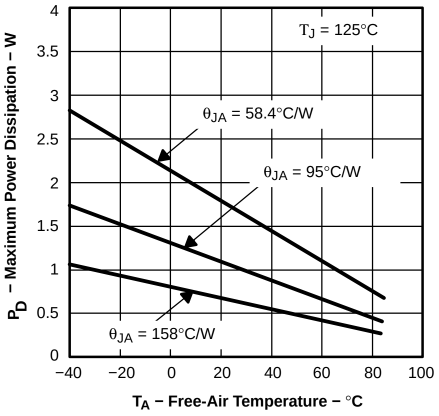
T_A is the ambient temperature (°C).

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} is the thermal coeffiecient from the silicon junctions to the case (°C/W).

θ_{CA} is the thermal coeffiecient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the THS3120 and THS3121 are offered in an 8-pin MSOP with PowerPAD package offering even better thermal performance. The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the available packages. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application note (literature number SLMA002). The following graph also illustrates the effect of not soldering the PowerPAD to a PCB. The thermal impedance increases substantially which may cause serious heat and performance issues. Be sure to always solder the PowerPAD to the PCB for optimum performance.



Results are With No Air Flow and PCB Size = 3"x 3"
θJ_A = 58.4°C/W for 8-Pin MSOP w/PowerPad (DGN)
θJ_A = 95°C/W for 8-Pin SOIC High−K Test PCB (D)
θJ_A = 158°C/W for 8-Pin MSOP w/PowerPad w/o Solder

Figure 59. Maximum Power Distribution vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to not only consider quiescent power dissipation, but also dynamic power dissipation. Often times, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DESIGN TOOLS

Evaluation Fixtures, Spice Models, and Application Support

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal an evaluation board has been developed for the THS3120 and THS3121 operational amplifier. The board is easy to use, allowing for straightforward evaluation of the device. The evaluation board can be ordered through the Texas Instruments web site, www.ti.com, or through your local Texas Instruments sales representative.

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF-amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS3121 is available through the Texas Instruments web site (www.ti.com). The PIC is also available for design assistance and detailed product information. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

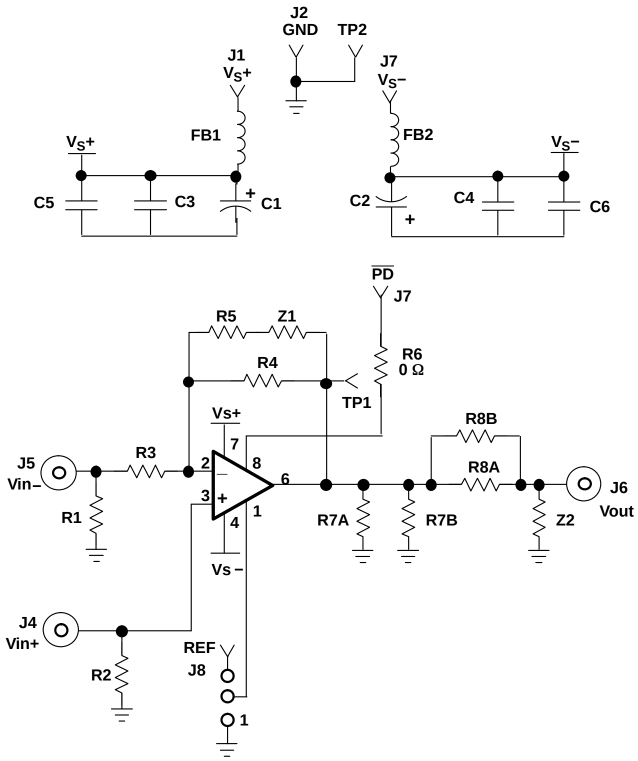


Figure 60. THS3120 EVM Circuit Configuration

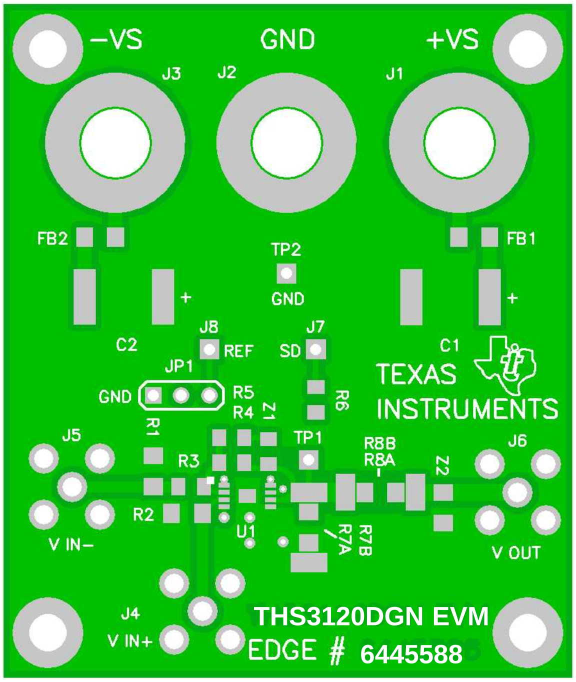


Figure 61. THS3120 EVM Board Layout (Top Layer)

NOTE: The Edge number for the THS3121 is 6445589.

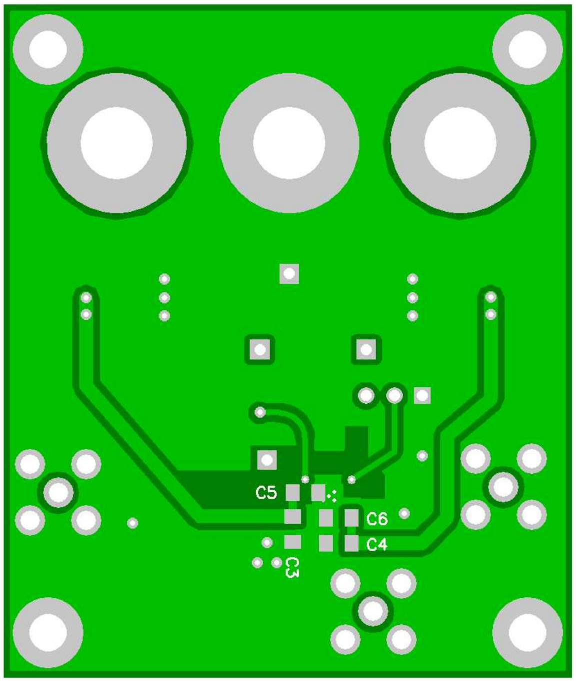


Figure 62. THS3120 EVM Board Layout (Bottom Layer)

Table 2. Bill of Materials

THS3120DGN and THS3121DGN EVM					
ITEM	**DESCRIPTION**	**SMD SIZE**	**REFERENCE DESIGNATOR**	**PCB QUANTITY**	**MANUFACTURER'S PART NUMBER**[1]
1	BeadD, Ferrite, 3 A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00
2	Cap. 6.8 µF, Tanatalum, 35 V, 10%	D	C1, C2	2	(AVX) TAJD685K035R
3	Open	0805	R5, Z1	2	
4	Cap. 0.1 µF, Ceramic, X7R, 50 V	0805	C3, C4	2	(AVX) 08055C104KAT2A
5	Cap. 100 pF, Ceramic, NPO, 100 V	0805	C5, C6	2	(AVX) 08051A101JAT2A
6	Resistor, 0 Ω, 1/8 W, 1%	0805	R6[2]	1	(Phycomp) 9C08052A0R00JLHFT
7	Resistor, 124 Ω, 1/8 W, 1%	0805	R3	1	(Phycomp) 9C08052A1240FKHFT
8	Resistor, 499 Ω, 1/8 W, 1%	0806	R4	1	(Phycomp) 9C08052A4990FKHFT
9	Open	1206	R7A, Z2	2	
10	Resistor, 49.9 Ω, 1/4 W, 1%	1206	R2, R8A	2	(Phycomp) 9C12063A49R9FKRFT
11	Resistor, 0 Ω, 1/4 W, 1%	1206	R1	1	(Phycomp) 9C12063A53R6FKRFT
12	Open	2512	R7B, R8B	2	
13	Header, 0.1" CTRS, 0.025" SQ pins	3 Pos.	JP1[2]	1	(Sullins) PZC36SAAN
14	Shunts		JP1[2]	1	(Sullins) SSC02SYAN
15	Jack, banana receptance, 0.25" dia. hole		J1, J2, J3	3	(SPC) 813
16	Test point, red		J7[2], J8[2], TP1	3	(Keystone) 5000
17	Test point, black		TP2	1	(Keystone) 5001
18	Connector, SMA PCB jack		J4, J5, J6	3	(Amphenol) 901-144-8RFX
19	Standoff, 4-40 hex, 0.625" length			4	(Keystone) 1808
20	Screw, Phillips, 4-40, 0.250"			4	SHR-0440-016-SN
21	IC, THS3120		U1[2]	1	(TI) THS3120DGN
22	Board, printed-circuit (THS3120)		[2]	1	(TI) EDGE # 6445588
23	IC, THS3121		U1	1	(TI) THS3121DGN
24	Board, printed-circuit (THS3121)			1	(TI) EDGE # 6445589

(1) The manufacturer's part numbers were used for test purposes only.
(2) Applies to the THS3120DGN EVM only.

ADDITIONAL REFERENCE MATERIAL

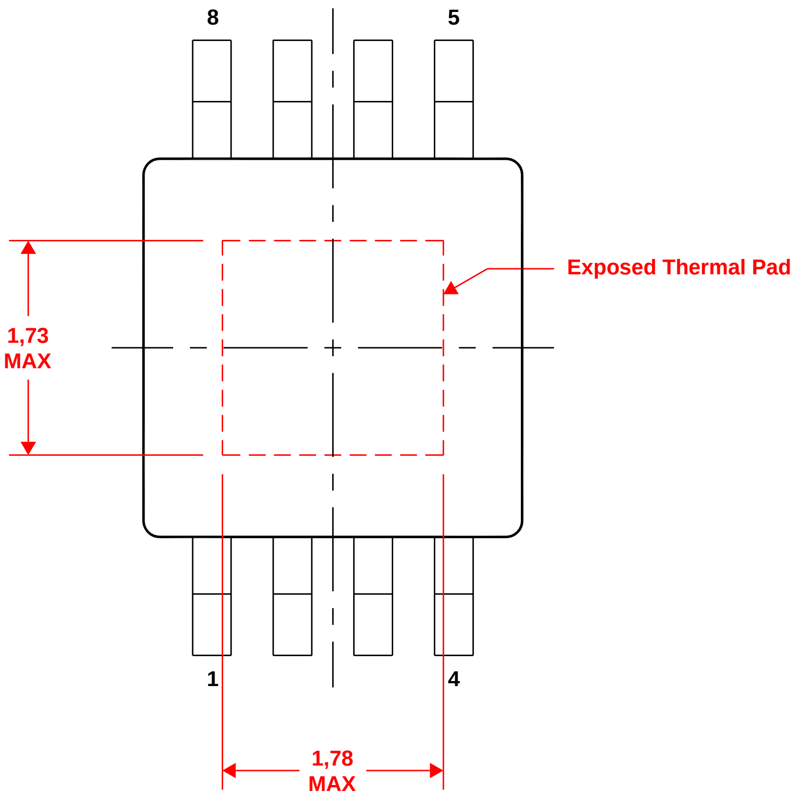
- PowerPAD Made Easy, application brief (SLMA004)
- PowerPAD Thermally Enhanced Package, technical brief (SLMA002)
- Voltage Feedback vs Current Feedback Amplifiers, (SLVA051)
- Current Feedback Analysis and Compensation (SLOA021)
- Current Feedback Amplifiers: Review, Stability, and Application (SBOA081)
- Effect of Parasitic Capacitance in Op Amp Circuits (SLOA013)
- Expanding the Usability of Current-Feedback Amplifiers, by Randy Stephens, 3Q 2003 Analog Applications Journal www.ti.com/sc/analogapps).

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

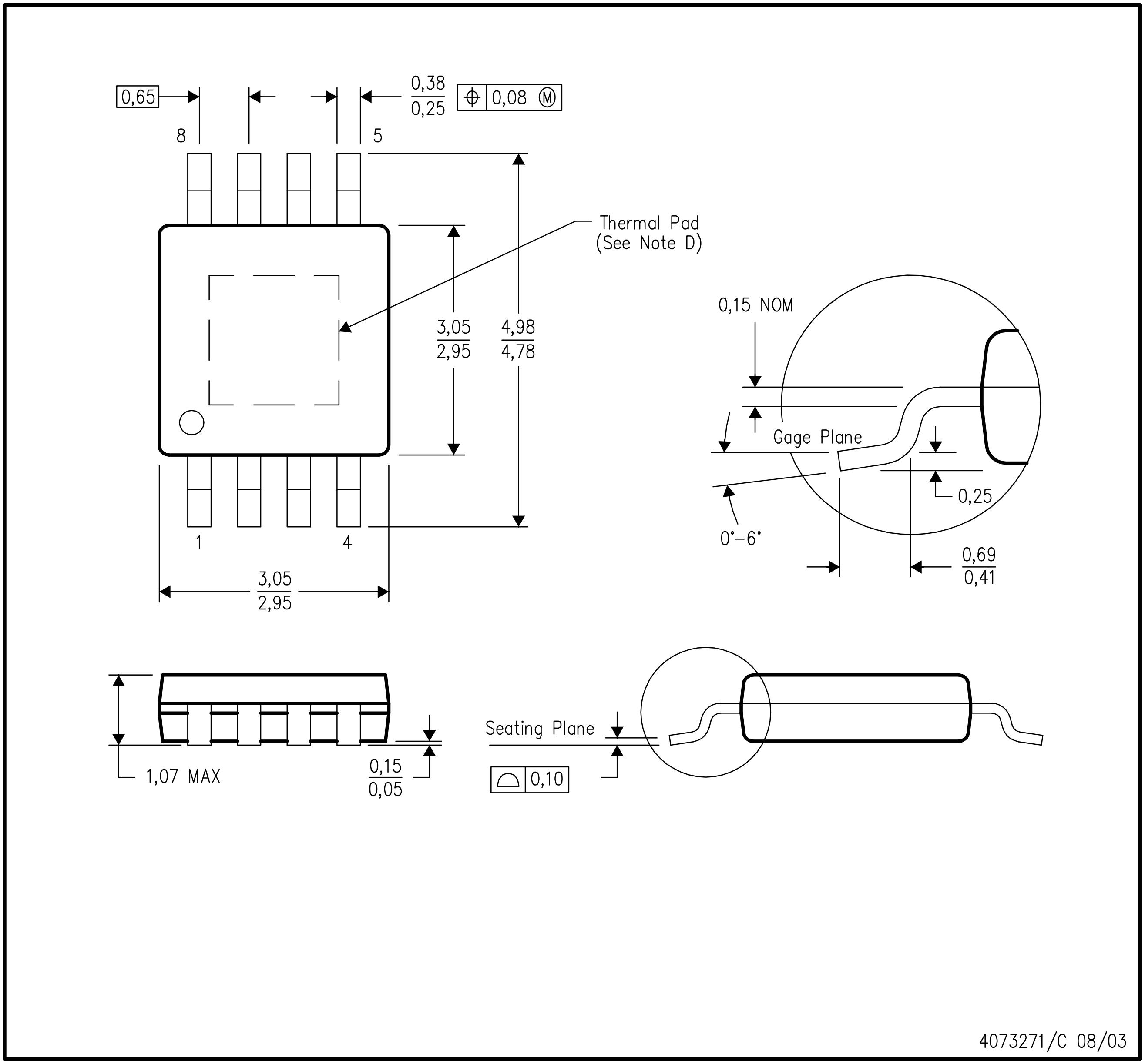
NOTE: All linear dimensions are in millimeters

PPTD041

Exposed Thermal Pad Dimensions

PowerPAD is a trademark of Texas Instruments

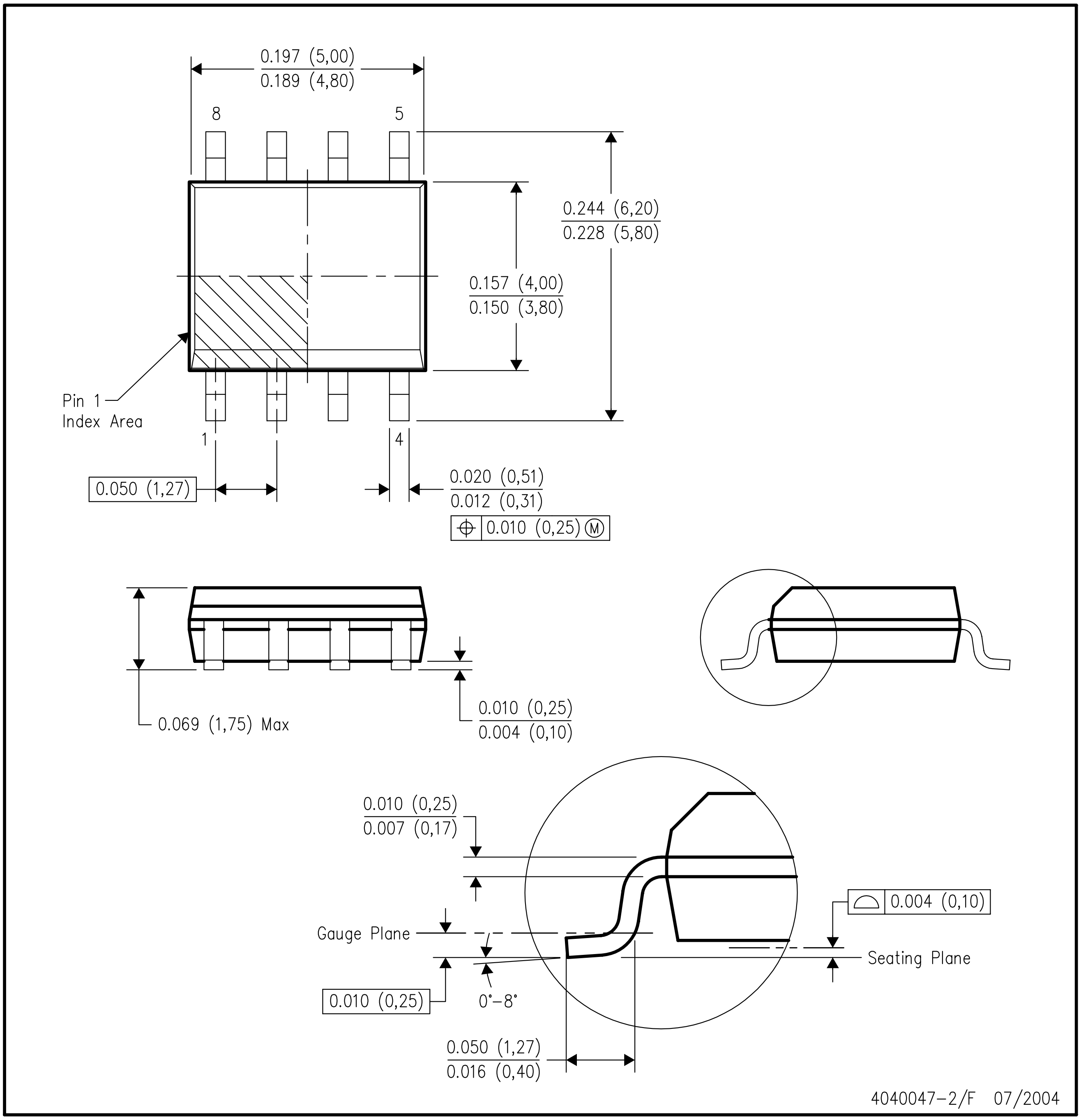
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. Falls within JEDEC MO-187

PowerPAD is a trademark of Texas Instruments.

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AA.

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