TL7726
Hex Clamping Circuit

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Contents

List of Illustrations

Introduction

This application report describes both the parasitic effects present in integrated circuits (ICs) and the problems that can result when protecting precision analog components with conventional methods. Specifically illustrated are how these problems can be overcome by using the TL7726 hex clamping circuit.

All semiconductor ICs, regardless of function and manufacturer, are vulnerable to voltages and currents exceeding the absolute maximum ratings. Although semiconductor manufacturers often build in protection features such as electrostatic-discharge (ESD) protection, voltage clamping, and current limitation, the devices may fail if operated outside the manufacturer's absolute maximum ratings.

Main failure mechanisms result from overvoltage stress of the semiconductor material. CMOS devices are particularly vulnerable in this regard, even at low-voltage levels, due to inherent parasitic structures. The best understood parasitic effect is latch-up, which is caused by parasitic thyristor action caused by overvoltage stress. If sufficient current is injected into either the input or output pins of the device, the thyristor triggers and a short circuit results between the supply rails (latch-up). This usually results in catastrophic device failure.

Through careful semiconductor design and by using the device within the manufacturers' absolute maximum voltage ratings, the effects of overvoltage stress can be greatly reduced. For precision analog circuits, this externally applied voltage level should be tightly controlled; the voltage should be no more than 0.3 V above the positive supply or 0.3 V below ground. Since it is difficult to predict if an applied voltage falls within these limits, external clamping circuits in the form of silicon diodes are often employed.

Zener diodes seem to be an obvious choice for this function. Unfortunately, due to poor voltage tolerance and asymmetrical clamping, the protected circuitry may not only be inadequately clamped but may suffer from reduced performance. For example, the dynamic range of an analog-to-digital converter may be reduced.

The preferred use of Schottky diodes proves similarly inadequate. The forward voltage of a Schottky diode is 400 mV. While this can protect the device for the majority of fault conditions, it still allows voltage levels in excess of the manufacturers' absolute maximum levels to be developed across the device. In effect, the device is being operated outside the recommended conditions and its continued function may be impaired.

Parasitic Transistors in Complementary MOS Circuits

The normal operating effects of the parasitic transistors inherent when making complementary MOS (CMOS) components is not particularly critical; however, the resultant structures shown in Figure 1 allow a clear explanation of parasitic effects when operation is not restricted to normal ranges.

The manufacturing process of high-speed digital CMOS circuits begins with an N-doped substrate (see Figure 1) into which a P-doped well is diffused followed by N-doped regions for the drains and sources of the N-channel transistors; the well itself is connected via a P-doped contact to the substrate (GND). P-doped zones in the N-doped substrate provide the drains and sources of the P-channel transistors.

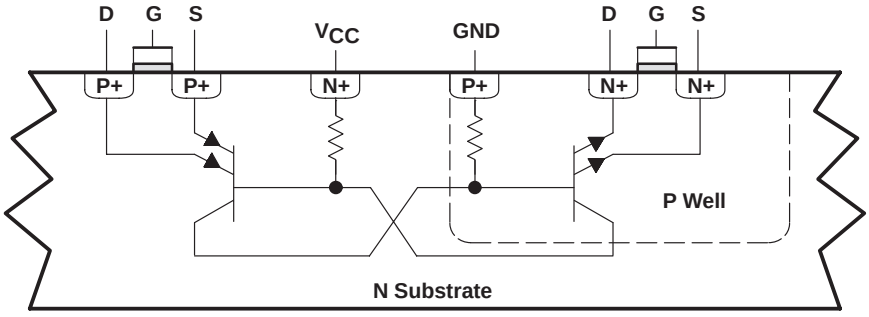

Figure 1. Parasitic Bipolar Transistors in CMOS Circuits

Latch-Up

The substrate itself is connected to the positive supply voltage (V_{CC}) via an N-doped contact. This produces both parasitic npn and pnp transistors; together these make up a pnpn structure of a thyristor (see Figure 2). The anode of this parasitic thyristor is connected to the positive supply and the cathode to GND; all other connections to this element (inputs and outputs) are gates of the thyristor. If a large enough current is injected into the input or output of this element, the thyristor is triggered. This effect is known as latch-up, and the resulting short circuit between the supply rails usually causes destruction of the component.

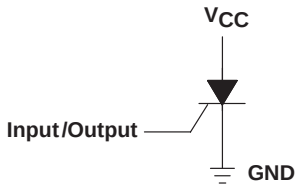

Figure 2. Structure of Parasitic Thyristor

Guard Rings

Latch-up effects have been reduced by incorporating additional guard rings in the structure. Guard rings are circular N- or P-doped zones surrounding the endangered elements, the N zones being connected to the positive supply rail and the P zones to the most negative supply rail (usually the substrate supply rails). These guard rings (see Figure 3) provide additional collectors for the parasitic transistors, which collect most of the current circulating in the substrate and divert it to the supply voltage rails; to a large extent, these eliminate the danger of latch-up. With modern logic circuits, such as high-speed CMOS, guard rings prevent latch-up from occurring until at least 300 mA is injected into an input or output at an operating temperature of 125°C. Since the gain of the parasitic transistors decreases at lower temperatures, the sensitivity of the thyristors at lower temperatures is reduced. At normal temperatures with careful device design, currents of over 1 A are necessary to provoke latch-up.

Linear CMOS (analog process) ICs are tested for susceptibility to latch-up by injecting a current pulse with an amplitude of 100 mA at an ambient temperature of 25°C into the inputs and outputs. This current is chosen to simulate a practical overload condition, while eliminating any risk of damage. The protective elements of ICs are in fact designed to withstand, without risk of damage, a continuous current of 5 mA in the clamping diodes.

The danger of component destruction as a result of latch-up due to parasitic transistors can therefore be reduced with careful chip design but does not entirely eliminate them; this is particularly evident with high-impedance (high-sensitivity) circuits.

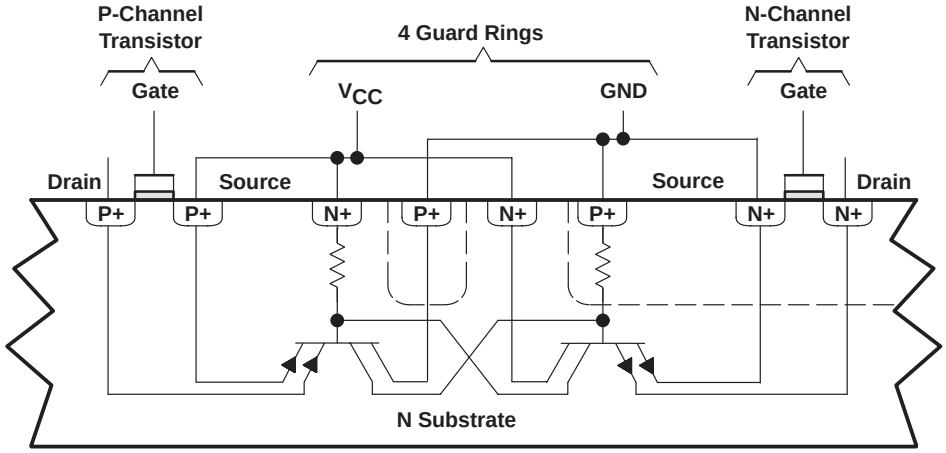

Figure 3. Guard Rings in CMOS Circuits

CMOS Internal-Input-Protection Circuitry

Use CMOS-input diode-protection circuitry, as shown in Figure 4, and assume the input is derived from the voltage source V1 = 24 V. The supply voltage (V_{CC}) is 5 V. A series resistor (R1 = 100 kΩ) ensures that the current in the internal clamping diode (D1) is limited to an acceptable value. A potential problem can occur if a neighboring input is connected similarly and is then controlled by the voltage source V2 = 0 V. In this case, a pnp transistor is created between the two clamping diodes D1 and D2. As a result, part of the current flowing through D1 (emitter) is diverted to D2 (collector); the N-doped substrate, which is connected to the supply voltage, then functions as the base of a parasitic transistor. Even when the gain of this transistor is comparatively low (0.01–0.1), the current through the R2 resistor creates a voltage drop that distorts the signal at the input and causes malfunction.

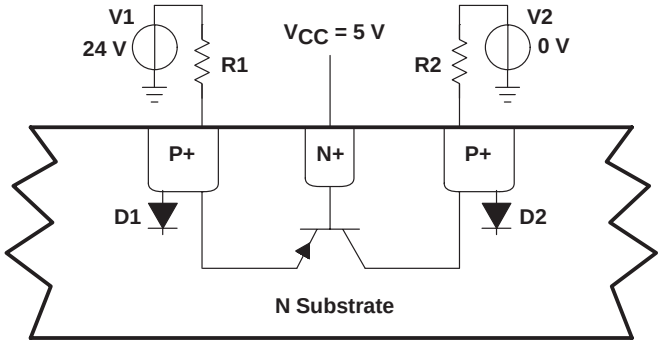

Figure 4. Parasitic Transistors in Input-Protection Circuits

This effect can be reduced through the use of additional guard rings (see Figure 3) but not entirely eliminated. Absolute maximum input voltages are given in data sheets, and if these limits are observed, parasitic effects will be insignificant. With digital CMOS circuits, it is permissible for the input voltage to be up to 0.5 V more positive than V_{CC} or 0.5 V more negative than the substrate without danger of malfunction. With analog circuits that operate at currents several orders of magnitude lower, voltage must be more tightly controlled; the input voltage should not be allowed to be more than 0.3 V above or below the supply voltage.

Silicon integrated protection or clamping diodes have a typical forward voltage (V_f) of 0.7 V at room temperature. The input voltage delta is 0.3 V, since the negative temperature coefficient of the forward voltage (≈ –2 mV/°C) must be taken into account. As mentioned before, sensitive circuits can malfunction with currents of only a few microamps, at which the forward voltage of a silicon diode at room temperature may be significantly below 0.7 V.

If under any conditions input voltages could exceed these maximum values, then additional precautions are necessary; these usually take the form of external clamping diodes on the input (see Figure 5).

External Clamping Diodes

Silicon diodes are of only limited use for protection since their forward voltage is close to that of the clamping diodes that are already integrated into an IC; therefore, only a part of the excess current is diverted into the external diodes. This approach is suitable when the circuit needs to be protected only from destruction. Because of their smaller geometry, the integrated clamping diodes have a higher forward resistance so a majority of the current is diverted to the external diodes. As protection against malfunction, conventional silicon diodes are not totally effective.

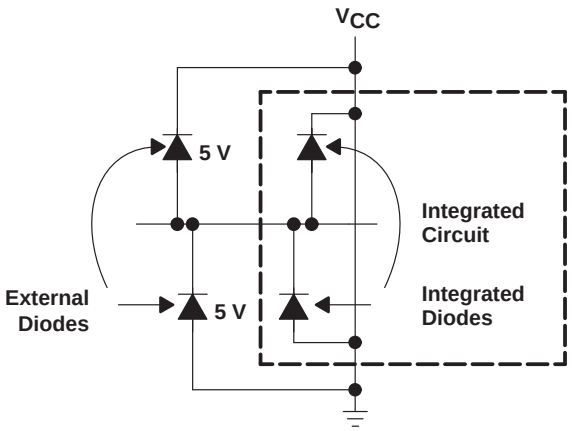

Figure 5. Protection Circuit With External Clamping Diodes

Better results can be expected with the use of germanium or Schottky diodes. These have significantly lower forward voltages (germanium: $V_f = 0.3$ V, Schottky: $V_f = 0.4$ V). Germanium diodes are seldom used at the present time, have high-leakage characteristics, and can be hard to obtain. If either diode has excessively high forward resistance, they are ineffective anyway.

TL7726 Hex Clamping Circuit

In order to prevent the activation of parasitic transistors, clamping diodes with exceptionally low forward voltages are necessary, and these can only be realized with an active circuit, as shown in Figure 6.

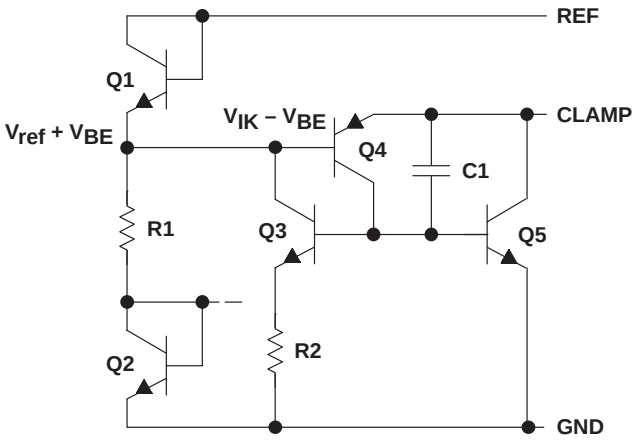

Figure 6. Simplified Circuit of the TL7726

Due to the effects described previously, neither diodes or conventional components are a panacea for protection, particularly for the demanding requirements of analog applications. For this reason, Texas Instruments has developed a dedicated IC that fully meets such requirements, the TL7726 hex clamping circuit. Figure 7 compares the current and voltage characteristics for a range of silicon diodes and a typical TL7726.

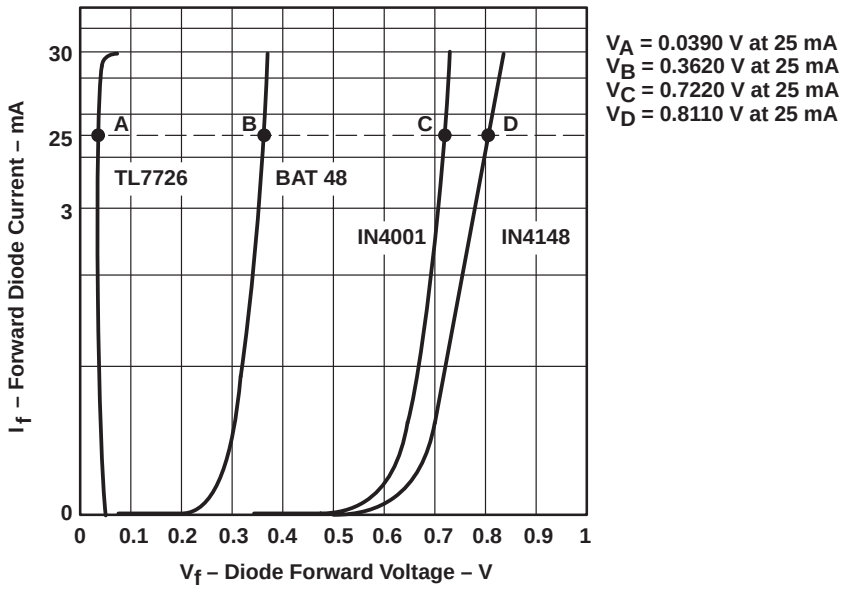

Figure 7. Current and Voltage Characteristics for Various Devices

Device Description

The TL7726 is comprised of six identical active voltage clamping circuits that have been specifically designed to protect vulnerable analog inputs from overvoltage stress. Under fault conditions, the TL7726 provides a forward-voltage drop of only 200 mV at 20 mA. Furthermore, the device provides symmetrical protection to both positive- and negative-going transient voltages (effectively replacing up to twelve diodes).

Under normal operation, the TL7726 offers a very high input impedance to ground and draws less than 10 μA; however, under fault conditions, a low-impedance path is offered to clamp the protected node at a voltage between V_{ref} to V_{ref} + 200 mV and between GND to GND −200 mV. This clamping operation is specified over the full operating temperature range.

The TL7726 is available in an 8-pin DIP (P package) or an 8-pin SOIC (D package). The TL7726C is characterized for operation from 0°C to 70°C. The TL7726I is characterized for operation from −40°C to 85°C. The TL7726Q is characterized for operation from −40°C to 125°C.

Circuit Operation

As shown in Figure 6, an internal reference voltage is generated across transistor Q1. This reference connected as a diode is a diode forward-voltage drop more negative than the external connection REF. The current through Q1, which is determined by the resistor R1, is only a few microamps; therefore, the supply rail of the circuit to be protected (usually connected to REF) is only very slightly loaded, allowing the TL7726 to be used with battery-powered equipment. The transistor Q2 generates a reference voltage with a circuit complementary to Q1 that limits voltages more negative than GND.

The voltage to be limited is connected to CLAMP. If the voltage at this input becomes more positive than the internal reference voltage at the emitter of Q1 plus the forward voltage of the base-emitter diode of Q4, a collector current flows in Q4. This current comes in part from the base of Q3, whose collector current further increases the base current of Q4. This feedback ensures that the base current of Q5 and the collector current increase simultaneously. This circuit approach ensures that a current of only a few microamps flows in REF as long as the clamp voltage, V_{IK}, is the same as or smaller than the reference voltage, V_{ref}. A small increase of the voltage at CLAMP causes the current to increase very rapidly (see Figures 8 and 9). The circuit behaves like an external low-resistance Zener diode whose breakdown voltage can be set by a reference voltage at REF.

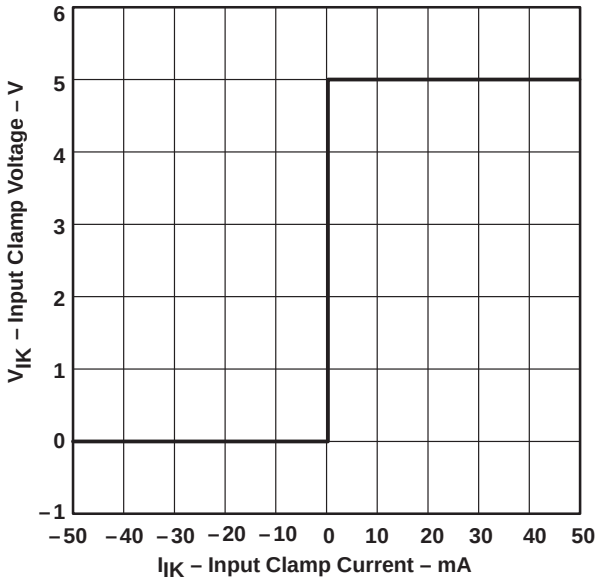

Figure 8. Characteristics of the TL7726 (V_{ref} = 5 V)

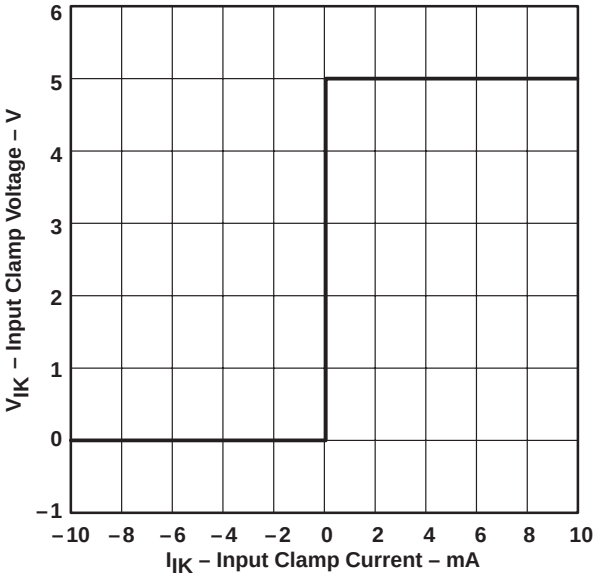

Figure 9. Characteristics of the TL7726 at Low Current (V_{ref} = 5 V)

A complementary circuit has the effect that if the input sees a voltage that is more negative than GND, the resulting current (flowing outward) also increases very rapidly. In this voltage range, the circuit behaves like a very low resistance diode having a forward voltage of only some tenths of a millivolt.

The characteristics of the TL7726 cannot be properly represented using linear axes. Therefore, mixed log/linear axes are used (see Figure 10) so the voltage limits over a very wide range can be shown in detail.

Overvoltages at device pins are often of very short duration but of high amplitude. The hex clamping circuit must be able to provide reliable protection under these conditions, so the device has been designed such that a continuous current of 50 mA is permissible at the clamp input. However, the maximum power dissipation of the package must be taken into account in case such currents flow simultaneously into several inputs.

Extremely rapid operation of the hex clamping circuit has been achieved with the capacitor C1 (see Figure 6), which essentially consists of the collector-base (Miller) capacitance of Q5. This ensures that Q5 is immediately switched on if there are rapid voltage changes. Figure 11 shows that voltage limiting is achieved with virtually no delay. Figure 12 shows the circuit used to make these measurements. Since this circuit reacts to practically any voltage change, it must be noted that several microseconds elapse from a change of amplitude until a new stable value is reached (see Figure 13).

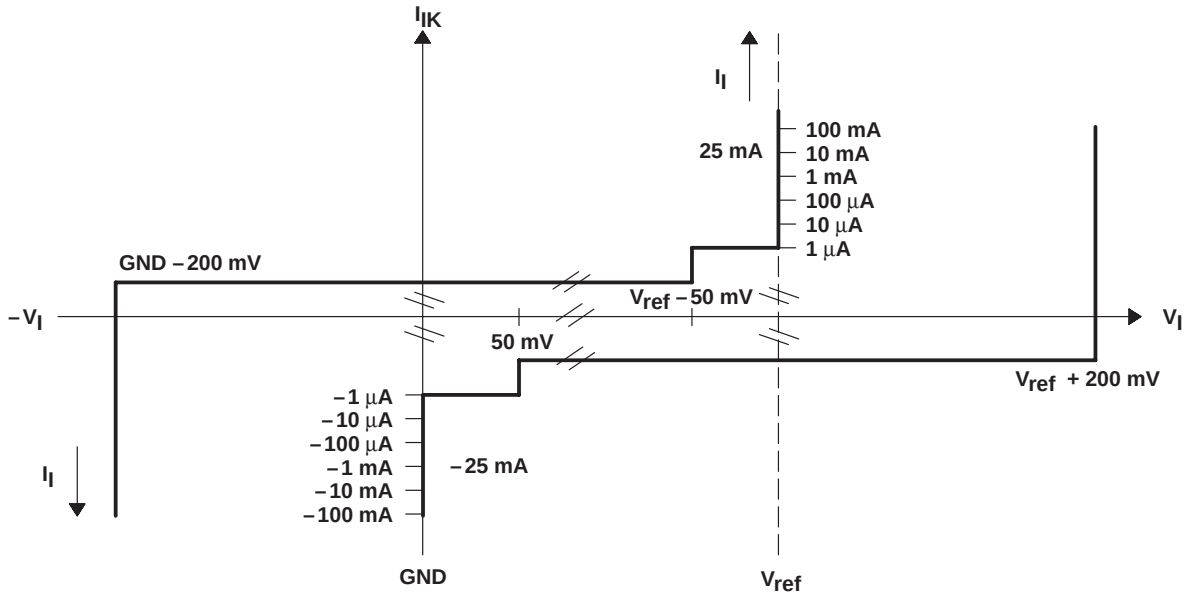

Figure 10. Current and Voltage Limits of TL7726

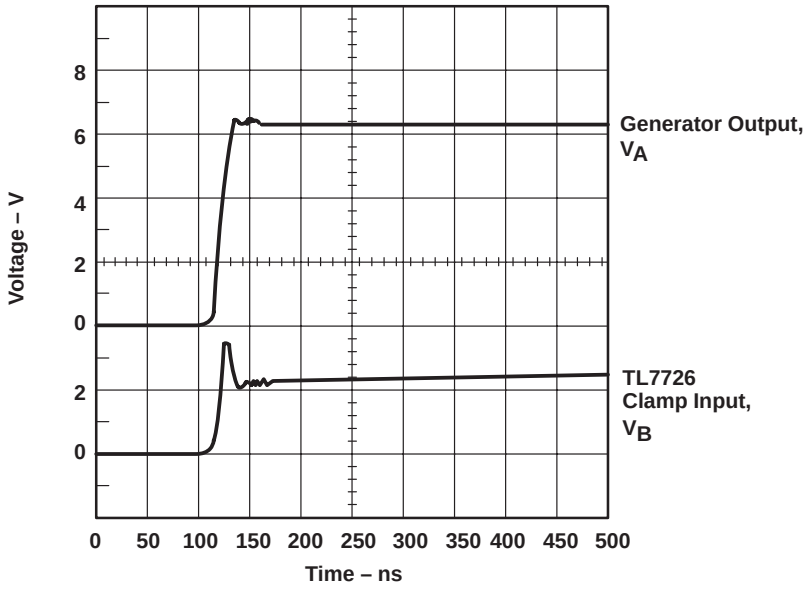

Figure 11. Behavior of TL7726 With Rapid Voltage Changes

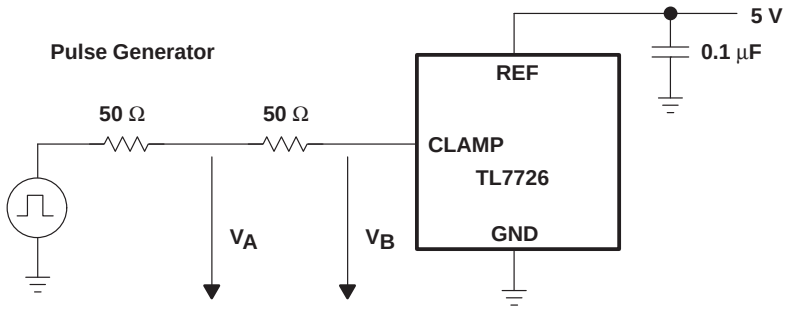

Figure 12. Measurement Circuit

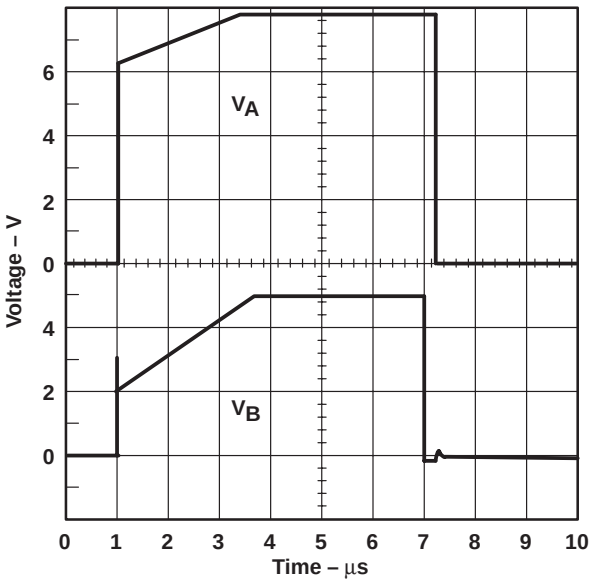

Figure 13. Settling Time at the Input of the Hex Clamping Circuit

Application Examples Using the TL7726

The TL7726 was developed to protect the inputs of linear (analog) ICs against overvoltage and to ensure the reliable operation of these components both in demanding applications and in harsh environments. A typical application of the TL7726 is extremely simple, as shown in Figure 14.

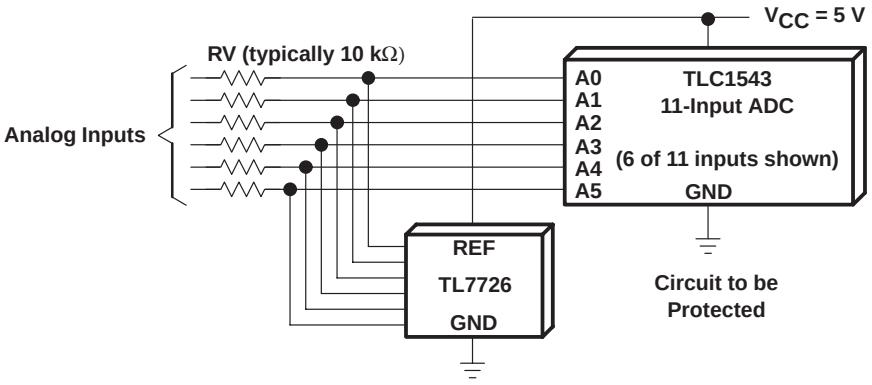

Figure 14. Typical Application of the Hex Clamping-Circuit TL7726

The TL7726 is ideal for protecting the inputs of the TI range of multiple input analog-to-digital converters. The TL7726 can reliably handle currents up to 50 mA. The series current-limit resistor (RV) is chosen to limit the current to this level. The clamp voltage level is set to be within 200 mV of V_{ref} and GND.

The reference voltage pin (REF) of the hex clamping circuit is connected to the supply voltage (V_{CC}) of the circuit to be protected whose inputs are connected to the CLAMP inputs (see Figure 14). The requirement for series resistors depends on the particular application. If the input signal to be limited is supplied by a comparatively high-impedance source, and if only undefined currents must be prevented from flowing into the substrate of the circuit to be protected, such resistors are not needed. However, in most cases, voltages of considerable amplitude can be expected. These are coupled into the signal inputs and cause significant interference. In such cases, the TL7726 should also be protected against damage; this can only be ensured if the current that flows can be limited to an acceptable amount with a series resistor. The TL7726 reliably diverts currents up to ±50 mA where the difference of the voltage between the input voltage (V_{IK}) and the reference voltage (depending on whether current is flowing to REF or GND) is only a few hundred millivolts. The RV series resistor can be chosen over a wide range depending on the requirements of the circuit to be protected. Resistors from a few tens of ohms up to several tens of kilohms (i.e., 20 Ω to 40 kΩ) can be used.

When choosing series resistors used to limit current flowing into the TL7726, consideration should be given to the maximum power dissipation [$P_{D(max)}$] that the TL7726 can withstand. The limiting factors are the maximum permissible device temperature of 150°C and the thermal resistance ($R_{\theta JA}$) between the device and ambient temperature. The following expression applies (see the TL7726 data sheet):

$$P_{D(max)} = \frac{150°C - T_A}{R_{\theta JA}}$$

where:

T_A = ambient temperature
$R_{\theta JA}$ (D package) = 172°C/W
$R_{\theta JA}$ (P package) = 105°C/W

given the following derating factors

Derating factor (D package) = $1/R_{\theta JA}$ = 5.8 mW/°C
Derating factor (P package) = $1/R_{\theta JA}$ = 9.5 mW/°C

Current Flow

Consideration should be given to the path taken by the current that flows into the TL7726. A positive current flowing into a CLAMP terminal is channeled to GND (see Figure 6 and Figure 15); similarly, a negative current flows to REF. Since REF is normally connected to the V_{CC} rail supplying other circuits, this voltage source must be able to withstand the current flow. In most cases, only short duration voltages need to be limited; this usually means that the filter capacitor in the power supply must be of sufficiently large capacitance and the ground return of sufficiently large size to prevent excessive ground bounce.

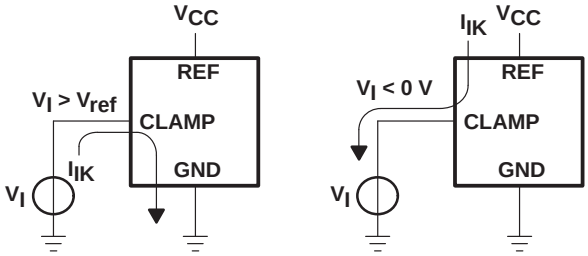

Figure 15. Current Flow Paths

Summary

Until recently, the protection of analog circuits in harsh environments where the inputs could be subjected to undefined overvoltages was only possible with considerable extra circuitry. Although this circuitry gave protection against destruction, it often limited the performance of the protected device. The availability of the TL7726 hex clamping circuit now provides both reliable and transparent protection operation for up to six analog inputs in a single package.