

Specification for BTHQ 128064AVC1-STF-06-LED02YG-COG

Version November 2004

BTHQ 18064AVC1-STF-06-LED02YG-COG incl. UC 1601

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DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2004.11.18	<p>First Release.</p> <p>Based on</p> <p>a.) Test Specification: VL-TS-COG-BTC12864-10 REV A, 2004.11.17</p> <p>b.) VL-QUA-012B REV.W 2004.03.20</p> <p>According to VL-QUA-012B, LCD size is small because Unit Per Laminate=15 which is more than 6pcs/Laminate.</p>	ZHANG YAN FANG	LIN RONG SHOU

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**Specification
of
LCD Module Type
Item No.: COG-BTC12864-10**

1. General Description

- 128 x 64 dots STN Yellow Positive Transflective LCD Graphic Module.
- Viewing Direction: 6 O'clock.
- Driving duty: 1/65 Duty, 1/9 bias.
- "ULTRA CHIP" UC1601 (COG) LCD Controller-Driver or equivalent.
- Logic Power Supply: +3V.
- FPC connection.
- Yellow Green LED02 Backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	67.5(W) x 82.5(H) x 8.5(D)(Include FPC and Backlight)	mm
Viewing area (V.A.)	60.00 MIN.(W) x 40.00 MIN.(H)	mm
Active area (A.A.)	56.945(W) x 37.425(H)	mm
Display format	128 x 64	dots
Dot size	0.43(W) x 0.57(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.445(W) x 0.585(H)	mm
Weight:	TBD	grams

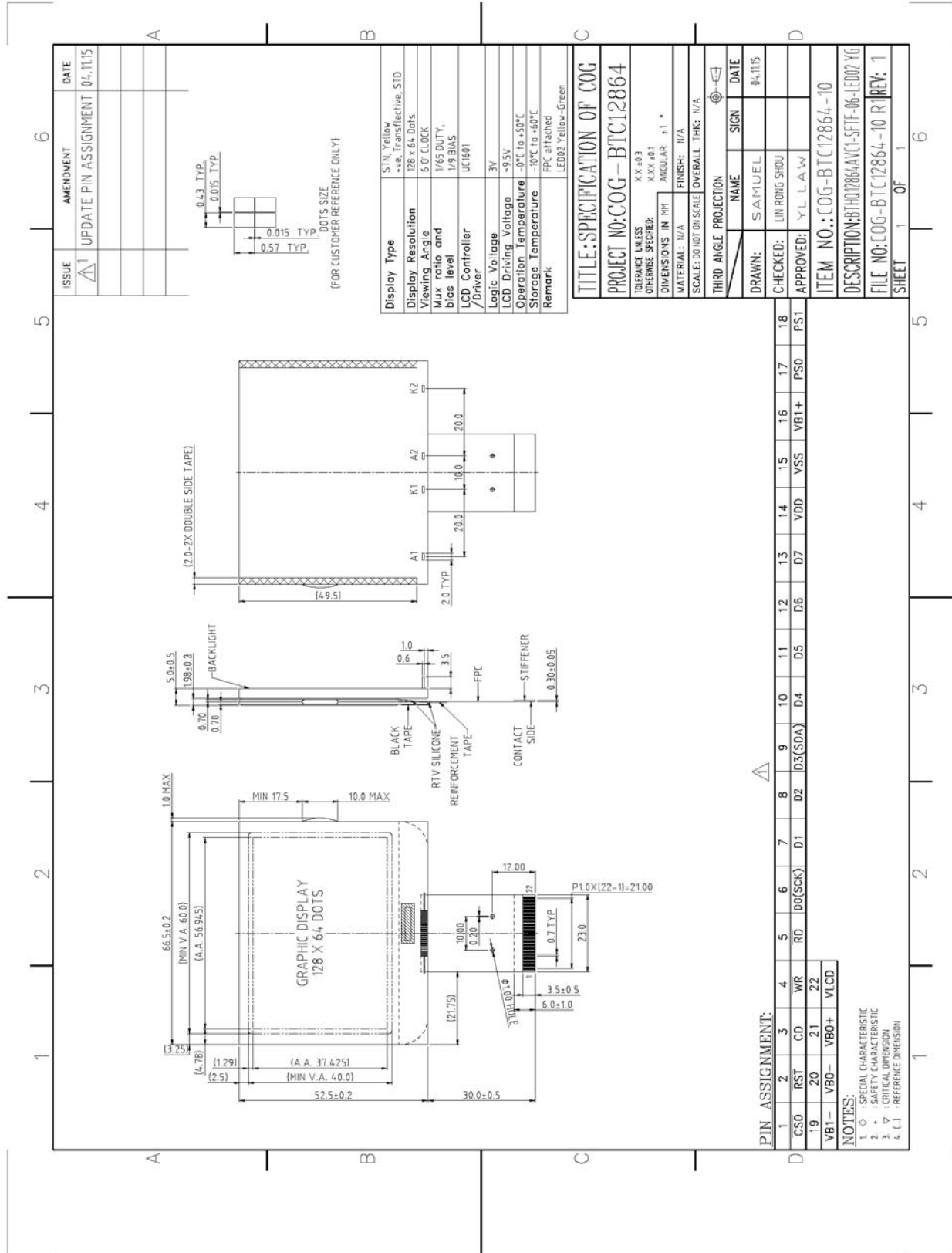


Figure 1: Module Specification

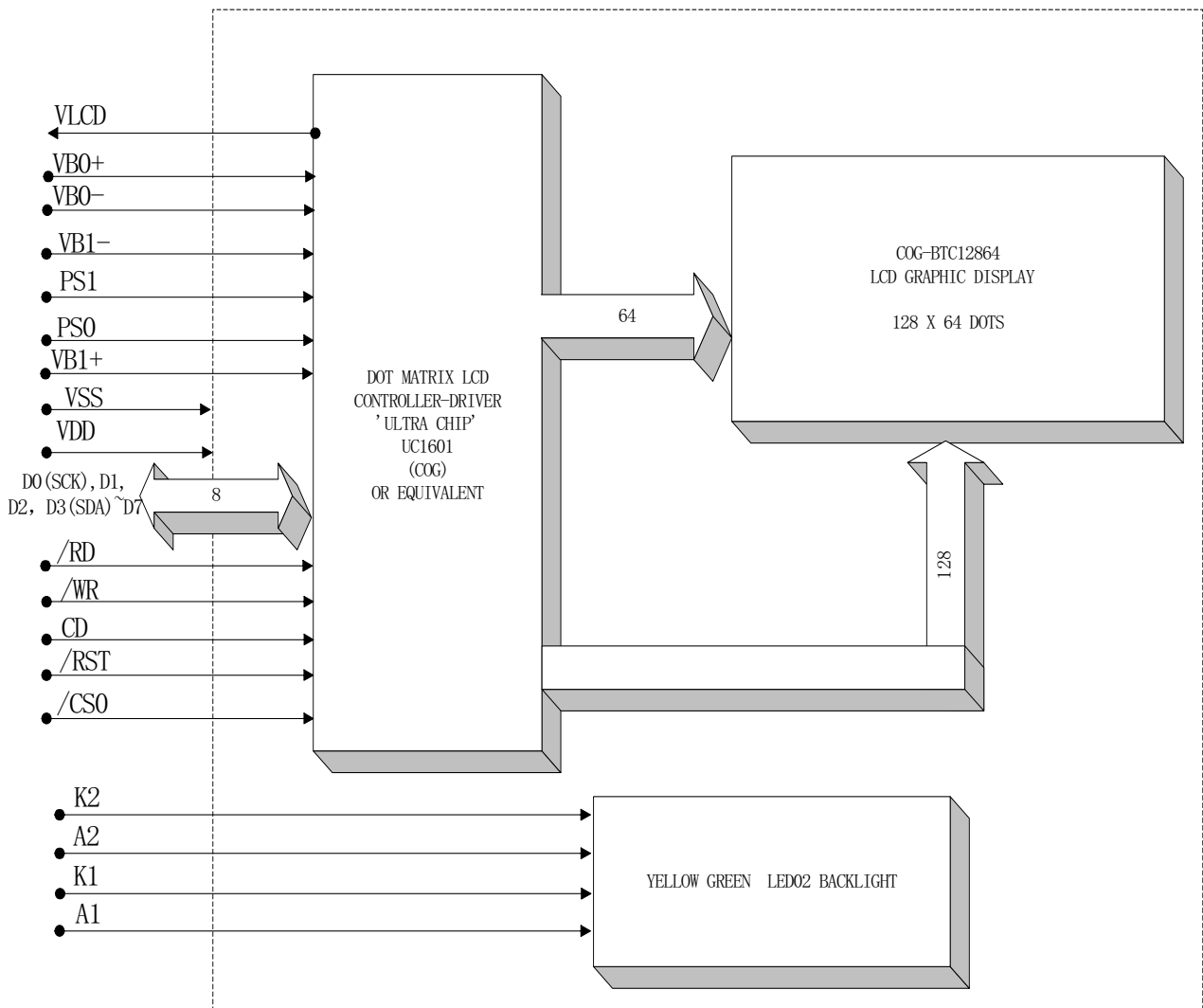


Figure 2: Block diagram

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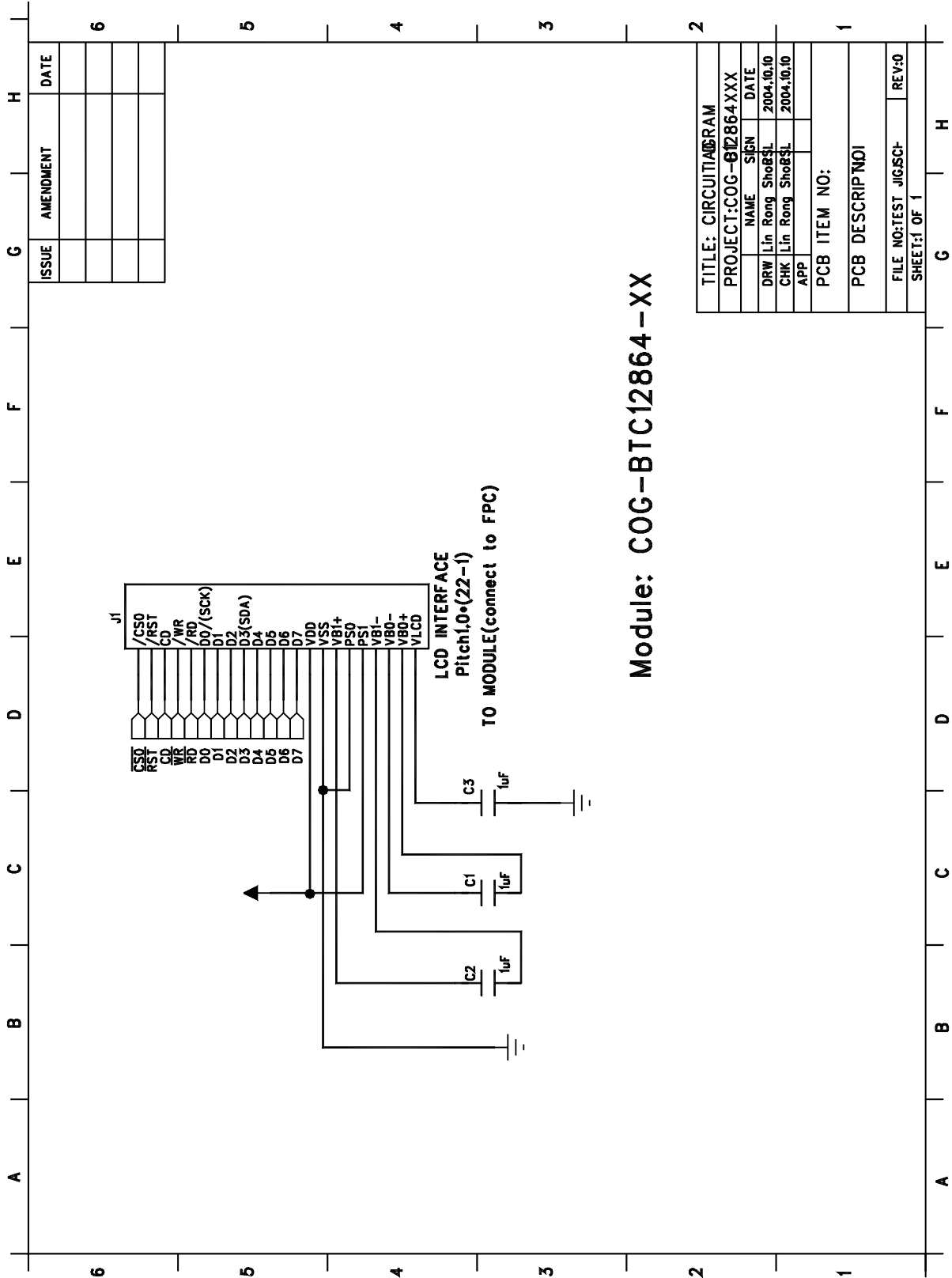


Figure 3: Application Circuit

3. Interface signals

Table 2

Pin No.	Symbol	Description																											
1	$\overline{CS0}$	Chip Select. In parallel mode and S8 mode, chip is selected when $\overline{CS0}$ = "L" and CS1= "H". When the chip is not selected, D[7:0] may be high impedance.																											
2	\overline{RST}	When \overline{RST} = "L", all control registers are re-initialized by their default states. When \overline{RST} is not used, connect the pin to VDD.																											
3	CD	Select Command or Display Data for read/write operation. "L": Command "H": Display data																											
4	\overline{WR}	RD/WR(WR[1:0]) controls the read/write operation of the host interface.																											
5	\overline{RD}	In parallel mode, RD/WR(WR[1:0]) meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used. Connect to VSS.																											
6	D0(SCK)	Bi-directional bus for both serial and parallel host interfaces.																											
7	D1	In S8 and S9 mode, connect unused pins to VDD or VSS.																											
8	D2																												
9	D3(SDA)																												
10	D4																												
11	D5																												
12	D6																												
13	D7																												
		<table border="1"> <thead> <tr> <th></th> <th>PS=1x</th> <th>Ps=0x</th> </tr> </thead> <tbody> <tr> <td>D0</td> <td>D0</td> <td>SCK</td> </tr> <tr> <td>D1</td> <td>D1</td> <td></td> </tr> <tr> <td>D2</td> <td>D2</td> <td></td> </tr> <tr> <td>D3</td> <td>D3</td> <td>SDA</td> </tr> <tr> <td>D4</td> <td>D4</td> <td></td> </tr> <tr> <td>D5</td> <td>D5</td> <td></td> </tr> <tr> <td>D6</td> <td>D6</td> <td></td> </tr> <tr> <td>D7</td> <td>D7</td> <td></td> </tr> </tbody> </table>		PS=1x	Ps=0x	D0	D0	SCK	D1	D1		D2	D2		D3	D3	SDA	D4	D4		D5	D5		D6	D6		D7	D7	
	PS=1x	Ps=0x																											
D0	D0	SCK																											
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D3	D3	SDA																											
D4	D4																												
D5	D5																												
D6	D6																												
D7	D7																												
14	VDD	VDD1 is the digital power supply and it should be connected to a voltage source that is no higher than VDD2&3. VDD2&3 is the analog power supply and it should be connected to the same power source. Minimize the trace resistance for VDD2&3.																											
15	VSS	Ground.																											
17	PS0	PS[1:0] Parallel/Serial.																											
18	PS1	Serial modes: "LL": serial (S8) "LH": serial (S9) Parallel modes: "HL": 8080 "HH": 6800																											
16	VB1+	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of CBX value between VBX+ and VBX-. The resistance of these four traces directly affects the SEG driving strength of the resulting LCD module. Minimize the trace resistance is critical in achieving high quality image.																											
19	VB1-																												
20	VB0-																												
21	VB0+																												
22	VLCD	Main LCD Power Supply. A by-pass capacitor CL is optional. When CL is used, connect CL between VLCD and VSS, and keep the trace resistance under 300 Ohm.																											
-	A	Anode of LED Backlight.																											
-	K	Cathode of LED Backlight.																											

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings – for IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	V_{DD}	-0.3	+3.3	V
LCD generator supply voltage	V_{DD2}	-0.3	+3.3	V
Analog circuit supply voltage	V_{DD3}	-0.3	+3.3	V
Voltage difference between V_{DD} and $V_{DD2/3}$	$V_{DD2/3} - V_{DD}$		1.2	V
LCD generated voltage	V_{LCD}	-0.3	+12	V
Any input/output	V_{IN}/V_{OUT}	-0.4	$V_{DD}+0.3$	V

Note:

1. V_{DD} is based on $V_{SS} = 0V$.
2. Stress values listed above may cause permanent damages to the device.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for $T_a \leq 40^\circ C$ < 95% RH for $T_a > 40^\circ C$				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: $981 \text{ m/s}^2 = 100g$ Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 3V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic & booster)	VDD-VSS		2.85	3.0	3.15	V
LCD driving voltage (Built-in)	VLCD-VSS	At Ta = 0°C, Character mode, VDD = 3V, Note 1	-	9.5	-	V
		At Ta = +25°C, Character mode, VDD = 3V, Note 1	8.9	9.1	9.3	V
		At Ta = +50°C, Character mode, VDD = 3V, Note 1	-	8.6	-	V
Input signal voltage	V _{IH}	“H” level	0.8 VDD1	-	-	V
	V _{IL}	“L” level	-	-	0.2VDD1	V
Supply Current (Logic & booster)	IDD	Character mode, Note 1	-	0.5	0.75	mA
		Checker board mode, Note 1	-	0.54	0.81	mA
Supply Voltage of Yellow Green LED02 backlight	VLED02	Forward current =60mA	1.9	2.1	2.3	V
Wavelength of Yellow Green LED02 backlight	λ	No. of LED chips =2x4=8 dies.	-	570	-	nm
Luminance (on the backlight surface) of backlight			18	24	-	cd/m ²

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

Parallel bus timing characteristics (for 8080 MCU)

At $T_a = 0^\circ\text{C}$ to $+50^\circ\text{C}$, $V_{DD} = 3\text{V} \pm 5\%$.

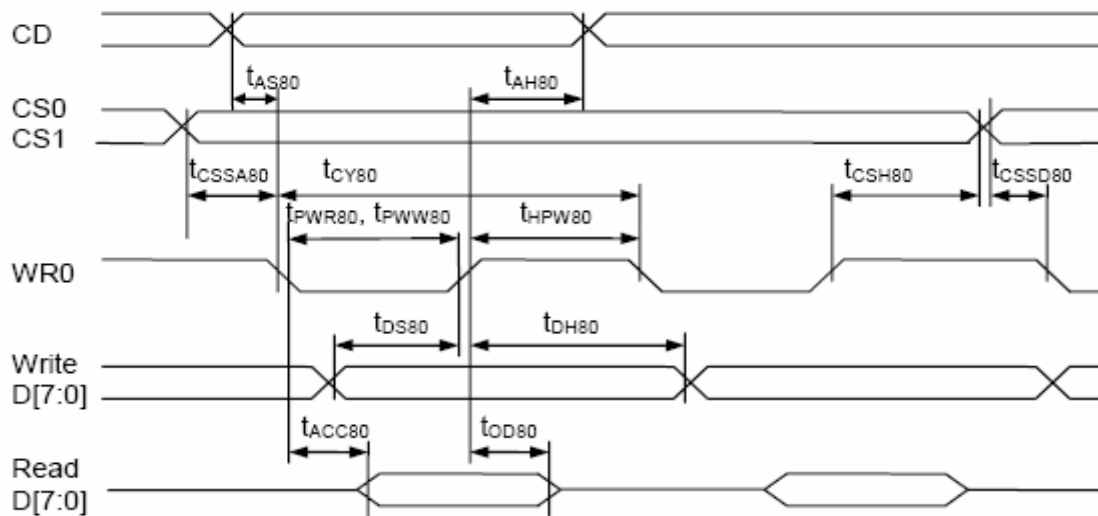


Figure: 4 Parallel Bus Timing Characteristics (for 8080 MCU)

At $T_a = 0^\circ\text{C}$ to $+50^\circ\text{C}$, $V_{DD} = 3\text{V} \pm 5\%$.

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80}	CD	Address setup time		0	–	nS
t_{AH80}		Address hold time		40	–	nS
t_{CY80}		System cycle time		135	–	nS
t_{PWR80}	WR1	Pulse width (read)		65	–	nS
t_{PWW80}	WR0	Pulse width (write)		65	–	nS
t_{HPW80}	WR0, WR1	High pulse width		65	–	nS
t_{DS80}	D0~D7	Data setup time		30	–	nS
t_{DH80}		Data hold time		20	–	nS
t_{ACC80}		Read access time	$C_L = 100\text{pF}$	–	50	nS
t_{OD80}		Output disable time		10	50	nS
t_{CSSA80}	CS1/CS0	Chip select setup time		10		nS
t_{CSSD80}				10		nS
t_{CSH80}				20		nS

Parallel bus timing characteristics (for 6800 MCU)

At $T_a = 0^\circ\text{C}$ to $+50^\circ\text{C}$, $V_{DD} = 3\text{V} \pm 5\%$.

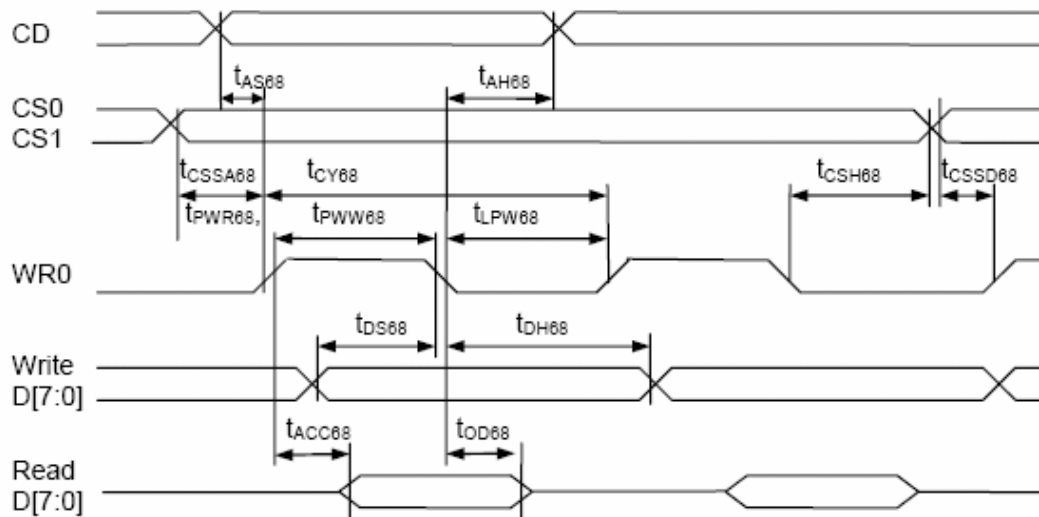


Figure: 5 Parallel Bus Timing Characteristics (for 6800 MCU)

At $T_a = 0^\circ\text{C}$ to $+50^\circ\text{C}$, $V_{DD} = 3\text{V} \pm 5\%$.

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68}	CD	Address setup time		0	–	nS
t_{AH68}		Address hold time		40	–	nS
t_{CY68}		System cycle time		135	–	nS
t_{PWR68}	WR1	Pulse width (read)		65	–	nS
t_{PWW68}		Pulse width (write)		65	–	nS
t_{LPW68}		Low pulse width		65	–	nS
t_{DS68}	D0~D7	Data setup time		30	–	nS
t_{DH68}		Data hold time		15	–	nS
t_{ACC68}		Read access time	$C_L = 100\text{pF}$	–	50	nS
t_{OD68}		Output disable time		10	50	nS
T_{CSSA68}	CS1/CS0	Chip select setup time		10		nS
T_{CSSD68}				10		
T_{CSH68}				20		

Serial Bus Timing Characteristics (for S8)

At Ta= 0°C to +50°C, VDD=3V±5%.

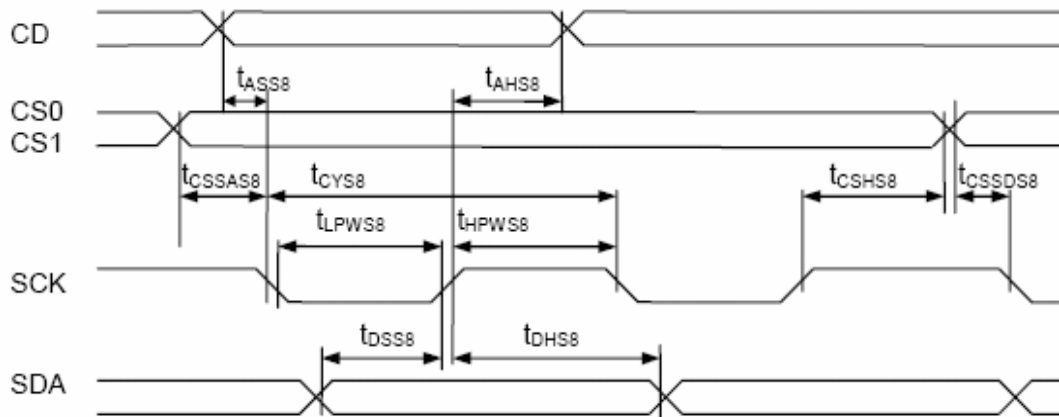


Figure: 6 Serial Bus Timing Characteristics (for S8)

At Ta= 0°C to +50°C, VDD=3V±5%.

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	-	nS
t_{AHS8}		Address hold time		40	-	nS
t_{CYS8}	SCK	System cycle time		135	-	nS
t_{LPWS8}		Low pulse width		65	-	nS
t_{HPWS8}		High pulse width		65	-	nS
t_{DSS8}	SDA	Data setup time		30	-	nS
t_{DHS8}		Data hold time		15	-	nS
t_{CSSAS8}	CS1/CS0	Chip select setup time		10		nS
t_{CSSDS8}				10		
t_{CSHS8}				20		

Serial bus timing characteristics (for S9)

At Ta= 0°C to +50°C, VDD=3V±5%.

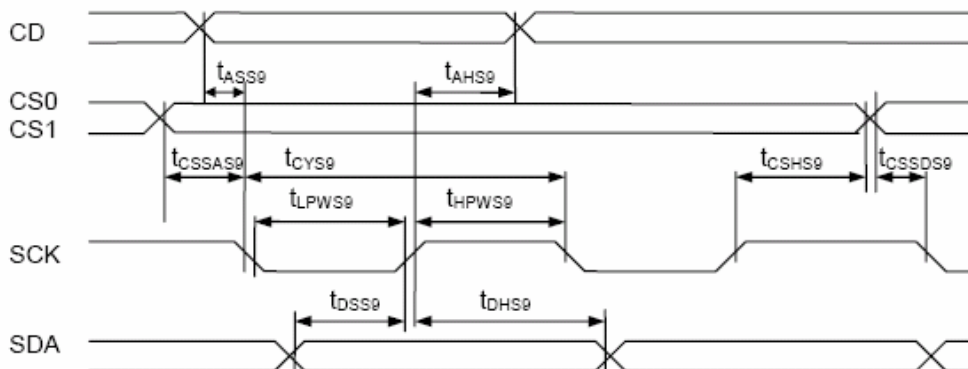


Figure: 7 Serial Bus Timing Characteristics (for S9)

At Ta= 0°C to +50°C, VDD=3V±5%.

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{ASS0}	CD	Address setup time		0	–	nS
t _{AHS0}		Address hold time		40	–	nS
t _{CYS0}	SCK	System cycle time		135	–	nS
t _{LPWS0}		Low pulse width		65	–	nS
t _{HPWS0}		High pulse width		65	–	nS
t _{DSS0}	SDA	Data setup time		30	–	nS
t _{DHS0}		Data hold time		15	–	nS
t _{CSSAS0}	CS1/CS0	Chip select setup time		10		nS
t _{CSSDS0}				10		
t _{CSSH0}				20		

Reset characteristics

At Ta= 0°C to +50°C, VDD=3V±5%.

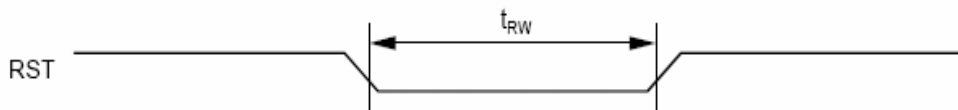


Figure: 8 Reset Characteristics

At Ta= 0°C to +50°C, VDD=3V±5%

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{RW}	RST	Reset low pulse width		1	–	μS

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6. LCD Cosmetic Conditions

- a.) Reference document follow VL-QUA-012B.
- b.) LCD size of the product is small.

7. Remark:

- a.) Identification labels will be stuck on the module without obstructing the viewing area of display,
- b.) Data Modul does not responsible for any polarizer defect after the protective film has been removed from the display.
- c.) The stiffener on FPC/FFC/COF must not be bent during or after assembly.