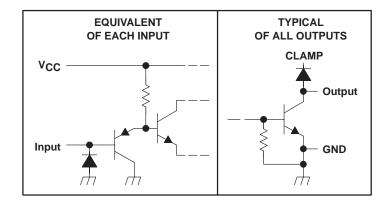
- Characterized for Use to 300 mA
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- High-Voltage Outputs (100 V Typ)
- Output Clamp Diodes for Transient Suppression (300 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- pnp Transistor Inputs Reduce Input Current
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications
- Plastic DIP (P) With Copper-Lead Frame Provides Cooler Operation and Improved Reliability

description

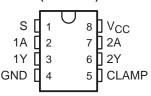
The SN75476 through SN75478 are dual peripheral drivers designed for use in systems that require high current, high voltage, and fast switching times. The SN75476, SN75477, and SN75478 provide AND, NAND, and OR drivers respectively. These devices have diode-clamped inputs as well as high-current, high-voltage clamp diodes on the outputs for inductive transient protection.

The SN75476, SN75477, and SN75478 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



D OR P PACKAGE (TOP VIEW)



Function Tables SN75476

SN75476 (each AND driver)

| INPU | OUTPUT | | | | |
|------|--------|---|--|--|--|
| Α | A S | | | | |
| Н | Н | Н | | | |
| L | Χ | L | | | |
| X | L | L | | | |

SN75477 (each NAND driver)

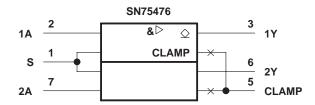
| INPU | OUTPUT | | | | |
|------|--------|---|--|--|--|
| Α | A S | | | | |
| Н | Н | L | | | |
| L | X | Н | | | |
| X | L | Н | | | |

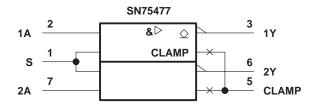
SN75478 (each OR driver)

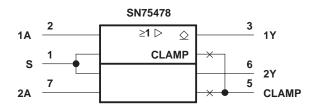
| INPU | OUTPUT | |
|------|--------|---|
| Α | S | Υ |
| Н | Х | Н |
| Х | Н | Н |
| L | L | L |

H = high level, L = low level X = irrelevant

logic symbols†

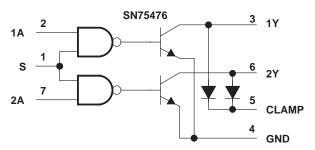




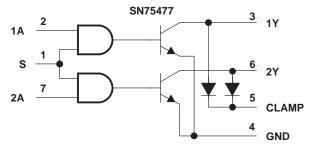


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

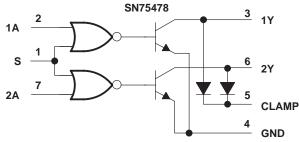
logic diagrams (positive logic)



Positive Logic: Y = AS or $\overline{A} + \overline{S}$



Positive Logic: $Y = \overline{AS}$ or $\overline{A} + \overline{S}$



Positive Logic: Y = A+S or $\overline{A} \overline{S}$

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) | 7 V |
|---|------------------------------|
| Input voltage, V _I | 5.5 V |
| Continuous output current (see Note 2) | 400 mA |
| Peak output current: $t_W \le 10$ ms, duty cycle $\le 50\%$ | 500 mA |
| $t_W \le 30 \text{ ns}, \text{ duty cycle} \le 0.002\% \dots$ | 3 A |
| Output clamp current, IOK | 400 mA |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T _A | 0°C to 70°C |
| Storage temperature range, T _{stq} | 65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | |
| | |

NOTES: 1. Voltage values are with respect to network GND.

2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous power dissipation ratings.

DISSIPATION RATING TABLE

| PACKAGE | $T_{\mbox{A}} \le 25^{\circ}\mbox{C}$ POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING | | |
|---------|--|--|---------------------------------------|--|--|
| D | 725 mW | 5.8 mW/°C | 464 mW | | |
| Р | 1000 mW | 8.0 mW/°C | 640 mW | | |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|-----|-----|-----|------|
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, V _{IL} | | | 8.0 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |

SN75476 THRU SN75478 DUAL PERIPHERAL DRIVERS

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electrical characteristics over recommended operating free-air temperature range

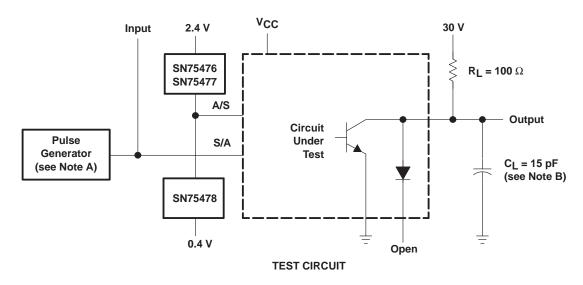
| | PARAMETER | | TEST C | TEST CONDITIONS | | | MAX | UNIT |
|--------------------|------------------------------|--------------------------|--|--|-----|------|------|------|
| VIK | Input clamp voltage | | I _I = -12 mA | I _I = -12 mA | | | -1.5 | V |
| | | | V _{CC} = 4.5 V, | I _{OL} = 100 mA | | 0.16 | 0.3 | |
| VOL | Low-level output voltage | | $V_{IH} = 2 V$ | I _{OL} = 175 mA | | 0.22 | 0.5 | V |
| | | | V _{IL} = 0.8 V | I _{OL} = 300 mA | | 0.33 | 0.6 | |
| V _{O(BR)} | Output breakdown voltage | | $V_{CC} = 4.5 \text{ V},$ | I _{OH} = 100 μA | 70 | 100 | | V |
| V _{R(K)} | Output clamp reverse voltage | | $V_{CC} = 4.5 V,$ | I _R = 100 μA | 70 | 100 | | V |
| V _F (K) | Output clamp forward voltage | | $V_{CC} = 4.5 V,$ | I _F = 300 mA | 0.8 | 1.15 | 1.6 | V |
| ЮН | High-level output current | | V _{CC} = 4.5 V, V _{IL} = 0.8 V, | V _{IH} = 2 V, V _{OH} = 70 V | | 1 | 100 | μΑ |
| lн | High-level input current | High-level input current | | V _I = 5.5 V | | 0.01 | 10 | μΑ |
| I | Low level input ourrent | A input | V 55V | V- 0.9.V | | -80 | -110 | |
| ¹IL | Low-level input current | S input | $V_{CC} = 5.5 \text{ V},$ | $V_{I} = 0.8 V$ | | -160 | -220 | μΑ |
| | | SN75476 | | V _I = 5 V | | 10 | 17 | |
| Іссн | Supply current, outputs high | SN75477 | V _{CC} = 5.5 V | V _I = 0 | | 10 | 17 | mA |
| | | SN75478 | | V _I = 5 V | | 10 | 17 | |
| | | SN75476 | | V _I = 0 | | 54 | 75 | |
| ICCL | Supply current, outputs low | SN75477 | V _{CC} = 5.5 V | V _I = 5 V | | 54 | 75 | mA |
| | | SN75478 | | V _I = 0 | | 54 | 75 | |

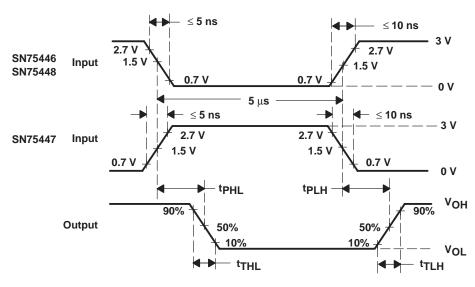
[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

| | PARAMETER | TEST CO | MIN | TYP | MAX | UNIT | |
|------------------|--|--|-------------------------------|--------------------|-----|------|----|
| ^t PLH | Propagation delay time, low-to-high-level output | | | | 200 | 350 | ns |
| t _{PHL} | Propagation delay time, high-to-low-level output | $C_L = 15 pF,$ | $R_L = 100 \Omega$, | | 200 | 350 | ns |
| tTLH | Transition time, low-to-high-level output | See Figure 1 | | 50 | 125 | ns | |
| tTHL | Transition time, high-to-low-level output | | | | 90 | 125 | ns |
| VOH | High-level output voltage after switching | V _S = 55 V, See Figure 2 | $I_O \approx 300 \text{ mA},$ | V _S -18 | | | mV |

PARAMETER MEASUREMENT INFORMATION





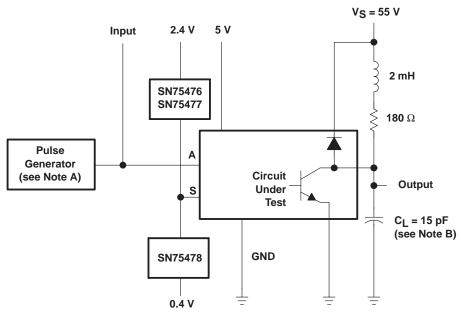
NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, $Z_O = 50 \Omega$.

B. C_L includes probe and jig capacitance.

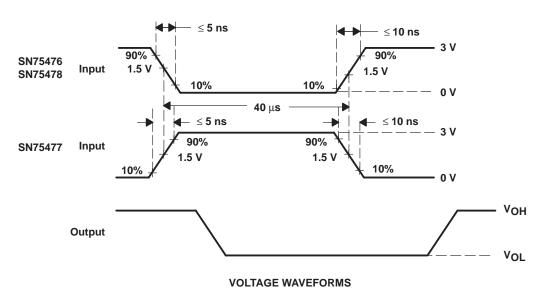
Figure 1. Test Circuit and Voltage Waveforms, Switching Characteristics

VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \Omega$.

B. C_L includes probe and jig capacitance.

Figure 2. Latch-Up Test Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM



i.com 18-Sep-2008

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp (3) |
|------------------|-----------------------|-----------------|--------------------|------|----------------|----------------------------|------------------|--------------------|
| SN75476D | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI |
| SN75476DR | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI |
| SN75476P | OBSOLETE | PDIP | Р | 8 | | TBD | Call TI | Call TI |
| SN75477D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75477DE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75477DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75477DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75477DRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75477DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75477P | ACTIVE | PDIP | Р | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75477PE4 | ACTIVE | PDIP | Р | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75478D | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI |
| SN75478P | ACTIVE | PDIP | Р | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75478PE4 | ACTIVE | PDIP | Р | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

18-Sep-2008

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TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| | Device | | Package Drawing | | | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|-----------|------|--------------------|---|------|--------------------------|--------------------------|---------|---------|---------|------------|-----------|------------------|
| I | SN75477DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |





*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75477DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



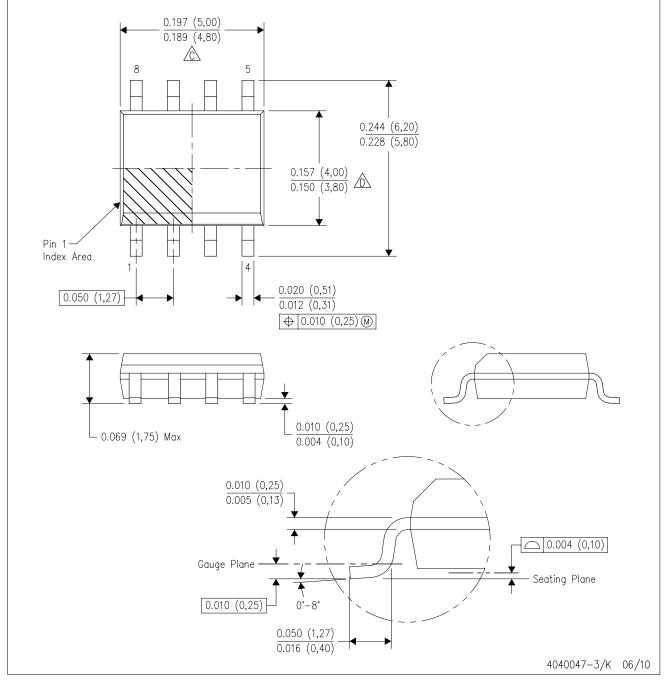
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.



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