FAIRCHILD
SEMICONDUCTOR™

March 1999
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74LVT574 • 74LVTH574
Low Voltage Octal D-Type Flip-Flop with 3-STATE Outputs

General Description

The LVT574 and LVTH574 are high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

The LVTH574 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These octal flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT574 and LVTH574 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

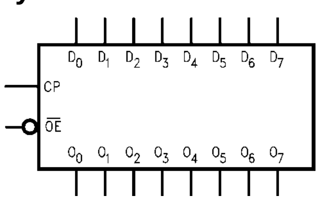
- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH574), also available without bushold feature (74LVT574).
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink –32 mA/+64 mA
- Functionally compatible with the 74 series 574
- Latch-up performance exceeds 500 mA

Ordering Code:

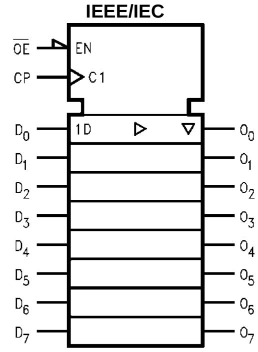
Order Number	Package Number	Package Description
74LVT574WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, .300” Wide
74LVT574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
74LVT574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVT574MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LVTH574WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, .300” Wide
74LVTH574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
74LVTH574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVTH574MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering code.

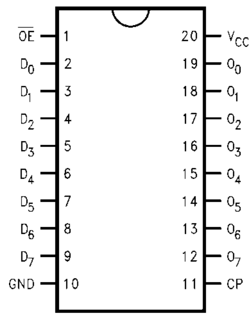
Logic Symbols



IEEE/IEC



Connection Diagram



Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
O_0–O_7	3-STATE Outputs

Truth Table

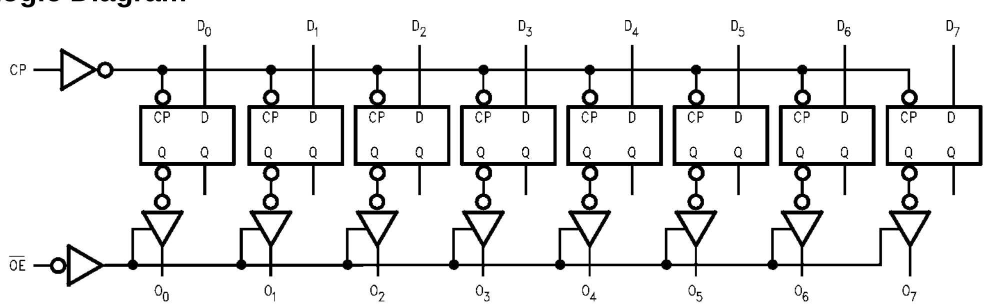
Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	↑	L	H
L	↑	L	L
X	L	L	O_o
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↑ = LOW-to-HIGH Transition
O_o = Previous O_o before HIGH to LOW of CP

Functional Description

The LVT574 and LVTH574 consist of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	–0.5 to +4.6		V
V_I	DC Input Voltage	–0.5 to +7.0		V
V_O	DC Output Voltage	–0.5 to +7.0	Output in 3-STATE	V
		–0.5 to +7.0	Output in High or Low State (Note 2)	
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at High State	mA
		128	$V_O > V_{CC}$ Output at Low State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	–65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	High-Level Output Current		–32	mA
I_{OL}	Low-Level Output Current		64	mA
T_A	Free-Air Operating Temperature	–40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 1: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 2: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40°C to +85°C Min	Typ (Note 3)	Max	Units	Conditions
V_{IK}	Input Clamp Diode Voltage	2.7			–1.2	V	I_I = –18 mA
V_{IH}	Input HIGH Voltage	2.7–3.6	2.0			V	$V_O \leq 0.1V$ or
V_{IL}	Input LOW Voltage	2.7–3.6			0.8	V	$V_O \geq V_{CC} - 0.1V$
V_{OH}	Output HIGH Voltage	2.7–3.6	V_{CC} – 0.2			V	I_{OH} = –100 µA
		2.7	2.4				I_{OH} = –8 mA
		3.0	2.0				I_{OH} = –32 mA
V_{OL}	Output LOW Voltage	2.7			0.2	V	I_{OL} = 100 µA
		2.7			0.5		I_{OL} = 24 mA
		3.0			0.4		I_{OL} = 16 mA
		3.0			0.5		I_{OL} = 32 mA
		3.0			0.55		I_{OL} = 64 mA
$I_{I(HOLD)}$ (Note 4)	Bushold Input Minimum Drive	3.0	75			µA	V_I = 0.8V
			–75				V_I = 2.0V
$I_{I(OD)}$ (Note 4)	Bushold Input Over-Drive Current to Change State	3.0	500			µA	(Note 5)
			–500				(Note 6)
I_I	Input Current	3.6			10	µA	V_I = 5.5V
	Control Pins	3.6			±1		V_I = 0V or V_{CC}
	Data Pins	3.6			–5		V_I = 0V
					1		$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current	0			±100	µA	0V ≤ V_I or V_O ≤ 5.5V
$I_{PU/PD}$	Power up/down 3-STATE Output Current	0–1.5V			±100	µA	V_O = 0.5V to 3.0V V_I = GND or V_{CC}
I_{OZL}	3-STATE Output Leakage Current	3.6			–5	µA	V_O = 0.5V
I_{OZH}	3-STATE Output Leakage Current	3.6			5	µA	V_O = 3.0V

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Typ (Note 3)	Max	Units	Conditions
$I_{OZH}+$	3-STATE Output Leakage Current	3.6			10	μA	$V_{CC} < V_O \leq 5.5V$
I_{CCH}	Power Supply Current	3.6			0.19	mA	Outputs High
I_{CCL}	Power Supply Current	3.6			5	mA	Outputs Low
I_{CCZ}	Power Supply Current	3.6			0.19	mA	Outputs Disabled
$I_{CCZ}+$	Power Supply Current	3.6			0.19	mA	$V_{CC} \leq V_O \leq 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)	3.6			0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 4: Applies to bushold versions only (74LVTH574).

Note 5: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 6: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$ Min	Typ	Max	Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 10)	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150			150		MHz
t_{PHL}	Propagation Delay	1.8		4.6	1.8	5.3	ns
t_{PLH}	CP to O_n	1.8		4.5	1.8	5.3	
t_{PZL}	Output Enable Time	1.5		5.2	1.5	6.1	ns
t_{PZH}		1.5		4.8	1.5	5.9	
t_{PLZ}	Output Disable Time	2.0		4.4	2.0	4.4	ns
t_{PHZ}		2.0		4.8	2.0	5.1	
t_S	Setup Time	2.0			2.4		ns
t_H	Hold Time	0.3			0.0		ns
t_W	Pulse Width	3.3			3.3		ns
t_{OSHL}	Output to Output Skew (Note 11)			1.0		1.0	ns
t_{OSLH}				1.0		1.0	

Note 10: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

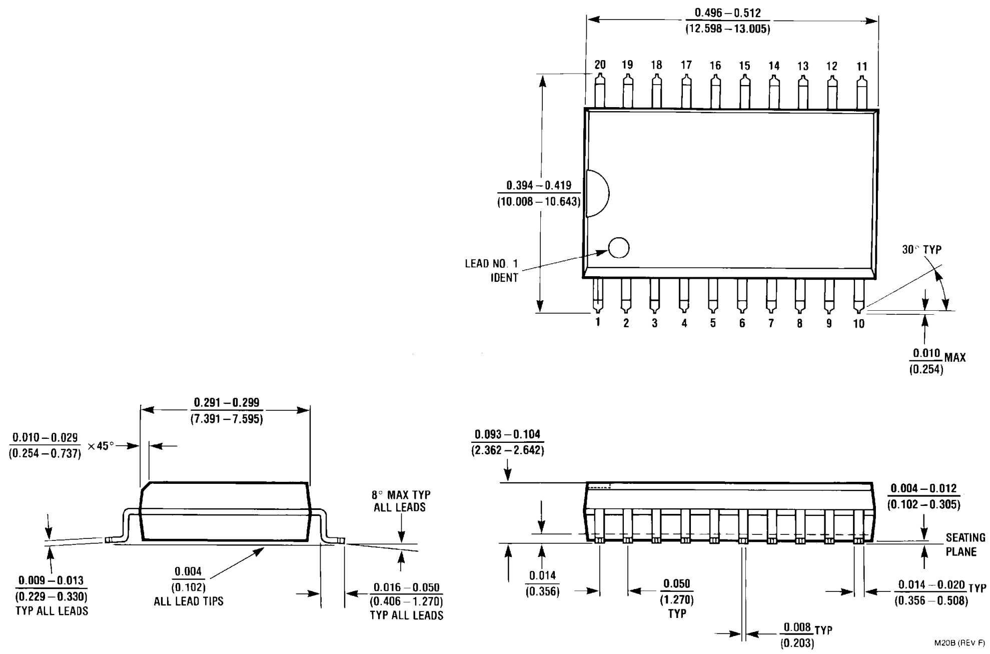
Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Capacitance (Note 12)

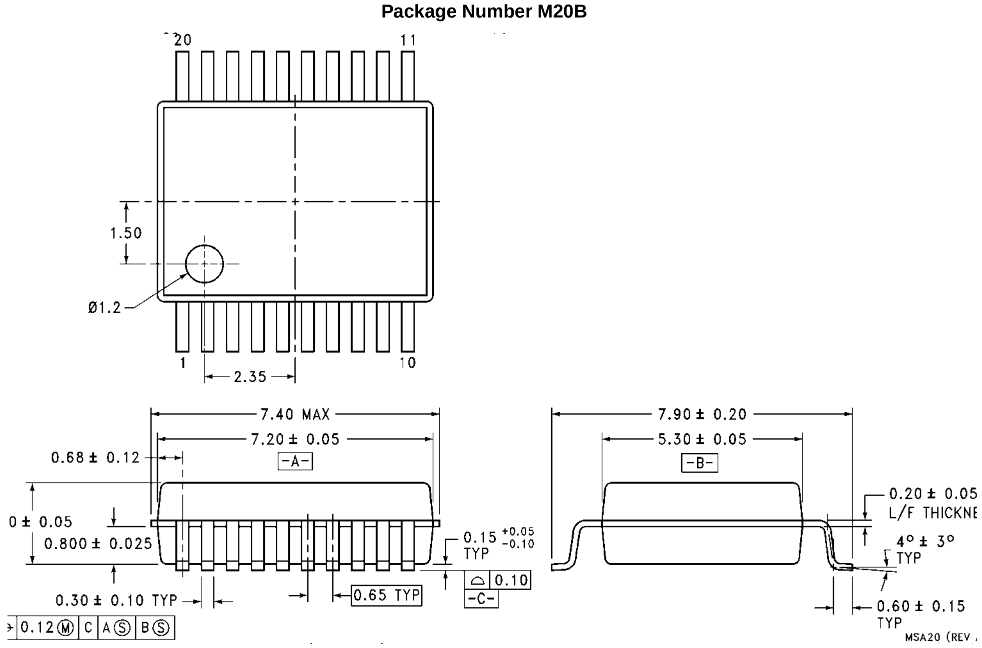
Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	4	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}	6	pF

Note 12: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted

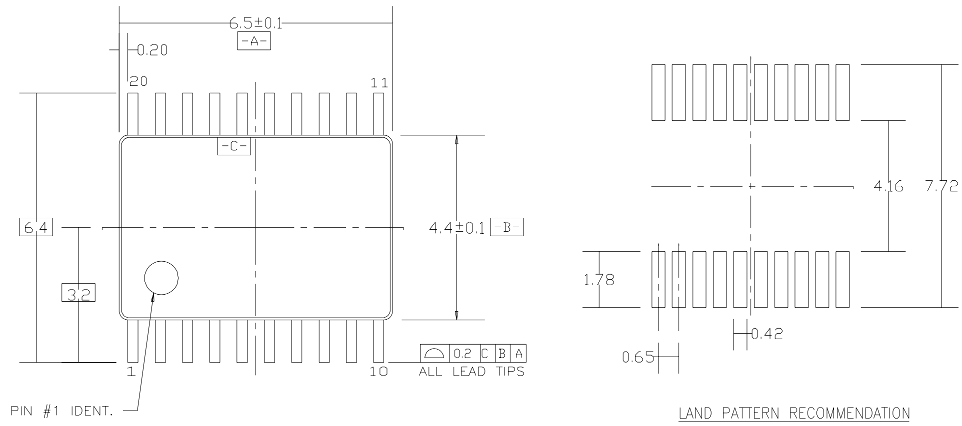


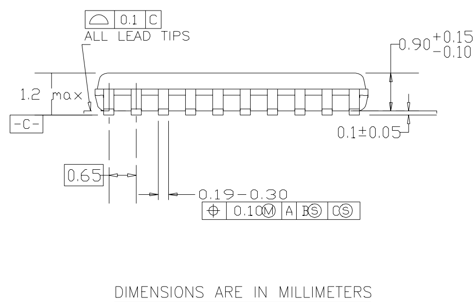
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, .300” Wide
Package Number M20B

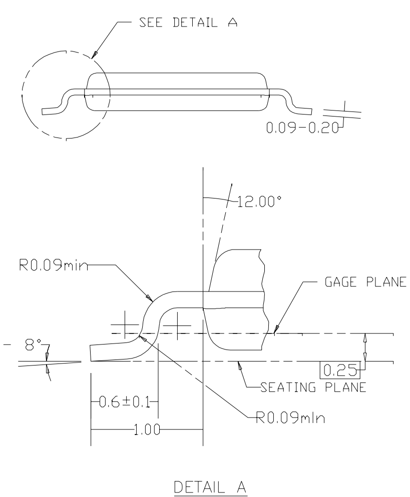


20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)







NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

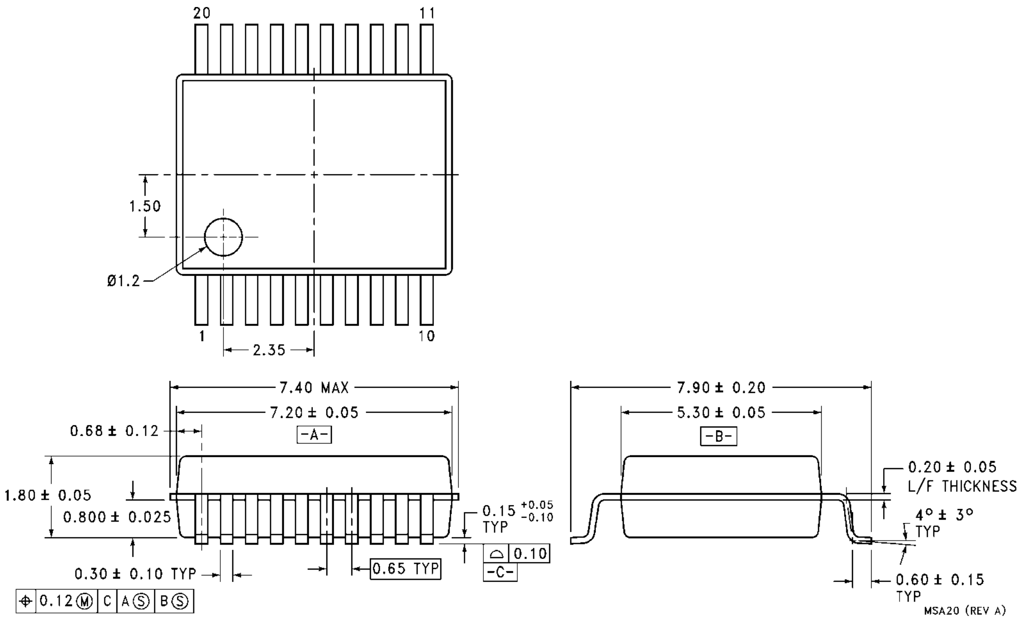
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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