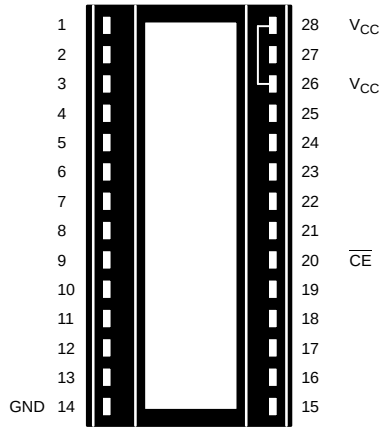
DALLAS SEMICONDUCTOR

DS1213B
SmartSocket 16K/64K

FEATURES

- Accepts standard 2K x 8 or 8K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 2K x 8 to 8K x 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT



28-PIN INTELLIGENT SOCKET

PIN DESCRIPTION

$\overline{CE}$ – Conditioned Chip Enable
V_{CC} – Switched V_{CC}
GND – Ground
All pins pass through except 20, 26 and 28.

DESCRIPTION

The DS1213B SmartSocket is a 28-pin, 600 mil DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either 24-pin 2K x 8 (lower-justified) or 28-pin 8K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility . The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, the internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption.

Using the SmartSocket saves printed circuit board space since the SRAM/SmartSocket combination occupies no more area than the SRAM alone. The SmartSocket modifies only pins 20, 26 and 28, to nonvolatize the RAM. All other pins are passed straight through.

OPERATION

The DS1213B SmartSocket performs five circuit functions required to battery back up a CMOS memory. The first function involves switching between the battery and the V_{CC} supply, depending on which is greater. The switch has a voltage drop of less than 0.2 volts.

The second function is power-fail detection. The DS1213B constantly monitors the V_{CC} supply. When V_{CC} falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable.

The third function, write protection, is accomplished by holding the RAM chip enable signal to within 0.2 volts of V_{CC} or the battery supply whichever is greater. If the incoming chip enable signal is active at the time power fail detection occurs, write protection is delayed until after the current memory cycle is complete to avoid corruption of data. Power fail detection occurs in the range of 4.75 to 4.5 volts. During nominal power supply conditions the chip enable signal will be passed through from the socket pin to the socket contact with a maximum propagation delay of 20 ns.

The fourth function the DS1213B performs is to check battery status to warn of potential data loss. Each time that V_{CC} power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory access to the SmartSocket is inhibited. Battery status can, therefore, be determined by a three–step process. First, a read cycle is performed to any location in the memory, in order to save the contents of that location. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, then the battery voltage is less than 2.0 V and data is in danger of being corrupted.

The fifth function the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to ensure reliability. The DS1213B SmartSocket provides two batteries and an internal isolation switch to select between them. During battery back up, the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. Each of the two internal lithium cells has a 45 mAh capacity.

NOTE: As shipped from Dallas Semiconductor, battery voltage cannot be measured on the V_{CC} socket contact. Only after V_{CC} has been applied to the device for the first time and then removed will the battery voltage be present on socket contacts 28, 26 and 20.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	40°C to 70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Voltage	V_{CC}	4.75	5.0	5.5	V	1,3
Logic 1 PIN 20 L	V_{IH}	2.2		V_{CC}+0.3	V	1,3
Logic 0 PIN 20 L	V_{IL}	-0.3		+ 0.8	V	1,3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Current	I_{CC}			5	mA	3, 4, 5
PIN 26 U, PIN 28 U Supply Voltage	V_{CCO}	V_{CC} -0.2			V	1, 3, 8
PIN 26 U, PIN 28 U Supply Current	I_{CCO}			80	mA	3,8
PIN 20 L $\overline{CE}$ Input Leakage	I_{IL}	-1.0		+1.0	µA	3, 4
PIN 20 U $\overline{CE}$ Output @ 2.4 V	I_{OH}	-1.0			mA	2, 3
PIN 20 U $\overline{CE}$ Output @ .4V	I_{OL}			4.0	mA	2, 3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} < 4.5V)

PIN 20 U Output	V_{OHL}	V_{CC} -0.2 V_{BAT}-0.2			V	1, 3
PIN 26 U, PIN 28U Battery Current	I_{BAT}			1	µA	3, 6
PIN 26 U, PIN 28 U Battery Voltage	V_{BAT}	2	3	3.6	V	1, 3

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance PIN 20 L	C_{IN}			5	pF	3
Output Capacitance PIN 20 U	C_{OUT}			7	pF	3

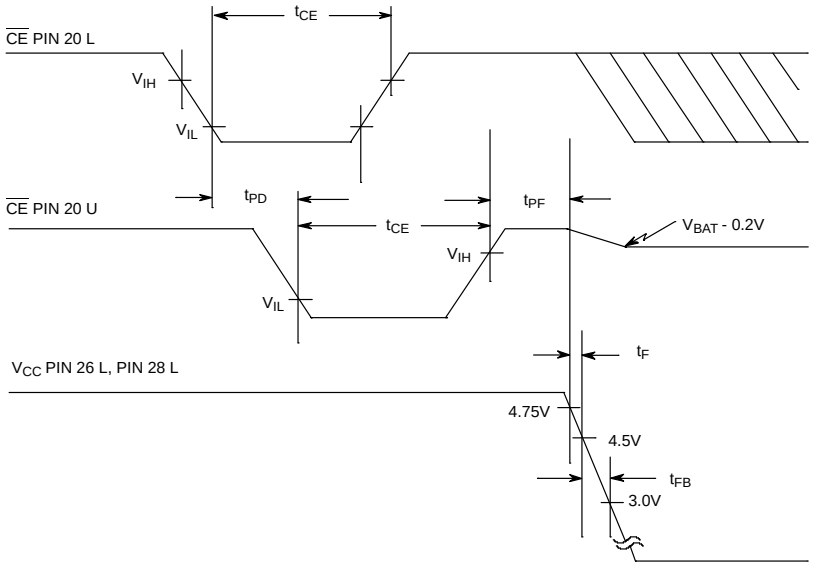
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2,9
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

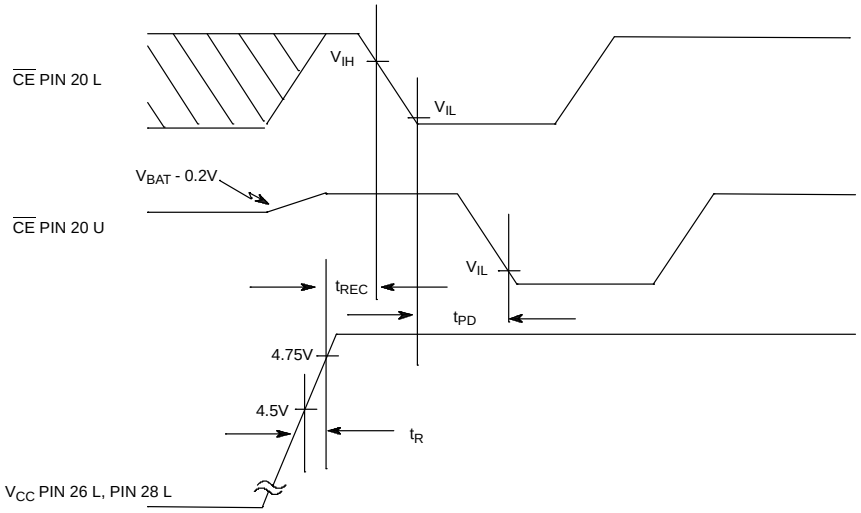
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CCI} < 4.75 V)

Recovery at Power-Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate 4.75 - 4.5 V	t_F	300			µs	
V_{CC} Slew Rate 4.5 - 3 V	t_{FB}	10			µs	
V_{CC} Slew Rate 4.5-4.75 V	t_R	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	7

TIMING DIAGRAM: POWER-DOWN



TIMING DIAGRAM: POWER-UP



WARNINGS:

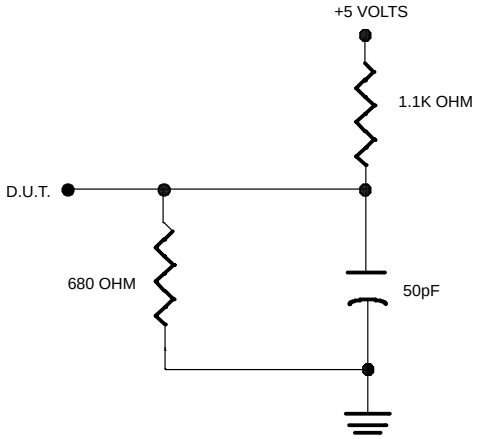
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal will discharge internal lithium source because exposed voltage pins are present.

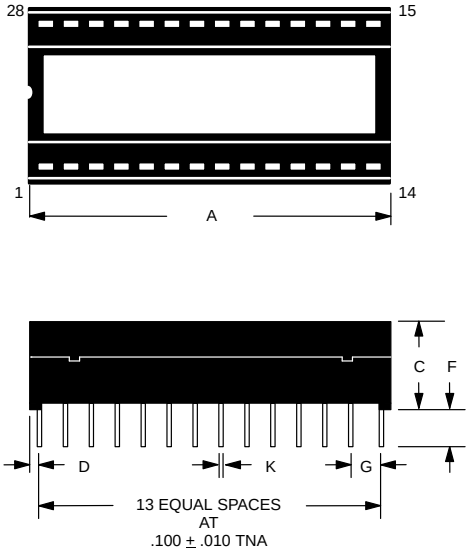
NOTES:

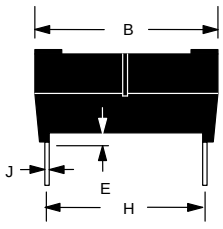
1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Pin locations are designated “U” (for upper) when a parameter definition refers to the socket receptacle and “L” (for lower) when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Pin 26 L may be connected to V_{CC} or left disconnected at the PC board.
6. I_{BAT} is the maximum load current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
7. t_{CE} max. must be met to ensure data integrity on power loss.
8. V_{CC} is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.

OUTPUT LOAD Figure 1



DS1213B INTELLIGENT SOCKET 28 PIN (FOR 600–MIL DIP)





PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	1.380 35.05	1.420 36.07
B IN. MM	0.690 17.53	0.720 18.29
C IN. MM	0.370 9.39	0.420 10.67
D IN. MM	0.035 0.89	0.065 1.65
E IN. MM	0.015 0.38	0.035 0.89
F IN. MM	0.120 3.04	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53