Z i L O G

eZ80[®] Microprocessors

eZ80L92 Product Brief

PB008607-0103

Product Block Diagram

eZ80L92 MPU						
24-Bit GPIO		Infrared Encoder/ Decoder		2 UART		
I ² C	SPI		6 PRT		WDT	
Real- Time Clock	4 CS + WSG		JTAG		ZDI	

Features

The eZ80L92 microprocessor is a member of ZiLOG's eZ80[®] product family. It offers the following features:

- High-performance, pipelined eZ80® CPU available at 20MHz or 50MHz maximum speed
- 24 bits of General-Purpose I/O
- IrDA TM compatible Infrared Encoder/Decoder
- 2 UARTs with independent baud rate generators
- I²C with independent clock rate generator
- SPI with independent clock rate generator
- Glueless external memory interface with 4 Chip Selects, independent WAIT state generators, and external WAIT input pin; supports Z80, Intel, and Motorola bus-compatible peripherals.
- Six 16-bit Counter/Timers with prescalers and direct input/output drive capability
- Interrupt controller supports internal and external maskable interrupts as well as a non-maskable interrupt input
- Watch-Dog Timer

- Real-time clock with on-chip 32 KHz oscillator, selectable 50/60 Hz input, and separate V_{DD} pin for battery backup
- JTAG Debug Interface (also supports ZiLOG Debug Interface)
- New DMA-like eZ80[®] instructions
- Power management features including SLEEP/ HALT modes and peripheral power-down controls
- 100-pin LQFP package
- 3.0–3.6V supply voltage with 5V tolerant inputs
- Operating Temperature Ranges:
 - Standard: 0°C to +70°C
 - Extended: -40°C to +105°C

General Description

The eZ80L92 is a power-efficient, optimized pipeline architecture microprocessor operating up to 50 MHz. It is part of a line of eZ80®-based standard products targeted toward industrial, communication, security, automation, and embedded Internet applications.

eZ80[®] CPU Core

The eZ80[®] can operate in Z80-compatible (64KB) mode or full 24-bit (16 MB) addressing mode. Considering both the increased clock speed and processor efficiency, the eZ80[®]'s processing power rivals the performance of 16-bit microprocessors. The eZ80[®] improves on the world-famous Z80 architecture. Like the Z80, it features dual bank registers for fast context switching.

eZ80L92 Peripherals

General-Purpose Input/Output

The eZ80L92 microprocessor features 24 bits of General-Purpose Input or Output (GPIO). All port

signals are programmable in Input or Output modes. The 24 port bits can be used as vectored interrupt sources. The pins can be set to recognize either level- or edge-triggered interrupts.

Infrared Encoder/Decoder

- Supports IrDATM SIR format
- Operates seamlessly with the on-chip UART
- Interfaces with IrDA TM-compliant transceivers
- Supports transmit/receive up to 115.2kbps

Universal Asynchronous Receiver/ Transmitters

Each of the two Universal Asynchronous Receiver/ Transmitters (UART) devices contains control registers and a Baud Rate Generator (BRG).

- The Baud Rate Generator produces a lower-frequency bit clock from the system clock. All standard baud rates up to 115 kbps and some rates higher than 115 kbps are supported.
- The UART module implements all the logic required to support asynchronous communications and hardware flow control. The module also contains separate 16-byte-deep transmit and receive FIFOs.

Inter-Integrated Circuit

The Inter-Integrated Circuit (I²C) device contains control registers and its own clock rate generator. The I²C operates in four modes: Master Transmit or Receive, Slave Transmit or Receive.

Serial Peripheral Interface

The Serial Peripheral Interface (SPI) device contains control registers and its own clock rate generator. The SPI is a synchronous interface allowing several SPI-type devices to be interconnected. The SPI may be configured as either a master or a slave.

Programmable Reload Timers

The eZ80L92 features six Programmable Reloadable Counter Timers (PRT). Each timer is a 16-bit down counter and offers a 4-bit clock prescaler with four selectable taps for $CLK \div 4$, $CLK \div 16$,

CLK \div 64, and CLK \div 256. The timers' two modes of operation are single-pass and continuous count mode. Four timers can be driven through a GPIO input pin for external event count. Two others allow the ability to drive their outputs through GPIO pins.

Watch-Dog Timer

The Watch-Dog Timer (WDT) features four programmable time-out periods: 218, 222, 225, or 227 clock cycles. It allows the user to monitor the status of a time-out and generate a RESET or non-maskable interrupt. The WDT can operate from either the system clock or the on-chip 32 KHz oscillator used by the RTC.

Real-Time Clock

The real-time clock (RTC) allows counting of seconds, minutes, hours, days-of-the-week, day-of-the-month, month, year, and century. Alarms and interrupts can be set for seconds, minutes, hours, and day-of-the-week. The real-time clock input can be taken from the on-chip 32 KHz oscillator or from a 50/60 Hz input. The real-time clock operates from an isolated $V_{\rm DD}$ pin to allow constant operation from a battery.

Chip Select/Wait State Generator and WAIT Pin

There are four chip selects for external devices. Each chip select may be programmed for either memory or I/O space. Each memory chip select can be individually programmed on a 64KB boundary. The I/O chip selects can choose a 256-byte section of I/O space. The WAIT input pin allows interface with slow peripherals. The chip selects support Z80-, Intel-, and Motorola-style buses.

JTAG Debug Interface

The IEEE1149.1-compatible JTAG interface supports all of the ZDI functions plus the following features: software break points, 64-word trace buffer, complex break points using address and data masks, and cascadable triggers.

ZiLOG Debug Interface

The ZiLOG Debug Interface (ZDI) incorporates most of the functions of an In-Circuit Emulator onchip. ZDI allows the user to single-step code, change registers, edit programs, and view status of internal registers.

Block Transfer Instructions

Four new block transfer instructions with expanded repeat capability are added to the eZ80[®] CPU. These provide performance similar to hardware DMAs.

Power Management

Several power management features are supported on the eZ80L92. Peripheral power-down registers allow independent clock gating of on-chip peripherals under software control while operating under normal conditions. The CPU can write to these control registers to disable the clock from driving any one of the peripherals when they are inactive.

In addition, execution of the HALT instruction suspends eZ80[®] CPU operation and eliminates clock power associated with the CPU core. Normal operation can be restored via external and peripheral interrupts or hardware reset.

Execution of a sleep instruction provides the lowest power consumption. In SLEEP mode, only the on-chip RTC 32KHz crystal oscillator remains active to drive the RTC and the WDT. All other peripherals, the system clock, and the primary oscillator are disabled. An RTC alarm, a WDT time-out, or hardware reset can restart the CPU.

Electrical Features Summary

• Power supply: $3.3 \text{ V} \pm 300 \text{ mV}$

• Standard temperature: 0°C to 70°C

• Extended temperature: -40°C to +105°C

• Supply current @ 20MHz: <30mA (typical)

• Supply current in HALT mode with peripherals powered down: <10mA (typical)

• Supply current in SLEEP mode: <50μA (typical)

Support Tools

The following development tools are available to program and debug applications using the eZ80L92 microprocessor:

- eZ80L92 compact Ethernet modules
- eZ80L92 evaluation and development board
- ZPAK low-cost emulator with JTAG and ZDI interfaces
- ZiLOG Developer's Suite IDE (ZDS) including assembler, linker, debugger, and simulator
- ZiLOG ANSI C-Compiler
- Metro IPWorksTM TCP/IP software stack and RTOS, supporting the following protocols:
 - TCP, UDP, IP, ARP, RARP, ICMP, IGMP, PPP
 - FTP, SMTP, HTTP, TELNET, DNS
 - TFTP, SNMP, DHCP/BOOTP, TIMEP
- eZ80L92 Development Kit, including:
 - eZ80L92 Module
 - eZ80[®] Development Platform
 - ZPAKII emulator with JTAG/ZDI
 - ZDSII, ANSI C-Compiler
- Third-party tools from IAR, CMX, and First Silicon Solutions:
 - IAR Embedded Workbench IDE for eZ80[®] with C/C++ compiler, debugger, assembler and linker
 - IAR eZ80[®] MakeApp peripheral software drivers generator
 - IAR eZ80[®] VisualState software statemachine generator
 - CMX Embedded TCP/IP Software Suite for eZ80[®]
- First Silicon Solutions' low-cost JTAG/ZDI emulators

The Metro IPWorksTM TCP/IP software stack is available via download from <u>zilog.com</u>.



Pin Diagram

Figure 1 diagrams the pin configuration of the eZ80L92 100-pin LQFP microprocessor.

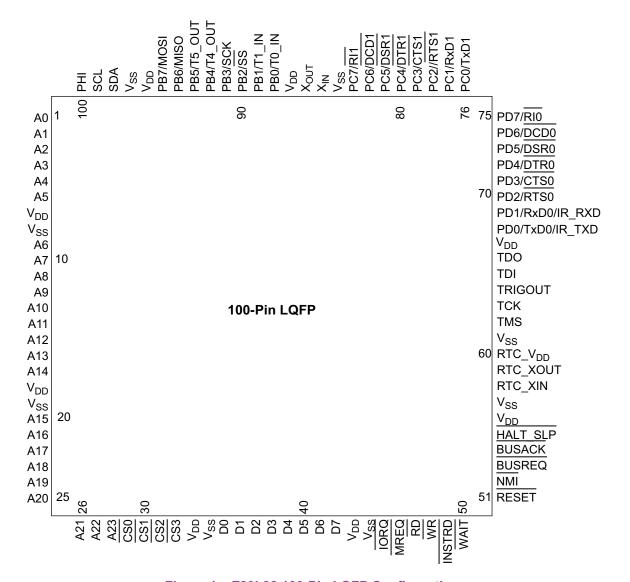


Figure 1. eZ80L92 100-Pin LQFP Configuration



Block Diagram

Figure 2 illustrates a block diagram of the eZ80L92 microprocessor.

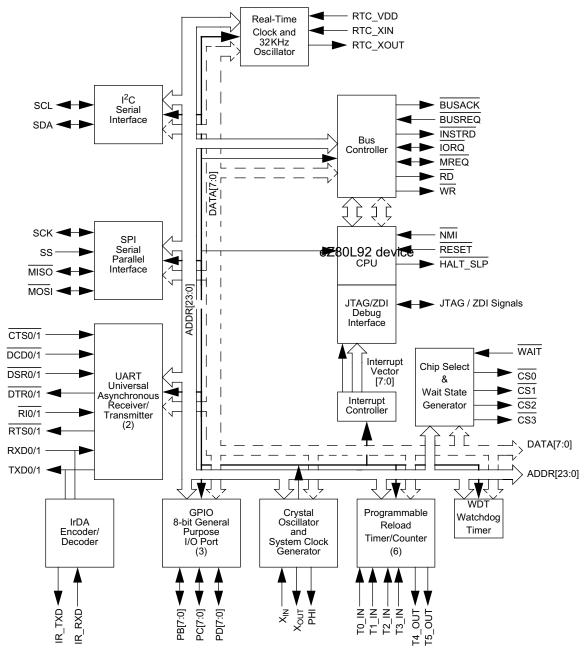


Figure 2. eZ80L92 Block Diagram



Related Products

Other integrated devices of interest include:

eZ80190	50 MHz eZ80 [®] CPU, 8KB SRAM, 16x16 Multiply with 40-bit Accumulators, 32 bits GPIO, 6 Counter Timers with Prescalers, WDT, 4 channel CS+WSG, 2-Channel DMA, 2 UZI Channels, ZDI, On-Chip Oscillator.
eZ80F92	20MHz eZ80 [®] CPU, low-power modes, 128KB+256B Flash, 8KB SRAM, 24 bits GPIO, IrDA, 2 UART, I ² C, SPI, 6 Counter Timers with I/O features, WDT, RTC, 4 channel CS+WSG, JTAG, ZDI, PLL.
eZ80F93	20MHz eZ80 [®] CPU, low-power modes, 64KB+256B Flash, 4KB SRAM, 24 bits GPIO, IrDA, 2 UART, I ² C, SPI, 6 Counter Timers with I/O features, WDT, RTC, 4 channel CS+WSG, JTAG, ZDI.
eZ80F91	50MHz eZ80 [®] CPU, low-power modes, 256KB+512B Flash, 8KB SRAM, 32 bits GPIO, 10/ 100 EMAC, IrDA, 2 UART, I ² C, SPI, 6 Counter Timers with I/O features, WDT, RTC, 4 channel CS+WSG, JTAG, ZDI, PLL.
Z80S180	Improved Z80™ CPU, 1MB MMU, 2 DMA, 2 16-bit PRTs, 2 UARTs, CSIO, up to 33MHz clock speed
Z80181	Z8S180 CPU, SCC, CTC, 16-bit GPIO, up to 33MHz clock speed
Z80182	Z8S180 CPU, 2 ESCC, 24-bit GPIO, 16550 Mimic interface, up to 33MHz clock speed
Z84C00	Z80™ CPU (up to 20 MHz)
Z84C15	Z80™ CPU, 2 SIO, 4x8 CTC, 2 PIO, WDT, up to 16MHz clock speed

Ordering Information

PSI	Part	Description
eZ80L92AZ020SC	20 MHz, Standard Temperature	eZ80L92 microprocessor
eZ80L92AZ020EC	20 MHz, Extended Temperature	eZ80L92 microprocessor
eZ80L92AZ050SC	50 MHz, Standard Temperature	eZ80L92 microprocessor
eZ80L92AZ050EC	50 MHz, Extended Temperature	eZ80L92 microprocessor
eZ80L920210ZCO	eZ80L92 Development Kit	Complete eZ80 [®] development kit



This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters

532 Race Street San Jose, CA 95126 Telephone: 408.558.8500 Fax: 408.558.8300

www.ZiLOG.com

Document Disclaimer

ZiLOG is a registered trademark of ZiLOG Inc. in the United States and in other countries. All other products and/or service names mentioned herein may be trademarks of the companies with which they are associated.

©2003 by ZiLOG, Inc. All rights reserved. Information in this publication concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. ZiLOG, INC. DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED IN THIS DOCUMENT. ZiLOG ALSO DOES NOT ASSUME LIABILITY FOR INTELLECTUAL PROPERTY INFRINGEMENT RELATED IN ANY MANNER TO USE OF INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED HEREIN OR OTHERWISE. Devices sold by ZiLOG, Inc. are covered by warranty and limitation of liability provisions appearing in the ZiLOG, Inc. Terms and Conditions of Sale. ZiLOG, Inc. makes no warranty of merchantability or fitness for any purpose Except with the express written approval of ZiLOG, use of information, devices, or technology as critical components of life support systems is not authorized. No licenses are conveyed, implicitly or otherwise, by this document under any intellectual property rights.