

MR48V256A

32,768-Word × 8-Bit FeRAM (Ferroelectric Random Access Memory)

GENERAL DESCRIPTION

The MR48V256A is a nonvolatile 32,768-word x 8-bit ferroelectric random access memory (FeRAM) developed in the ferroelectric process and silicon-gate CMOS technology. Unlike SRAMs, this device, whose cells are nonvolatile, eliminates battery backup required to hold data. This device has no mechanisms of erasing and programming memory cells and blocks, such as those used for various EEPROMs. Therefore, the write cycle time can be equal to the read cycle time and the power consumption during a write can be reduced significantly. The MR48V256A can be used in various applications, because the device is guaranteed for the write/read tolerance of 10^{12} cycles per bit and the rewrite count can be extended significantly.

FEATURES

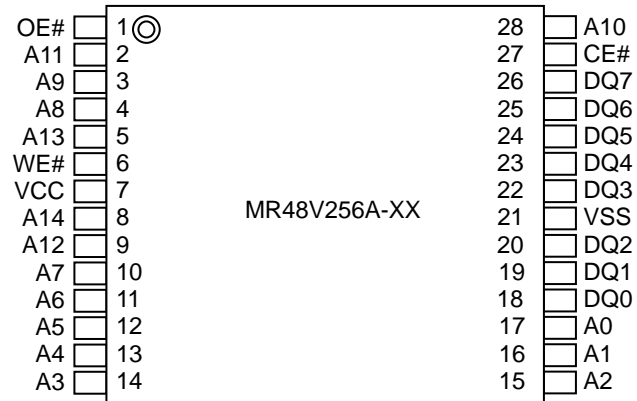
- 32,768-word × 8-bit configuration
- A single 3.3 V ± 0.3 V power supply
- Read access time: 70 ns (Max.)
- Write enable time: 70 ns (Min.)
- Random read/write cycle time 150 ns (Min.)
- Read/write tolerance 10^{12} cycles/bit
- Data retention 10 years
- Guaranteed operating temperature range -40 to 85°C (Extended temperature version)
- Package options:
28-pin plastic TSOPI (TSOP(1)28-08134-0.55-ZK)

PRODUCT FAMILY

| Family | Access Time | | Read/Write Cycle Time | Package |
|-----------|----------------|----------------|-----------------------|-------------|
| | Relative to CE | Relative to OE | | |
| MR48V256A | 70ns | 40ns | 150ns | 28pin TSOPI |

PIN CONFIGURATION

28-pin plastic TSOP1



Note:

Signal names that end with # indicate that the pins are negative-true logic.

PIN DESCRIPTIONS

| Pin Name | Description |
|-----------------------------------|---|
| CE# | Chip enable (input, negative logic) Latches an address by low input, activates the FeRAM, and enables a read or write operation. |
| OE# | Output enable (input, negative logic) The FeRAM is in read mode when the FeRAM is active and this pin is low, and data is output after the specified time. |
| WE# | Write enable (input, negative logic) The FeRAM is in write mode when the FeRAM is active and this pin is low, and data is capture at the timing of WE#="H" or CE#="H", whichever is earlier. |
| A14 to A0 | Address (input) The FeRAM captures an address at the timing when CE#="L" is established. |
| DQ7 to DQ0 | 3-state data bus (input/output) Outputs data in the read mode, and captures data in the write mode. |
| V _{CC} , V _{SS} | Power supply Apply the specified voltage to V _{CC} . Connect V _{SS} to ground. |

TRUTH TABLE

| Operating Mode | CE# | WE# |
|-----------------|-----|-----|
| Standby Mode | H | X |
| Address Latched | ↓ | X |
| Read Mode | L | H |
| Write Mode | L | ↓ |

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Note |
|--|---------------------|----------|----------------|------|--------------------------|
| | | Min. | Max. | | |
| Pin Voltage (Input Signal) | V_{IN} | -0.5 | $V_{CC} + 0.5$ | V | |
| Pin Voltage (Input/Output Voltage) | V_{INQ}, V_{OUTQ} | -0.5 | $V_{CC} + 0.5$ | V | |
| Power Supply Voltage | V_{CC} | -0.5 | 4.6 | V | |
| Storage Temperature (Extended Temperature Version) | T_{stg} | -55 | 125 | °C | |
| Operating Temperature (Extended Temperature Version) | T_{opr} | -40 | 85 | °C | |
| Power Dissipation | P_D | 1,000 | | mW | |
| Allowable Input Current | I_{IN} | ± 20 | | mA | $T_a = 25^\circ\text{C}$ |
| Allowable Output Current | I_{OUT} | ± 20 | | mA | $T_a = 25^\circ\text{C}$ |

Note:

The application of stress (voltage, current, or temperature) that exceeds the absolute maximum rating may damage the device. Therefore, do not allow actual characteristics to exceed any one parameter ratings

Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Unit | Note |
|--|----------|---------------------|----------------------|------|------|
| Power Supply Voltage | V_{CC} | 3.0 | 3.3 | V | |
| Ground Voltage | V_{SS} | 0.0 | 0.0 | V | |
| Input High Voltage | V_{IH} | $V_{CC} \times 0.8$ | $V_{CC} + 0.3$ | V | 1 |
| Input Low Voltage | V_{IL} | -0.3 | $V_{CC} \times 0.15$ | V | 2 |
| Operating Temperature (Extended Temperature Version) | T_a | -40 | 85 | °C | |

Notes:

1. Overshoots with the pulse width of 20 ns or less and the voltage of $V_{CC} + 1.0$ V or less are allowed.
2. Undershoots with the pulse width of 20 ns or less and the voltage of -1.0 V or more are allowed.

Capacitance

| Parameter | Symbol | Min. | Max. | Unit | Note |
|--------------------------|-----------|------|------|------|------|
| Input Capacitance | C_{IN} | — | 6 | pF | 1 |
| Input/Output Capacitance | C_{OUT} | — | 8 | pF | 1 |

Note:

Sampling value. Measurement conditions are $V_{IN} = V_{OUT} = \text{GND}$, $f = 1\text{MHz}$, and $T_a = 25^\circ\text{C}$

DC Characteristics

(Under recommended operating conditions)

| Parameter | Symbol | Condition | Min. | Max. | Unit | Note |
|----------------------------------|-----------|---|----------------------|----------------------|---------------|------|
| Output High Voltage | V_{OH} | $I_{OH} = -2 \text{ mA}$ | $V_{CC} \times 0.85$ | — | V | |
| | | | | | | |
| Output Low Voltage | V_{OL} | $I_{OL} = 2 \text{ mA}$ | — | $V_{CC} \times 0.15$ | V | |
| | | | | | | |
| Input Leakage Current | I_{LI} | — | -10 | 10 | μA | |
| Output Leakage Current | I_{LO} | — | -10 | 10 | μA | |
| Power Supply Current (Standby) | I_{CCS} | $V_{IN} = 0.2\text{V}$ or $V_{CC}-0.2\text{V}$, $CE\# = V_{CC}-0.2\text{V}$ $I_{OUT} = 0 \text{ mA}$ | — | 400 | μA | |
| Power Supply Current (Operating) | I_{CCA} | Read Cycle, $t_{RC} = \text{Min.}$ $V_{IN} = 0.2\text{V}$ or $V_{CC}-0.2\text{V}$, $CE\# = 0.2\text{V}$, $I_{OUT} = 0 \text{ mA}$ | — | 10 | mA | 1 |

Note:

1. Average current. Address change must be one time or less during time t_{RC} .

Read/Write Cycles and Data Retention

(Under recommended operating conditions)

| Parameter | Min. | Max. | Unit | Note |
|------------------|-----------|------|-------|------|
| Read/Write Cycle | 10^{12} | — | Cycle | 1 |
| Data Retention | 10 | — | Year | |

Notes:

1. This is applicable to the read cycle, write cycle, and CE-only cycle counts.
This is the cycle count per bit (for one address).

AC Characteristics (Read Cycle)

(Under recommended operating conditions)

| Parameter | Symbol | -70 | | Unit | Note |
|----------------------------------|------------|------|------|------|------|
| | | Min. | Max. | | |
| Address Set-up Time | t_{AVEL} | 5 | — | ns | |
| Address Hold Time (CE#) | t_{ELAX} | 10 | — | ns | |
| CE# High Pulse Width | t_{EHEL} | 80 | — | ns | |
| Output Hold Time (CE#) | t_{EHQX} | 5 | — | ns | |
| Output High Impedance Time (CE#) | t_{EHQZ} | — | 25 | ns | |
| CE# Active Time | t_{ELEH} | 70 | 2000 | ns | |
| Read Cycle Time (CE# cycle Time) | t_{ELEL} | 150 | — | ns | |
| CE# Access Time | t_{ELQV} | — | 70 | ns | 1 |
| Output Low Impedance Time (CE#) | t_{EHQX} | 5 | — | ns | |
| Output Hold Time (OE#) | t_{GHQX} | 5 | — | ns | |
| Output High Impedance Time (OE#) | t_{GHQZ} | — | 25 | ns | |
| OE# Access Time | t_{GLQV} | — | 40 | ns | 1 |
| Output Low Impedance Time (OE#) | t_{GLQX} | 5 | — | ns | |

Notes:

The read data is output at the point where all of the maximum values of t_{ELQV} and t_{GLQV} are satisfied.

AC Characteristics (Write Cycle)

(Under recommended operating conditions) Note 1

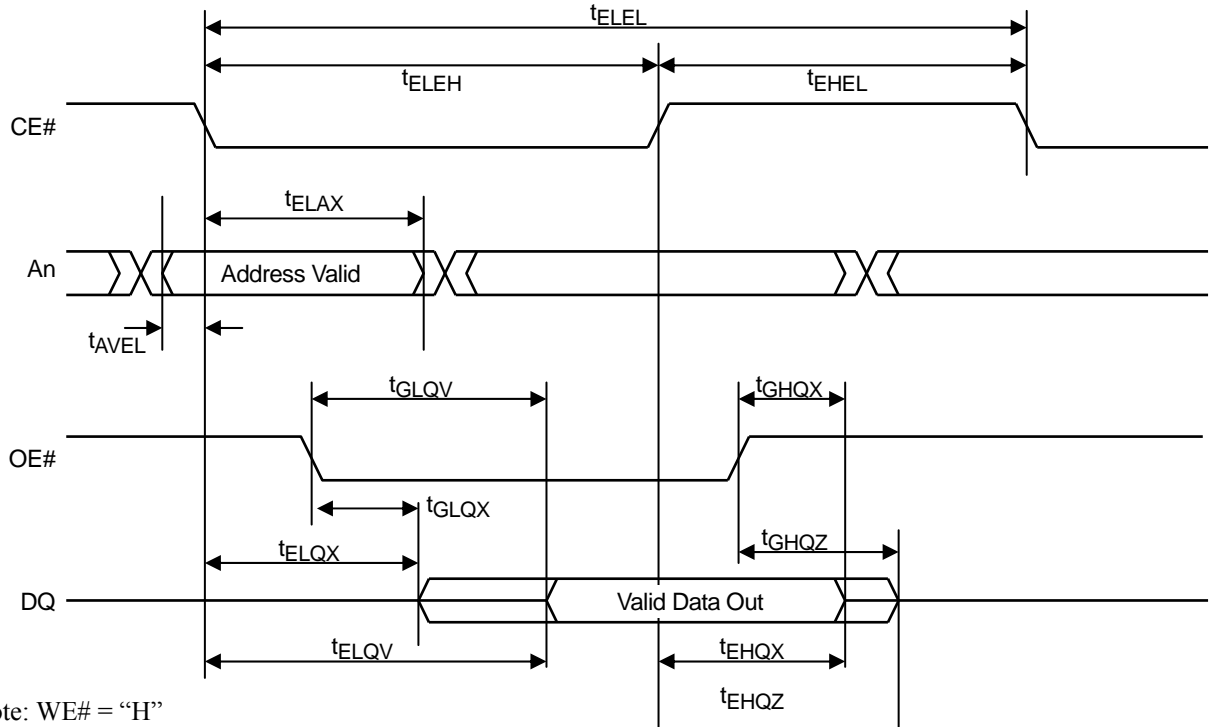
| Parameter | Symbol | -70 | | Unit | Note |
|--|-------------------|------|------|------|------|
| | | Min. | Max. | | |
| Address Set-up Time | t_{AVEL} | 5 | — | ns | |
| Data Set-up Time (WE#) | t_{DVWH} | 20 | — | ns | |
| Data Set-up Time (CE#) | t_{DVEH} | 40 | — | ns | |
| Address Hold Time (CE#) | t_{ELAX} | 10 | — | ns | |
| Data Hold Time (CE#) | t_{EHDX} | 0 | — | ns | |
| CE# High Pulse Width | t_{EHEL} | 80 | — | ns | |
| CE# Active Time | t_{ELEH} | 70 | 2000 | ns | |
| Write Cycle Time (CE# Cycle Time) | t_{ELEL} | 150 | — | ns | |
| Write Command Set-up Time (CE# to WE#) | t_{ELWH} | 70 | — | ns | |
| Data Hold Time (WE#) | t_{WHDX} | 0 | — | ns | |
| Write Command Pulse Width | t_{WLWH} | 40 | — | ns | |
| WE# Set-up Time (CE#) | t_{ELWL} | 0 | — | ns | 1 |
| WE# Hold Time (CE#) | t_{WHEH} | 0 | — | ns | 1 |

Notes:

“CE# controlled WRITE” mode or “OE# controlled WRITE” mode is decided by the relationship between CE# and OE#.

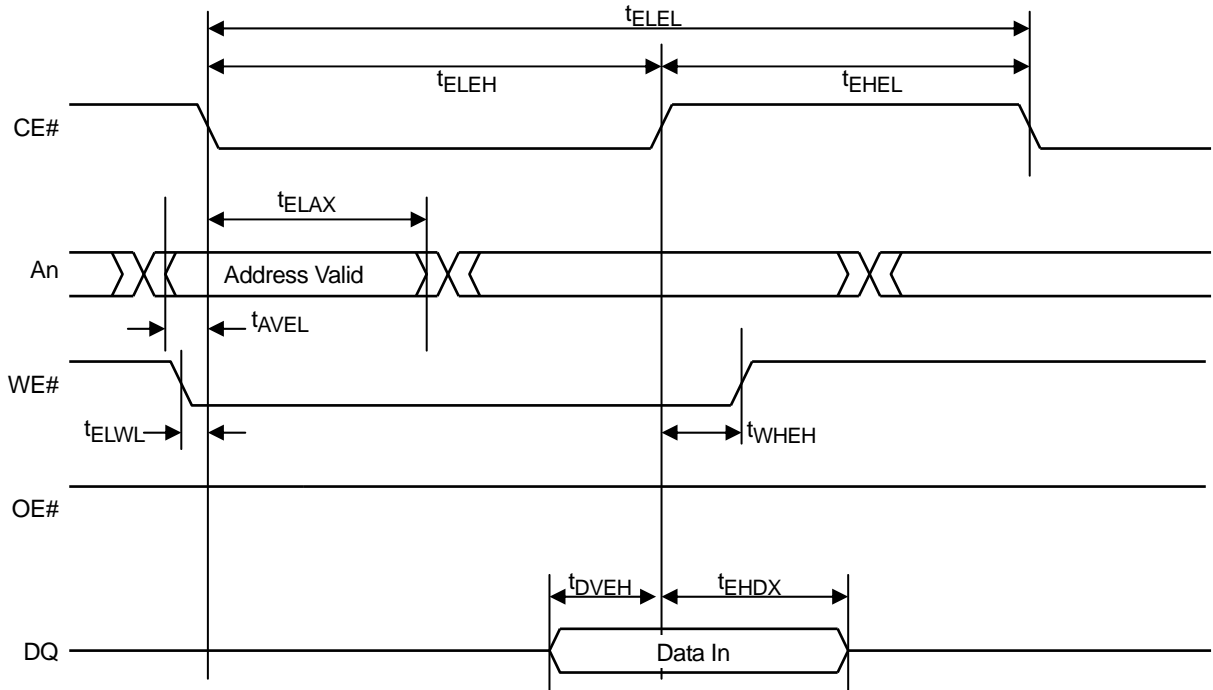
Timing Diagrams

•Read cycle

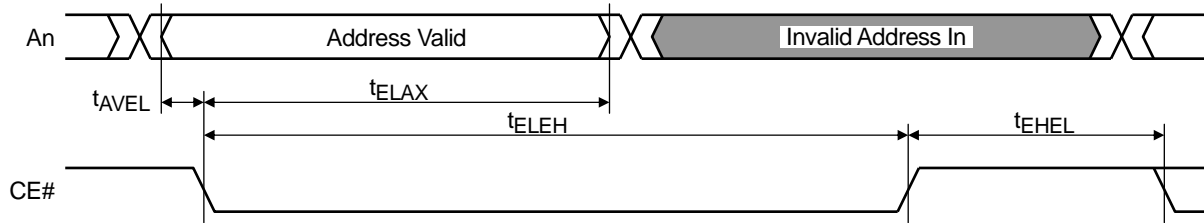


Note: WE# = "H"

•Write cycle



•CE-Only Cycle



Note: OE# = "H", WE# = "H", DQ = High-Z

•Power-On and Power-Off Characteristics

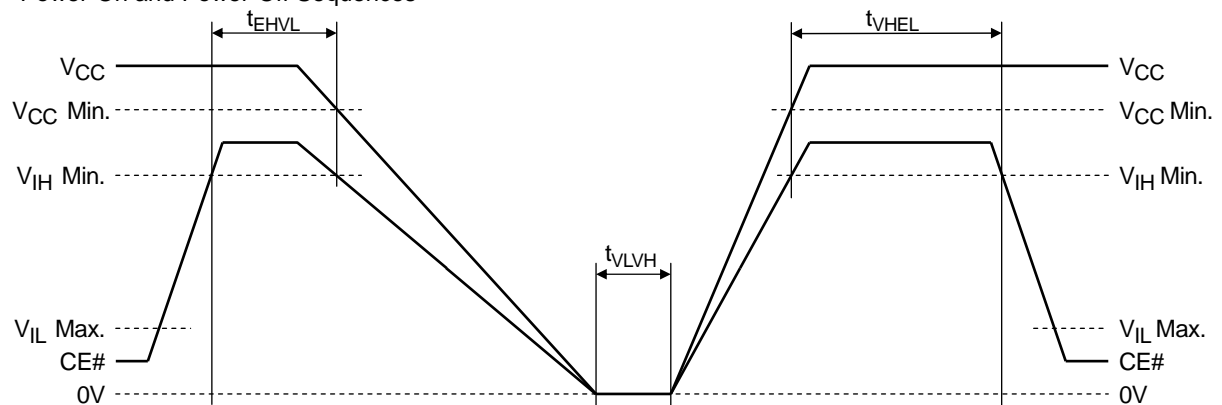
(Under recommended operating conditions)

| Parameter | Symbol | Min. | Max. | Unit | Note |
|------------------------------|------------|------|------|---------|------|
| Power-On CE# High Hold Time | t_{VHEL} | 50 | — | μ s | 1, 2 |
| Power-Off CE# High Hold Time | t_{EHVL} | 100 | — | ns | 1 |
| Power-On Interval Time | t_{VLVH} | 1 | — | μ s | 2 |

Notes:

1. To prevent an erroneous operation, be sure to maintain CE#="H", and set the FeRAM in an inactive state (standby mode) before and after power-on and power-off.
2. Powering on at the intermediate voltage level will cause an erroneous operation; thus, be sure to power up from 0 V.
3. Enter all signals at the same time as power-on or enter all signals after power-on.

•Power-On and Power-Off Sequences



REVISION HISTORY

| Document No. | Date | Page | | Description |
|----------------|---------------|------------------|-----------------|--|
| | | Previous Edition | Current Edition | |
| PEDR48V256A-01 | Mar. 30, 2010 | – | – | Preliminary edition 1 from PJDR48V256A-05 |
| PEDR48V256A-02 | Aug. 26, 2010 | 1 | 1 | Package code name |
| | | 1,4,5 | 1,4,5 | Input Voltage 2.0/0.8 ⇒ V _{CC} x 0.8 / V _{CC} x 0.2 |
| PEDR48V256A-03 | Dec. 02, 2010 | 4 | 4 | Input Voltage V _{IL} V _{CC} x 0.2 ⇒ V _{CC} x 0.15 |
| PEDR48V256A-04 | Mar. 04, 2011 | 1,2,4 | 1,2,4 | Pin name VDD ⇒ VCC temperature version ⇒ Extended version |
| PEDR48V256A-05 | Sep. 05, 2011 | 8,9 10 | 8,9 10 | OE# wave in Timing chart Input signal state in power-on |
| PEDR48V256A-06 | Oct. 17, 2011 | 1-12 | 1-12 | Changed corporate name and logo to LAPIS Semiconductor. |

NOTES

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