



N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)	Q _g (Typ.)		
20	0.396 at V _{GS} = 4.5 V	0.5			
	0.456 at $V_{GS} = 2.5 \text{ V}$	0.2	0.75		
	0.546 at V _{GS} = 1.8 V	0.2	0.75		
	1.100 at V _{GS} = 1.5 V	0.05			

FEATURES

TrenchFET® Power MOSFET: 1.2 V Rated



Gate-Source ESD Protected: 1000 V

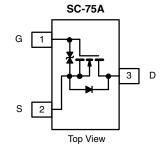
Material categorization: For definitions of compliance please see www.vishav.com/doc?99912

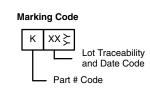


HALOGEN FREE

APPLICATIONS

- Load/Power Switching for Portable Devices
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- **Battery Operated Systems**
- **Power Supply Converter Circuits**





Ordering Information: Si1012CR-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS	S (T _A = 25 °C, unl	ess otherwise n	ioted)	
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	v	
O-ations - Davis Onward (T., 450,00)3	T _A = 25 °C	I_	0.63 ^{a, b}	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C	I _D	0.5 ^{a, b}	Α
Pulsed Drain Current (t = 300 μs)		I _{DM}	2	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	0.2 ^{a, b}	A
M	T _A = 25 °C	D	0.24 ^{a, b}	W
Maximum Power Dissipation ^a	T _A = 70 °C	P _D	0.15 ^{a, b}	VV
Operating Junction and Storage Temperature Ra	T _J , T _{stq}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Mariana Indiana An Analisa da	t ≤ 5 s	R _{thJA}	440	530	°C/W
Maximum Junction-to-Ambient ^D	Steady State		540	650	C/VV

a. Surface mounted on 1" x 1" FR4 board.

b. t = 5 s.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V, } I_D = 250 \mu\text{A}$	20			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		17		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	ι _D = 250 μΑ		- 1.8			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.4		1	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 30		
		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$			± 1		
Zava Cata Valtaga Dvain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μΑ	
Zero Gate Voltage Drain Current		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			10	1	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	2			Α	
		$V_{GS} = 4.5 \text{ V}, I_D = 0.6 \text{ A}$		0.330	0.396	Ω	
	D	$V_{GS} = 2.5 \text{ V}, I_D = 0.3 \text{ A}$		0.380	0.456		
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 1.8 \text{ V}, I_D = 0.3 \text{ A}$		0.420	0.546		
		$V_{GS} = 1.5 \text{ V}, I_D = 0.05 \text{ A}$		0.720	1.100		
Forward Transconductance	9 _{fs}	$V_{DS} = 10 \text{ V}, I_D = 0.5 \text{ A}$		7.5		S	
Dynamic ^b							
Input Capacitance	C _{iss}			43			
Output Capacitance	C _{oss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		14		pF	
Reverse Transfer Capacitance	C _{rss}			8			
Tatal Cata Charres	Qg	$V_{DS} = 10 \text{ V}, V_{GS} = 8 \text{ V}, I_D = 0.6 \text{ A}$		1.3	2		
Total Gate Charge				0.75	1.2	nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 0.6 \text{ A}$		0.15			
Gate-Drain Charge	Q_{gd}			0.13			
Gate Resistance	R _g	f = 1 MHz	2.4	12.2	24.4	Ω	
Turn-On Delay Time	t _{d(on)}			11	20		
Rise Time	t _r	V_{DD} = 10 V, R_L = 20 Ω		16	24	20	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 0.5$ A, V_{GEN} = 4.5 V, R_g = 1 Ω		26	39	ns	
Fall Time	t _f			11	20		
Drain-Source Body Diode Characterist	ics						
Pulse Diode Forward Current ^a	I _{SM}				2	Α	
Body Diode Voltage	V_{SD}	I _S = 0.5 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			10	15	ns	
Body Diode Reverse Recovery Charge	Q_{rr}	L = 0.5 A dl/dt = 100 A/···		2	4	nC	
Reverse Recovery Fall Time	t _a	$I_F = 0.5 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}$		5			
Reverse Recovery Rise Time		t _b		5		ns	

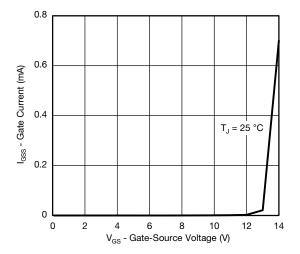
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.

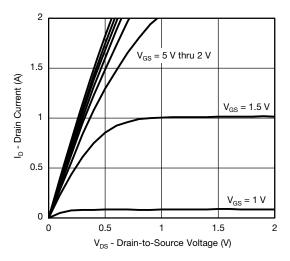
b. Guaranteed by design, not subject to production testing.



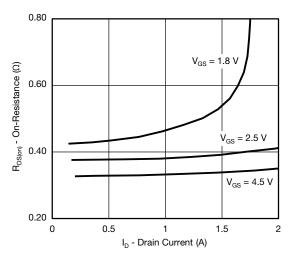
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



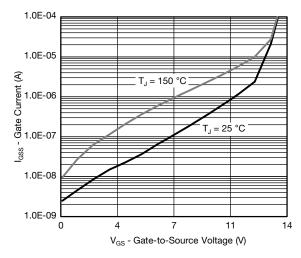
Gate Current vs. Gate-Source Voltage



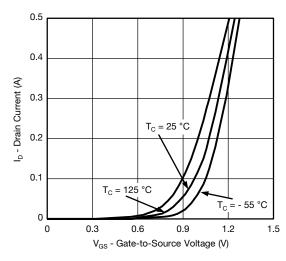
Output Characteristics



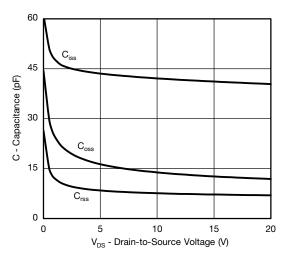
On-Resistance vs. Drain Current



Gate Current vs. Gate-Source Voltage



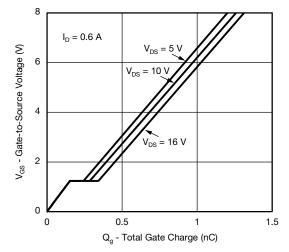
Transfer Characteristics



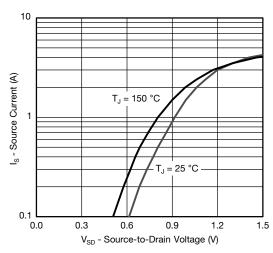
Capacitance

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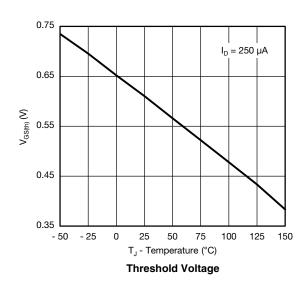
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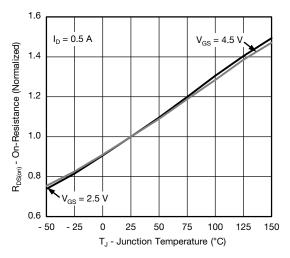




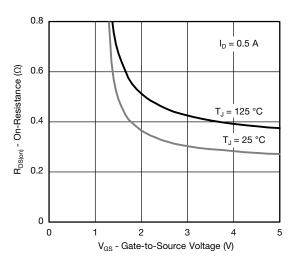


Soure-Drain Diode Forward Voltage

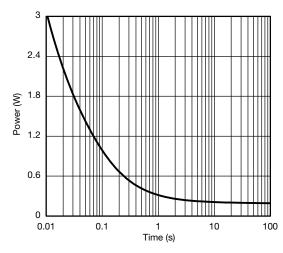




On-Resistance vs. Junction Temperature



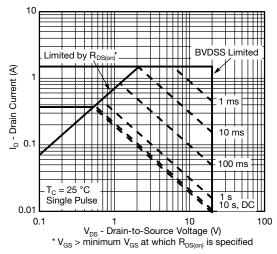
On-Resistance vs. Gate-to-Source Voltage



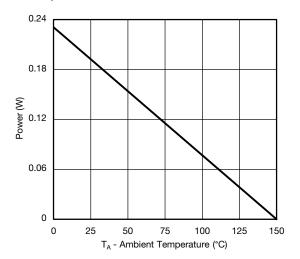
Single Pulse Power, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

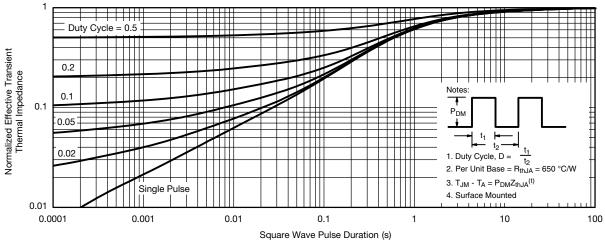






Power Derating, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

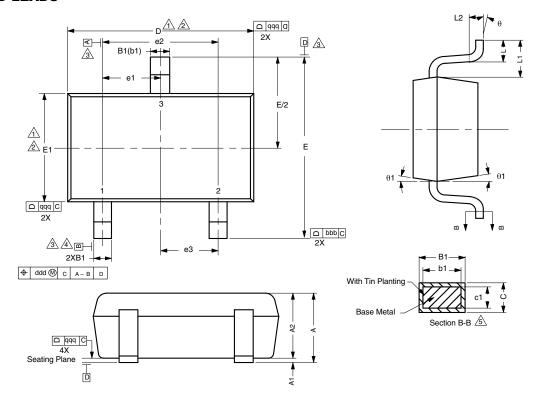


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67519.



SC-75A: 3-LEADS



Notes

Dimensions in millimeters will govern.

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.10 mm per end. Dimension E1 does not include Interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.10 mm per side.

Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interelead flash, but including any mismatch between the top and bottom of the plastic body.

2\Datums A, B and D to be determined 0.10 mm from the lead tip.

4 Terminal positions are shown for reference only.

These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIMENSIONS	TOLERANCES
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.10

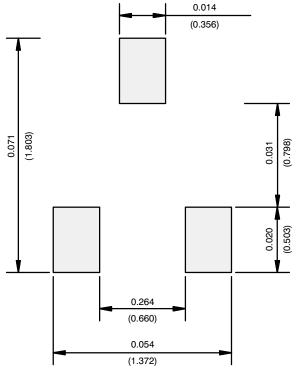
DIM.	MIN.	NOM.	MAX.	NOTE
Α	-	-	0.80	
A ₁	0.00	-	0.10	
A ₂	0.65	0.70	0.80	
B ₁	0.19	-	0.24	5
b ₁	0.17	-	0.21	
С	0.13	-	0.15	5
C ₁	0.10	-	0.12	5
D	1.48	1.575	1.68	1, 2
E	1.50	1.60	1.70	
E ₁	0.66	0.76	0.86	1, 2
e ₁				
e ₂	1.00 BSC			
e ₃				
L	0.15	0.205	0.30	
L ₁	0.40 REF			
L ₂	0.15 BSC			
θ	0°	-	8°	
θ_1	4°	-	10°	
ECN: E11-	2210-Rev. D,	08-Aug-11		

ECN: E11-2210-Rev. D, 08-Aug-11

DWG: 5868



RECOMMENDED MINIMUM PADS FOR SC-75A: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index

APPLICATION NOTE



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