SM802117



ClockWorks™ GbE (125MHz) Ultra-Low Jitter, LVPECL Frequency Synthesizer

General Description

The SM802117 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution for GbE Ethernet clock signals. It is based upon a unique patented RotaryWave® architecture that provides very low phase noise.

The device operates from a 3.3V or 2.5V power supply and synthesizes LVPECL output clocks at 125MHz. There are two differential clock outputs each with it's own OE pin allowing them to be disabled independently. The SM802117 accepts a 25 MHz crystal or LVCMOS reference clock.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

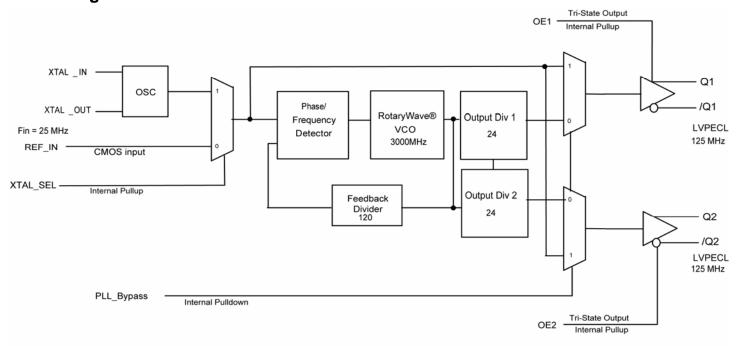
Features

- Generates one or two LVPECL clock outputs at 125MHz
- 2.5V or 3.3V operating range
- Typical phase jitter @ 125MHz (1.875MHz to 20MHz): 115fs
- Industrial temperature range (–40°C to +85°C)
- Green, RoHS, and PFOS compliant
- Available in 24-pin 4mm × 4mm QFN package

Applications

• Gigabit Ethernet - PHY

Block Diagram



ClockWorks is a trademark of Micrel, Inc RotaryWave is a registered trademark of Multigig, Inc.

Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax + 1 (408) 474-1000 • http://www.micrel.com

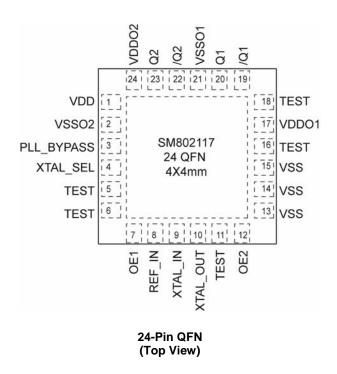
Ordering Information

| Part Number | Marking | Shipping | Temperature Range | Package |
|---------------|---------|---------------|-------------------|------------|
| SM802117UMG | 802117 | Tube | –40°C to +85°C | 24-Pin QFN |
| SM802117UMGTR | 802117 | Tape and Reel | –40°C to +85°C | 24-Pin QFN |

Note:

1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration



Pin Description

| Pin Number | Pin Name | Pin Type | Pin Level | Pin Function |
|--------------------------|------------|-----------------|------------------------------------|--|
| 19, 20 | /Q1, Q1 | O (DIE) | LVPECL | Differential Clock Output from Bank 1 |
| 19, 20 | /Q1, Q1 | O, (DIF) | LVFECL | 125MHz |
| 22, 23 | /Q2, Q2 | O (DIE) | LVDECL | Differential Clock Output from Bank 2 |
| 22, 23 | /Q2, Q2 | O, (DIF) LVPECL | | 125MHz |
| 24 | VDDO2 | PWR | | Power Supply for Output Bank 2 |
| 2 | VSSO2 | PWR | | Power Supply Ground for Output Bank 2 |
| | | | LVOVOO | PLL Bypass, Selects Output Source |
| 3 | DIL DVDACC | 1 (05) | | 0 = Normal PLL Operation |
| 3 | PLL_BYPASS | I, (SE) | LVCMOS | 1 = Output from Input Reference Clock or Crystal |
| | | | | 45KΩ pull-down |
| 4 VIAL CEL L (CE) LVCMCC | | LVCMOS | Selects PLL Input Reference Source | |
| 4 | XTAL_SEL | I, (SE) | LVCIVIOS | 0 = REF_IN, 1 = XTAL, 45KΩ pull-up |

Pin Description (Continued)

| Pin Name | Pin Type | Pin Level | Pin Function |
|----------|--|--|--|
| TEST | | | Factory Test pins, Do not connect anything to these pins. |
| VDD | PWR | | Core Power Supply |
| VSS | PWR | | Core Power Supply Ground |
| VDDO1 | PWR | | Power Supply for Output Bank 1 |
| VSSO1 | PWR | | Power Supply Ground for Output Bank 1 |
| REF_IN | I, (SE) | LVCMOS | Reference Clock Input |
| VTAL IN | L (CE) | orustal | Crystal Reference Input, no load caps needed. |
| ATAL_IN | I, (SE) | Crystai | See Fig. 5. |
| VTAL OUT | 0 (85) | orustal | Crystal Reference Output, no load caps needed. |
| XTAL_OUT | O, (SE) | Crystai | See Fig. 5. |
| OE1 | I, (SE) | LVCMOS | Output Enable, Q1 disables to tri-state, |
| | , , , | | 0 = Disabled, 1 = Enabled, 45KΩ pull-up |
| OE2 | I, (SE) | LVCMOS | Output Enable, Q2 disables to tri-state, 0 = Disabled, 1 = Enabled, 45ΚΩ pull-up |
| | TEST VDD VSS VDDO1 VSSO1 REF_IN XTAL_IN XTAL_OUT OE1 | TEST VDD PWR VSS PWR VDDO1 PWR VSSO1 PWR REF_IN I, (SE) XTAL_IN I, (SE) XTAL_OUT O, (SE) OE1 I, (SE) | TEST PWR VDD PWR VSS PWR VDD01 PWR VSS01 PWR REF_IN I, (SE) LVCMOS XTAL_IN I, (SE) crystal XTAL_OUT O, (SE) crystal OE1 I, (SE) LVCMOS |

Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal.

Crystal load capacitance is built inside the die so no external capacitance is needed. See the Selecting a Quartz crystal for the Clockworks Flex I Family of Precision Synthesizers application note for further details.

Contact Micrel's HBW applications group if you need assistance on selecting a suitable crystal for your application at hbwhelp@micrel.com.

Truth Table

| PLL_BYPASS | XTAL_SEL | INPUT | OUTPUT |
|------------|----------|--------|-------------|
| 0 | _ | - | PLL |
| 1 | _ | - | XTAL/REF_IN |
| _ | 0 | REF_IN | _ |
| _ | 1 | XTAL | _ |

SM802117 Micrel, Inc.

Absolute Maximum Ratings⁽¹⁾

| Supply Voltage (V _{DD} , V _{DDO1/2}) | +4.6V |
|---|----------------|
| Input Voltage (V _{IN}) | |
| Lead Temperature (soldering, 20sec.). | 260°C |
| Case Temperature | 115°C |
| Storage Temperature (T _s) | 65°C to +150°C |

Operating Ratings⁽²⁾

| Supply Voltage (V _{DD} , V _{DDO1/2}) | +2.375V to +3.465V |
|---|--------------------|
| Ambient Temperature (T _A) | 40°C to +85°C |
| Junction Thermal Resistance ⁽³⁾ | |
| QFN (θ_{JA}) | |
| Still-Air | 50°C/W |
| QFN (Ψ _{JB}) | |
| Junction-to-Board | 30°C/W |

DC Electrical Characteristics⁽⁴⁾

 V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

 $V_{DD} = 3.3V \pm 5\%, V_{DDO1/2} = 2.5V \pm 5\%$

 $T_A = -40^{\circ}C \text{ to } +85^{\circ}C.$

| Symbol | Parameter | Condition | Min. | Тур. | Max. | Units |
|---------------------------------------|---|--------------------|-------|------|-------|-------|
| V _{DD} , V _{DDO1/2} | 2.5V Operating Voltage | | 2.375 | 2.5 | 2.625 | V |
| V _{DD} , V _{DDO1/2} | 3.3V Operating Voltage | | 3.135 | 3.3 | 3.465 | V |
| I _{DD} | Supply current V _{DD} + V _{DDO} | 125MHz - 1 output | | 97 | 125 | mA |
| REF_IN XTAL_SEL = 0 Outputs open | 125MHz - 2 outputs | | 114 | 148 | mA | |
| I _{DD} | Supply current V _{DD} + V _{DDO} | 125MHz - 1 output | | 87 | 113 | mA |
| XTAL | XTAL_SEL = 1 Outputs open | 125MHz - 2 outputs | | 104 | 135 | mA |

LVPECL OUTPUT DC Electrical Characteristics (4)

 $V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

 V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 2.5V ±5%

 T_A = -40°C to +85°C. R_L = 50Ω to $V_{DDO}-2V$

| Symbol | Parameter | Condition | Min. | Тур. | Max. | Units |
|--------------------|----------------------|-----------|--------------------------|-------------------------|--------------------------|-------|
| V _{OH} | Output High Voltage | | V _{DDO} – 1.145 | V _{DDO} - 0.97 | V _{DDO} - 0.845 | V |
| V _{OL} | Output Low Voltage | | V _{DDO} – 1.945 | V _{DDO} – 1.77 | V _{DDO} – 1.645 | V |
| V _{SWING} | Output Voltage Swing | | 0.6 | 0.8 | 1.0 | V |

Note:

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. 3.
- The circuit is designed to meet the AC and DC specifications shown in the above table(s) after thermal equilibrium has been established.

LVCMOS (PLL_BYPASS, XTAL_SEL, OE1/2) DC Electrical Characteristics (4)

 V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_{A} = -40°C to +85°C.

| Symbol | Parameter | Condition | Min. | Тур. | Max. | Units |
|-----------------|--------------------|--|------|------|-----------------------|-------|
| V _{IH} | Input High Voltage | | 2 | | V _{DD} + 0.3 | V |
| V _{IN} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I _{IH} | Input High Current | $V_{DD} = V_{IN} = 3.465V$ | | | 150 | μΑ |
| I _{IL} | Input Low Current | V _{DD} = 3.465V, V _{IN} = 0V | -150 | | | μА |

REF_IN DC Electrical Characteristics(4)

 V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = -40°C to +85°C.

| Symbol | Parameter | Condition | Min. | Тур. | Max. | Units |
|-----------------|--------------------|--|------|------|-----------------------|-------|
| V _{IH} | Input High Voltage | | 1.1 | | V _{DD} + 0.3 | V |
| V _{IL} | Input Low Voltage | | -0.3 | | 0.6 | V |
| I _{IN} | Input Current | XTAL_SEL = V _{IL} , V _{IN} = 0V to V _{DD} | -5 | | 5 | μА |
| IIIN | mpat Garrent | XTAL_SEL = V _{IH} , V _{IN} = V _{DD} | | 20 | | μΑ |

Crystal Characteristics

| Parameter | Condition | Min. | Тур. | Max. | Units | |
|------------------------------------|-----------------|------|--------------------------------|------|-------|--|
| Mode of Oscillation | 10 to 12pF Load | F | Fundamental, Parallel Resonant | | | |
| Frequency | | | 25 | | MHz | |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω | |
| Shunt Capacitor, C0 | | | 1 | 5 | pF | |
| Correlation Drive Level | | | 10 | 100 | uW | |

AC Electrical Characteristics^(4, 5)

 $V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

 V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 2.5V ±5%

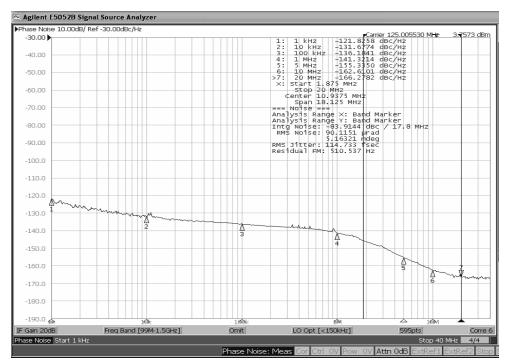
 T_A = $-40^{\circ}C$ to $+85^{\circ}C$. R_L = 50Ω to $V_{DDO}-2V$

| Symbol | Parameter | Condition | Min. | Тур. | Max. | Units |
|----------------------|---------------------------------|---|------|------------|------|-------|
| F _{OUT} | Output Frequency | | | 125 | | MHz |
| F _{REF} | Reference Input Frequency | | | 25 | | MHz |
| T_R/T_F | LVPECL Output Rise/Fall Time | 20% – 80% | 80 | 175 | 350 | ps |
| ODC | Output Duty Cycle | | 48 | 50 | 52 | % |
| T _{SKEW} | Output-to-Output Skew | Within bank. Note ⁶ | | | 45 | ps |
| T _{LOCK} | PLL Lock Time | | | | 20 | ms |
| T _{jit} (∅) | RMS Phase Jitter ⁽⁷⁾ | 125MHz Integration Range (1.875MHz – 20MHz) Integration Range (12kHz – 20MHz) | | 115 254 | | fs |
| | Spurious Noise Components | 25MHz | | -85 | | dBc |

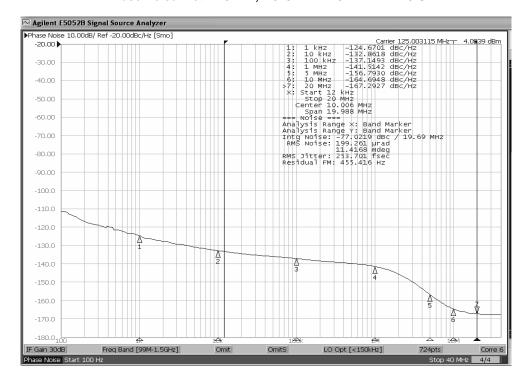
Notes:

- 5. All phase noise measurements were taken with an Agilent 5052B phase noise system.
- 6. Defined as skew between outputs at the same supply voltage and with equal load conditions and same frequency; Measured at the output differential crossing points.
- 7. Measured using 25MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz.

Phase Noise Plots

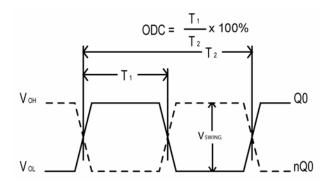


Phase Noise Plot: 125MHz, 1.875MHz - 20MHz 115fS



Phase Noise Plot: 125MHz, 12kHz – 20MHz 254fS

Timing Diagrams



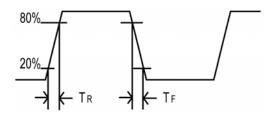


Figure 1. Duty Cycle Tlming

Figure 2. All Outputs Rise/Fall Time

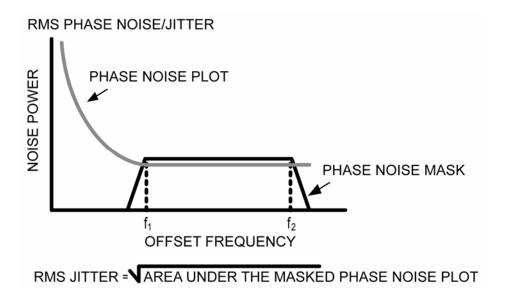


Figure 3. RMS Phase/Noise/Jitter

Input and Output Stage

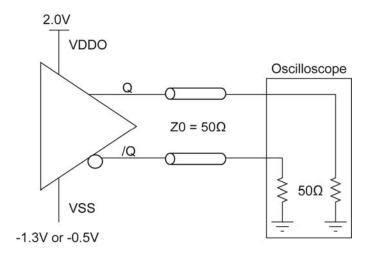


Figure 4. LVPECL Output Load and Test Circuit

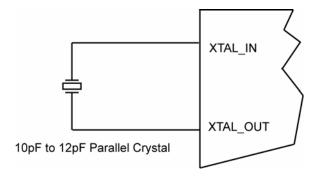
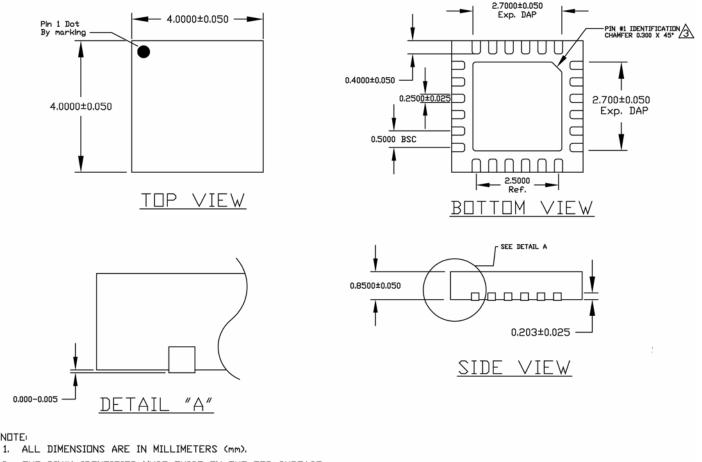


Figure 5. Crystal Input Interface

Package Information



NOTE:

THE PIN#1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.

3. CHAMFER STYLE PIN 1 IDENTIFIER ON BOTTOM SIDE

24-Pin QFN

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB www.micrel.com

Micrel makes no representations or warranties with respect to the accuracy or completeness of the information furnished in this data sheet. This information is not intended as a warranty and Micrel does not assume responsibility for its use. Micrel reserves the right to change circuitry, specifications and descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Micrel's terms and conditions of sale for such products. Micrel assumes no liability whatsoever, and Micrel disclaims any express or implied warranty relating to the sale and/or use of Micrel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is a Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2011 Micrel, Incorporated.