16-Bit 28-Pin Starter Development Board User's Guide

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Table of Contents

Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE on-line help. Select the Help menu, and then Topics to open a list of available on-line help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the 16-Bit 28-Pin Starter Development Board. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Warranty Registration
- Recommended Reading
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the 16-Bit 28-Pin Starter Development Board as a development tool to emulate and debug firmware on a target board. The manual layout is as follows:

- **Chapter 1. Introduction** – Introduces the 16-Bit 28-Pin Starter Development Board and provides a brief description of the hardware.
- **Chapter 2. Tutorial** – Details the step-by-step process for getting the 16-Bit 28-Pin Starter Development Board up and running with the MPLAB® ICD 2 in-circuit debugger.
- **Chapter 3. Demonstration Program** – Describes the operational functionality of the sample code that is preprogrammed into the dsPIC33F device.
- **Chapter 4. Development Hardware** – Describes the hardware on the 16-Bit 28-Pin Starter Development Board.
- **Appendix A. Drawings and Schematics** – Provides a diagram of the hardware layout, and schematic diagrams for the 16-Bit 28-Pin Starter Development Board.
- **Appendix B. Bill of Materials (BOM)** – Lists the parts used in the 16-Bit 28-Pin Starter Development Board.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

<table>
<tr><th>Description</th><th>Represents</th><th>Examples</th></tr>
<tr><td colspan="3">Arial font:</td></tr>
<tr><td rowspan="2">Italic characters</td><td>Referenced books</td><td>MPLAB® IDE User’s Guide</td></tr>
<tr><td>Emphasized text</td><td>...is the only compiler...</td></tr>
<tr><td rowspan="3">Initial caps</td><td>A window</td><td>the Output window</td></tr>
<tr><td>A dialog</td><td>the Settings dialog</td></tr>
<tr><td>A menu selection</td><td>select Enable Programmer</td></tr>
<tr><td>Quotes</td><td>A field name in a window or dialog</td><td>“Save project before build”</td></tr>
<tr><td>Underlined, italic text with right angle bracket</td><td>A menu path</td><td><u>File>Save</u></td></tr>
<tr><td rowspan="2">Bold characters</td><td>A dialog button</td><td>Click OK</td></tr>
<tr><td>A tab</td><td>Click the Power tab</td></tr>
<tr><td>‘bnnnn</td><td>A binary number where n is a digit</td><td>‘b00100, ‘b10</td></tr>
<tr><td>Text in angle brackets < ></td><td>A key on the keyboard</td><td>Press <Enter>, <F1></td></tr>
<tr><td colspan="3">Courier font:</td></tr>
<tr><td rowspan="6">Plain Courier</td><td>Sample source code</td><td>#define START</td></tr>
<tr><td>Filenames</td><td>autoexec.bat</td></tr>
<tr><td>File paths</td><td>c:\mcc18\h</td></tr>
<tr><td>Keywords</td><td>_asm, _endasm, static</td></tr>
<tr><td>Command-line options</td><td>-Opa+, -Opa-</td></tr>
<tr><td>Bit values</td><td>0, 1</td></tr>
<tr><td>Italic Courier</td><td>A variable argument</td><td>file.o, where file can be any valid filename</td></tr>
<tr><td>0xnnnn</td><td>A hexadecimal number where n is a hexadecimal digit</td><td>0xFFFF, 0x007A</td></tr>
<tr><td>Square brackets [ ]</td><td>Optional arguments</td><td>mcc18 [options] file [options]</td></tr>
<tr><td>Curly brackets and pipe character: { | }</td><td>Choice of mutually exclusive arguments; an OR selection</td><td>errorlevel {0|1}</td></tr>
<tr><td rowspan="2">Ellipses...</td><td>Replaces repeated text</td><td>var_name [, var_name...]</td></tr>
<tr><td>Represents code supplied by user</td><td>void main (void)
{ ...
}</td></tr>
</table>

WARRANTY REGISTRATION

Please complete the enclosed Warranty Registration Card and mail it promptly. Sending in the Warranty Registration Card entitles users to receive new product updates. Interim software releases are available at the Microchip web site.

RECOMMENDED READING

This user's guide describes how to use 16-Bit 28-Pin Starter Development Board. Other useful documents are listed below. The following Microchip documents are available and recommended as supplemental reference resources.

dsPIC30F Family Reference Manual (DS70046)

Consult this document for detailed information on dsPIC30F device operation. This reference manual explains the operation of the dsPIC30F DSC family architecture and peripheral modules, but does not cover the specifics of each device. Refer to the appropriate device data sheet for device-specific information.

dsPIC30F2010 Data Sheet (DS70118)

This data sheet summarizes the features of the dsPIC30F2010. It provides essential information needed to develop software for this device.

dsPIC30F/33F Programmer's Reference Manual (DS70157)

This manual is a software developer's reference for the dsPIC30F/33F 16-bit DSC family of devices. It describes the instruction set in detail and also provides general information to assist in developing software for the dsPIC30F/33F DSC family.

dsPIC33FJ12GP201/202 Data Sheet (DS70264)

This data sheet summarizes the features of the dsPIC33FJ12GP201/202. It provides essential information needed to develop software for these devices.

dsPIC33FJ12MC201/202 Data Sheet (DS70265)

This data sheet summarizes the features of the dsPIC33FJ12MC201/202. It provides essential information needed to develop software for these devices.

PIC24HJ12GP201/202 Data Sheet (DS70282)

This data sheet summarizes the features of the PIC24HJ12GP201/202. It provides essential information needed to develop software for these devices.

PIC24FJ64GA004 Data Sheet (DS39881)

This data sheet summarizes the features of the PIC24FJ64GA004. It provides essential information needed to develop software for this device.

MPLAB ASM30, MPLAB LINK30 and Utilities User’s Guide (DS51317)

This document details Microchip Technology’s language tools for dsPIC® DSC devices based on GNU technology. The language tools discussed are:

- MPLAB ASM30 Assembler
- MPLAB LINK30 Linker
- MPLAB LIB30 Archiver/Librarian
- Other Utilities

MPLAB C30 C Compiler User’s Guide (DS51284)

This document details the use of Microchip’s MPLAB C30 C Compiler for dsPIC DSC devices to develop an application. MPLAB C30 is a GNU-based language tool, based on source code from the Free Software Foundation (FSF). For more information about the FSF, see www.fsf.org.

Other GNU language tools available from Microchip are:

- MPLAB ASM30 Assembler
- MPLAB LINK30 Linker
- MPLAB LIB30 Librarian/Archiver

MPLAB IDE Simulator, Editor User’s Guide (DS51025)

Consult this document for more information pertaining to the installation and implementation of the MPLAB Integrated Development Environment (IDE) Software.

To obtain any of these documents, visit the Microchip web site at www.microchip.com.

THE MICROCHIP WEB SITE

Microchip provides online support via our web site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

DEVELOPMENT SYSTEMS CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

The Development Systems product group categories are:

- **Compilers** – The latest information on Microchip C compilers and other language tools. These include the MPLAB C18 and MPLAB C30 C compilers; MPASM™ and MPLAB ASM30 assemblers; MPLINK™ and MPLAB LINK30 object linkers; and MPLIB™ and MPLAB LIB30 object librarians.
- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB ICE 2000 and MPLAB ICE 4000.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debugger, MPLAB ICD 2.
- **MPLAB® IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB SIM simulator, MPLAB IDE Project Manager and general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include the MPLAB PM3 and PRO MATE® II device programmers and the PICSTART® Plus and PICkit™ 1 development programmers.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com

DOCUMENT REVISION HISTORY

Revision A (March 2007)

- Initial release of this document.

NOTES:

Chapter 1. Introduction

1.1 INTRODUCTION

The 16-Bit 28-Pin Starter Development Board serves as a development kit and evaluation tool for Microchip's 16-bit digital signal controllers and microcontrollers. Topics discussed in this chapter include:

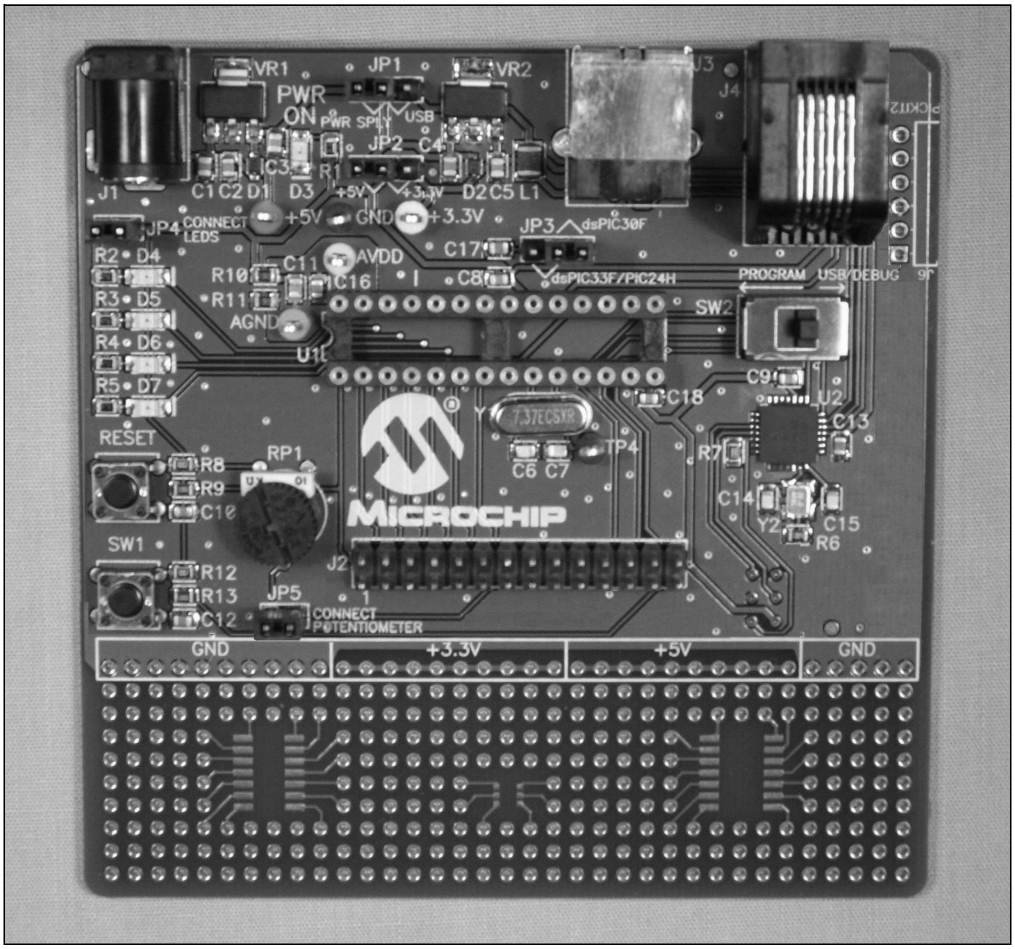
- Development Kit Contents
- Development Board Functionality and Features
- Demonstration Program
- Power Selection
- UART Communication Via USB
- Device Selection
- On-board Peripheral Selection

1.2 DEVELOPMENT KIT CONTENTS

The following items make up the 16-Bit 28-Pin Starter Development Board Development Kit:

- The 16-Bit 28-Pin Starter Development Board printed circuit board (see Figure 1-1)
- Preprogrammed dsPIC33FJ12GP202 device
- The 16-Bit 28-Pin Starter Development Board CD-ROM containing this manual, 16-bit documentation and demonstration program code

FIGURE 1-1: 16-BIT 28-PIN STARTER DEVELOPMENT BOARD



For information on the components used on the 16-Bit 28-Pin Starter Development Board, see **Chapter 4. "Development Hardware"**.

1.3 DEVELOPMENT BOARD FUNCTIONALITY AND FEATURES

The 16-Bit 28-Pin Starter Development Board is an easy-to-use tool that allows you to begin development with dsPIC30F/33F and PIC24 devices. The following capabilities are provided.

Development Board Power

- On-board +5V regulator or +3.3V regulator for V_{DD} and AV_{DD}
- USB power source or 9V DC power source input jack
- Power-on indicator LED

MPLAB ICD 2 Connections

- MPLAB ICD 2 programming connector

UART Communication Channel

- Single UART communication channel via USB bridge

Device Clocking

- 7.37 MHz crystal

Miscellaneous

- Reset push button for resetting the device
- Four LEDs for status indicators
- Push button switch (SW1)
- Potentiometer (RP1) for use with ADC
- All device I/O pins are brought out to a header for test point and prototyping access

1.4 DEMONSTRATION PROGRAM

The 16-Bit 28-Pin Starter Development Board is supplied with a pre-loaded device that demonstrates the following board functionality:

- Interrupt handling using Timer1 to toggle the LEDs
- UART functionality using the on-board USB to echo characters sent from a PC terminal programmed with a 9600 baud rate

Refer to **Chapter 3. “Demonstration Program”** for additional information.

1.5 POWER SELECTION

The 16-Bit 28-Pin Starter Development Board has the option of being powered by a 9V DC power supply or by the USB bus. The position of jumper JP1 determines which power source is used. Connect jumper pins 1 and 2 for the 9V power supply or jumper pins 2 and 3 for the USB.

In addition, jumper JP2 selects either a +5V or +3.3V power source for the targeted device. For dsPIC30F devices, connect jumper pins 1 and 2 for the +5V operation. For dsPIC33F and PIC24 devices, connect jumper pins 2 and 3 for the +3.3V operation.

1.6 UART COMMUNICATION VIA USB

The dsPIC30F/33F and PIC24 devices use an on-board PIC18 and USB interface for UART communications. With switch SW2 in the USB position, the PIC18 is connected to the target device, providing that the UART-to-USB bridge connection has been made. The appropriate USB device driver must be installed prior to UART-to-USB communication. See **Section 2.6.3 "Installing the USB Driver"** for details.

1.7 DEVICE SELECTION

The position of jumper JP3 determines which family of device (dsPIC30F or dsPIC33F/PIC24) to use.

1.8 ON-BOARD PERIPHERAL SELECTION

All on-board peripherals, such as LEDs, potentiometers, and the PIC18 (USB bridge), can be disconnected from the target devices via JP4, JP5 and SW2, respectively.

Chapter 2. Tutorial

2.1 INTRODUCTION

This chapter is a self-paced tutorial to get you started using the 16-Bit 28-Pin Starter Development Board. Topics covered in this chapter include:

- Tutorial Overview
- Equipment Needed
- Creating the Project
- Building the Code
- Programming the Chip
- Running the Application
- Debugging the Code
- Programming the Device for Stand-alone Operation
- Summary

2.2 TUTORIAL OVERVIEW

The tutorial program is located on the CD-ROM provided with the development kit, in the `demo_33F.c` file. The tutorial program is written in C code; therefore, the C30 compiler is required. This program echoes any characters that are sent to the 16-Bit 28-Pin Starter Development Board from the PC via the USB interface. In addition, the program toggles four LEDs. Timer1 is used to create a periodic interrupt, which toggles the LEDs.

The source file is used with a linker script file (`p33fj12gp202.gld`) and a header file (`p33fj12gp202.h`) to form a complete project. This simple project uses a single source code file; however, more complex projects might use multiple assembler and compiler source files as well as library files and precompiled object files.

> **Note:** The CD-ROM provided with the development kit also includes tutorial programs for dsPIC30F, dsPIC33F, and PIC24 devices. This chapter makes reference to the files used for dsPIC33F devices only. If you want to apply the tutorials to dsPIC30F or PIC24 devices, simply substitute the files mentioned in this text with the appropriate device-related file.

There are four steps to this tutorial:

1. Creating a project in MPLAB IDE.
2. Assembling and linking the code.
3. Programming the chip with the MPLAB ICD 2.
4. Debugging the code with the MPLAB ICD 2.

2.3 EQUIPMENT NEEDED

To complete this tutorial, you will need the following items:

1. 16-Bit 28-Pin Starter Development Board
2. 9V, 500 mA Plug-in Power Supply with barrel style plug (optional)
3. MPLAB ICD 2 In-Circuit Debugger
4. USB cable
5. PC running Microsoft Windows® with MPLAB IDE 7.52 or later
6. MPLAB C30 Compiler

2.4 CREATING THE PROJECT

The first step is to create a project and a workspace in MPLAB IDE. Typically, there is one project in one workspace.

A project contains the files needed to build an application (source code, linker script files, etc.) along with their associations to various build tools and build options.

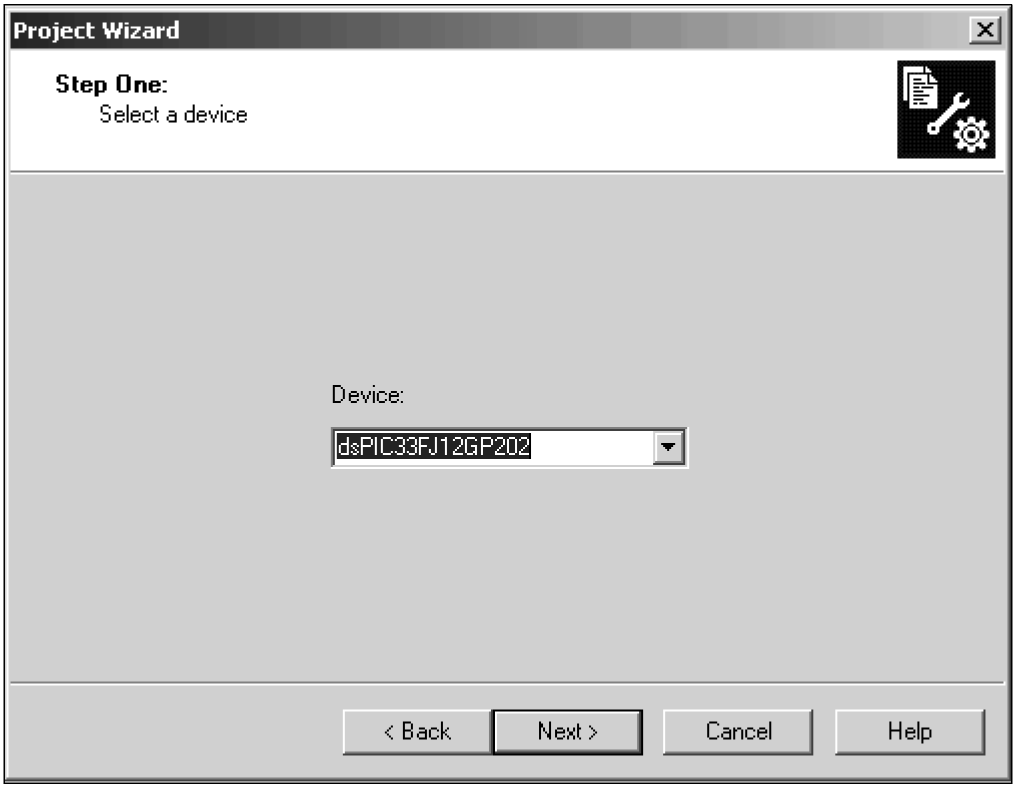
A workspace contains one or more projects and information on the selected device, debug tool and/or programmer, open windows and their location and other MPLAB IDE configuration settings.

MPLAB IDE contains a Project Wizard to help create new projects. Before starting, create a folder for the project files for this tutorial (`C:\Tutorial` is assumed in the instructions that follow). From the Example Code directory on the 16-Bit 28-Pin Starter Development Board Kit CD, copy the `demo_33F.c` file into the `C:\Tutorial` folder.

2.4.1 Select a Device

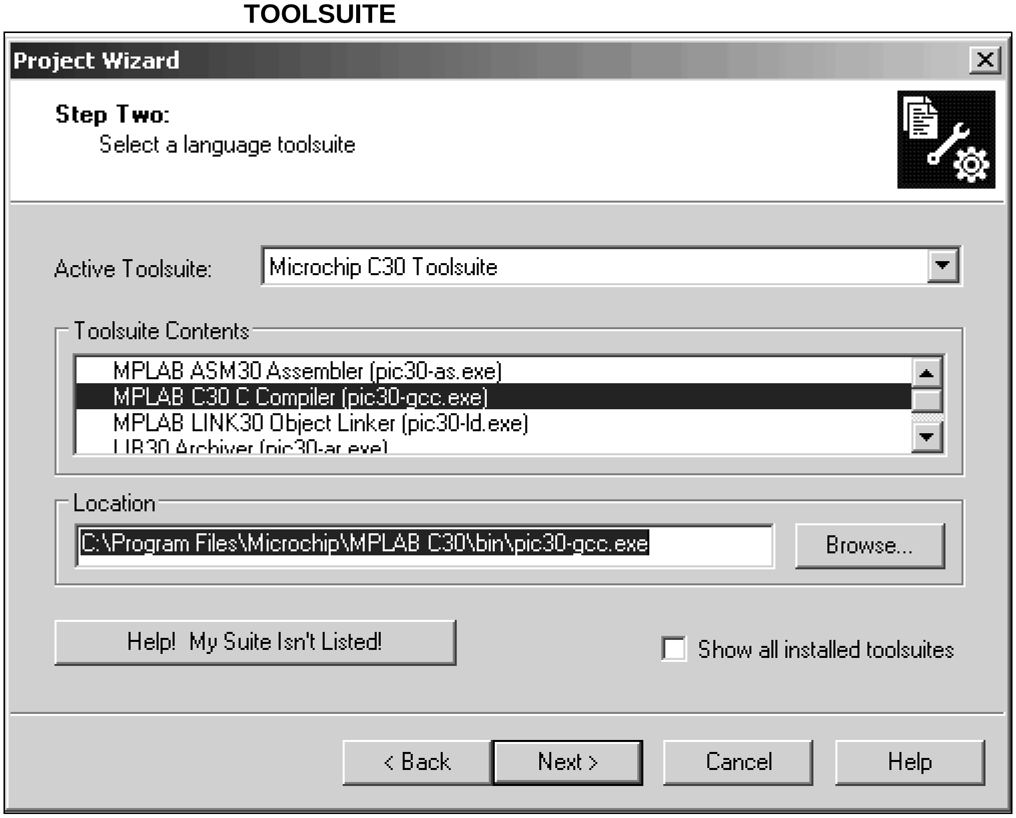
1. Start MPLAB IDE.
2. Close any workspace that might be open (*File>Close Workspace*).
3. From the *Project* menu, select *Project Wizard.*
4. From the Welcome screen, click **Next >** to display the Project Wizard Step One dialog (see Figure 2-1).

FIGURE 2-1: PROJECT WIZARD, STEP 1, SELECT A DEVICE



5. From the **Device:** pull-down list, select `dsPIC33FJ12GP202` and click **Next >**. The Project Wizard Step Two dialog appears.

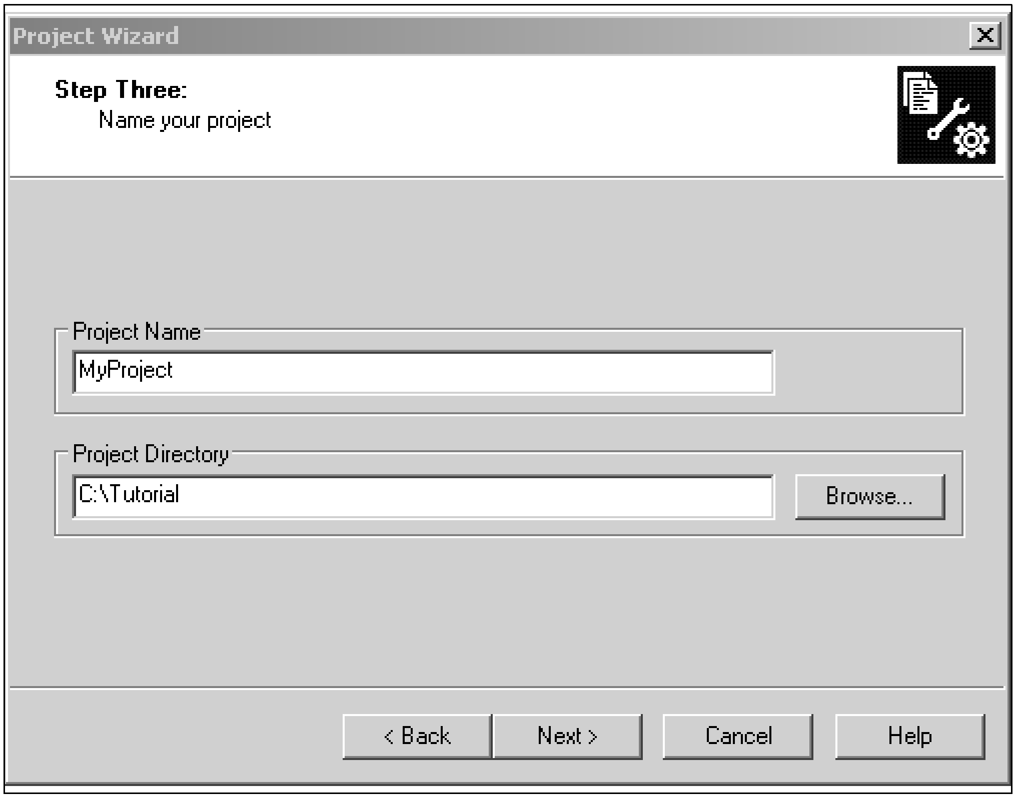
FIGURE 2-2: PROJECT WIZARD, STEP 2, SELECT LANGUAGE TOOLSUITE



2.4.2 Select Language Toolsuite

1. From the **Active Toolsuite:** pull-down menu, select **Microchip C30 Toolsuite**. This toolsuite includes the compiler and linker that will be used.
2. Click **Next >** to continue. The Project Wizard Step Three dialog appears.

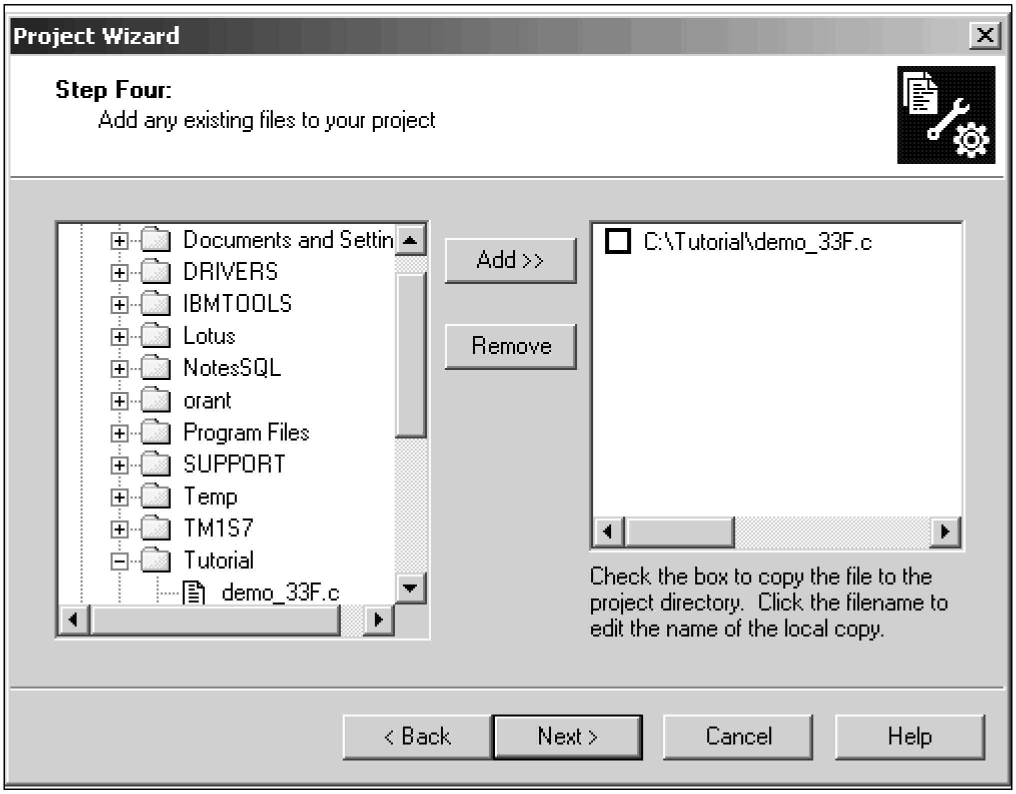
FIGURE 2-3: PROJECT WIZARD, STEP 3, NAME YOUR PROJECT



2.4.3 Name Your Project

1. In the **Project Name** text box, type `MyProject`.
2. Click **Browse...** and navigate to `C:\Tutorial\` to place your project in the Tutorial folder.
3. Click **Next >** to continue. The Project Wizard Step Four dialog appears.

FIGURE 2-4: PROJECT WIZARD, STEP 4, ADD FILES TO PROJECT

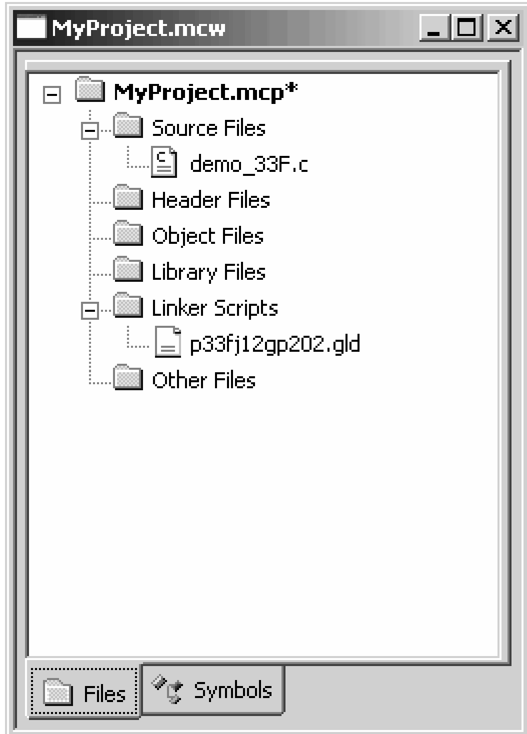


2.4.4 Add Files to the Project

1. Locate the `C:\Tutorial` folder and select the `demo_33F.c` file.
2. Click **Add >>** to include the file in the project.
3. Expand the `C:\Program Files\Microchip\MPLAB C30\support\gld` folder and select the `p33fj12gp202.gld` file.
4. Click **Add >>** to include this file in the project. There should now be two files in the project.
5. Click **Next >** to continue.
6. When the summary screen appears, click **Finish.**

After the Project Wizard completes, the MPLAB IDE project window shows the `demo_33F.c` file in the **Source Files** folder, and the `p33fj12gp202.gld` file in the **Linker Scripts** folder (see Figure 2-5).

FIGURE 2-5: MPLAB® IDE PROJECT WINDOW

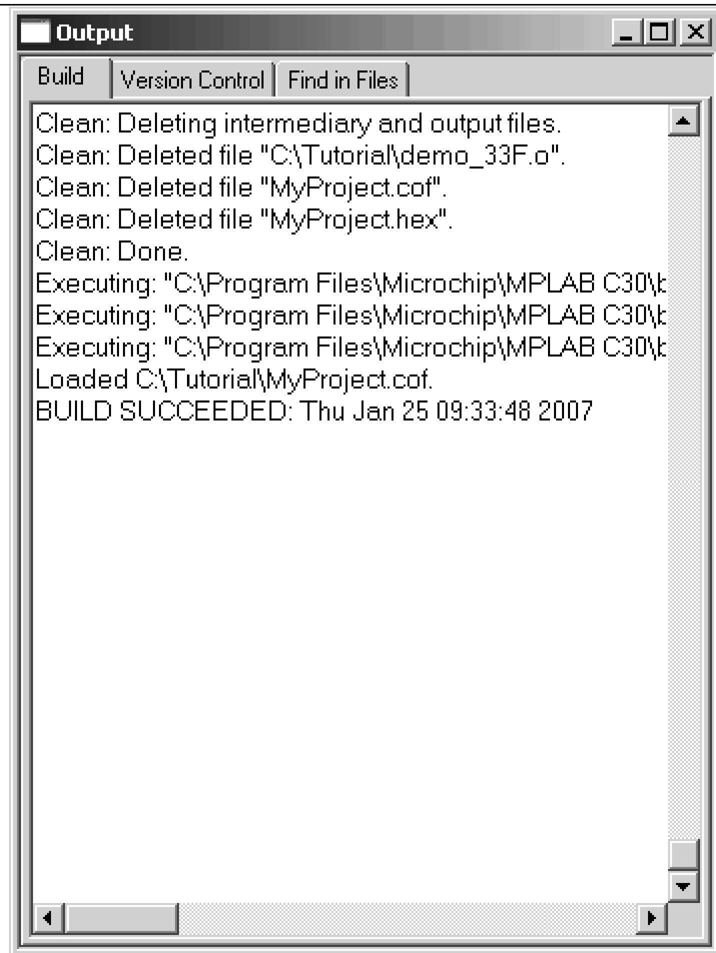


A project and workspace have now been created in MPLAB IDE. `MyProject.mcw` is the workspace file and `MyProject.mcp` is the project file. Double click the `demo_33F.c` file in the project window to open the file.

2.5 BUILDING THE CODE

1. From the *Project* menu select **Build All**. The Build Output window appears.

FIGURE 2-6: BUILD OUTPUT WINDOW



2. Observe the progress of the build.
3. When the BUILD SUCCEEDED message appears, you are ready to program the device.

2.6 PROGRAMMING THE CHIP

The MPLAB ICD 2 In-Circuit Debugger can be used to program and debug the device on the 16-Bit 28-Pin Starter Development Board. For this demonstration, we will use the **Debug** option, which will need to be selected. From the MPLAB IDE main screen, select the pull-down menu and change **Release** to **Debug**.

Note:	Before proceeding, make sure that the USB driver for the MPLAB ICD 2 has been installed on the PC (see the "*MPLAB ICD 2 User's Guide"*, (DS51331) for more details regarding the installation of the MPLAB ICD 2).

Use the following MPLAB IDE procedures to program the dsPIC30F/33F and PIC24 devices.

2.6.1 Set Up The Device Configuration

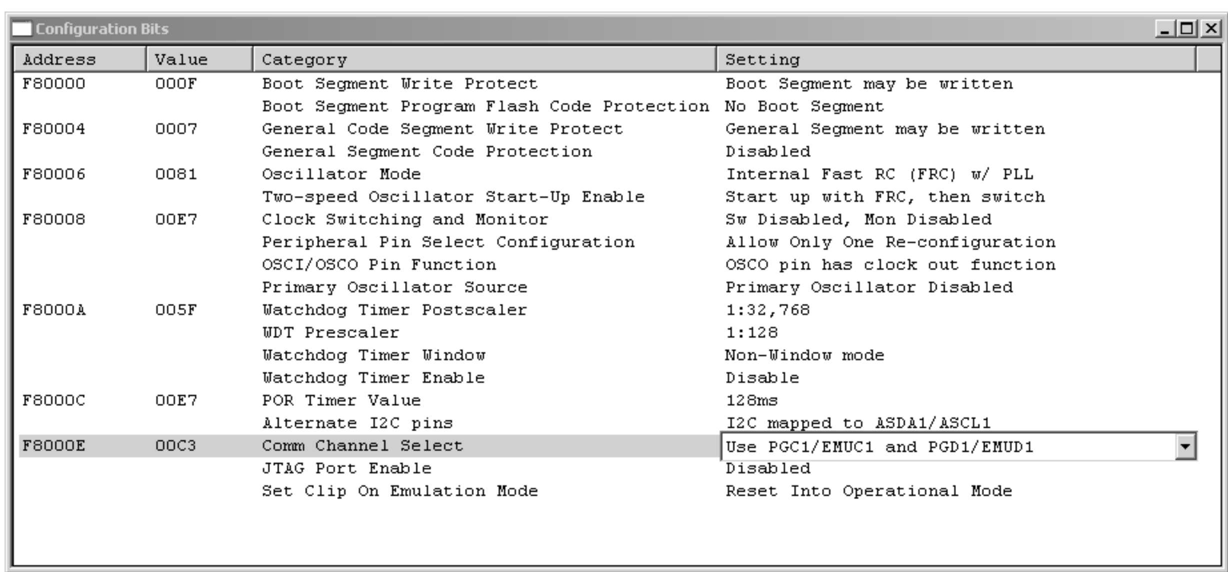
Use the *Configure>Configuration Bits* menu to display the configuration settings. The Configuration Bits window is shown in Figure 2-7.

The device Configuration bits determine global device operating parameters, such as clock source, brown out threshold voltage and so on. For this code example, the following configuration settings will be defined:

- The oscillator source will be set to internal FRC with PLL
- The primary oscillator will be disabled
- The watchdog timer will be disabled

Using these configuration settings will ensure that the device runs at maximum speed.

FIGURE 2-7: CONFIGURATION SETTINGS


Configuration Bits

Address	Value	Category	Setting
F80000	000F	Boot Segment Write Protect	Boot Segment may be written
		Boot Segment Program Flash Code Protection	No Boot Segment
F80004	0007	General Code Segment Write Protect	General Segment may be written
		General Segment Code Protection	Disabled
F80006	0081	Oscillator Mode	Internal Fast RC (FRC) w/ PLL
		Two-speed Oscillator Start-Up Enable	Start up with FRC, then switch
F80008	00E7	Clock Switching and Monitor	Sw Disabled, Mon Disabled
		Peripheral Pin Select Configuration	Allow Only One Re-configuration
		OSCI/OSCO Pin Function	OSCO pin has clock out function
		Primary Oscillator Source	Primary Oscillator Disabled
F8000A	005F	Watchdog Timer Postscaler	1:32,768
		WDT Prescaler	1:128
		Watchdog Timer Window	Non-Window mode
		Watchdog Timer Enable	Disable
F8000C	00E7	POR Timer Value	128ms
		Alternate I2C pins	I2C mapped to ASDA1/ASCL1
F8000E	00C3	Comm Channel Select	Use PGC1/EMUC1 and PGD1/EMUD1
		JTAG Port Enable	Disabled
		Set Clip On Emulation Mode	Reset Into Operational Mode

2.6.2 Select the MPLAB ICD 2 Communication Pins

All dsPIC30F/33F and PIC24 devices use a pair of I/O pins (PGCx/EMUCx and PGDx/EMUDx) for initially loading your application program into the device, and for communicating with the MPLAB ICD 2 In-Circuit Debugger. Typically, these pins can be used by your application program for other functions after your program is loaded into the device. However, these application functions are not available while you are connected to the MPLAB ICD 2 for debugging.

To circumvent this issue, most dsPIC30F/33F and PIC24 devices use one or more sets of alternate pins for MPLAB ICD 2 communication. These alternate pins are identified as EMUC*x* and EMUD*x*, where *x* designates the number of the pin pair. By selecting an alternate set of pins for the MPLAB ICD 2, you can safely use the original I/O pins for your application.

For this development board, the pin pairs, PGCx/EMUCx, on device pins 4, 5, 11 and 12 are used for debugging.

Note:	SW2 must be switched to the “Program” position for dsPIC30F devices when the application is being programmed into a device with MPLAB ICD 2. Once programming is complete, SW2 must be switched back to the “USB/Debug” position for UART communication via the USB bridge. See Figure 4-1 for the location of this switch.

To select the MPLAB ICD 2 communication pins:

1. On the Configuration Bits screen (Figure 2-7), go to the **Comm Channel Select** category.
2. In the **Setting** column, set this parameter to **Use PGC1/EMUC1 and PGD1/EMUD1**.

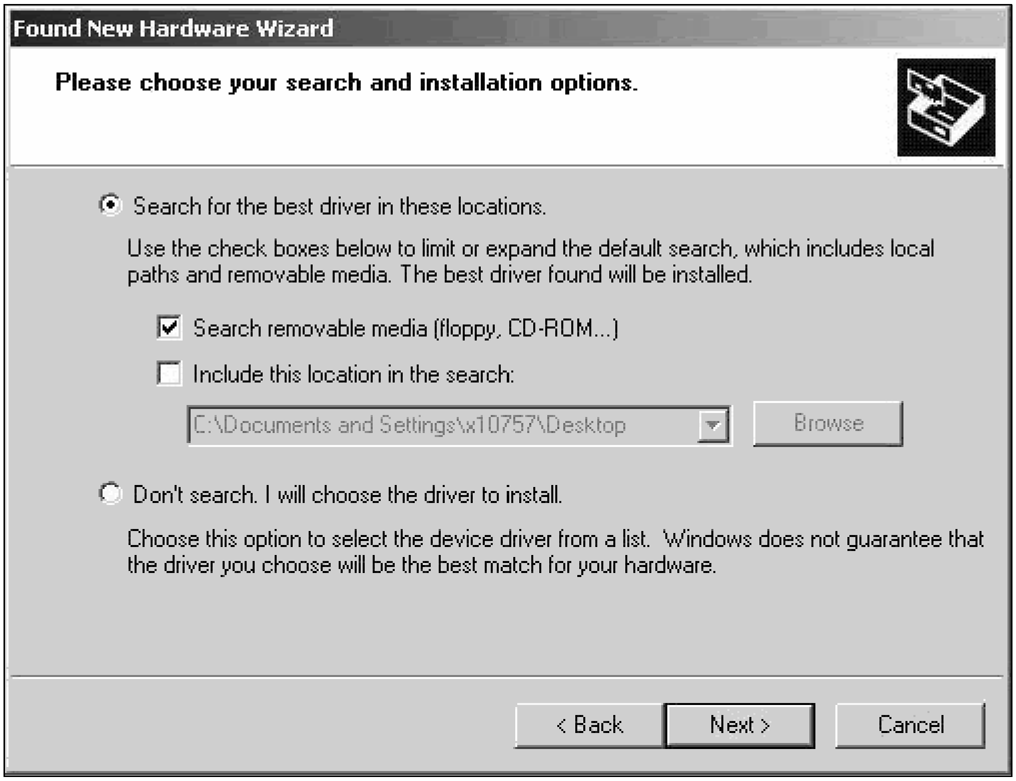
2.6.3 Installing the USB Driver

1. Apply power to the board. Refer to **Section 1.5 “Power Selection”** for details.
2. Select the dsPIC33F device configuration. Refer to **Section 1.7 “Device Selection”** for details.
3. Connect the 16-Bit 28-Pin Starter Development Board to the PC with the USB cable. The Found New Hardware Wizard dialog appears as shown in Figure 2-8.

FIGURE 2-8: FOUND NEW HARDWARE WIZARD

4. Select **No, not this time**, then click **Next >** to continue. The Found New Hardware Wizard, Select Installation Location dialog appears.
5. Select **install from a list or specific location**, then click **Next >** to continue. The Found New Hardware Wizard, Search and Installation Options dialog appears as shown in Figure 2-9.

FIGURE 2-9: FOUND NEW HARDWARE WIZARD, SEARCH AND INSTALLATION OPTIONS



> **Note:** Before continuing to the next step, make sure that the 16-Bit 28-Pin Starter Development Board CD-ROM is inserted in the CD-ROM drive.

6. Select the **Search for the best driver in these locations** radio button and select the **Search removable media (floppy, CD-ROM...)** check box, then click **Next >** to continue.
7. Windows installs the USB driver. Select **Finish** to close the Found New Hardware Wizard.

2.6.4 Connect the MPLAB ICD 2 In-Circuit Debugger

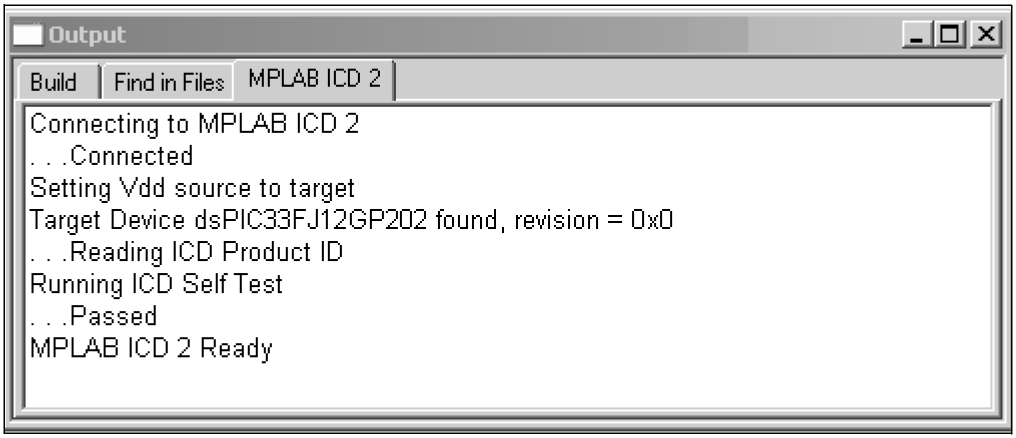
1. Connect the MPLAB ICD 2 to the PC with the USB cable.
2. Connect the MPLAB ICD 2 to J4 on the 16-Bit 28-Pin Starter Development Board with the short RJ-11 (telephone) cable.
3. For dsPIC30F devices only, verify that SW2 is in the “Program” position.

2.6.5 Enable MPLAB ICD 2 Connection

1. From the *Debugger* menu, click *Select Tool>MPLAB ICD 2* to designate the MPLAB ICD 2 as the debug tool in MPLAB IDE.
2. From the *Debugger* menu, select *Connect* to connect the debugger to the device. The MPLAB IDE should report that it found the device, as shown in Figure 2-10.

> **Note:** MPLAB IDE may need to download new firmware if this is the first time the MPLAB ICD 2 is being used with a dsPIC30F device. Allow it to do so. If any errors are shown, double click the error message to get more information.

FIGURE 2-10: ENABLING MPLAB® ICD 2

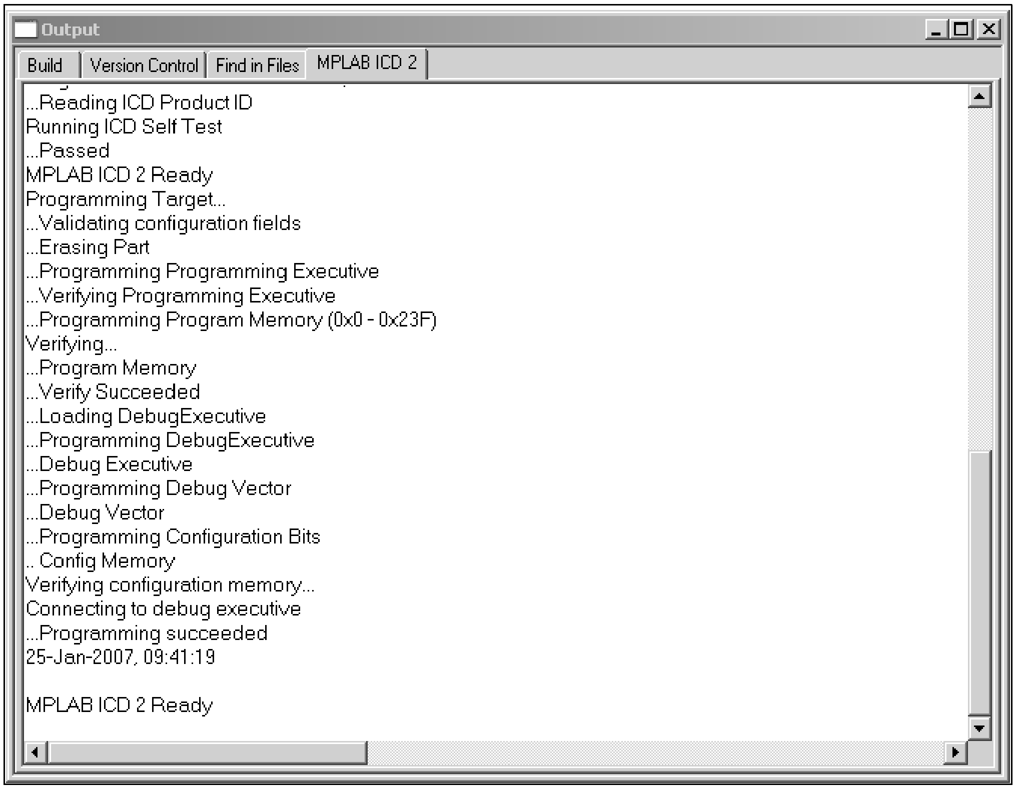


2.6.6 Program the Device

> **Note:** SW2 must be switched to the “Program” position for dsPIC30F devices when the application is being programmed into a device with MPLAB ICD 2. Once programming is complete, SW2 must be switched back to the “USB/Debug” position for UART communication via the USB bridge. See Figure 4-1 for the location of this switch.

From the *Debugger* menu, select *Program* to program the part. The output window (Figure 2-11) displays the program steps as they occur.

FIGURE 2-11: PROGRAMMING THE DEVICE



2.7 RUNNING THE APPLICATION

2.7.1 Configure the UART-to-USB Connection

1. On the PC, right click **My Computer** and select **Properties**.
2. Select the **Hardware** tab and click **Device Manager**.
3. In the **Ports** group, verify that an additional COM port is mapped. This COM port is from the PCB to the PC and will used in the HyperTerminal demonstration.
4. Open the Windows® HyperTerminal program from the CD-ROM and select the *File>Properties* menu and verify that the correct COM port is selected for the USB cable from the PCB.

   The COM settings for this port are: 9600 bits per second, no parity, 8 data bits and 1 stop bit. When a character is entered on the keyboard, it should be echoed enclosed in quotes (i.e., input a, output “a”) on the HyperTerminal display when the demonstration program is running.

2.7.2 Executing the Application

Note:	SW2 must be switched to the “Program” position for dsPIC30F devices when the application is being programmed into a device with MPLAB ICD 2. Once programming is complete, SW2 must be switched back to the “USB/Debug” position for UART communication via the USB bridge. See Figure 4-1 for the location of this switch.

Select *Debugger>Run* to execute the code. All four LEDs on the development board should start blinking twice per second. (If using a dsPIC30F device, switch SW2 to USB after executing the code.)

2.8 DEBUGGING THE CODE

The MPLAB ICD 2 In-Circuit Debugger can be used to run, halt and step the code. A breakpoint can be set to halt the program once the code has executed the instruction at the breakpoint. The contents of the RAM and registers can be viewed whenever the processor has been halted.

The MPLAB ICD 2 In-Circuit Debugger uses the following function keys to access the main debugging functions:

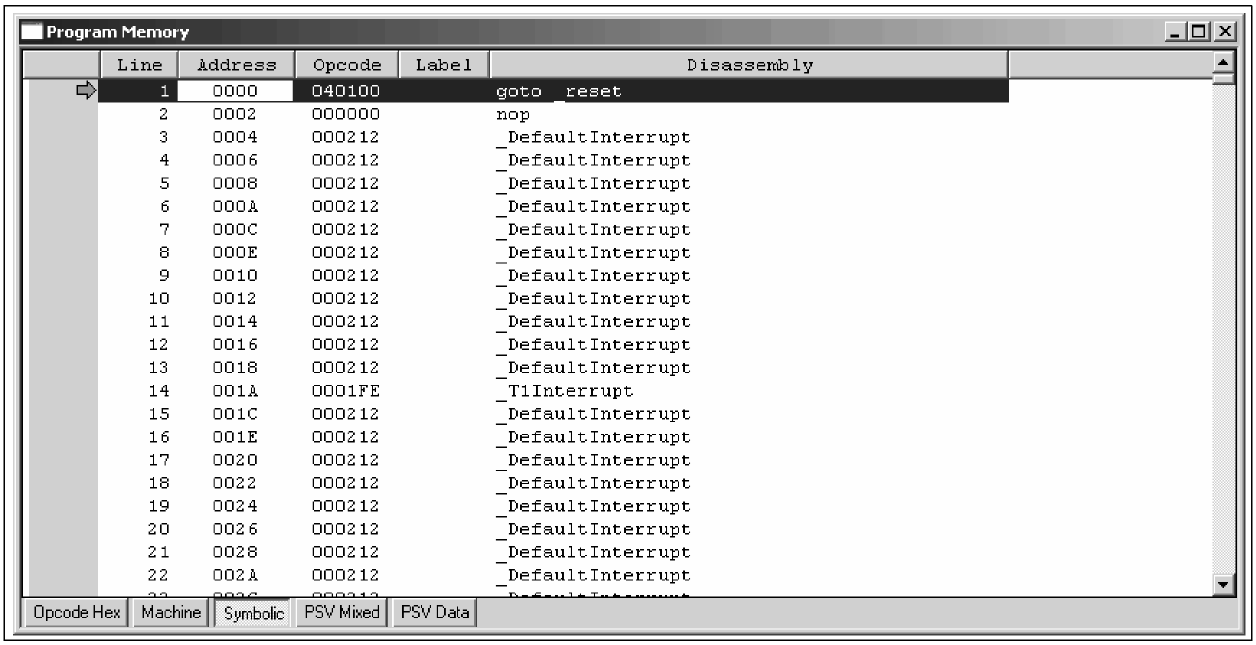
- <F5> Halt
- <F6> Reset
- <F7> Single Step
- <F9> Run

In addition, there are more functions available by right clicking on a line of source code. The most important of these are **Set Breakpoint** and **Run to Cursor**.

2.8.1 Display the Code

1. From the *View* menu, select *Program Memory*.
2. In the Program Memory window, select the **Symbolic** tab, as shown in Figure 2-12.

FIGURE 2-12: PROGRAM MEMORY WINDOW



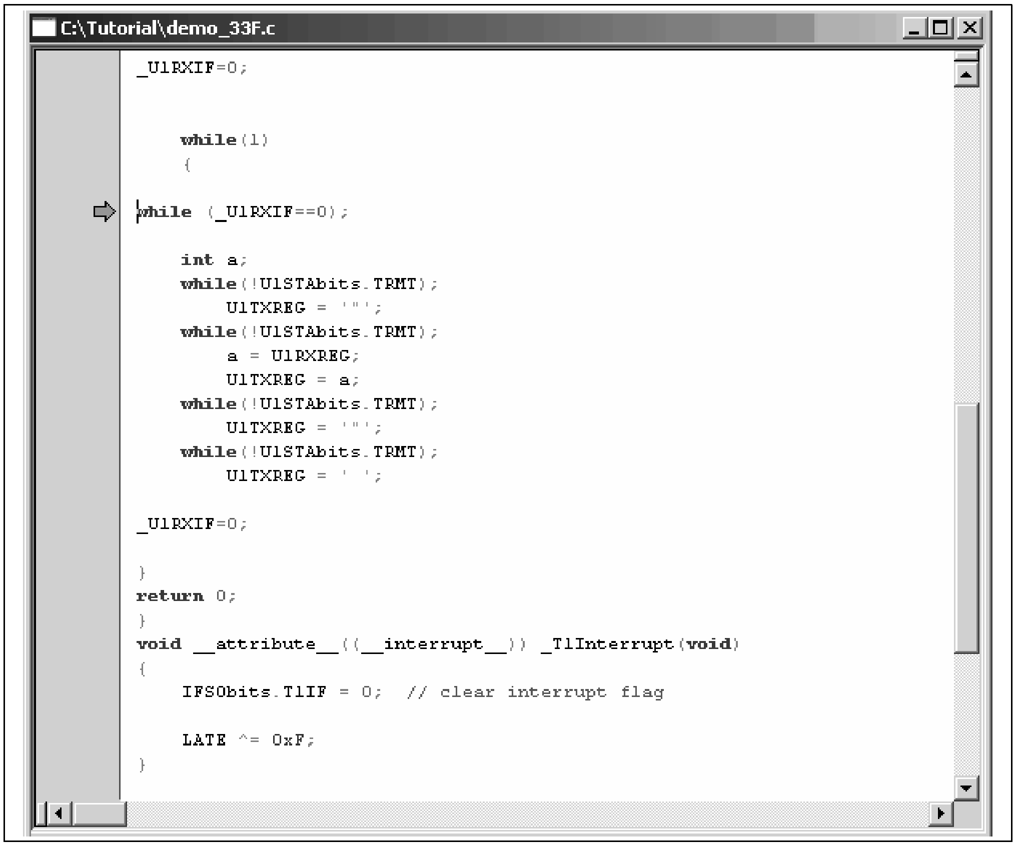
3. Press <F5> to halt the processor and press <F6> to reset the processor. The program memory now shows a green arrow pointing to the line of code at address 00000, which is the reset location.

   The instruction at this location is `goto _reset`. This code is added by the linker to make the program branch to the start of the code in the `demo_33F.c` file.

2.8.2 Step the Program

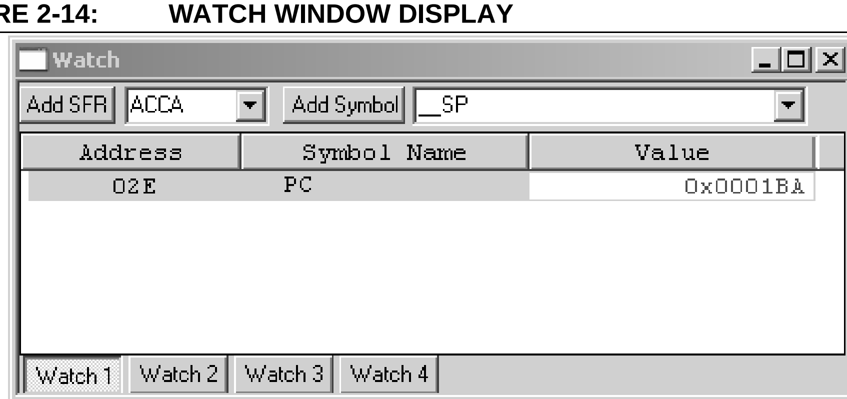
1. After halting the program, press <F7> to single step the code. Notice the location of the green arrow when single stepping. In this demonstration, the code will halt in the `while` loop of the UART, as shown in Figure 2-13.

FIGURE 2-13: SOURCE CODE WINDOW



2. Right click the line of code, `LATE ^= 0xF;`,and choose *Run to Cursor*. The green arrow moves to the bracket below the line of code because it has executed the prior lines of code up to and including `LATE ^= 0xF;`.
3. From the *View* menu, select *Watch* to open a Watch window.
4. From the **Add SFR** pull-down list, display **PC**.
5. Click **Add SFR** to add the PC register to the Watch window.
6. Press <F7> a few times and watch the PC value increment (see Figure 2-14). PC is the repeat loop counter that increments with each step.

FIGURE 2-14: WATCH WINDOW DISPLAY



2.8.3 Set Breakpoint

1. To set a breakpoint, right click a code line and select *__Set Breakpoint__* from the pop-up menu.

> **Note:** An alternate method is to simply double click the line. This feature may need to be enabled using the *__Edit>Properties__* menu.

As an example, find the following line of code and set a breakpoint on this line:

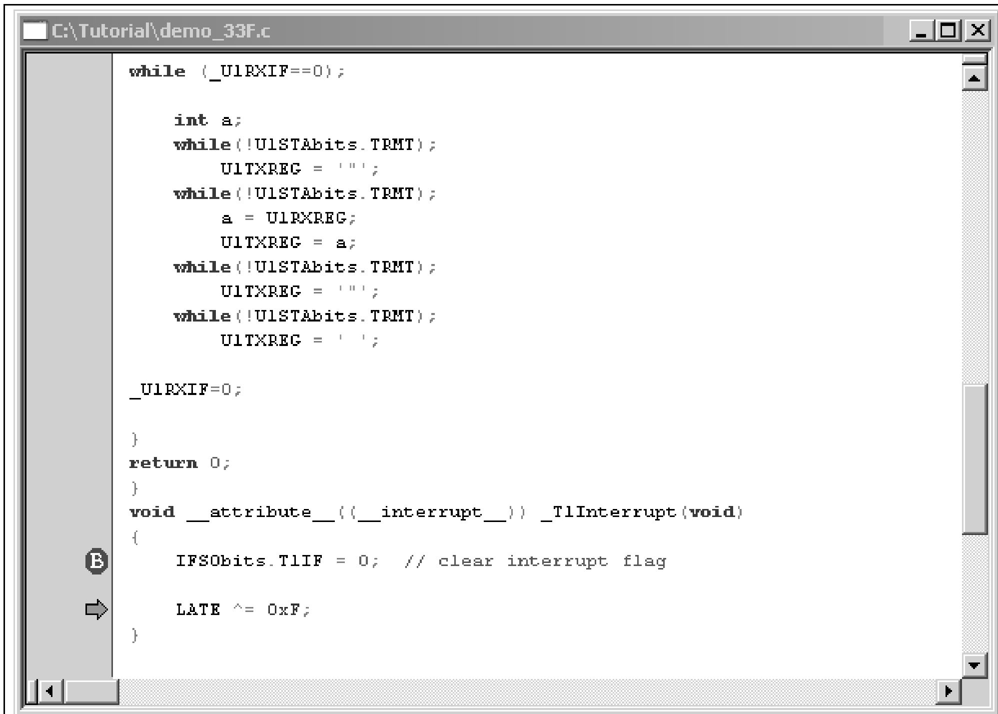
```
IFS0bits.T1IF = 0;
```

A red stop sign should appear in the gutter (gray bar on the left) of the source code window.

2. Press <F6> to reset the device, then <F9> to execute the code. The program halts on the instruction following the breakpoint as shown in Figure 2-15. When MPLAB ICD 2 is halted, the next instruction is executed. Observe that the LEDs on the development board remain lit.

> **Note:** The instruction on which the code halts could be elsewhere in the code if the breakpoint is set on a branch or call instruction. Refer to **Section 12. "Important Notes"** in the readme file `MPLAB ICD 2.txt` located in the `C:\MPLAB IDE\READMES` directory for additional operational information on the MPLAB ICD 2.

FIGURE 2-15: SETTING BREAKPOINT



2.9 PROGRAMMING THE DEVICE FOR STAND-ALONE OPERATION

The previous example showed you the basics of code debugging using the MPLAB ICD 2. When you have fully debugged your application, you will want to run the code without using the MPLAB ICD 2. In the following example, the MPLAB ICD 2 is enabled as a device programmer instead of a debugger.

1. Starting with the project you have created in this tutorial, select MPLAB ICD 2 as the device programmer. From the *Programmer* menu, select the *Select Programmer>MPLAB ICD 2* option.

   If you were previously using the MPLAB ICD 2 as a debugger tool, you will receive a warning message indicating that the tool cannot be enabled as a programmer and a debugger at the same time. Click **OK** in the warning message to continue.

Note:	SW2 must be switched to the "Program" position for dsPIC30F devices when the application is being programmed into a device with MPLAB ICD 2. Once programming is complete, SW2 must be switched back to the "USB/Debug" position for UART communication via the USB bridge. See Figure 4-1 for the location of this switch.

2. From the *Program* menu, select *Program* to program the part. The output window will look similar to Figure 2-11, except that the debugging features of the device will not be enabled.
3. Remove the MPLAB ICD 2 programming cable connected to J4. When the cable is unplugged, the device will begin to run the application.

2.10 SUMMARY

This tutorial demonstrates the main features of the MPLAB IDE and MPLAB ICD 2 as they are used with the 16-Bit 28-Pin Starter Development Board. Upon completing this tutorial, you should be able to:

- Create a project using the Project Wizard
- Set the Configuration bits
- Set up MPLAB IDE to use the MPLAB ICD 2 In-Circuit Debugger
- Program the chip with the MPLAB ICD 2
- View the code execution in program memory and source code
- View registers in a Watch window
- Set a breakpoint and make the code halt at a chosen location
- Use the function keys to reset, run, halt and single step the code
- Program the device for Debugger mode or stand-alone operation

NOTES:

Chapter 3. Demonstration Program

3.1 INTRODUCTION

This chapter provides an overview of the 16-Bit 28-Pin Starter Development Board demonstration program. Detailed information on the 16-Bit 28-Pin Starter Development Board hardware is presented in **Chapter 4. "Development Hardware"** and **Appendix A. "Drawings and Schematics"**.

Topics discussed in this chapter include:

- Demonstration Program Summary
- Demonstration Program Description
- Demonstration Program Setup

3.2 DEMONSTRATION PROGRAM SUMMARY

The 16-Bit 28-Pin Starter Development Board is shipped with a simple example application programmed into the dsPIC33FJ12GP202 device. This program demonstrates the use of key functionality.

3.3 DEMONSTRATION PROGRAM DESCRIPTION

When power is applied to the 16-Bit 28-Pin Starter Development Board the device begins executing the demonstration program. The program demonstrates the following functions:

- UART communication
- Timer interrupt

3.3.1 UART Communication

The demonstration program uses the UART peripheral to communicate with the PC HyperTerminal application via the on-board UART-to-USB bridge. The demonstration program waits for the character to be received from the PC, and echoes it back to the PC enclosed in quotes.

3.3.2 Timer Interrupt

To illustrate interrupt processing, the demonstration program uses Timer1 to generate interrupts, which cause the LEDs to blink. The clock prescaler and period register for Timer1 are configured to produce an interrupt every 250 ms.

3.4 DEMONSTRATION PROGRAM SETUP

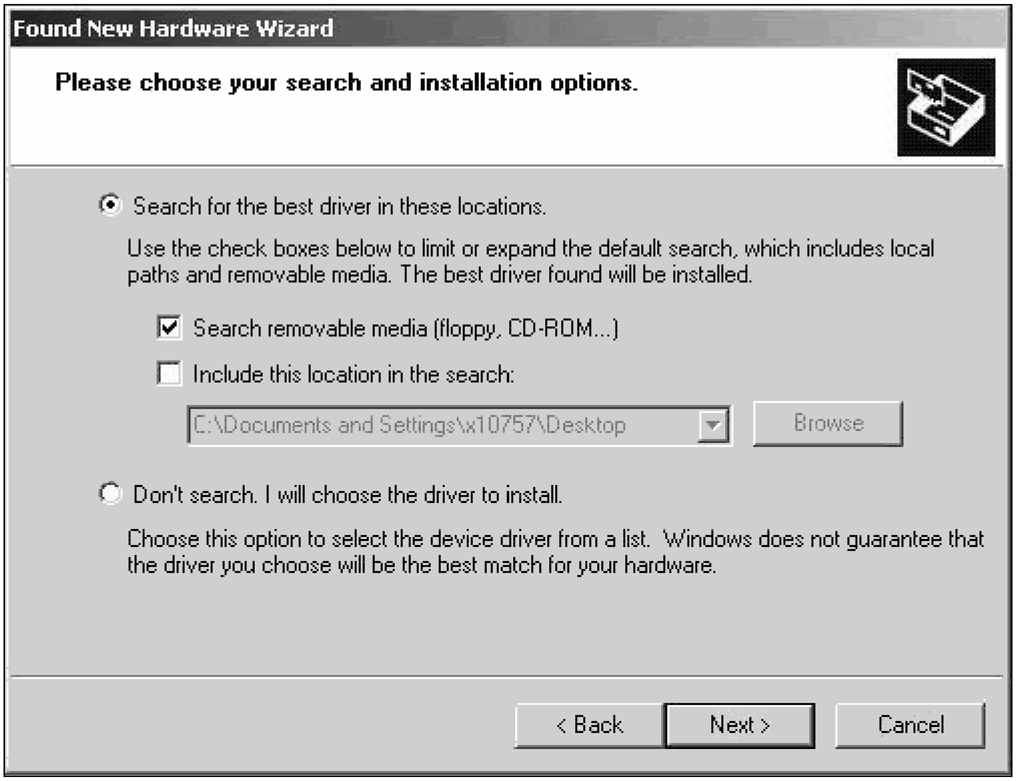
3.4.1 Installing the USB Driver

1. Apply power to the board. Refer to **1.5 "Power Selection"** for details.
2. Select the dsPIC33F device configuration. Refer to **1.7 "Device Selection"** for details.
3. Connect the 16-Bit 28-Pin Starter Development Board to the PC with the USB cable. The Found New Hardware Wizard dialog appears as shown in Figure 3-1.

FIGURE 3-1: FOUND NEW HARDWARE WIZARD

4. Select **No, not this time**, then click **Next >** to continue. The next Found New Hardware Wizard, Select Installation Location dialog appears.
5. Select **install from a list or specific location**, then click **Next >** to continue. The Found New Hardware Wizard, Search and Installation Options dialog appears as shown in Figure 3-2.

FIGURE 3-2: FOUND NEW HARDWARE WIZARD, SEARCH AND INSTALLATION OPTIONS



Note:	Before continuing to the next step, make sure that the 16-Bit 28-Pin Starter Development Board CD-ROM is inserted in the CD-ROM drive.

6. Select the **Search for the best driver in these locations** radio button and select the **Search removable media (floppy, CD-ROM...)** check box, then click **Next >** to continue.
7. Windows installs the USB driver. Select **Finish** to close the Found New Hardware Wizard.

3.4.2 Configure the UART-to-USB Connection

1. On the PC, right click **My Computer** and select **Properties**.
2. Select the **Hardware** tab and click **Device Manager**.
3. In the **Ports** group, verify that an additional COM port is mapped. This COM port is from the PCB to the PC and will used in the HyperTerminal demonstration.
4. Open the Windows® HyperTerminal program from the CD-ROM and select the *File>Properties* menu and verify that the correct COM port is selected for the USB cable from the PCB.

   The COM settings for this port are: 9600 bits per second, no parity, 8 data bits, and 1 stop bit. When a character is entered on the keyboard, it should be echoed enclosed in quotes (i.e., input a, output “a”) on the HyperTerminal display when the demonstration program is running.

NOTES:

Chapter 4. Development Hardware

4.1 INTRODUCTION

This chapter describes the 16-Bit 28-Pin Starter Development Board hardware, and includes the following topics:

- Hardware Overview
- Hardware Elements

4.2 HARDWARE OVERVIEW

FIGURE 4-1: 16-BIT 28-PIN STARTER DEVELOPMENT BOARD

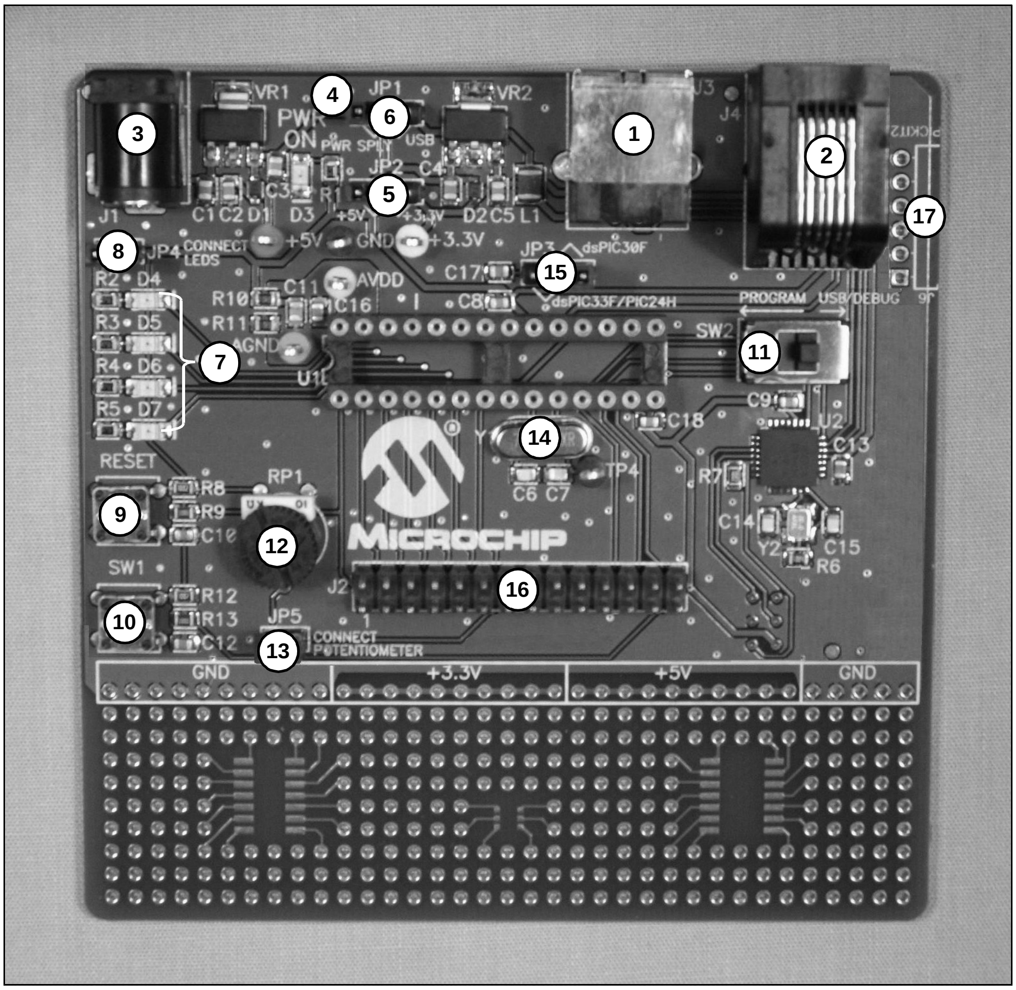


TABLE 4-1: 16-BIT 28-PIN STARTER DEVELOPMENT BOARD HARDWARE ELEMENTS

No.	Name	Description
1	J3	USB Port
2	J4	MPLAB® ICD 2 Connector
3	J1	Power Supply Connector
4	D3	Power On Indicator
5	JP2	+5V or +3.3V Jumper
6	JP1	Power Supply or USB Jumper
7	D4-D7	LED Indicators
8	JP4	LED Connect Jumper
9	RESET	Reset Button
10	SW1	Switch 1
11	SW2	Switch 2
12	RP1	Potentiometer
13	JP5	Potentiometer Connect Jumper
14	Y1	Oscillator
15	JP3	Device Selection Jumper
16	J2	I/O Header
17	J6	PICkit™ 2 Connector

4.3 HARDWARE ELEMENTS

4.3.1 USB Port (J3)

The 16-Bit 28-Pin Starter Development Board provides one USB communication channel. The USB communication channel is labeled J3. The device communicates using the UART to the on-board PIC18 through the U1RX and U1TX pins, which then communicates through the USB port. The USB port can also be used to power the development board.

4.3.2 MPLAB ICD 2 Connector (J4)

By way of this modular connector, the MPLAB ICD 2 can be connected for low-cost programming and debugging of the device.

4.3.3 Power Supply Connector (J1)

The 16-Bit 28-Pin Starter Development Board can be powered by a 9V AC/DC wall adapter with a standard 2.1 mm barrel plug.

4.3.4 Power On Indicator (D3)

A green LED is connected to the output of the regulators to indicate the presence of power.

4.3.5 +5V or +3.3V Jumper (JP2)

This jumper is used at +5V when a dsPIC30F family device is being used, and at +3.3V when a dsPIC33F or PIC24 family device is being used.

4.3.6 Power Supply or USB Jumper (JP1)

This jumper allows the circuit to be powered by a 9V power supply (J1) or by the USB port (J3).

4.3.7 LED Indicators (D4-D7)

LEDs are connected to the device for user operations.

4.3.8 LED Connect Jumper (JP4)

If removed, this jumper restricts the use of the LEDs.

4.3.9 Reset Button (RESET)

The $\overline{\text{MCLR}}$ Reset button is connected to the processor $\overline{\text{MCLR}}$ pin, which provides a hard Reset to the device.

4.3.10 Switch 1 (SW1)

This switch is connected to the devices for user operations.

4.3.11 Switch 2 (SW2)

This switch, when used with a dsPIC30F family device, programs the device to communicate with the PC by USB. If using a dsPIC33F or PIC24 family device, this switch should be in the USB position at all times.

4.3.12 Potentiometer (RP1)

This potentiometer is connected to the devices for the use of the ADC peripheral.

4.3.13 Potentiometer Connect Jumper (JP5)

This jumper allows the use of the potentiometer.

4.3.14 Oscillator (Y1)

A crystal oscillator (7.37 MHz) is supplied. The crystal oscillator can be used with the on-chip PLL circuit to provide internal instruction execution frequencies.

4.3.15 Device Selection Jumper (JP3)

This jumper determines whether the dsPIC30F or dsPIC33F/PIC24 device is used.

4.3.16 I/O Header (J2)

All device I/O pins are brought out to this header for test points and prototyping access.

4.3.17 PICkit™ 2 Connector (J6)

By way of this modular connector, the PICkit 2 can be connected for low cost programming and debugging of the device.

NOTES:

Appendix A. Drawings and Schematics

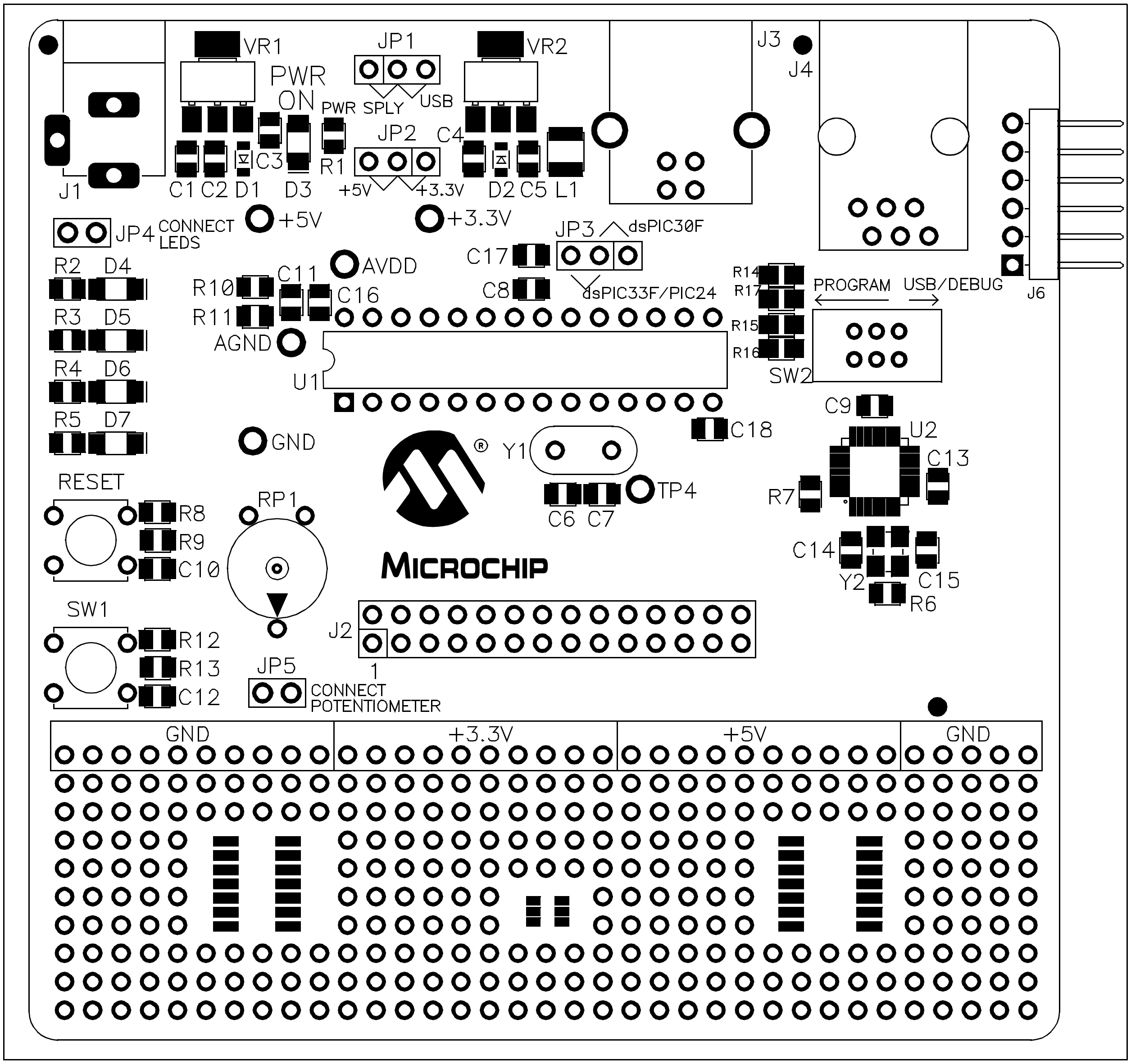
A.1 INTRODUCTION

This appendix contains the schematics and layouts for the 16-Bit 28-Pin Starter Development Board. Diagrams included in this appendix:

- 16-bit 28-Pin Starter Development Board Layout
- 16-bit 28-Pin Starter Development Board Schematics

A.2 16-BIT 28-PIN STARTER DEVELOPMENT BOARD LAYOUT

FIGURE A-1: 16-BIT 28-PIN STARTER DEVELOPMENT BOARD LAYOUT



A.3 16-BIT 28-PIN STARTER DEVELOPMENT BOARD SCHEMATICS

FIGURE A-2: 16-BIT 28-PIN STARTER DEVELOPMENT BOARD SCHEMATIC (SHEET 1 OF 2)

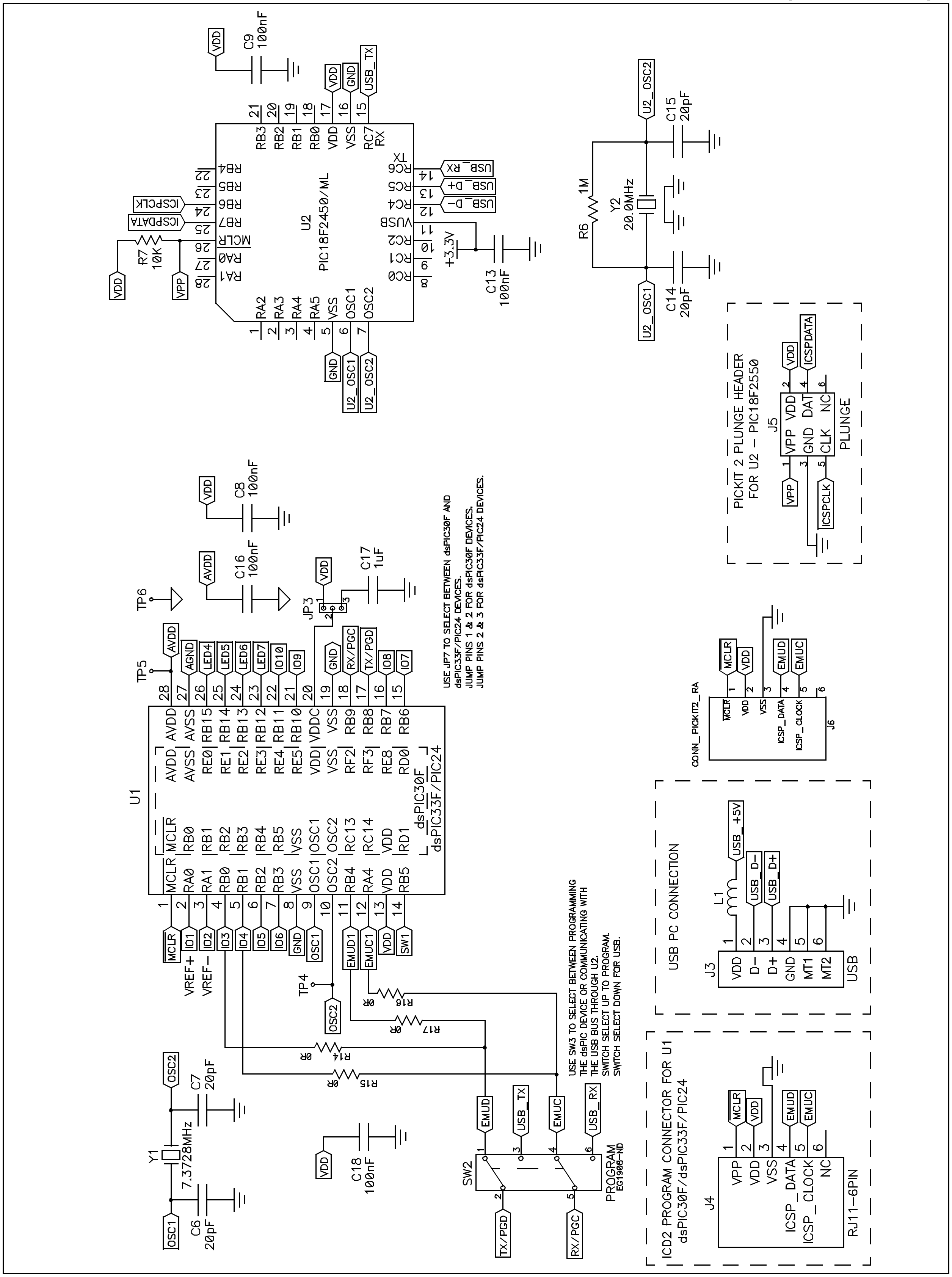
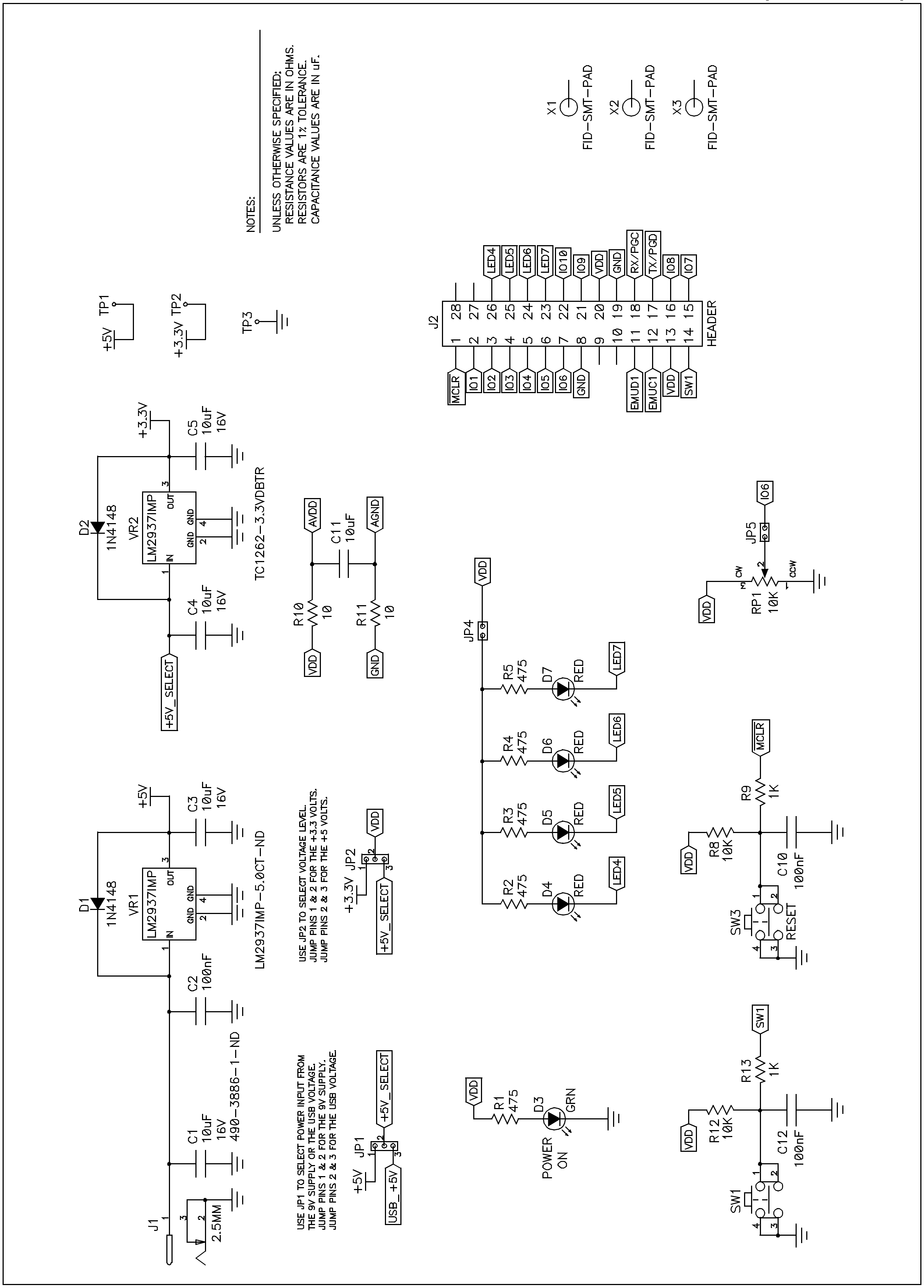


FIGURE A-3: 16-BIT 28-PIN STARTER DEVELOPMENT BOARD SCHEMATIC (SHEET 2 OF 2)



NOTES:

Appendix B. Bill of Materials (BOM)

TABLE B-1: BILL OF MATERIALS

Qty	Component Name	Reference	Value	Vendor	Vendor P/N
1	CAP-CRCW0805	C17	1 µF	Digi-Key	PCC2249CT-ND
5	CAP-CRCW0805	C1	10 µF	Digi-Key	490-3886-1-ND
		C3	10 µF		
		C4	10 µF		
		C5	10 µF		
		C11	10 µF		
4	CAP-CRCW0805	C6	20 pF	Digi-Key	478-3735-1-ND
		C7	20 pF		
		C14	20 pF		
		C15	20 pF		
8	CAP-CRCW0805	C2	100 nF	Digi-Key	PCC1864CT-ND
		C8	100 nF		
		C9	100 nF		
		C10	100 nF		
		C12	100 nF		
		C13	100 nF		
		C16	100 nF		
		C18	100 nF		
1	CNN-POWER-IN-MOD-2.5MM	J1	2.5 MM	Digi-Key	CP-102BH-ND
1	CNN-RJ11-ICSP-6-PIN-PTH	J4	RJ11-6-pin	Digi-Key	A31417-ND
1	CNN-USB-TYPE-B-PTH	J3	USB	Digi-Key	A31725-ND
2	DIO-1N4148WS-SOD-323	D1	1N4148	Digi-Key	1N4148WS-FDICT-ND
		D2	1N4148		
4	FOOT-BUMPON-RUBBER-0.375-ROUND	BOM1	BUMPON	Digi-Key	RBS-12-ND
		BOM2			
		BOM3			
		BOM4			
1	HDR-2X14-IC-STYLE	J2	HEADER	Digi-Key	929665-09-36-ND
1	ICP-DUAL-PIC-28-PIN-SDIP	U1	dsPIC33F	MCHP	dsPIC33F
1	ICP-PIC18F2450/ML-QFN-28-PIN-6X6MM	U2	PIC18F2450/ML	MCHP	PIC18F2450/ML
1	IND-1210	L1	60Ω	Digi-Key	240-2416-1-ND
2	JMP-2PIN-VIAS	JP4	1x2	Jameco	108337
		JP5	1x2		
3	JMP-3PIN-CFG2-VIAS	JP1	1x3	Jameco	109575
		JP2	1x3		
		JP3	1x3		
1	LED-LTST-C150XKT-1206-SMD	D3	GRN	Digi-Key	160-1169-1-ND

TABLE B-1: BILL OF MATERIALS (CONTINUED)

Qty	Component Name	Reference	Value	Vendor	Vendor P/N
4	LED-LTST-C150XKT-1206-SMD	D4	RED	Digi-Key	160-1167-1-ND
		D5			
		D6			
		D7			
1	POT-3352E-BOURNS-1T	RP1	10K	Digi-Key	3352E-103LF-ND
2	RES-CRCW0805	R9	1K	Digi-Key	RHM1.00KCCT-ND
		R13	1K		
1	RES-CRCW0805	R6	1M	Digi-Key	RHM1.00MCCT-ND
2	RES-CRCW0805	R10	10	Digi-Key	RHM10.0CCT-ND
		R11	10		
3	RES-CRCW0805	R7	10K	Digi-Key	RHM10.0KCCT-ND
		R8	10K		
		R12	10K		
5	RES-CRCW0805	R1	475	Digi-Key	RHM475CCT-ND
		R2	475		
		R3	475		
		R4	475		
		R5	475		
2	SWT-B3F1000-MOM-NO-PTH	SW3	RESET	Digi-Key	SW402-ND
		SW1	MOM-NO		
1	SWT-E-SWT-EG2209-VERT-PTH	SW2	PROGRAM	Digi-Key	EG1907-ND
1	TSP-P90R60	TP2	+3.3V - WHI	Digi-Key	5012K-ND
1	TSP-P90R60	TP1	+5V - RED	Digi-Key	5010K-ND
1	TSP-P90R60	TP6	AGND - ORN	Digi-Key	5013K-ND
1	TSP-P90R60	TP5	AVDD - YEL	Digi-Key	5014K-ND
2	TSP-P90R60	TP3	GND - BLK	Digi-Key	5011K-ND
		TP4	GND - BLK		
1	VRG-LM2937IMP-SOT223-SMT	VR1	+5V	Digi-Key	LM2937IMP-5.0CT-ND
1	VRG-TC1262IMP-SOT223-SMT	VR2	+3.3V	MCHP	TC1262-3.3VDBTR
1	XTL-200LS-PTH-CAN	Y1	7.3728 MHz	Digi-Key	X1084-ND
1	XTL-ABM8-SMT	Y2	20.0 MHz	Digi-Key	535-9136-1-ND
1	SOC-PIC-28-PIN-SDIP	SU1	SOCKET	Digi-Key	ED90054-ND
1	PCB-DSPICDEM-28-PIN-PLUS-DEMO	PCB1	BLANK PCB		
5	SHUNT, 2-PIN	SH1-5		Jameco	421454

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Buck/Boost Converter PICtail™ Plus Daughter Board User's Guide

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Table of Contents

NOTES:

Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE on-line help. Select the Help menu, and then Topics to open a list of available on-line help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the Chapter Name. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Warranty Registration
- Recommended Reading
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the Buck/Boost Converter PICtail Plus Daughter Board as a development tool to emulate and debug firmware on a target board. The manual layout is as follows:

- **Chapter 1. "Introduction"** – This chapter describes the Buck/Boost Converter PICtail Plus Daughter Board and provides a brief description of the hardware.
- **Chapter 2. "Hardware Overview"** – This chapter describes the Buck/Boost Converter PICtail Plus Daughter Board hardware.
- **Chapter 3. "Getting Started"** – This chapter describes the step-by-step process for getting your Buck/Boost Converter PICtail Plus Daughter Board up and running with the MPLAB® In-Circuit Debugger 2 (ICD 2) using a dsPIC33FJ16GS502 device.

- **Chapter 4. “Demonstration Program Operation”** – This chapter describes the operation of the Buck/Boost Converter PICtail Plus Daughter Board.
- **Appendix A. “Schematics and Layouts”** – This appendix illustrates the Buck/Boost Converter PICtail Plus Daughter Board layout and provides hardware schematic diagrams.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

<table>
<tr><th>Description</th><th>Represents</th><th>Examples</th></tr>
<tr><td colspan="3">Arial font:</td></tr>
<tr><td rowspan="2">Italic characters</td><td>Referenced books</td><td>MPLAB® IDE User’s Guide</td></tr>
<tr><td>Emphasized text</td><td>...is the only compiler...</td></tr>
<tr><td rowspan="3">Initial caps</td><td>A window</td><td>the Output window</td></tr>
<tr><td>A dialog</td><td>the Settings dialog</td></tr>
<tr><td>A menu selection</td><td>select Enable Programmer</td></tr>
<tr><td>Quotes</td><td>A field name in a window or dialog</td><td>“Save project before build”</td></tr>
<tr><td>Underlined, italic text with right angle bracket</td><td>A menu path</td><td><u>File>Save</u></td></tr>
<tr><td rowspan="2">Bold characters</td><td>A dialog button</td><td>Click OK</td></tr>
<tr><td>A tab</td><td>Click the Power tab</td></tr>
<tr><td>N‘Rnnnn</td><td>A number in Verilog format, where N is the total number of digits, R is the radix and n is a digit.</td><td>4‘b0010, 2‘hF1</td></tr>
<tr><td>Text in angle brackets < ></td><td>A key on the keyboard</td><td>Press <Enter>, <F1></td></tr>
<tr><td colspan="3">Courier New font:</td></tr>
<tr><td rowspan="7">Plain Courier New</td><td>Sample source code</td><td>#define START</td></tr>
<tr><td>Filenames</td><td>autoexec.bat</td></tr>
<tr><td>File paths</td><td>c:\mcc18\h</td></tr>
<tr><td>Keywords</td><td>_asm, _endasm, static</td></tr>
<tr><td>Command-line options</td><td>-Opa+, -Opa-</td></tr>
<tr><td>Bit values</td><td>0, 1</td></tr>
<tr><td>Constants</td><td>0xFF, ‘A’</td></tr>
<tr><td>Italic Courier New</td><td>A variable argument</td><td>file.o, where file can be any valid filename</td></tr>
<tr><td>Square brackets [ ]</td><td>Optional arguments</td><td>mcc18 [options] file [options]</td></tr>
<tr><td>Curly brackets and pipe character: { | }</td><td>Choice of mutually exclusive arguments; an OR selection</td><td>errorlevel {0|1}</td></tr>
<tr><td rowspan="2">Ellipses...</td><td>Replaces repeated text</td><td>var_name [, var_name...]</td></tr>
<tr><td>Represents code supplied by user</td><td>void main (void)
{ ...
}</td></tr>
</table>

WARRANTY REGISTRATION

Please complete the enclosed Warranty Registration Card and mail it promptly. Sending in the Warranty Registration Card entitles users to receive new product updates. Interim software releases are available at the Microchip web site.

RECOMMENDED READING

This user's guide describes how to use the Chapter Name. Other useful documents are listed below. The following Microchip documents are available and recommended as supplemental reference resources.

Readme for Chapter Name

For the latest information on using Chapter Name, read the "`Readme.txt`" (an ASCII text file) in the `Readme` subdirectory of the MPLAB IDE installation directory from the Buck/Boost Converter PICtail Plus Daughter Board CD. The Readme file contains update information and known issues that may not be included in this user's guide.

Readme Files

For the latest information on using other tools, read the tool-specific Readme files in the `Readme` subdirectory of the MPLAB IDE installation directory. The Readme files contain updated information and known issues that may not be included in this user's guide.

THE MICROCHIP WEB SITE

Microchip provides online support via our web site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
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- **Compilers** – The latest information on Microchip C compilers and other language tools. These include the MPLAB C18 and MPLAB C30 C compilers; MPASM™ and MPLAB ASM30 assemblers; MPLINK™ and MPLAB LINK30 object linkers; and MPLIB™ and MPLAB LIB30 object librarians.
- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB ICE 2000, MPLAB ICE 4000, and MPLAB REAL ICE™ in-circuit emulator.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debugger, MPLAB ICD 2.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB SIM simulator, MPLAB IDE Project Manager and general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include the MPLAB PM3 and PRO MATE II device programmers and the PICSTART® Plus and PICkit™ 1 development programmers.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com

DOCUMENT REVISION HISTORY

Revision A (August 2008)

This is the initial release of this document.

NOTES:

Chapter 1. Introduction

Modern power supplies are becoming smaller, more efficient, more flexible and less expensive. These desirable enhancements have come about as digital signal controllers are incorporated into Switch Mode Power Supply (SMPS) designs. Buck converters are used when the desired output voltage is smaller than the input voltage. Boost converters are used when the desired output voltage is higher than the input voltage.

This chapter introduces and provides an overview of the Buck/Boost Converter PICtail Plus Daughter Board. The following topics are included in this chapter:

- Overview
- Features
- Product Package

1.1 OVERVIEW

The Buck/Boost Converter PICtail Plus Daughter Board (also referred to as Daughter Board) is a power supply board. It consists of two independent DC/DC synchronous buck converters and one independent DC/DC boost converter. Figure 1-1 illustrates a block diagram of the Daughter Board.

All of the necessary power, drive and control signals are available in the J1 and J2 connectors. The 16-bit 28-pin Starter Development Board can be used to control one independent DC/DC synchronous buck converters. This board can also control two buck stages, or one buck and one boost stage with hardware modification on the 16-bit 28-pin Starter Development Board. Refer to **Section 2.4.2 "16-bit 28-pin Starter Development Board Controls Buck 1 and Boost Stages"** for more details.

The block diagram of the Daughter Board using the 16-bit 28-pin Starter Development Board is shown in Figure 1-2. All three stages of the Buck/Boost Converter PICtail Plus Daughter Board are controlled by the Explorer 16 Development Board. Figure 1-3 shows a block diagram of the Daughter Board using the Explorer 16 Development Board.

The control boards provide closed-loop Proportional-Integral-Derivative (PID) control in the software to maintain the desired output voltage level. The dsPIC® DSC device provides the necessary memory and peripherals for A/D conversion, PWM generation, analog comparison and general purpose I/O, excluding the need to perform these functions in external circuitry.

SMPS dsPIC® DSC devices are specifically designed to provide low-cost and efficient control for a wide range of power supply topologies. The specialized peripherals facilitate closed-loop feedback control of switch mode power supplies, providing communication for remote monitoring and supervisory control.

The Daughter Board enables the end user to easily transition from analog-to-digital implementation of the power application. The Daughter Board also aids in rapid development of buck converter, boost converter, multi-phase buck converter and two parallel buck converters.

The dsPIC33F SMPS family of devices provides the following features:

- Integrated program and data memory on a single chip
- Ultra-fast interrupt response time and hardware interrupt priority logic
- Up to 4 Msps, on-chip ADC with two SARs, and up to four dedicated and two shared sample/hold circuits for multiple loop control
- Four independent, high-resolution PWM generators specially designed to support different power topologies
- Four analog comparators for control loop implementation and system protection
- On-chip system communications (I^{2}C™/SPI/UART)
- On-chip Fast RC oscillator for lower system cost
- High-current sink/source for PWM pins: 16 mA/16 mA
- CPU performance: 40 MIPS
- Extensive power saving
- CodeGuard™ Security enabled

FIGURE 1-1: DAUGHTER BOARD BLOCK DIAGRAM

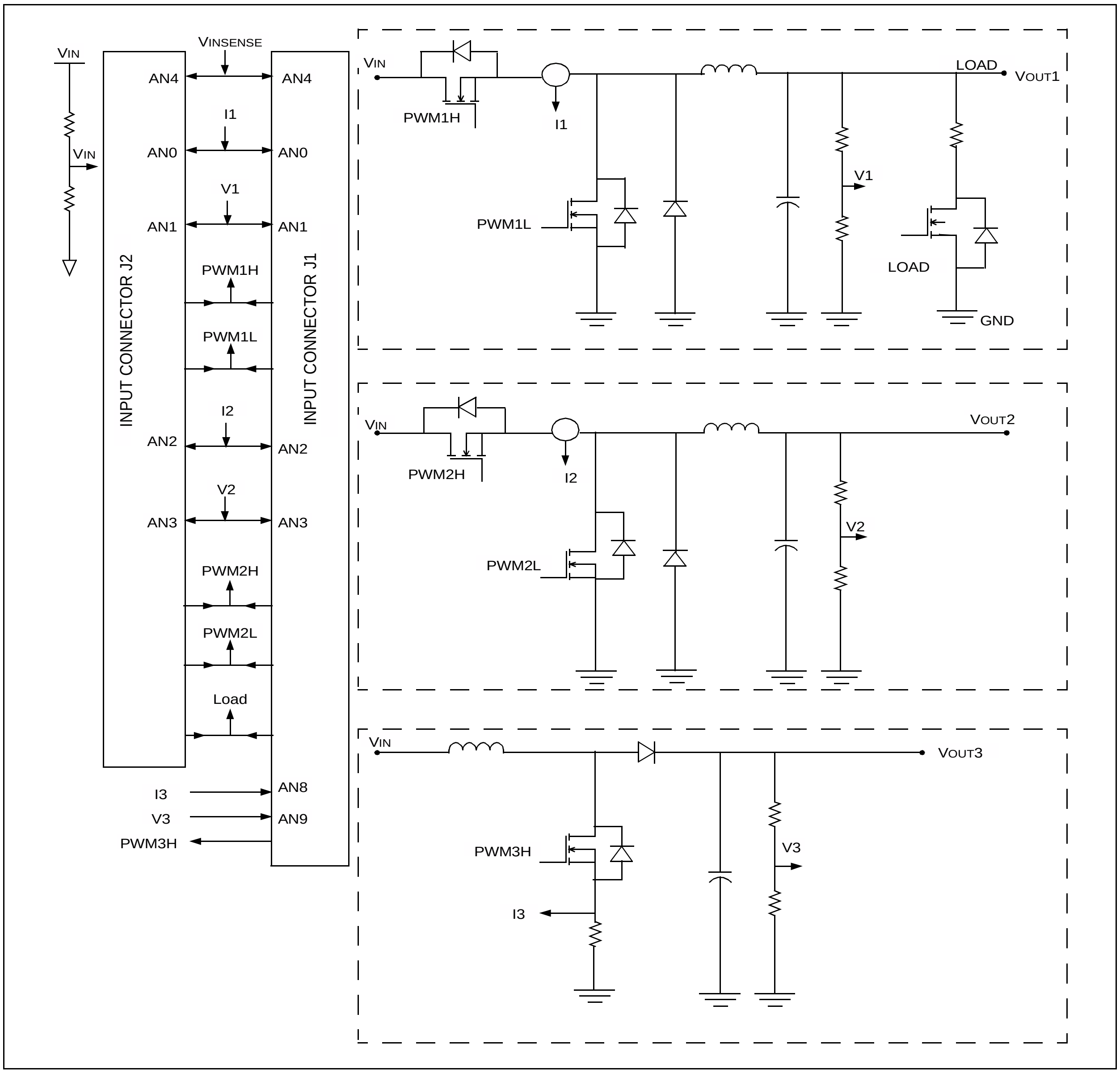


FIGURE 1-2: 16-BIT 28-PIN STARTER DEVELOPMENT BOARD WITH DAUGHTER BOARD

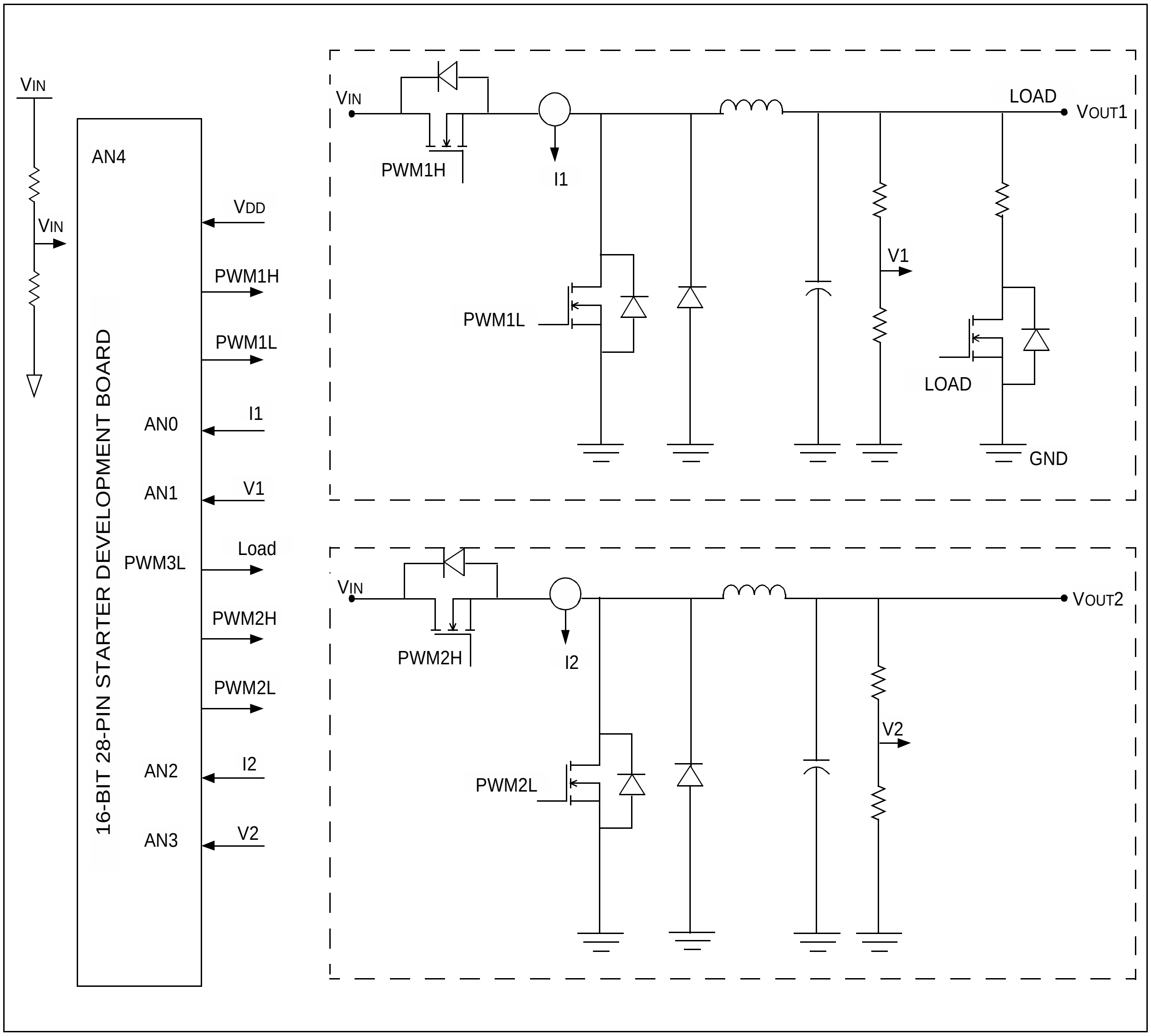
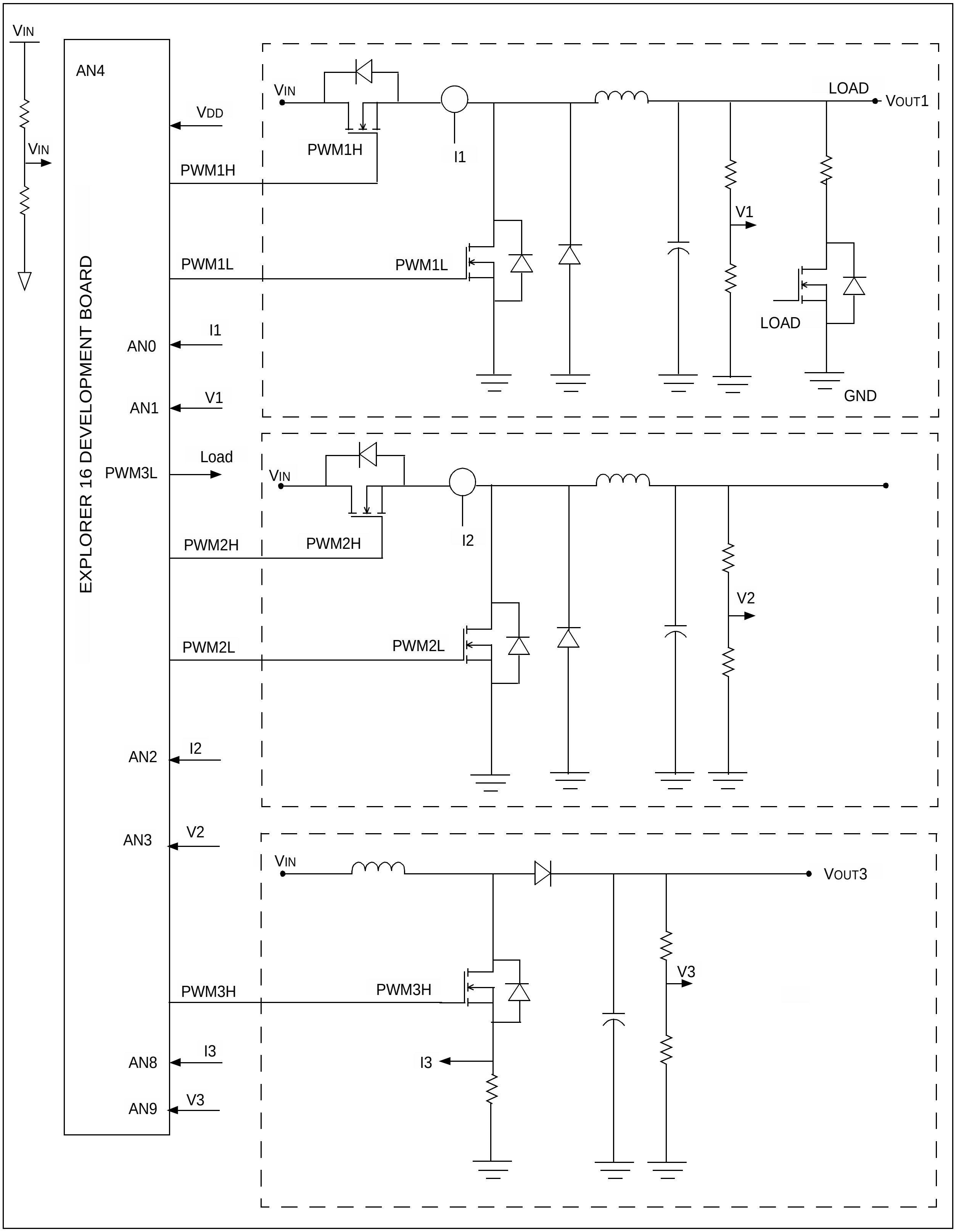


FIGURE 1-3: EXPLORER 16 DEVELOPMENT BOARD WITH DAUGHTER BOARD



1.2 FEATURES

The Buck/Boost Converter PICtail Plus Daughter Board provides the following features:

1.2.1 Power Stages

- Two synchronous buck converter power stages
- One boost converter power stage
- Voltage/current measurement for digital control of buck converters
- Voltage/current measurement for digital control of boost converter
- Switchable, one 5Ω/5W resistive load on Buck Converter 1 output (VOUT1)
- Buck Converter 1 output (VOUT1) on J4 connector for external loading
- Buck Converter 2 output (VOUT2) on J5 connector for external loading
- Boost Converter output (VOUT3) on J8 connector for external loading
- Connector J9 for auxiliary power input

1.2.2 Additional Features

- 5 kΩ Potentiometer (RP1) connected via jumper J10
- Input voltage source selection via jumper J6
- Additional resistive load R46 via jumper J11
- Connectors J1 and J2 (Explorer 16/16-bit 28-pin Starter Development Board)
- PMBus™ Connector (J3)

1.2.3 Daughter Board Power

- Auxiliary power input (J9): +7V to +15V (+9V nominal)
- 9V power input is through input connectors J2 and J1
- LED power-on indicator (D14)
- LED output voltage indicators (D11, D12 and D13)

Note: 9V input is supplied from the controller card (16-bit 28-pin Starter Development Board or Explorer 16 Development Board). All 16-bit 28-pin Starter Development Boards should have a blue wire connecting Pin 1 of J1 to Pin 28 of J2. If no blue wire connects them, connect a wire between them to supply the 9V input to the Buck/Boost Converter PICtail Plus Daughter Board.

1.3 PRODUCT PACKAGE

The Buck/Boost Converter PICtail Plus Daughter Board kit consists of the following items:

- Buck/Boost Converter PICtail Plus Daughter Board
- Buck/Boost Converter PICtail Plus Daughter Board CD

The CD consists of the application software, example code, Readme file and User's Guide.

NOTES:

Chapter 2. Hardware Overview

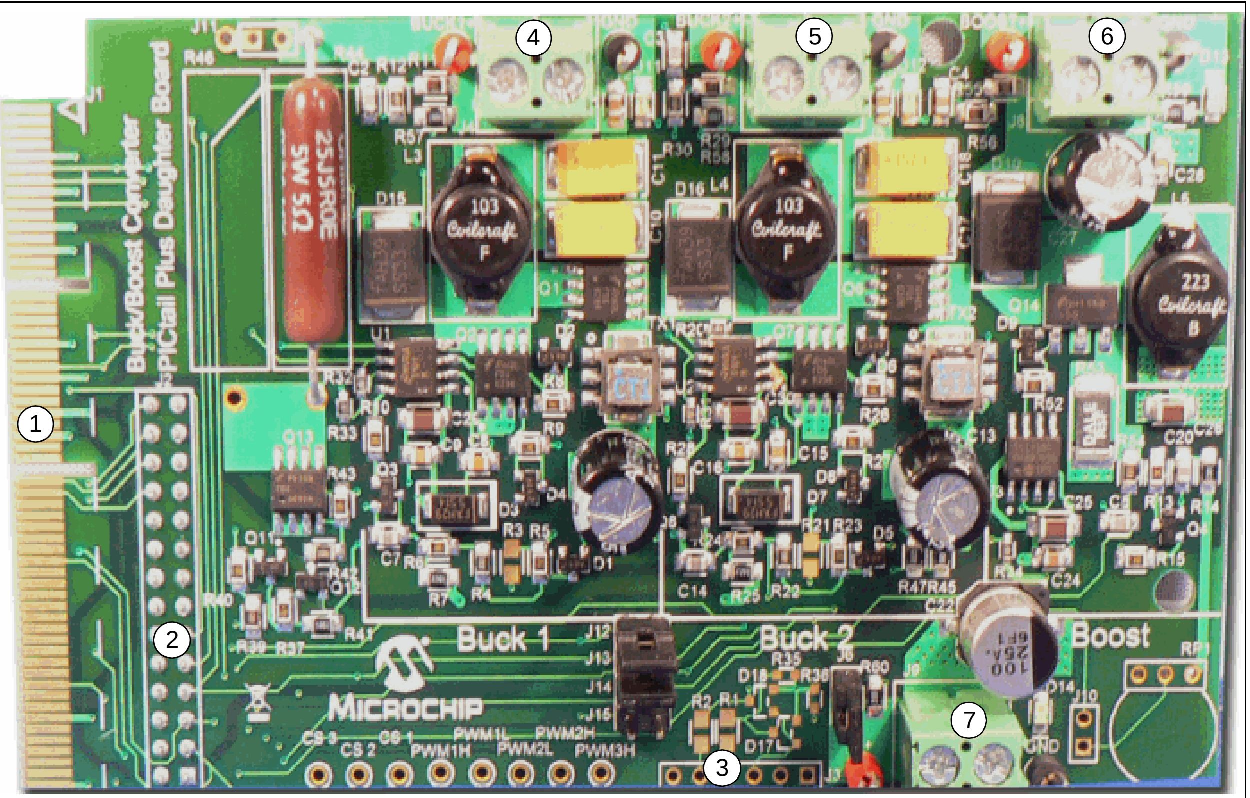
This chapter lists and describes the hardware elements and components of the Buck/Boost Converter PICtail Plus Daughter Board (also referred to as Daughter Board). The following topics are included:

- Daughter Board Connectors
- Using the Daughter Board with the Explorer 16 Development Board
- Using the Daughter Board with the 16-bit 28-pin Starter Development Board
- Power Rating of Converter Stage
- Power Rating of Converter Stage

2.1 DAUGHTER BOARD CONNECTORS

The Daughter Board consists of different power sections along with the input and output connectors for signal and power connections. Figure 2-1 depicts the Daughter Board, the input and output connectors and their locations.

FIGURE 2-1: BUCK/BOOST CONVERTER PICtail™ PLUS DAUGHTER BOARD



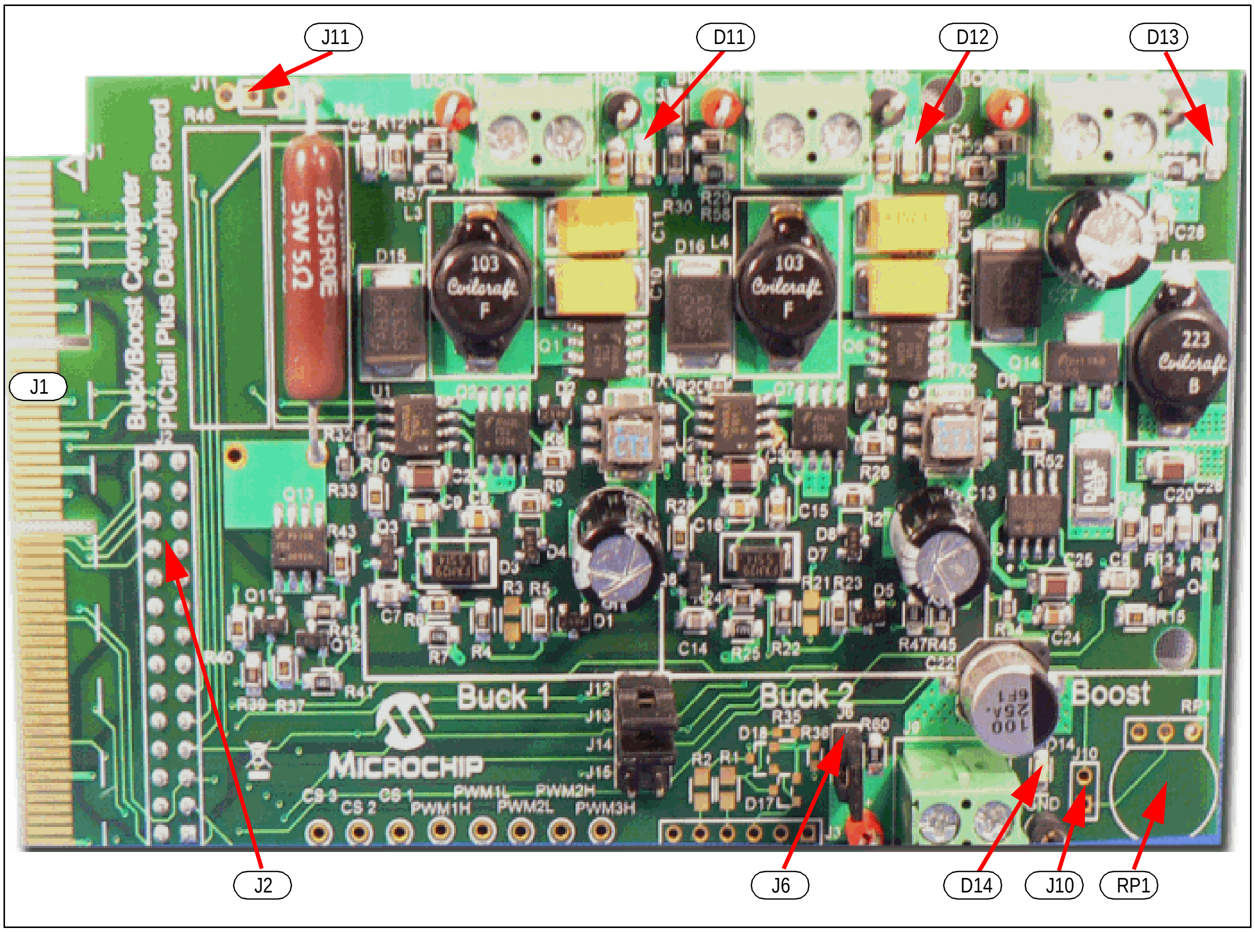
1. J1 – To connect Explorer 16 Development Board
2. J2 – To connect 16-bit 28-pin Starter Development Board
3. J3 – PMBus™ interface connector
4. J4 – VOUT1 connector
5. J5 – VOUT2 connector
6. J8 – VOUT3 connector
7. J9 – Auxiliary input power connector

> **Note:** The Daughter Board only consists of the three power trains of the DC/DC converter sections. Either the 16-bit 28-pin Starter Development Board with the dsPIC33FJ16GS502 device, or the Explorer 16 Development Board with the dsPIC33FJ16GS504 device can be used to control the DC/DC power sections of the Daughter Board. The J1 and J2 connectors provide the necessary signals for control purposes.

2.2 DAUGHTER BOARD USER HARDWARE INTERFACE

This section describes the hardware interface of the Daughter Board and the power rating of each converter's section. Figure 2-2 displays the hardware elements (pin headers, jumpers, LED and potentiometer).

FIGURE 2-2: BUCK/BOOST CONVERTER PICtail™ PLUS DAUGHTER BOARD HARDWARE ELEMENTS



2.2.1 Auxiliary Input Power Connector

The Daughter Board can be connected to the auxiliary/bench power DC source through the J9 input connector. Jumper J6 should be removed while working with the auxiliary/bench power DC source. See Figure A-5 for the location of this jumper.

2.2.2 PMBus Interface Connector J3

The Daughter Board allows the user to implement the PMBus on the SMPS dsPIC DSC device using the J3 connector. See Figure A-6 for the location of this jumper.

2.2.3 16-bit 28-pin Starter Development Board Connector J2

The two converter stage sections of the Daughter Board can be controlled using the 16-bit 28-pin Starter Development Board. Table 2-1 lists all of the power and signal connections on the Daughter Board J2 connector to the user interface with the 16-bit 28-pin Starter Development Board. See Figure A-6 for the location of this connector.

TABLE 2-1: SIGNAL AND POWER CONNECTION FOR 16-BIT 28-PIN STARTER DEVELOPMENT BOARD (J2)

Pin Number Primary	Assignment	Primary Use
1	NC	Not Connected
2	AN0	Analog Input 0 (Buck Converter 1 current)
3	AN1	Analog Input 1 (Buck Converter 1 voltage)
4	AN2	Analog Input 2 (Buck Converter 2 current)
5	AN3	Analog Input 3 (Buck Converter 2 voltage)
6	AN4	Analog Input 4 (Input Voltage)
7	NC	Not Connected
8	VSS	Ground reference for logic and I/O pins
9	NC	Not Connected
10	NC	Not Connected
11	NC	Not Connected
12	NC	Not Connected
13	VDD	Positive supply for logic and I/O pins
14	NC	Not Connected
15	RB15	PMBUSAUX2
16	RB5	PMBUSAUX1
17	SCL	SCL/TX
18	SDA	SCL/RX
19	VSS	Ground reference for logic and I/O pins
20	VDD	+3.3V_DIG
21	PWM3H	PWM Boost Converter
22	I/O	Load
23	PWM2H	PWM 2 High Output (Buck Converter 2)
24	PWM2L	PWM 2 Low Output (Buck Converter 2)
25	PWM1H	PWM 1 High Output (Buck Converter 1)
26	PWM1L	PWM 1 Low Output (Buck Converter 1)
27	NC	Not Connected
28	+9V	Input Voltage for two buck stages

2.2.4 Explorer 16 Development Board Connector J1

The two buck sections and one boost section of the Daughter Board can be controlled using the Explorer 16 Development Board. Table 2-2 lists all the power and signal connections on the Daughter Board J1 connector to the user interface with the Explorer 16 Development Board. See Figure A-6 for the location of this connector.

TABLE 2-2: SIGNAL AND POWER CONNECTION FOR THE EXPLORER 16 DEVELOPMENT BOARD (J1)

Pin Number Primary	Assignment	Primary Use
79	AN0	Analog Input 0 (Buck Converter 1 current)
80	AN1	Analog Input 1 (Buck Converter 1 voltage)
45	PWM1H	PWM 1 High Output (Buck Converter 1 drive)
46	PWM1L	PWM 1 Low Output (Buck Converter 1 drive)
8	AN2	Analog Input 2 (Buck Converter 2 current)
6	AN3	Analog Input 3 (Buck Converter 2 voltage)
12	PWM2H	PWM 2 High Output (Buck Converter 2 drive)
11	PWM2L	PWM 2 Low Output (Buck Converter 2 drive)
50	AN4	Analog Input 4 (Input Voltage)
102	AN8	Analog Input 8 (Boost Converter Voltage)
80	AN9	Analog Input 9 (Boost Converter Voltage)
17	PWM3H	PWM3H High Output (Boost Converter drive)
13	I/O	Load Drive for Buck Converter 1 Load
101	AN10	Analog Input 10 (POT RP1)
65	RB15	PMBUSAUX2
66	RB5	PMBUSAUX1
67	SCL	SCL/TX
68	SDA	SCL/RX
9, 10, 119, 120	3.3VDIG_GND	Ground Reference for Digital I/O pins
21, 22, 53, 54, 107, 108	+3.3V_DIG	Digital 3.3V
15, 16, 41, 42	9VANA_GND	Ground Reference for Logic and I/O pins
25, 26, 57, 58	+9V	9V Input Voltage
1-5, 14, 18-20, 23, 24, 27-30, 33-40, 43, 44, 49, 51, 52, 55, 56, 59-62, 69-78, 81-95, 97-100, 103-106, 109-118	NC	Not Connected

2.2.5 VOUT1 J4 (Buck1+)

An external load can be connected to VOUT1 through the J4 connector. One on-board parallel resistor, R44 (5Ω/5W), is connected at the output of VOUT1 through MOSFET Q13 to optionally load the Buck 1 converter circuit. Resistor R45 is on-board, and there is space to solder resistor R46 onto the board. When resistor R46 is connected to VOUT1, the J11 jumper must be open while working with +9V power from the control board. The on-board load resistor can be connected to VOUT1 by controlling the signal name “Load”. The “Load” signal is the I/O pin of the SMPS dsPIC DSC device, and is active-high. See Figure A-2 for the location of this connector.

2.2.6 VOUT2 J5 (Buck2+)

An external load can be connected to VOUT2 through the J5 connector. VOUT2 can load up to a maximum of 3 amps when the auxiliary input voltage source is connected at the J9 input connector. See Figure A-3 for the location of this connector.

2.2.7 VOUT3 J8 (Boost)

An external load can be connected to VOUT3 through the J8 connector. VOUT3 can load up to 0.75 amps when the auxiliary input voltage source is connected at the J9 input connector. See Figure A-4 for the location of this connector.

2.2.8 Jumpers

The Daughter Board consists of three jumpers that determine its features. Table 2-3 lists jumpers and their functions.

TABLE 2-3: JUMPERS

Jumpers	Description	Default Configurations
J6	Select either 9V power provided by the Explorer 16 Development Board or 16-bit 28-pin Starter Development Board, and an external power supply	Short with jumper header (closed)
J10	Connects potentiometer RP1 to AN10 on Explorer 16 Development Board	Open
J11	Connects R46 load resistor to VOUT1	Open
J12	Buck 2 voltage feedback selection	Short with jumper header (closed)
J13	Buck 2 current feedback selection	Short with jumper header (closed)
J14	Boost current feedback selection	Open
J15	Boost voltage feedback selection	Open

2.2.9 Potentiometer and LED

The Daughter Board consists of a potentiometer and LEDs for the user application. Table 2-4 lists components and their functions.

TABLE 2-4: POTENTIOMETERS AND LED

Label	Hardware Elements
RP1	Potentiometer connected to AN10 of Explorer 16 Development Board controller
D11	Buck 1 output LED
D12	Buck 2 output LED
D13	Boost output voltage LED
D14	Input voltage LED

2.2.10 Test Points

The Daughter Board provides the various test points of the PWM signals, feedback signals and input and output voltages for the user application. Table 2-5 lists the PWM test points that can be used to check the PWM gate pulse for all three power stages.

TABLE 2-5: PWM TEST POINTS

Test Points	Description
PWM1H	Buck MOSFET gate drive of Buck 1 converter stage
PWM1L	Synchronous MOSFET gate drive of Buck 1 converter stage
PWM2H	Buck MOSFET gate drive of Buck 2 converter stage
PWM2L	Synchronous MOSFET gate drive of Buck 2 converter stage
PWM3H	Boost MOSFET gate drive for Boost converter stage

Table 2-6 lists the feedback signal test points that can be used to check the feedback signal waveforms and values.

TABLE 2-6: FEEDBACK SIGNAL TEST POINTS

Test Points	Description
Current Sense1	Current feedback signal for Buck 1 converter stage
Current Sense2	Current feedback signal for Buck 2 converter stage
Current Sense3	Current feedback signal for Boost converter stage

Table 2-7 shows the power test points that can be used to verify the input and output voltages.

TABLE 2-7: POWER TEST POINTS

Test Points	Description
V+	Input Voltage Test Point
Buck1+	VOUT1 voltage test point
Buck2+	VOUT2 voltage test point
Boost+	VOUT3 voltage test point
GND	Ground potential test point

2.3 USING THE DAUGHTER BOARD WITH THE EXPLORER 16 DEVELOPMENT BOARD

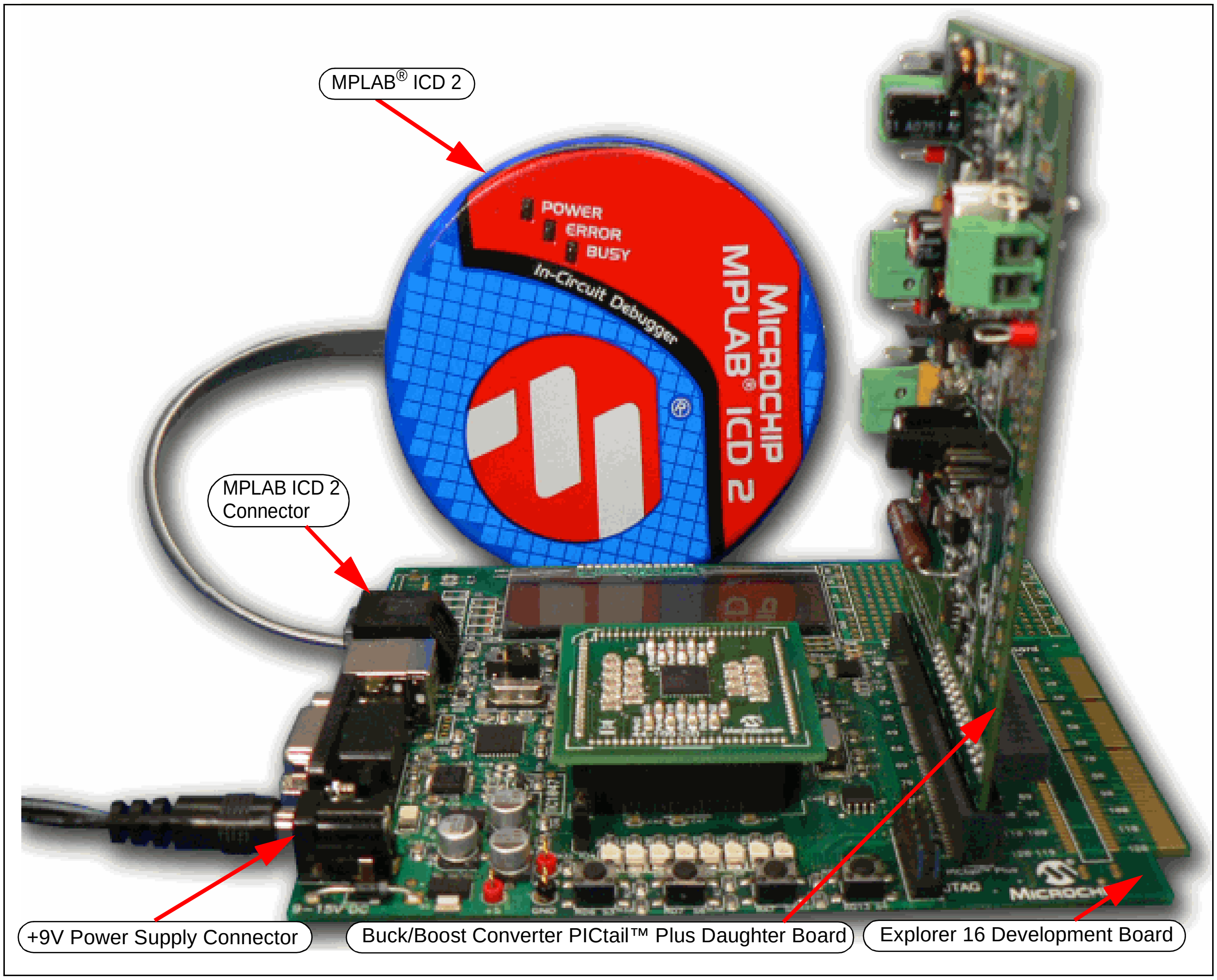
This section describes the hardware connection of the Daughter Board with the Explorer 16 Development Board. Figure 2-3 displays the Daughter Board hardware connection (MPLAB ICD 2 and power supply) to the Explorer 16 Development Board.

The dsPIC33FJ16GS504 SMPS device controls both buck stages (Buck 1 and Buck 2), as well as the boost stage through the Explorer 16 Development Board simultaneously.

> **Note:** To operate all three converters using the Explorer 16 Development Board, ensure that J12, J13 and J6 are shorted with the jumper header, and J14 and J15 are open before powering up the board.

The potentiometer R6 (10 kΩ), in series with the R12 resistor on the Explorer 16 Development Board, is connected to analog input channel (AN5) of the SMPS dsPIC DSC device. The potentiometer R6 on the Daughter Board is connected to the analog input channel (AN10) through the J10 jumper. Both potentiometers can be used for development purposes to simulate any feedback signal.

FIGURE 2-3: DAUGHTER BOARD CONNECTED TO THE EXPLORER 16 DEVELOPMENT BOARD

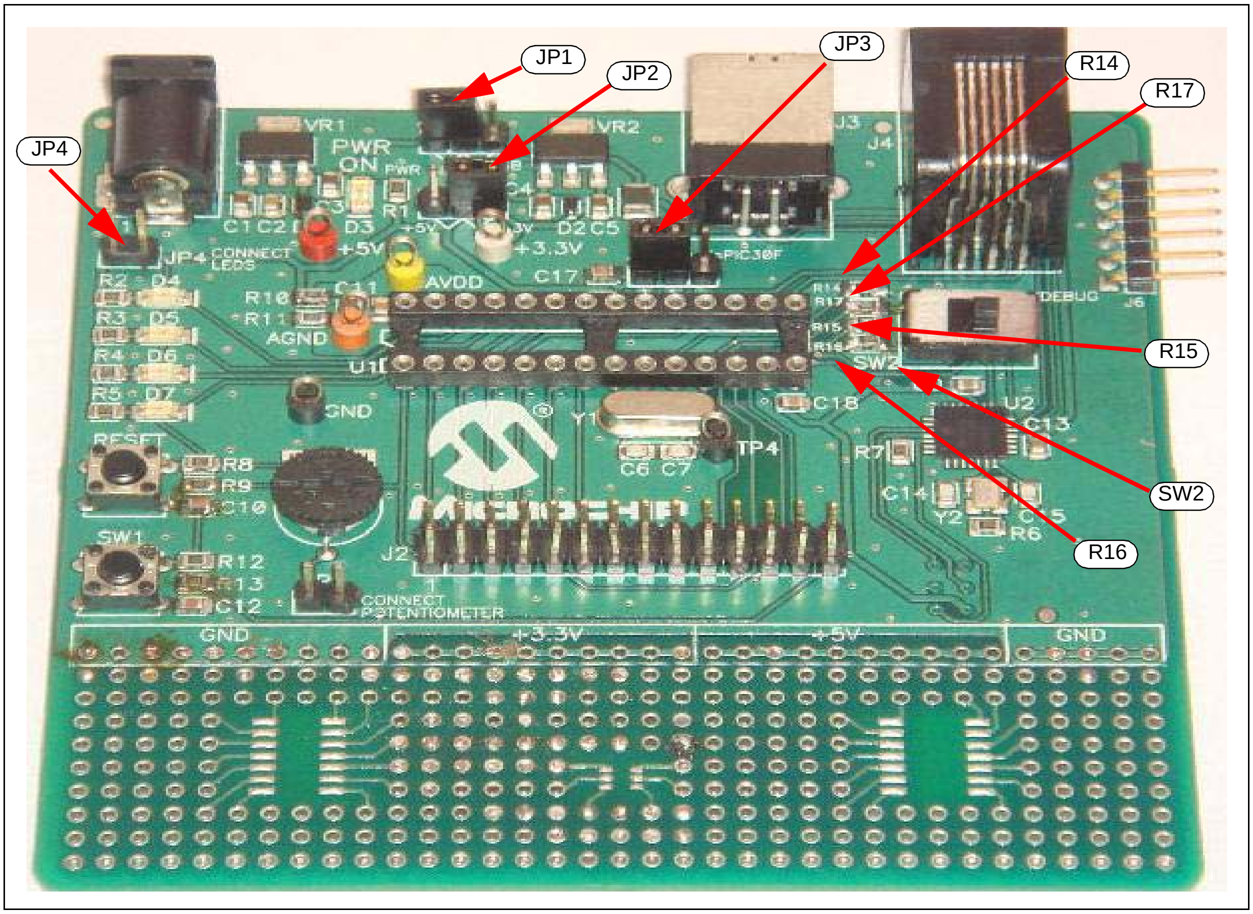


2.4 USING THE DAUGHTER BOARD WITH THE 16-BIT 28-PIN STARTER DEVELOPMENT BOARD

This section describes the use of a 16-bit 28-pin Starter Development Board with the Buck/Boost Converter PICtail Plus Daughter Board.

Figure 2-4 shows the 16-bit 28-pin Starter Development Board and its hardware elements. For more details, refer to the "*16-Bit 28-Pin Starter Development Board User's Guide*" (DS51656), which is available from the Microchip website (http://www.microchip.com).

FIGURE 2-4: 16-BIT 28-PIN STARTER DEVELOPMENT BOARD

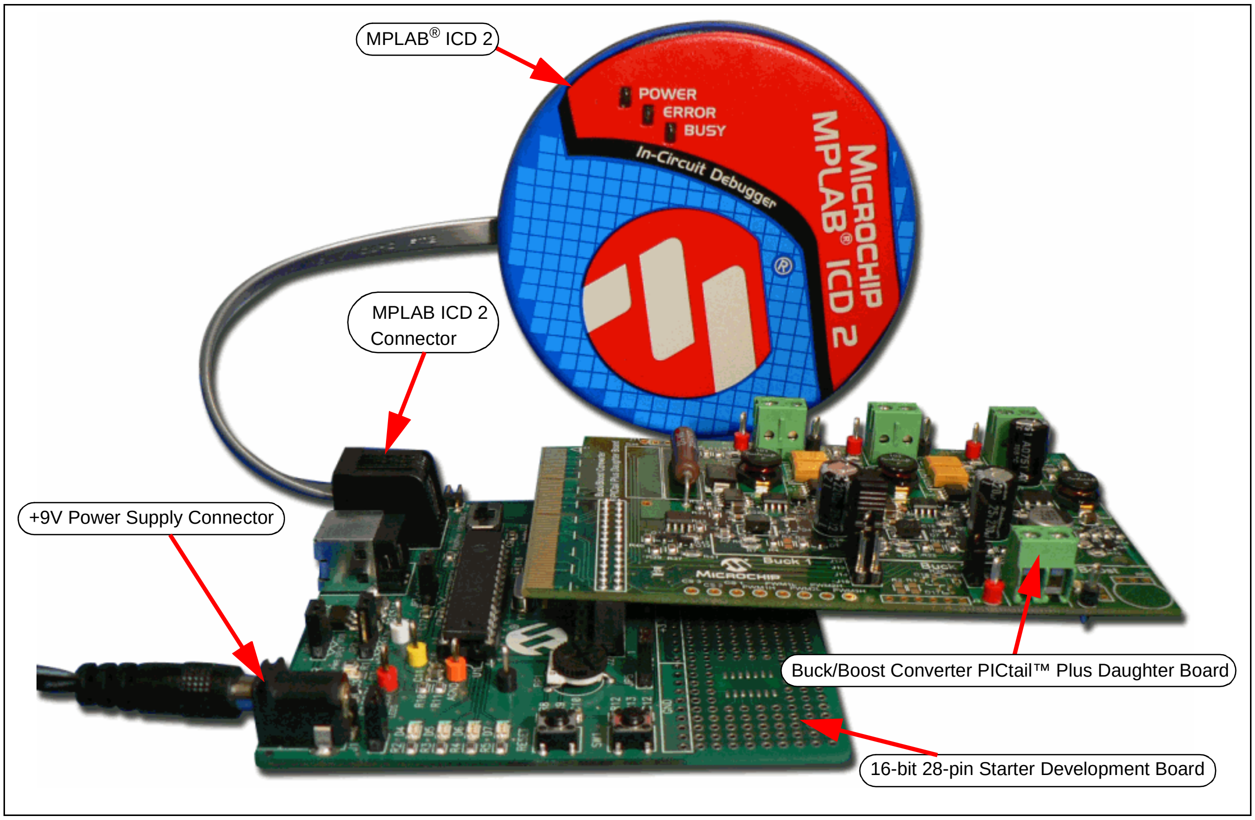


The potentiometer, RP1 (10 kΩ), with the J5 jumper on the 16-bit 28-pin Starter Development Board, is connected to the analog input channel (AN5) of the SMPS dsPIC DSC device. Figure 2-5 shows the connection of a 16-bit 28-pin Starter Development Board to a Daughter Board with ICD 2 and a 9V power supply.

Ensure that the following changes are made to the 16-bit 28-pin Starter Development Board prior to connecting the 16-bit 28-pin Starter Development Board to the Daughter Board:

- Remove resistors R14 and R15 (to control Buck 2 or Boost converter)
- JP1 in pin 1-2 position (supply)
- JP2 in pin 2-3 position (+3.3V)
- JP3 in 1-2 position (dsPIC33F/PIC24)
- JP4 open
- SW2 in USB/DEBUG mode

FIGURE 2-5: DAUGHTER BOARD HARDWARE CONNECTED TO A 16-BIT 28-PIN STARTER DEVELOPMENT BOARD



2.4.1 16-bit 28-pin Starter Development Board Controls Buck 1 and Buck 2 Stages (Default Jumper Configuration)

The dsPIC33FJ16GS502 SMPS device controls buck stages Buck 1 and Buck 2 through the 16-bit 28-pin Starter Development Board as the default configuration on the Daughter Board, refer to Table 2-3. The two buck stages can be controlled as multi-phase or as two parallel converters by shorting the VOUT1 (Buck1+) and VOUT2 (Buck2+) output, and by programming the output of buck stages to the same output voltage value.

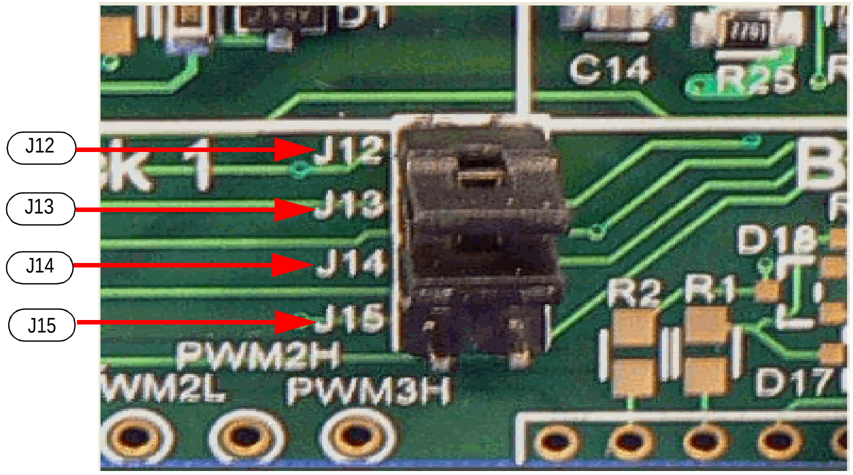
Note 1: To operate the two buck converters using the 16-bit 28-pin Starter Development Board, ensure that J12, J13 and J6 are shorted with the jumper header, and J14 and J15 are open before powering up the board.

2: The software file `Buck1 Voltage Mode with 28P Starter Board` on the Buck/Boost Converter PICtail Plus Daughter Board CD only provides control for the Buck 1 stage.

2.4.2 16-bit 28-pin Starter Development Board Controls Buck 1 and Boost Stages

This section describes the hardware changes that must be performed to control the Buck 1 and Boost stages. Figure 2-6 displays the feedback jumper, which must be modified in the Daughter Board. See Figure A-4 for the complete Daughter Board schematics.

FIGURE 2-6: FEEDBACK JUMPERS



2.4.2.1 HARDWARE

The following hardware changes are required in the Daughter Board to enable control of the Buck 1 and Boost stage:

- Jumper J12 and J13: Open
- Jumper J14 and J15: Short with jumper header (close)

2.4.2.2 SOFTWARE

The following additional changes in software are required to enable control of the Buck 1 and Boost stage:

- Boost Current feedback through analog input channel (AN2)
- Boost Voltage feedback through analog input channel (AN3)
- Boost PWM output (PWM3H)
- PWM2 output pin must be controlled by I/O port and driven low

> **Note:** The software file `Buck1 Voltage Mode with 28P Starter Board` on the Buck/Boost Converter PICtail Plus Daughter Board CD only provides control for the Buck 1 stage.

2.5 POWER RATING OF CONVERTER STAGE

All three DC/DC power stages in a Daughter Board can be loaded externally through the output terminal blocks J4, J5 and J8. For loading any power stage externally, the user must provide an auxiliary power source to the Daughter Board through input terminal block J9.

2.5.1 Buck 1 Converter

The Buck 1 converter stage is rated for a maximum output current of 3 amps through the J4 connector. The output voltage of the buck converter (VOUT1) can be programmed for 0V-5V output. The hardware gain [5k/(3.3k + 5k)] of the voltage feedback of VOUT1 is provided by the resistor divider network of R11 and R12. The hardware gain of the current feedback is provided by the current transformer (Tx1) with turns ratio (1:60) and burden resistor R5. The circuitry consists of R6, R7, C7 and Q3, and provides slope compensation for current feedback (Current Sense1).

2.5.2 Buck 2 Converter

The Buck 2 converter stage is rated for a maximum output current of 3 amps through the J5 connector. The output voltage of the buck converter (VOUT2) can be programmed for 0V-5V output. The hardware gain [5k/(3.3k + 5k)] of the voltage feedback of VOUT2 is provided by the resistor divider network of R29 and R30. The hardware gain of the current feedback is provided by the current transformer (Tx2) with turns ratio (1:60) and burden resistor R23. The circuitry consists of R24, R25, C14 and Q8, and provides slope compensation for current feedback (Current Sense2).

2.5.3 Boost Converter

The Boost converter stage is rated for a maximum output current of 0.75 amps through the J8 connector. The output voltage of the boost converter (VOUT3) can be programmed up to a maximum output of 20V. The hardware gain [20k/(20k + 3.3k)] of the voltage feedback of VOUT3 is provided by the resistor divider network of R55 and R56. The hardware gain of the current feedback is provided by the current sense resistor R53 (current sense boost/Current Sense3). The circuitry consists of R13, R14, C20 and Q4 and provides slope compensation for current feedback (current sense boost/Current Sense3).

NOTES:

Chapter 3. Getting Started

This chapter provides details to get started using the Daughter Board with the 16-bit 28-pin Starter Development Board using the dsPIC33FJ16GS502 SMPS device. The 16-bit 28-pin Starter Development Board is modified as per **Section 2.4 "Using the Daughter Board with the 16-bit 28-pin Starter Development Board"**. While working with the Daughter Board along with the Explorer 16 Development Board using a dsPIC33FJ16GS504 device, please refer to the Explorer 16-specific note that is specified in the corresponding instructions.

The following topics are covered in this chapter:

- Overview
- Creating the Project
- Building the Code
- Programming the Device
- Debugging the Code

3.1 OVERVIEW

This section describes the main features of MPLAB IDE and the MPLAB ICD 2 In-Circuit Debugger because they are used in the 16-bit 28-pin Starter Development Board. This section provides information on performing the following tasks:

1. Creating a project using the Project Wizard.
2. Assembling and linking the code, and setting the Configuration bits.
3. Setting up MPLAB IDE to use the MPLAB ICD 2 In-Circuit Debugger.
4. Programming the chip with MPLAB ICD 2.
5. Viewing code execution.
6. Viewing registers in the Watch window.
7. Setting a breakpoint and setting the code halt in the specific location.
8. Using the function keys to Reset, Run, Halt and Single Step the code.

Before performing these steps, save the Buck/Boost Converter PICtail Plus Daughter Board firmware from the CD in the following location: `C:\Program Files\Microchip\`

Note 1: The demo software using 16-bit 28-pin Starter Development Board will be under folder: `C:\Program Files\Microchip\Buck Boost PICtail Plus Board\Buck1 Voltage Mode with 28P Starter Board`.

2: The demo software using Explorer 16 Development Board will be under the folder: `C:\Program Files\Microchip\Buck Boost PICtail Plus Board\3-Stage Voltage Mode with Explorer 16`

3: Both the above folders comprise of the project file (`*.mcp`) and workspace file (`*.mcw`). The user can use these files to program the device, or the user can create their own project and workspace file by performing the steps listed in this Chapter.

3.2 CREATING THE PROJECT

This section describes the process of creating a project and workspace in MPLAB IDE. In any particular folder, one project and one workspace are present.

Note:	These instructions presume the use of MPLAB IDE v8.10 or later.

A project consists of files that are used to build an application (source code, linker script files, etc.) along with their association to various build tools and build options. The workspace consists of the following features:

- One or more projects
- Information on the selected device
- Debug tool and/or programmer, open windows and their location
- Other IDE configuration settings

MPLAB IDE provides a Project Wizard to create new projects.

3.2.1 Creating the Project

Using the Project Wizard involves four steps:

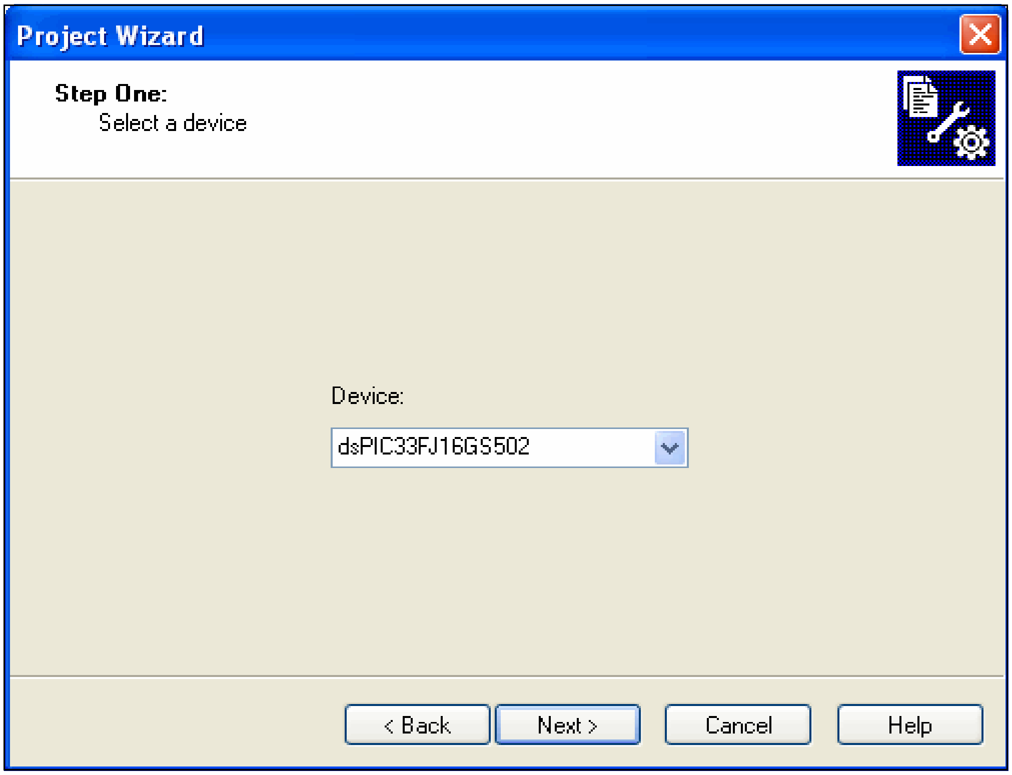
- Selecting the Device
- Selecting the Language Toolsuite
- Naming the Project
- Adding Files to the Project

Use the following procedures to complete each of the four steps.

3.2.1.1 PROJECT WIZARD STEP ONE – SELECTING THE DEVICE

1. Start MPLAB IDE.
2. Close any open workspace (*File>Close Workspace*).
3. Select *Project>Project Wizard*. The Welcome dialog appears.
4. Click **Next** to continue. The Select a device dialog appears.
5. From the Device drop-down list, select the required device, as shown in Figure 3-1.

FIGURE 3-1: SELECT A DEVICE



6. Click **Next** to continue. The Select a language toolsuite dialog appears, as shown in Figure 3-2.

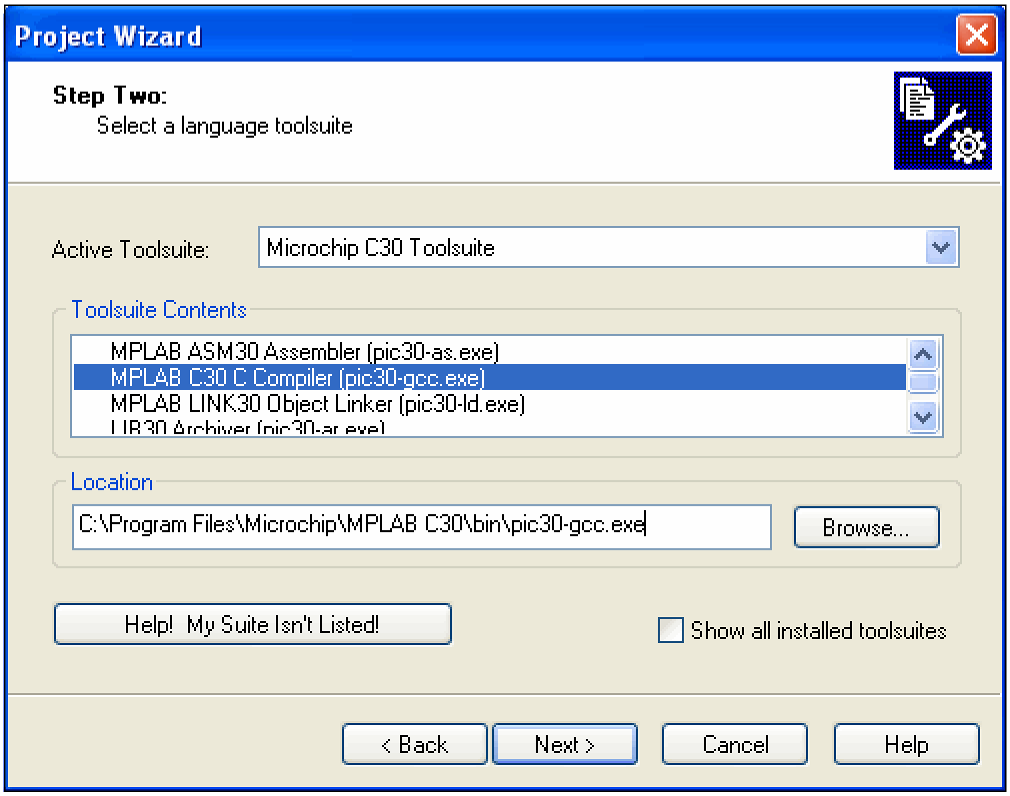
Note:	While using the Explorer 16 Development Board, select the dsPIC33FJ16GS504 device.

3.2.1.2 PROJECT WIZARD STEP TWO – SELECTING THE LANGUAGE TOOLSUITE

1. As shown in Figure 3-2, select Microchip C30 Toolsuite from the Active Toolsuite drop-down list. This toolsuite includes the assembler and linker that is to be used in the project.

Note:	To create a project that consists of source files written in a language other than Microchip Assembly, select the specific language toolsuite from the drop-down menu.

FIGURE 3-2: SELECT LANGUAGE TOOLSUITE



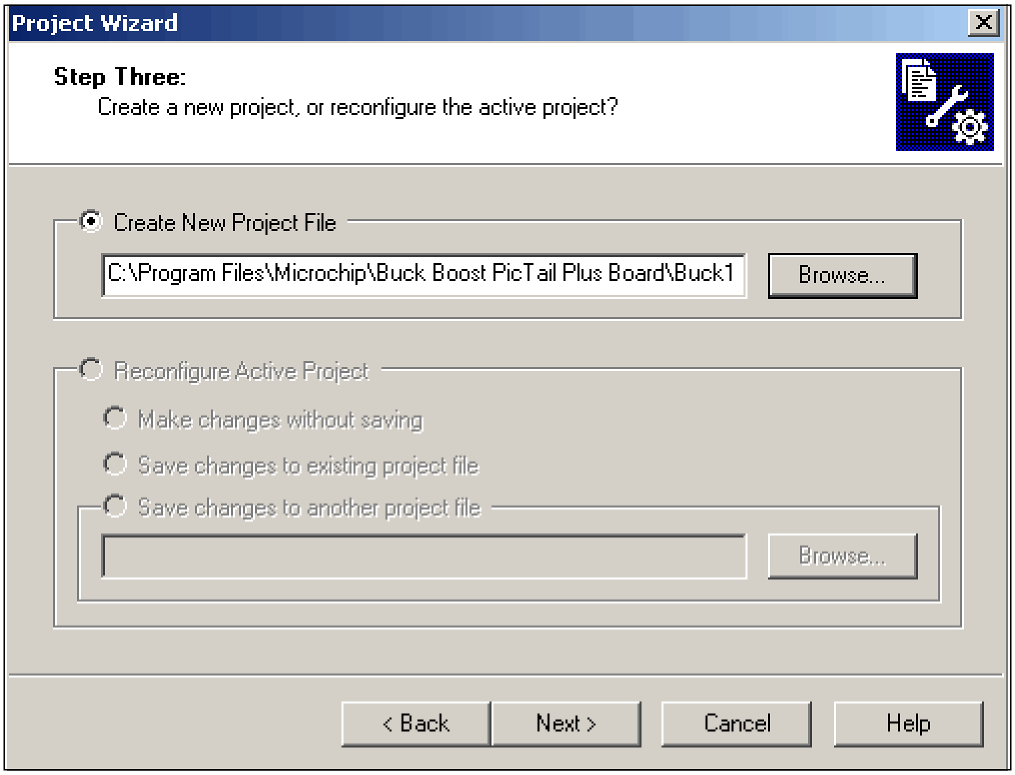
2. Select MPLAB C30 C Complier (`pic30-gcc.exe`) from the Toolsuite Contents options.
3. Click **Next** to continue. The Create a new project, or reconfigure the active project? dialog appears, as shown in Figure 3-3.

3.2.1.3 PROJECT WIZARD STEP THREE – NAME YOUR PROJECT

1. As shown in Figure 3-3, under Create New Project File, click **Browse...**, and navigate to:
   `C:\Program Files\Microchip\Buck BoostPicTail Plus Board\Buck1 Voltage Mode with 28P Starter Board.`

Note:	While using the Explorer 16 Development Board, navigate to the following path in the “Create New Project File”: `C:\Program Files\Microchip\Buck Boost PicTail Plus Board\3-Stage Voltage Mode with Explorer 16.`

FIGURE 3-3: NAME YOUR PROJECT



2. In the resulting Save Project As dialog, enter the project name as `Buck1 Voltage Mode.mcp`, and then click **Save**.

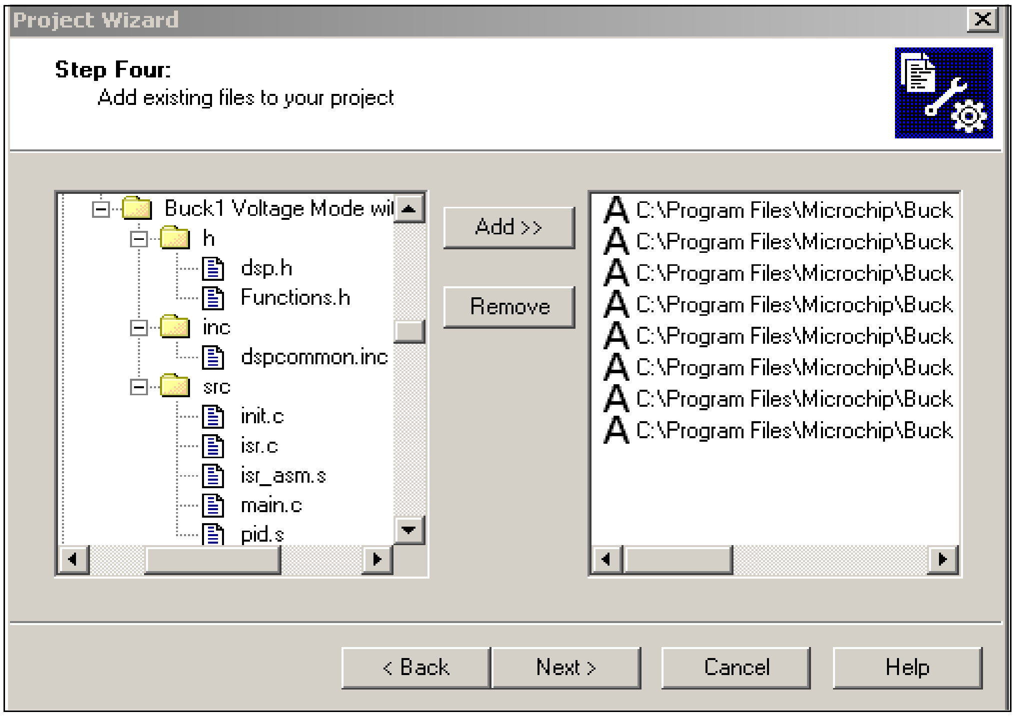
Note:	While using the Explorer 16 Development Board, enter the project name as `3-Stage Voltage Mode.mcp`.

3. Click **Next** to continue. The Add existing files to your project dialog appears, as shown in Figure 3-4.

3.2.1.4 PROJECT WIZARD STEP FOUR – ADD FILES TO YOUR PROJECT

1. As shown in Figure 3-4, from the left pane, navigate to `C:\...\Buck1 Voltage Mode with 28P Starter Board`, and select the following files:
   - `init.c`
   - `isr.c`
   - `main.c`
   - `dsp.h`
   - `function.h`
   - `dspcommon.inc`
   - `isr_asm.s`
   - `pid.s`

FIGURE 3-4: ADD FILES TO PROJECT



2. Click **Add** to include the files in the project. The selected files appear in the right pane.
3. Click **Next** to continue. The Summary dialog appears as shown in Figure 3-5.

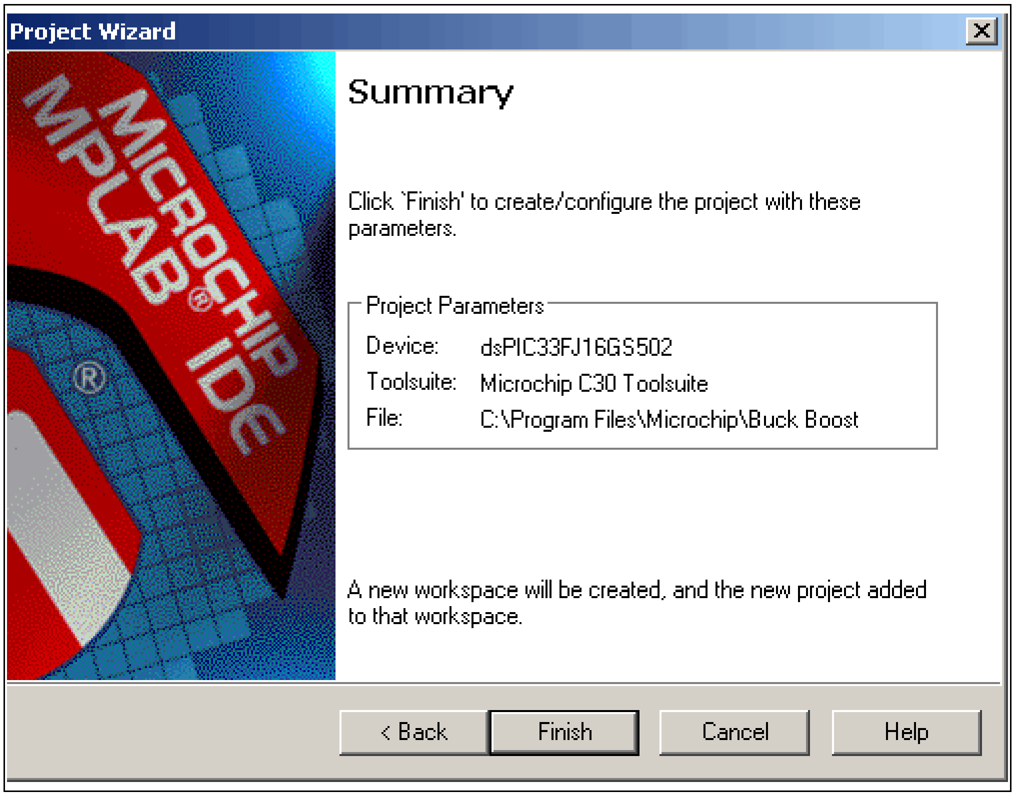
Note: While using the Explorer 16 Development Board, navigate to the following path: `C:\program Files\Microchip\Buck Boost PICtail Plus Board\3-Stage Voltage Mode with Explorer 16`, and select the following files:

- `init.c`
- `isr.c`
- `main.c`
- `dsp.h`
- `function.h`
- `dspcommon.inc`
- `isr_asm.s`
- `pid.s`

3.2.1.5 PROJECT SUMMARY

Click **Finish** to complete the project.

FIGURE 3-5: SUMMARY DIALOG



After completing the project wizard, the MPLAB IDE project window lists the following files in the `Source Files` folder:

- `isr.c`
- `main.c`
- `isr_asm.s`
- `pid.s`
- `init.c`

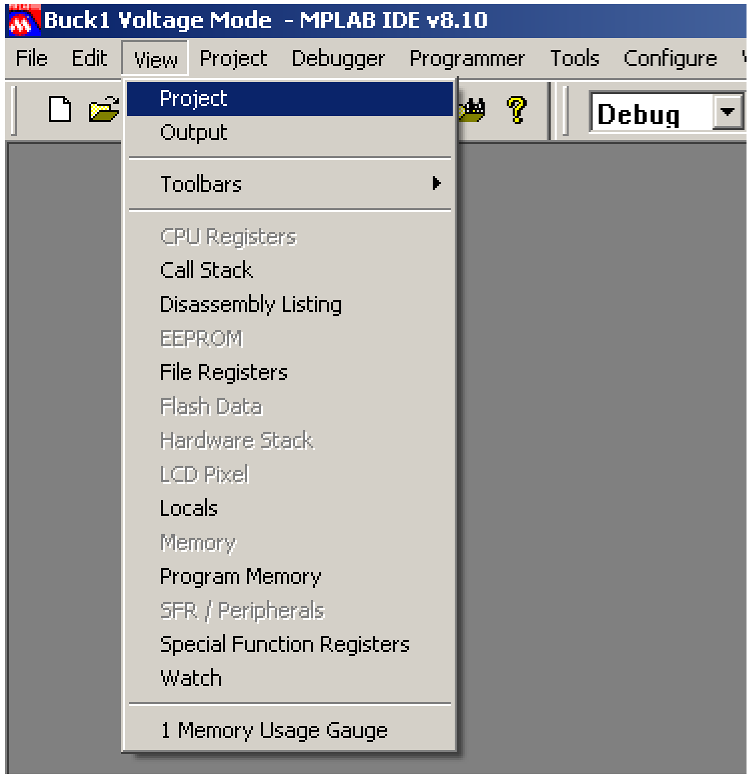
Note: While using the Explorer 16 Development Board, the MPLAB IDE project window lists the following files in the Source Files folder:

- `init.c`
- `isr.c`
- `main.c`
- `isr_asm.s`
- `pid.s`

3.2.1.6 VIEWING THE PROJECT

1. Click *View>Project* from the MPLAB IDE menu, as shown in Figure 3-6.

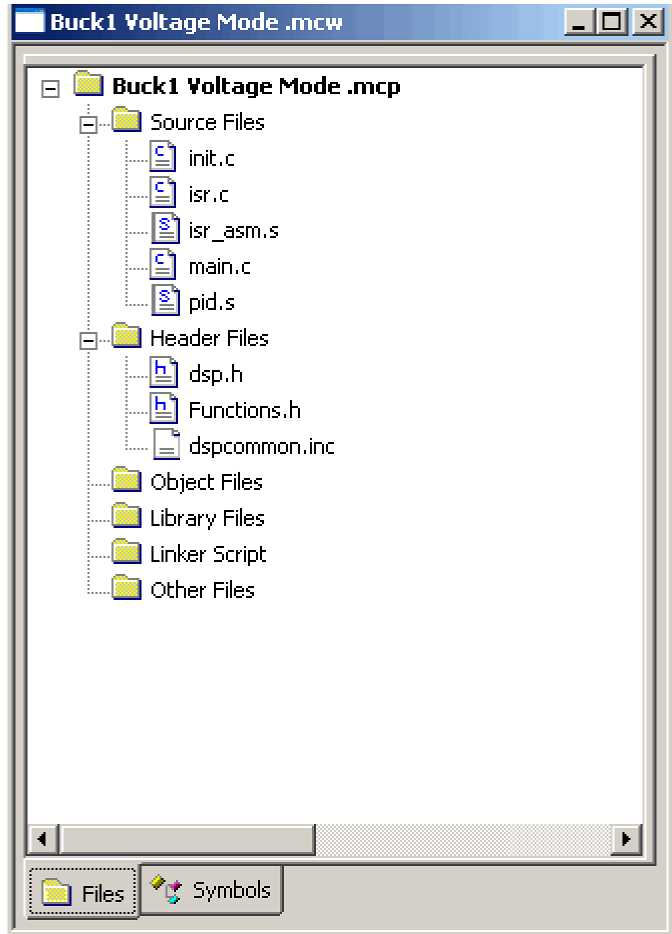
FIGURE 3-6: OPEN PROJECT FILE



The `Buck1 Voltage Mode.mcw` dialog appears, as shown in Figure 3-7. A project, `Buck1 Voltage Mode.mcp`, and workspace, `Buck1 Voltage Mode.mcp`, are created in MPLAB IDE.

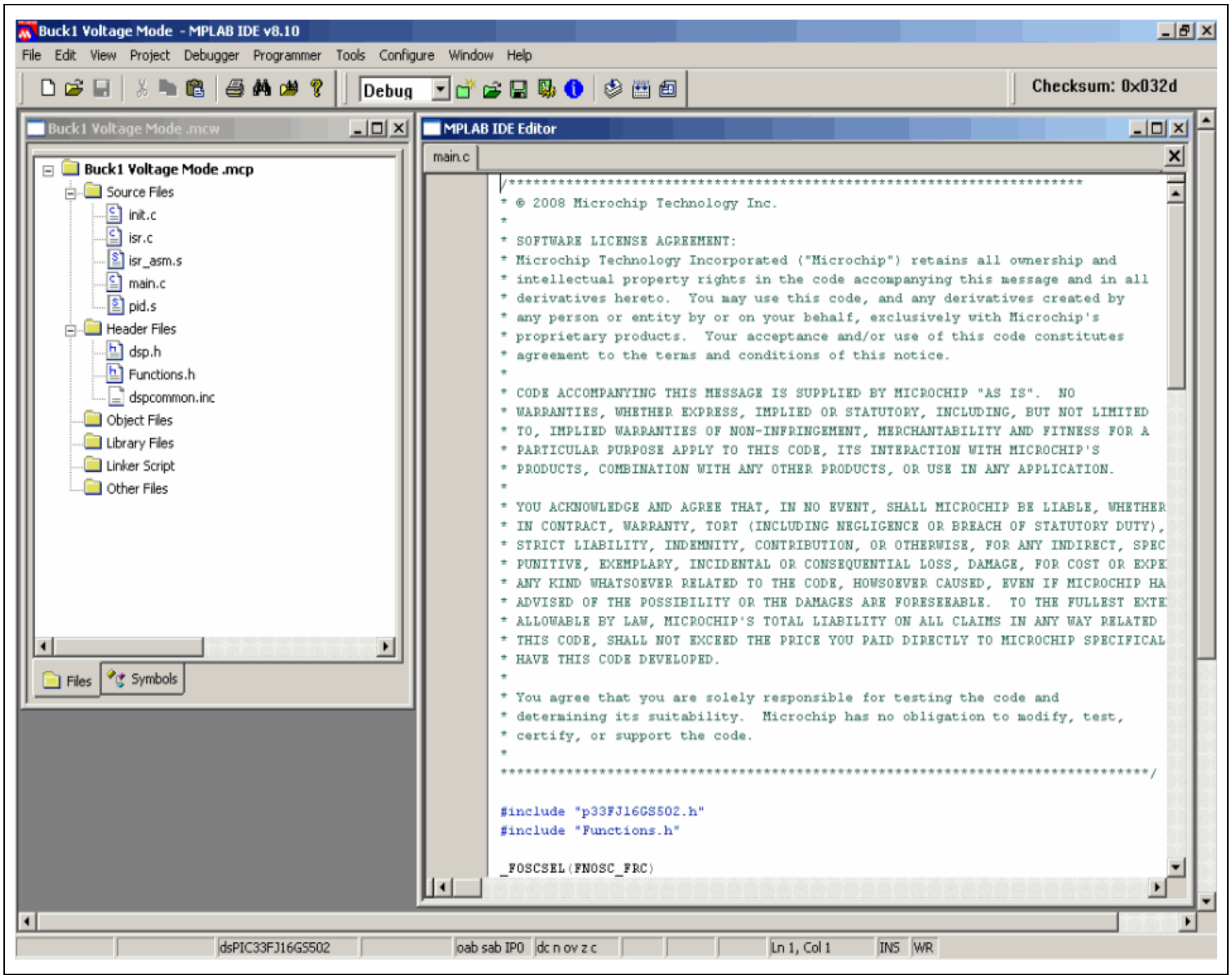
Note:	While using the Explorer 16 Development Board, the `3-Stage Voltage Mode.mcp` appears. A `3-Stage Voltage Mode.mcp` project and workspace, `3-Stage Voltage Mode.mcw`, are created in MPLAB IDE.

FIGURE 3-7: MPLAB® IDE PROJECT WINDOW



2. Double click the `main.c` file in the project window to open the file. The MPLAB IDE Workspace Window appears, as shown in Figure 3-8. This completes the project view process.

FIGURE 3-8: MPLAB® IDE WORKSPACE WINDOW



3.3 BUILDING THE CODE

Building the code consists of the following process:

- Assembling all of the `*.c` and `*.s` files to create the respective object files (`*.o`)
- Linking the object files to create the `3-Stage Voltage Mode.hex` and `3-Stage Voltage Mode.cof` output files

The `.hex` file contains the specific data to program the device. The `.cof` file contains additional information to debug at the source code level.

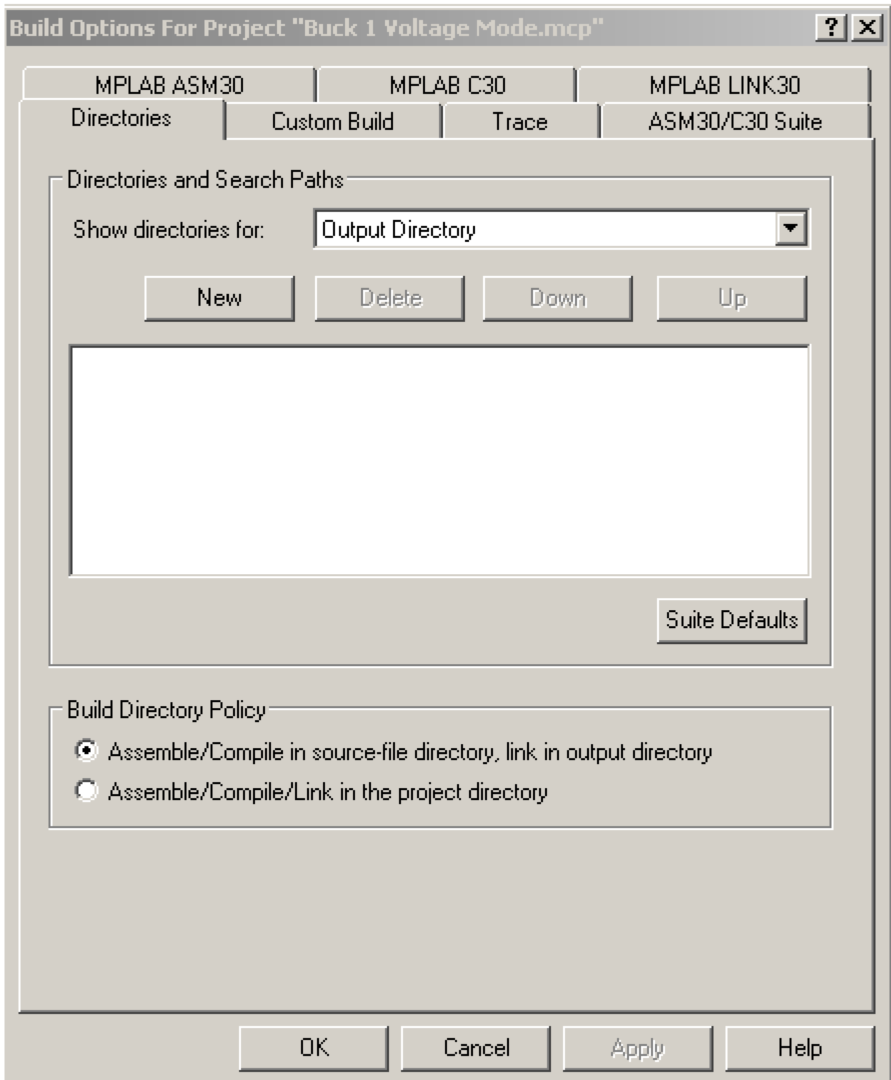
Before building the code, the user must set MPLAB ICD 2 to search for include files and to reserve space for the extra debug code.

3.3.1 Building the Code

To specify the Project Build Options:

1. Select *Build Options>Project* from the Project menu. The Build Options For Project "Buck 1 Voltage Mode.mcp" dialog appears, as shown in Figure 3-9.

FIGURE 3-9: BUILD OPTIONS



2. Select Assemble/Compile/Link in the project directory, and then click **OK**. This completes the code build process.

3.3.2 Linking the ICD 2 for Debugging

Select the Debug option from the drop-down menu of MPLAB IDE, as shown in Figure 3-10, so the linker will build the code for debugging. This sets aside the RAM for the MPLAB ICD 2 for use during debugging. If this is not performed, the MPLAB ICD 2 will not function properly in Debug mode.

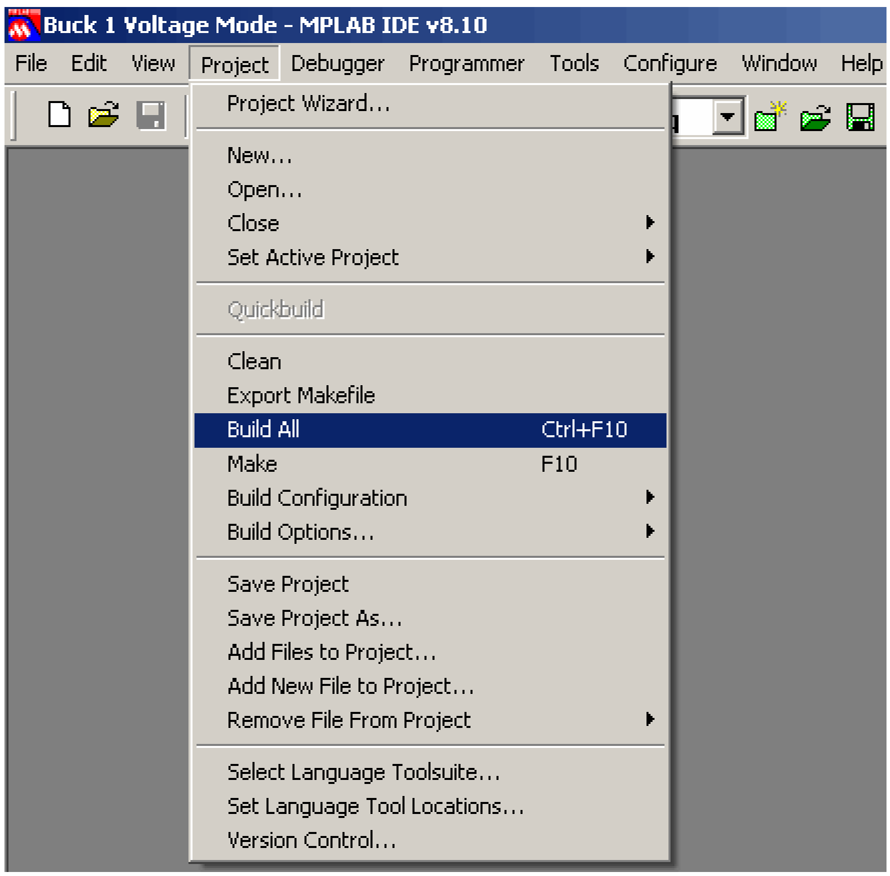
FIGURE 3-10: LINK PROJECT FOR MPLAB® ICD 2

3.3.3 Building the Project

To build the project:

1. Select *Project>Build All* from the MPLAB IDE menu, as shown in Figure 3-11.

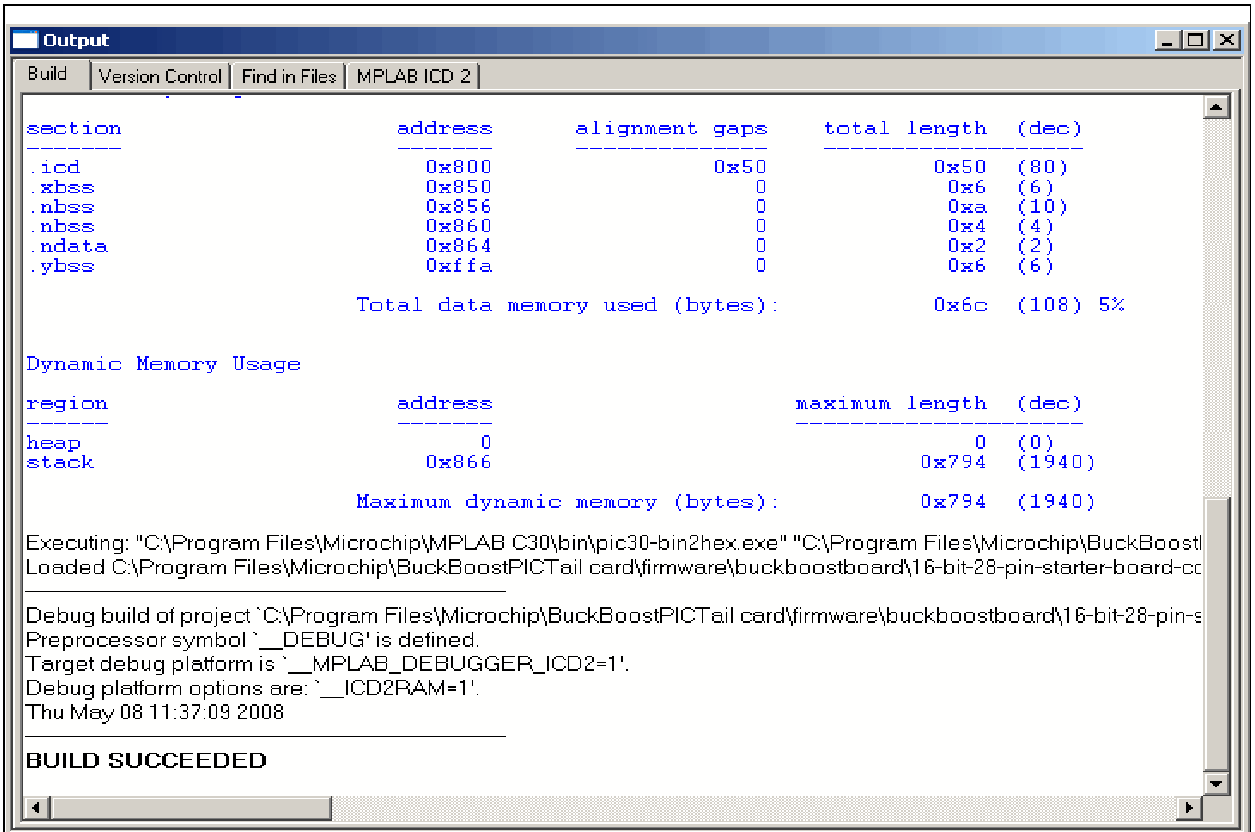
FIGURE 3-11: DualBuck MPLAB® IDE SCREEN



2. Observe the progress of the build in the Output window, as shown in Figure 3-12. This completes the project build process.

The device can be programmed if the build status is BUILD SUCCEEDED. If the build status is BUILD FAILED, the build errors that are listed must be resolved.

FIGURE 3-12: BUILD OUTPUT WINDOW



3.4 PROGRAMMING THE DEVICE

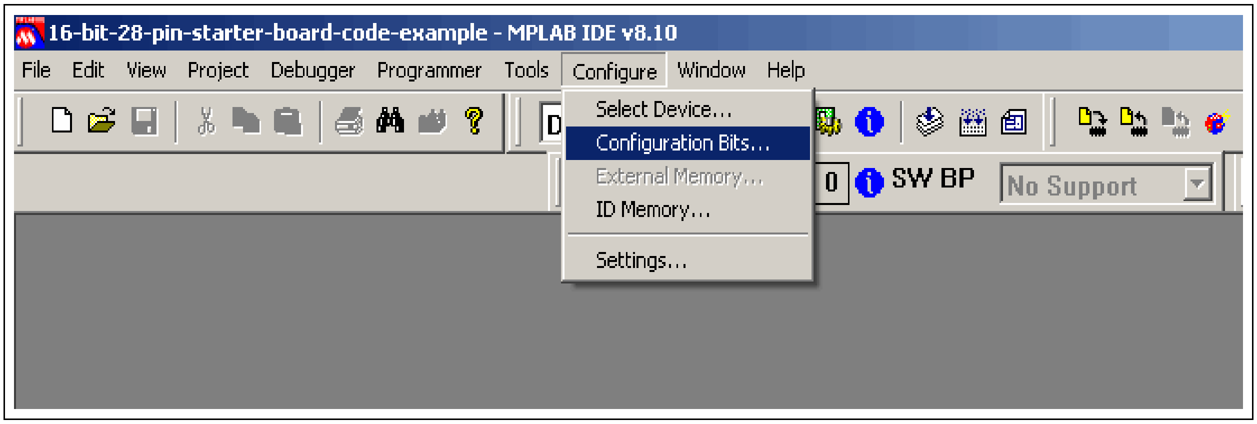
The MPLAB ICD 2 In-Circuit Debugger can be used to program and debug the dsPIC33FJ16GS502 device in-circuit on the Daughter Board.

> **Note:** Before proceeding, ensure that the USB driver for the MPLAB ICD 2 is installed on your PC. Refer to the "*MPLAB® ICD 2 In-Circuit Debugger User's Guide*" (DS51331) for details.

3.4.1 Setting up the Device Configuration

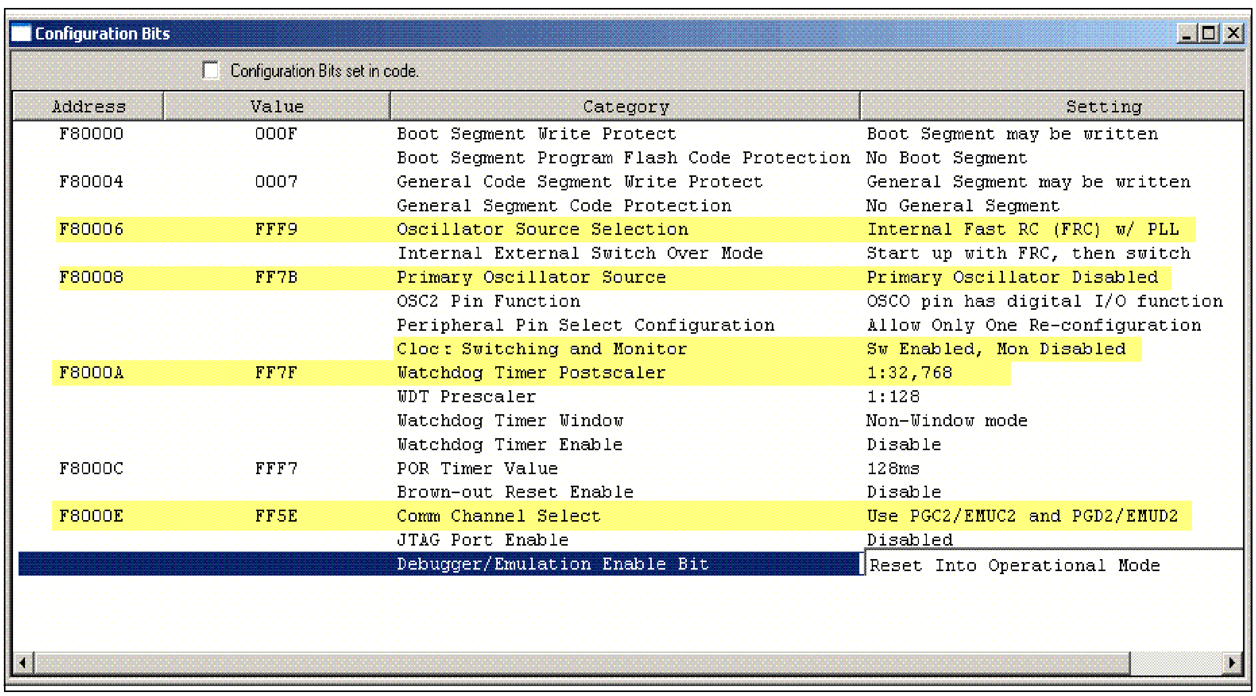
1. Select *Configure>Configuration Bits* from MPLAB IDE to display the configuration settings, as shown in Figure 3-13. The Configuration Bits window appears, as shown in Figure 3-14.

FIGURE 3-13: CONFIGURATION MENU



2. Set the Configuration bits as highlighted in Figure 3-14.

FIGURE 3-14: CONFIGURATION SETTINGS

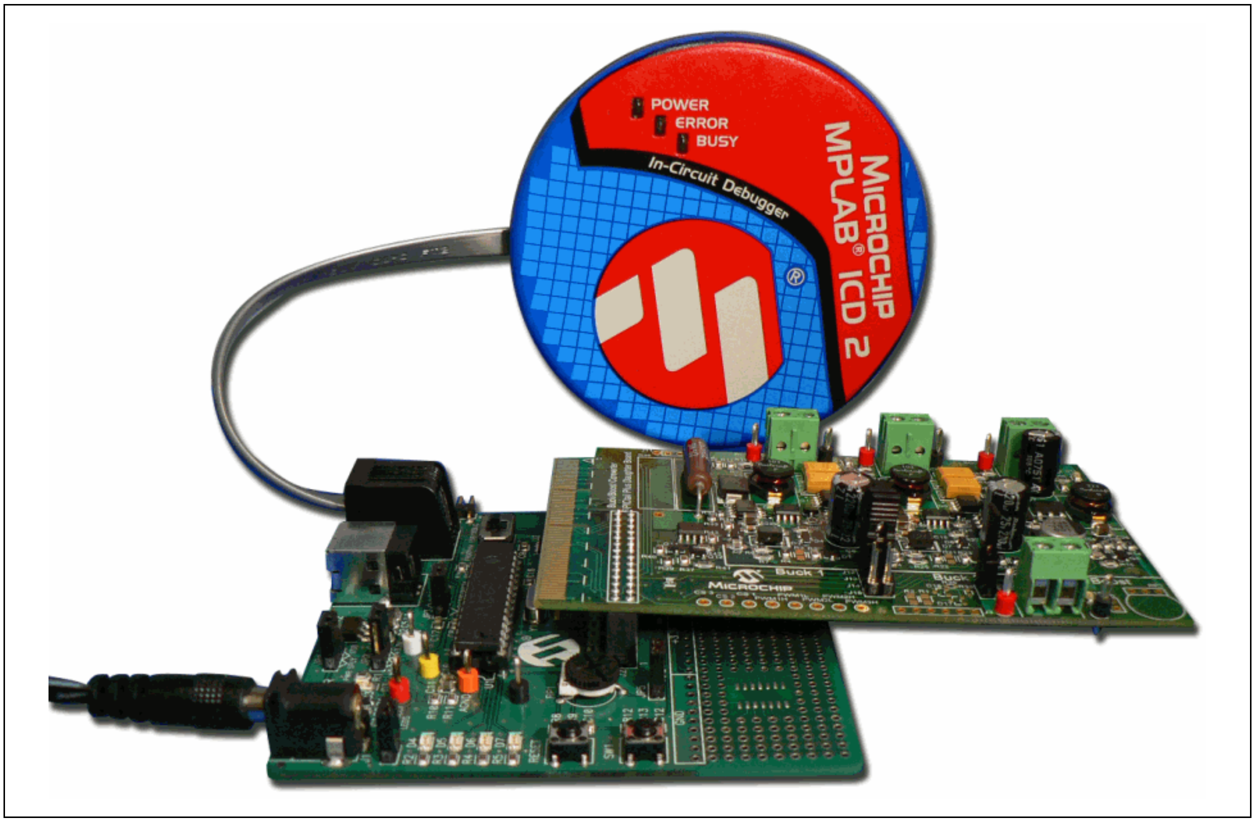


Address	Value	Category	Setting
F80000	000F	Boot Segment Write Protect	Boot Segment may be written
		Boot Segment Program Flash Code Protection	No Boot Segment
F80004	0007	General Code Segment Write Protect	General Segment may be written
		General Segment Code Protection	No General Segment
F80006	FFF9	Oscillator Source Selection	Internal Fast RC (FRC) w/ PLL
		Internal External Switch Over Mode	Start up with FRC, then switch
F80008	FF7B	Primary Oscillator Source	Primary Oscillator Disabled
		OSC2 Pin Function	OSCO pin has digital I/O function
		Peripheral Pin Select Configuration	Allow Only One Re-configuration
		Clock Switching and Monitor	Sw Enabled, Mon Disabled
F8000A	FF7F	Watchdog Timer Postscaler	1:32,768
		WDT Prescaler	1:128
		Watchdog Timer Window	Non-Window mode
		Watchdog Timer Enable	Disable
F8000C	FFF7	POR Timer Value	128ms
		Brown-out Reset Enable	Disable
F8000E	FF5E	Comm Channel Select	Use PGC2/EMUC2 and PGD2/EMUD2
		JTAG Port Enable	Disabled
		Debugger/Emulation Enable Bit	Reset Into Operational Mode

3.4.2 Connecting the MPLAB ICD 2 In-Circuit Debugger

1. Connect the MPLAB ICD 2 to the PC using the USB cable.
2. Connect the MPLAB ICD 2 to the 16-bit 28-pin Starter Development Board with the short RJ-11 (telephone) cable. Apply +9V power to the 16-bit 28-pin Starter Development Board.

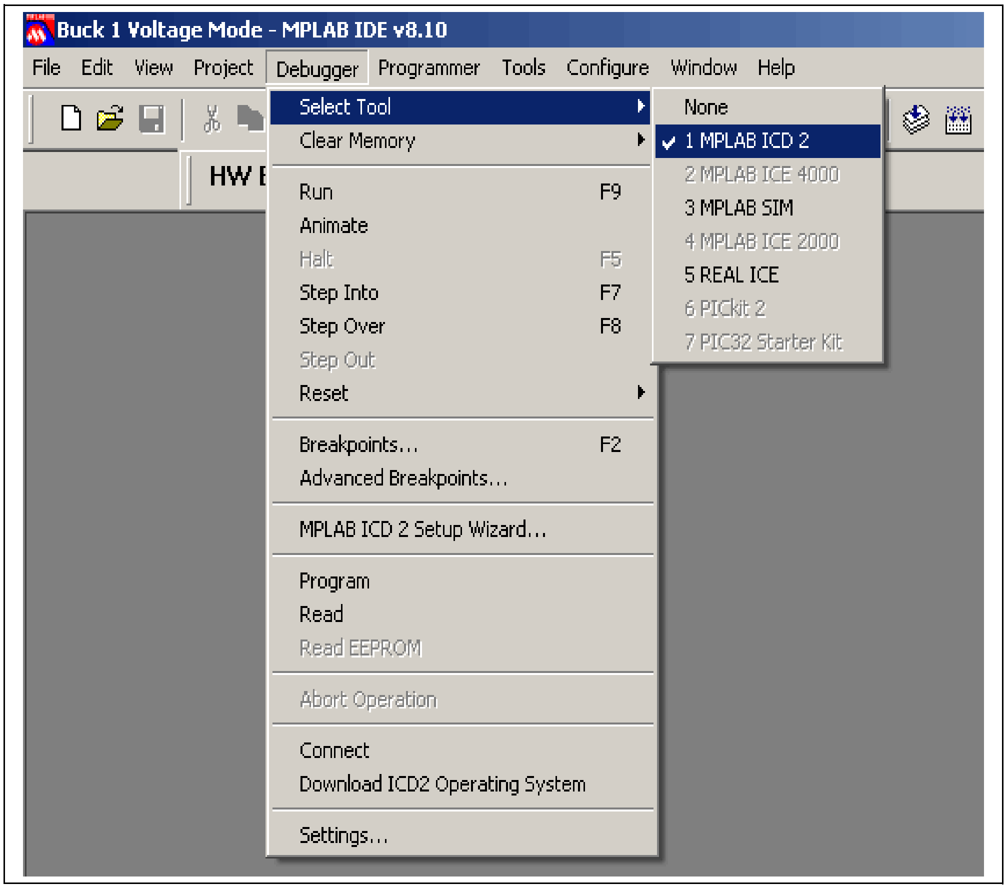
FIGURE 3-15: DAUGHTER BOARD CONNECTED TO MPLAB® ICD 2 IN-CIRCUIT DEBUGGER



3.4.3 Enabling the MPLAB ICD 2 Connection

1. Select *Debugger>Select Tool>MPLAB ICD 2* to designate the MPLAB ICD 2 as the debug tool in MPLAB IDE, as shown in Figure 3-16.

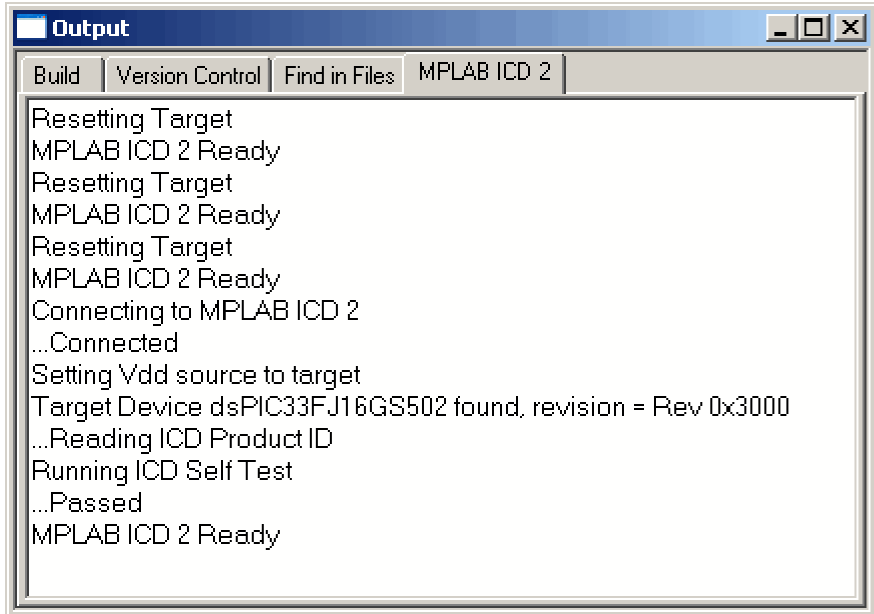
FIGURE 3-16: SELECTING THE DEBUGGER



2. Select *Debugger>Connect* to connect the debugger to the device.

   The MPLAB ICD 2 should report that it found the dsPIC33FJ16GS502 device, as shown in Figure 3-17.

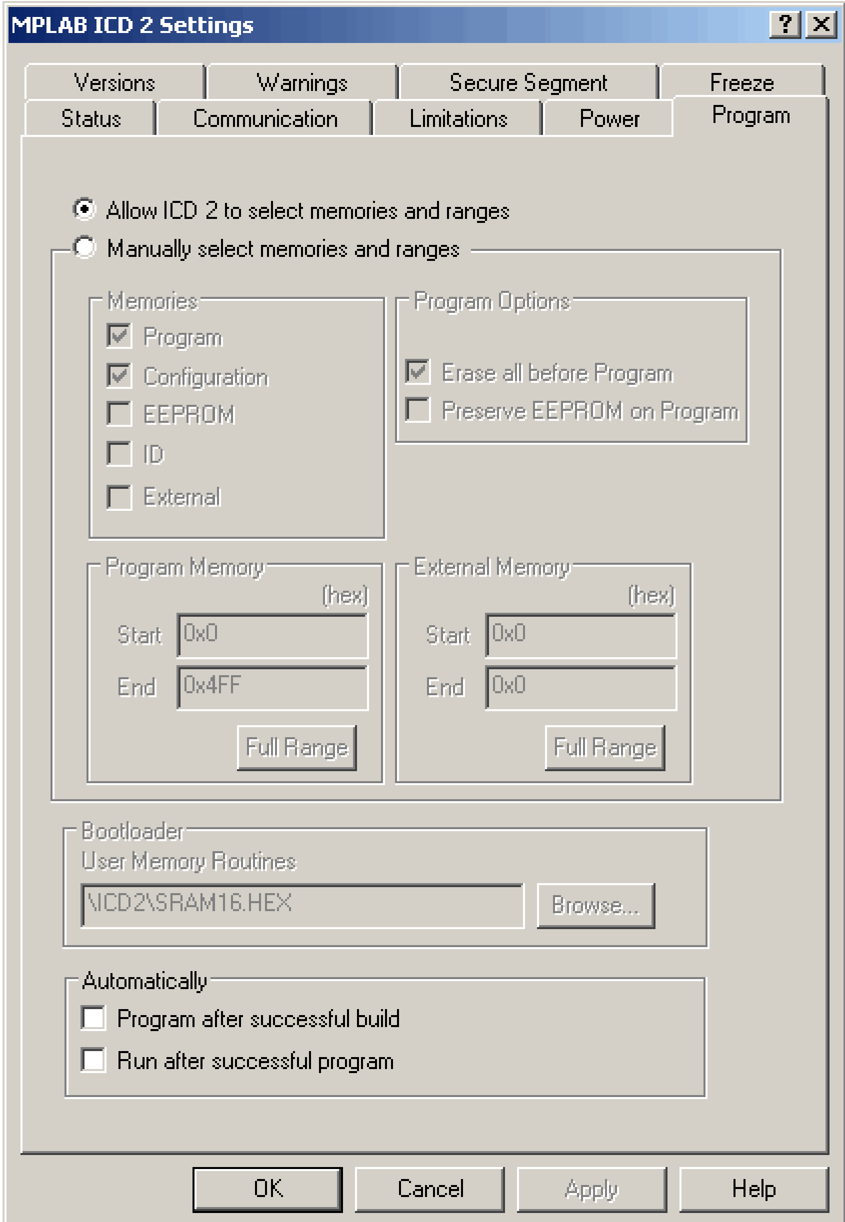
FIGURE 3-17: ENABLING MPLAB® ICD 2



3. Select *Debugger>Settings* to display the MPLAB ICD 2 Debugger settings.
4. Select the **Program** tab on the Debugger settings dialog box.
5. Select the Allow ICD 2 to select memories and ranges radio button, as shown in Figure 3-18. This setting will speed up operations by programming only a small part of the total program memory.

Note:	If this is the first time that the MPLAB ICD 2 is being used with a dsPIC33F device, it may need to download the new firmware. If any errors are shown, double click the error message to get more information.

FIGURE 3-18: SETTING PROGRAM MEMORY SIZE



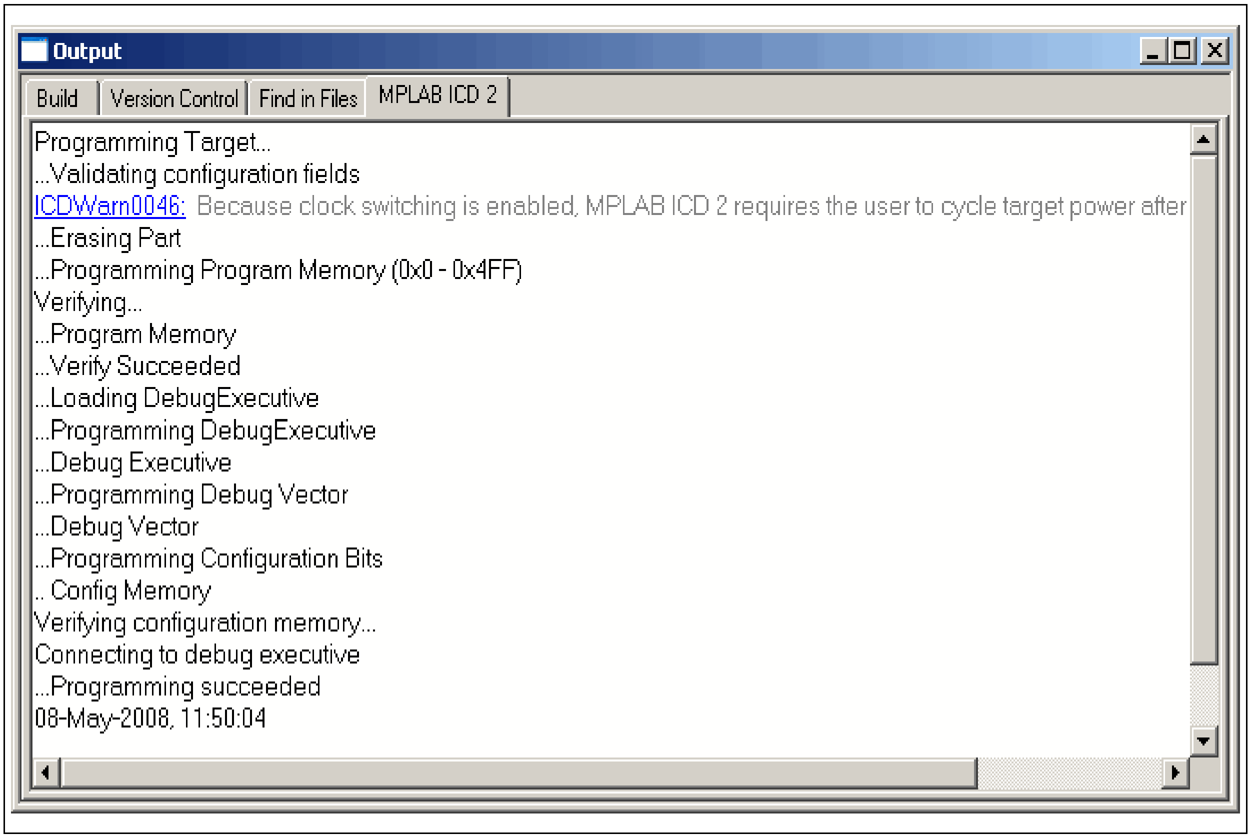
3.4.4 Programming the dsPIC33FJ16GS502 Device

To program the device:

1. From the Debugger, select *Debugger>Program*.

   The Output (Program Memory window), as shown in Figure 3-19, displays the program statuses as they appear.

FIGURE 3-19: PROGRAMMING THE dsPIC33FJ16GS502 DEVICE



2. Observe the process in the Output window. When MPLAB ICD 2 Ready appears, the device is programmed and ready to run.
3. Select *Debugger>Reset* to reset the code.
4. Select *Debugger>Run* to run the code.

3.5 DEBUGGING THE CODE

The MPLAB ICD 2 In-Circuit Debugger can be used to run, halt, and step the code. A breakpoint can be set to halt the program after the code has executed the instruction at the breakpoint. The contents of the RAM and registers can be viewed whenever the processor has been halted.

The MPLAB ICD 2 In-Circuit Debugger uses the following function keys to access the main debugging functions:

- <F5> – Halt
- <F6> – Reset
- <F7> – Single Step
- <F9> – Run

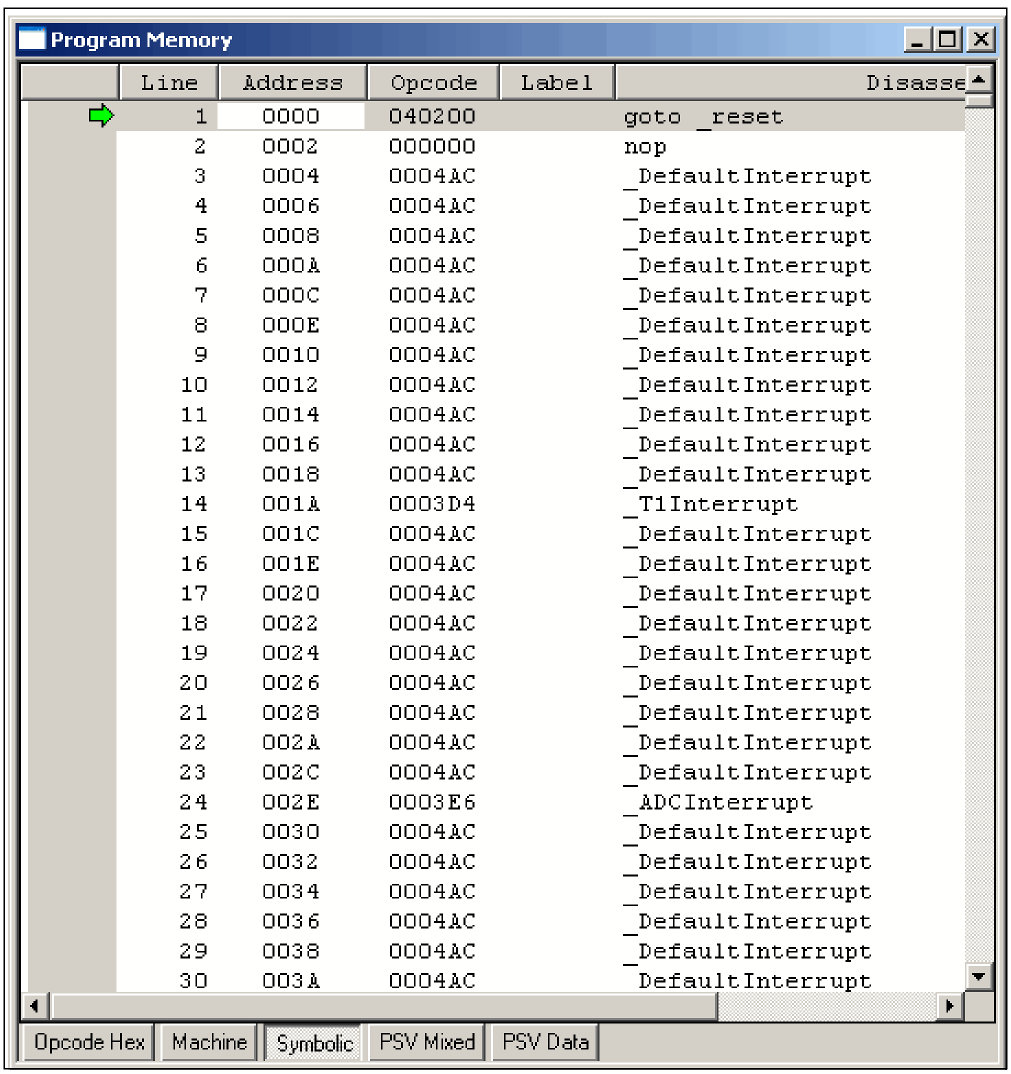
In addition to these, there are more functions accessible by right clicking on a line of source code. The most important of these are "Set Breakpoint" and "Run to Cursor".

3.5.1 Displaying the Code

To display the code:

1. Select *View>Program Memory*.
2. From the Program Memory window, select the **Symbolic** tab, as shown in Figure 3-20.

FIGURE 3-20: PROGRAM MEMORY WINDOW



3. Press <**F5**> to halt the processor and press <**F6**> to reset the processor. The Program Memory now displays a green arrow pointing to the line of code at address 0.

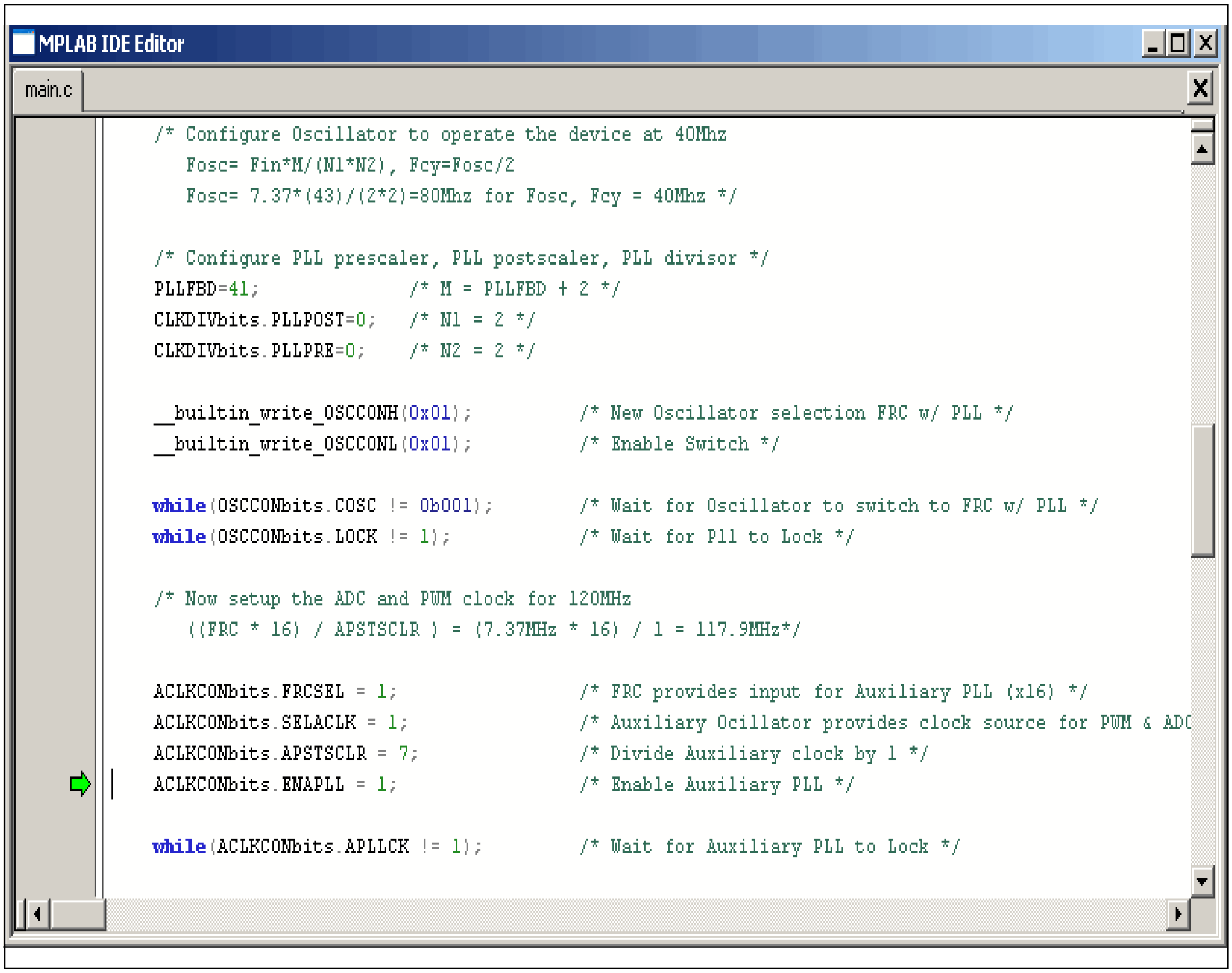
The instruction at this location is `goto 0x000100`. This code is added by the linker to make the program branch to the start of the code in the `main.c` file. The executable code starts from location 0x000100.

3.5.2 Stepping the Program

To step the program:

1. Press <**F7**> to single step the code. The green arrow now points to the code below `ACLKCONbits.ENAPLL = 1;` in the `main.c` source code, as shown in Figure 3-21.

FIGURE 3-21: SOURCE CODE WINDOW

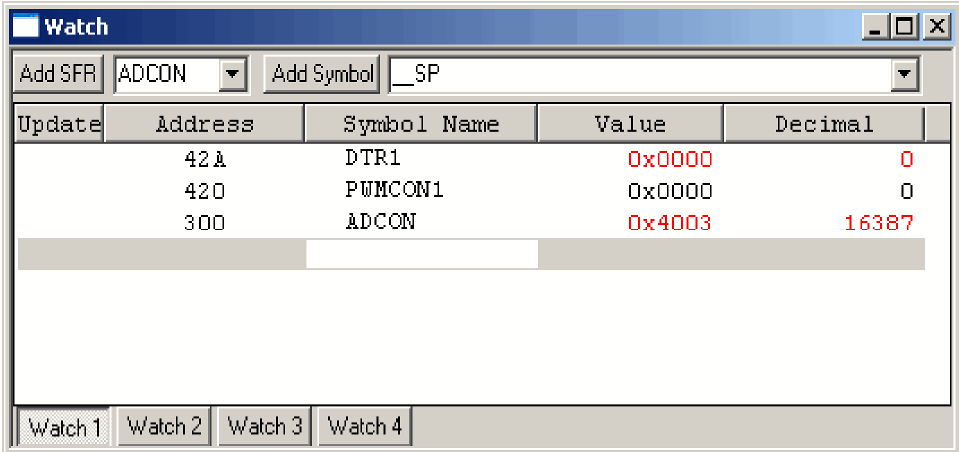


2. Right click the instruction up to which the code is to be executed and select Run to Cursor.

   The program is executed up to the instruction selected.

3. Select *View>Watch*. The Watch window appears, as shown in Figure 3-22.

FIGURE 3-22: WATCH WINDOW



4. Select DTR1 from the Add SFR drop-down list and click **Add SFR** to add the DTR1 register in the Watch window.
5. Select PWMCON1 from the Add SFR drop-down list and click **Add SFR** to add the PWMCON1 register in the Watch window.
6. Select ADCON from the Add SFR drop-down list and click **Add SFR** to add the ADCON register in the Watch window.

You will be able to see these registers change as you step through the code.

3.5.3 Setting the Breakpoint

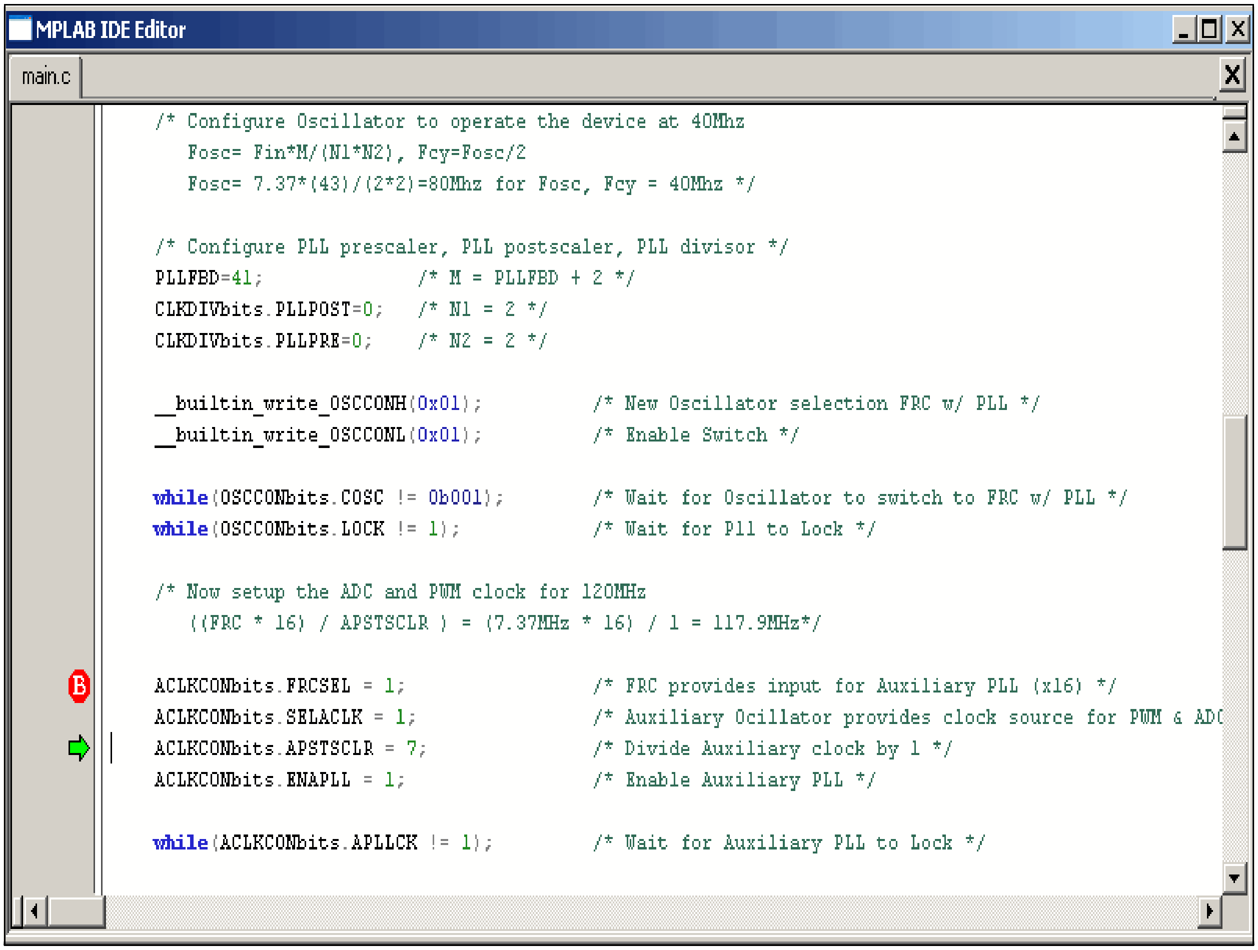
1. To set a breakpoint, right click a line of code and select Set Breakpoint from the pop-up menu.

   For example, find the following line of code and set a breakpoint on this line:

   ```
   ACLKCONbits.FRCSEL = 1;
   ```

   A red octagonal shape marked with a B appears in the gutter (gray bar on the left) of the source code window to designate the breakpoint location, as shown in Figure 3-23.

FIGURE 3-23: SETTING BREAKPOINT



2. Press **<F9>** to run the code.

   The program halts on the instruction following the breakpoint.

Note:	An alternate method to set a breakpoint is to simply double click the line. This feature may need to be enabled using the *Edit>Properties* menu.

NOTES:

Chapter 4. Demonstration Program Operation

The Buck/Boost Converter PICtail Plus Daughter Board CD supplied with the Buck/Boost Converter PICtail Plus Daughter Board consists of the source code for the 16-bit 28-pin Starter Development Board (Buck 1 stage only) and Explorer 16 Development Board (Buck 1, Buck 2 and Boost stages). To demonstrate a program that illustrates PID control of the output voltage on the Daughter Board, program the device with respective source code, available on the Daughter Board's CD, specified in **Section 3.2 "Creating the Project"**. The code can also be downloaded from the Microchip web site (http://www.microchip.com).

The following topics are included in this chapter:

- Program Demonstration
- Code Demonstration
- Other Code Examples

4.1 PROGRAM DEMONSTRATION

The demonstration program provides simultaneous closed-loop control of the output voltages.

The PID control scheme consists of the following parameters:

- **Proportional Error Gain (P-Gain)** – This parameter produces a correction factor that is proportional to the magnitude of the output voltage error.
- **Integral Error Gain (I-Gain)** – This parameter uses the cumulative voltage error to generate a correction factor that eliminates any residual error due to limitations in offset voltages and measurement resolution.
- **Derivative Error Gain (D-Gain)** – This parameter produces a correction factor that is proportional to the rate of change of the output error voltage, which helps the system respond quickly to changes in system condition.

Additional control parameters that the user can add to P, I and D Gain terms are as follows:

- **Second Derivative, or Jerk Error, Gain (J-Gain)** – This parameter produces a correction factor that is proportional to the change in the differential error (i.e., the derivative of the derivative). J-Gain is a high frequency term that tends to provide quick response to an impulse event.
- **Feed Forward Gain** – This parameter produces a correction factor based on the desired output voltage that is computed based on the magnitude of the input voltage, inductor current, and circuit attributes (i.e., inductor and capacitor values). This term allows the control loop to be proactive rather than reactive. In other words, when the input voltage changes, feed forward gain responds so that the control loop does not have to wait until the output voltage changes before making the appropriate gain correction.

- **Dead-Time Gain** – This parameter produces a correction factor that compensates for the fact that the feed forward gain term does not account for the energy lost due to the dead time of the PWM signal (the time when both MOSFETs are off).
- **Current-Limit Gain** – This parameter limits the cumulative control gain when the current is approaching its upper limit.

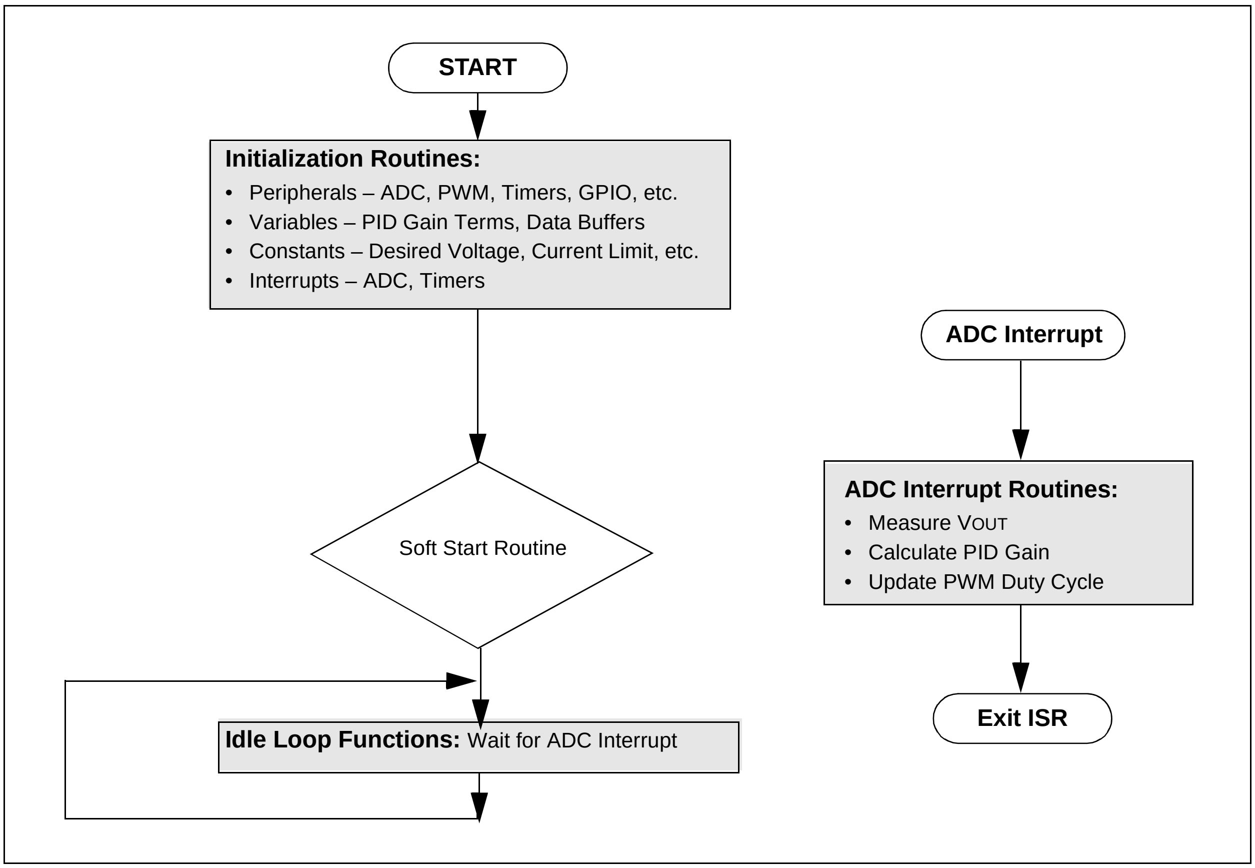
After the modifications have been made to the 16-bit 28-pin Starter Development Board, as specified in **Section 2.4 "Using the Daughter Board with the 16-bit 28-pin Starter Development Board"**, do the following:

- Connect the power supply
- Connect the MPLAB ICD 2
- Connect the Buck/Boost Converter PICtail Plus Daughter Board
- Connect the 9V power supply to the 16-bit 28-pin Starter Development Board as shown in Figure 2-5

Instructions for programming the dsPIC33FJ16GS502 SMPS device are provided in the Readme file of the respective software folder. **Chapter 4. "Demonstration Program Operation"** also describes how to program the dsPIC33FJ16GS502 device using the MPLAB ICD 2. Figure 4-1 illustrates the program flow of the demonstration program.

> **Note:** While using the Explorer 16 Development Board with the Daughter Board, the output voltages Buck1+, Buck2+ and Boost+ can be verified by measuring at output terminals J4, J5 and J8 respectively.

FIGURE 4-1: SMPS DEMONSTRATION PROGRAM FLOW CHART



4.2 CODE DEMONSTRATION

4.2.1 System Initialization

When power is applied to the board, the program starts by executing the following system initialization routines:

- **Peripherals** – The required peripherals (PWM, ADC, Timers and GPIO) are configured and enabled.
- **Variables** – Program variables are defined. RAM locations and register usage are defined and documented.
- **Constants** – Program constants are defined including reference set points for both VOUT1 and VOUT2, input voltage, current limits, fault conditions, PWM periods and Timer periods.
- **Interrupts** – The ADC and Timer Interrupts are set up and enabled.
- **System Stabilization** – All outputs are discharged to ensure a stable value at start-up.

4.2.2 Fault Check

The program checks the ADC for input undervoltage and output overvoltage conditions. If a fault occurs, the PWM outputs are disabled until the fault condition is cleared. If no fault is detected, the program proceeds.

4.2.3 Soft Start

The Soft Start Routine ramps up the output voltage in an open-loop fashion to bring the system within the operating range of the PID control loop. This routine ensures that the output does not overshoot the desired voltage. It also limits the current at start-up.

4.2.4 ADC Interrupt

The ADC Interrupt is the heart of the demo program. This routine takes up approximately 75% of the execution time. It performs all the PID calculations and applies any needed corrections to the output.

4.2.5 System Idle Loop

Note 1: The ADC Interrupt can occur any time during program execution.

2: The ADC Interrupt takes priority over any other tasks that the program is performing.

All auxiliary functions are performed in the system idle routine. This is the time available to the CPU while the demo program is waiting for an ADC Interrupt. Non-critical functions can be performed in this loop. During this time the input voltage, fault timers and Soft Start flag are checked.

4.3 OTHER CODE EXAMPLES

There are several other code examples are available on the Microchip website. Refer to the Readme files located in each code example folder for details on what each code example demonstrates. Check the Microchip web site (http://www.microchip.com) for the latest updates to the code examples and for additional code examples.

NOTES:

Appendix 1. Schematics and Layouts

This appendix provides the board layout followed by schematics for the Buck/Boost Converter PICtail Plus Daughter Board.

FIGURE 1-1: BOARD LAYOUT

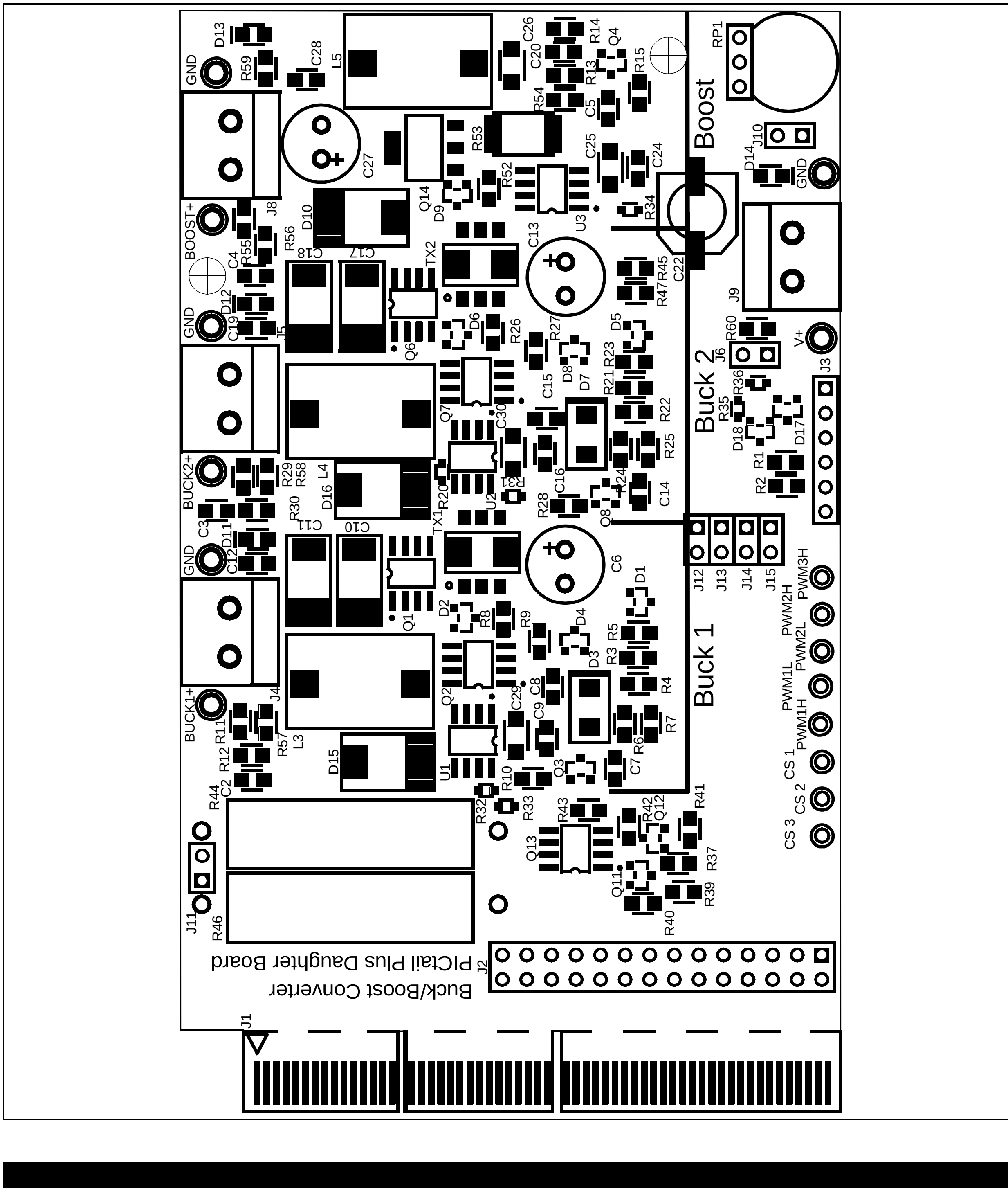


FIGURE 1-2: DAUGHTER BOARD SCHEMATIC 1 OF 5

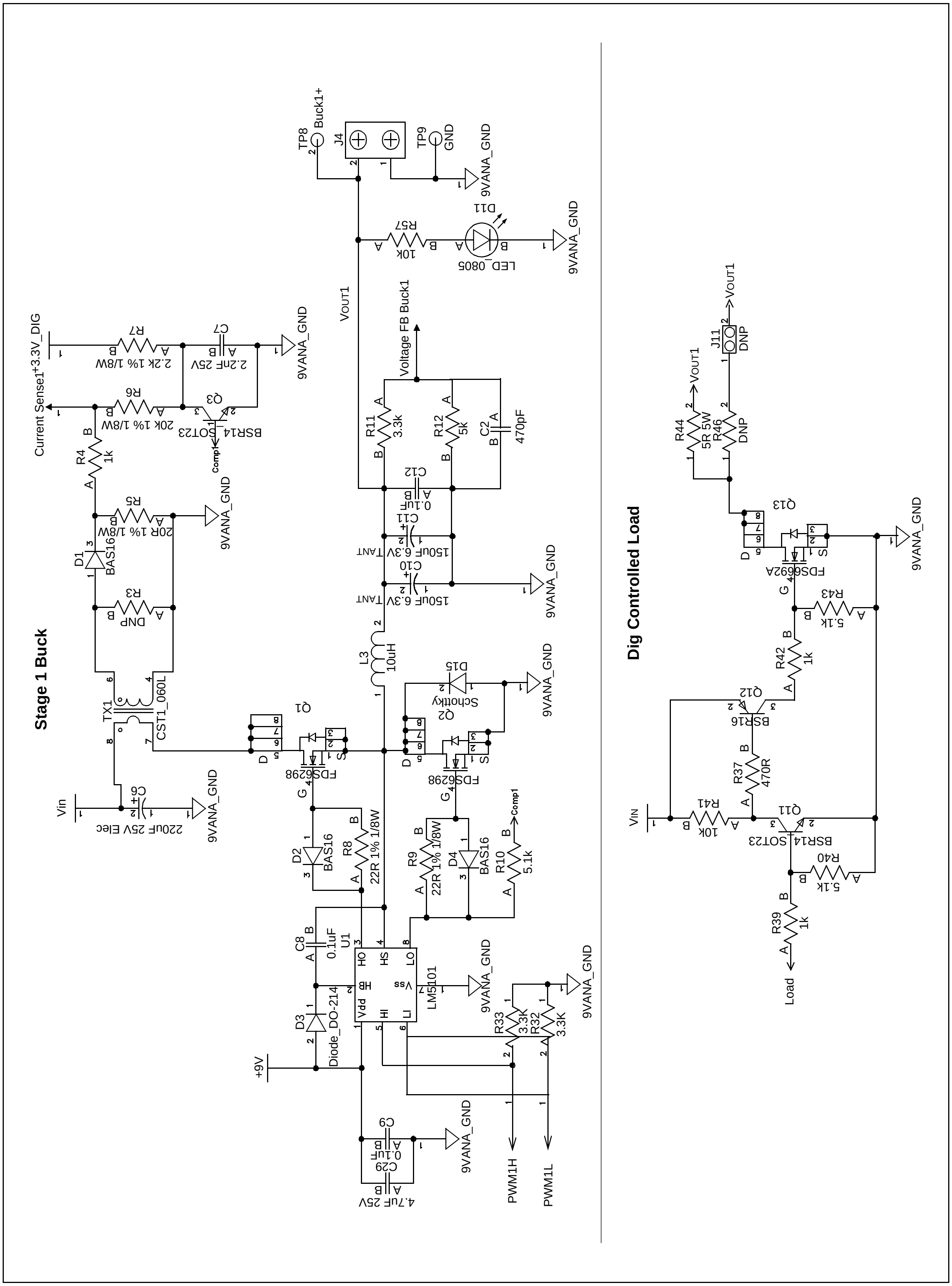


FIGURE 1-3: DAUGHTER BOARD SCHEMATIC 2 OF 5

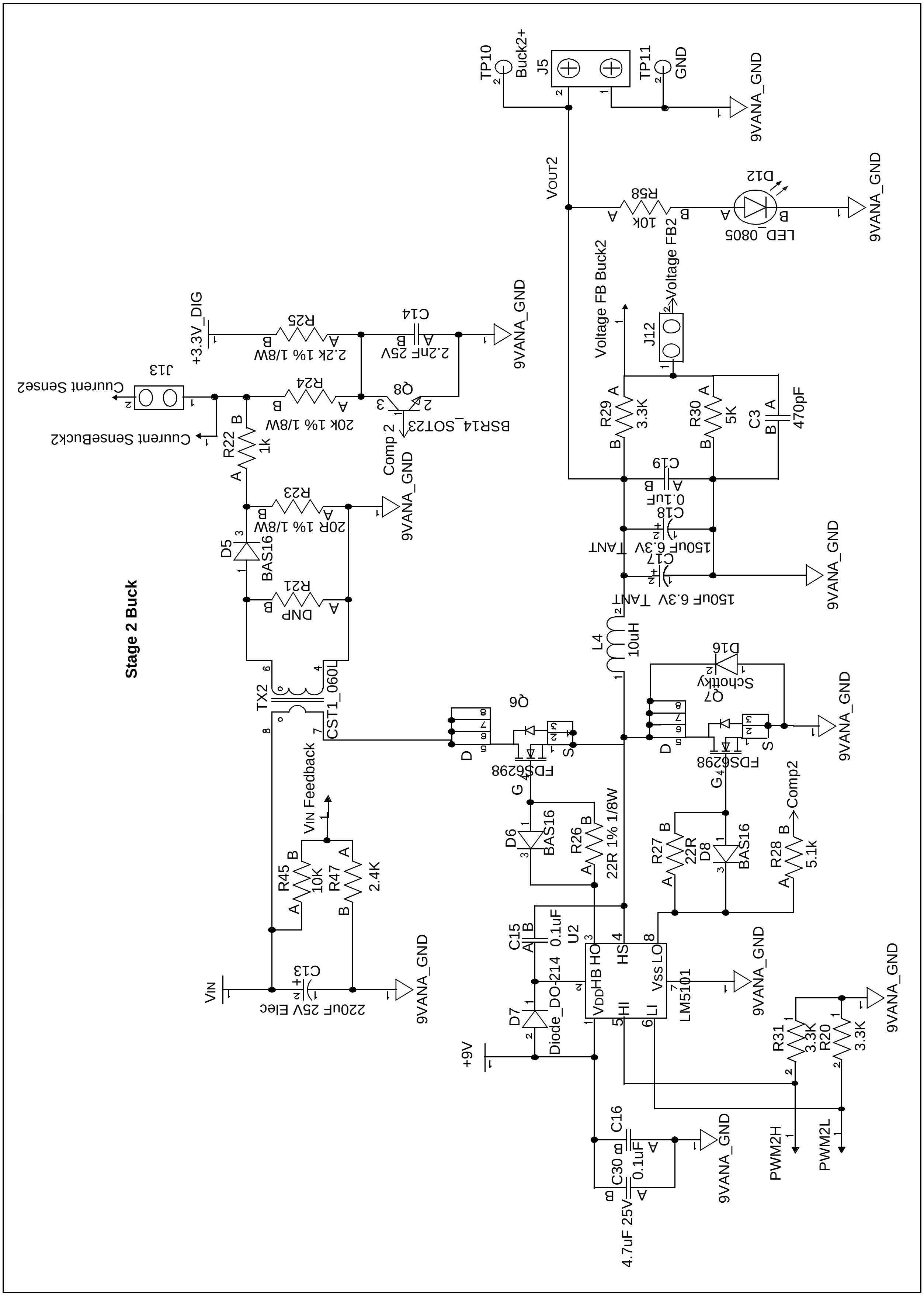


FIGURE 1-4: DAUGHTER BOARD SCHEMATIC 3 OF 5

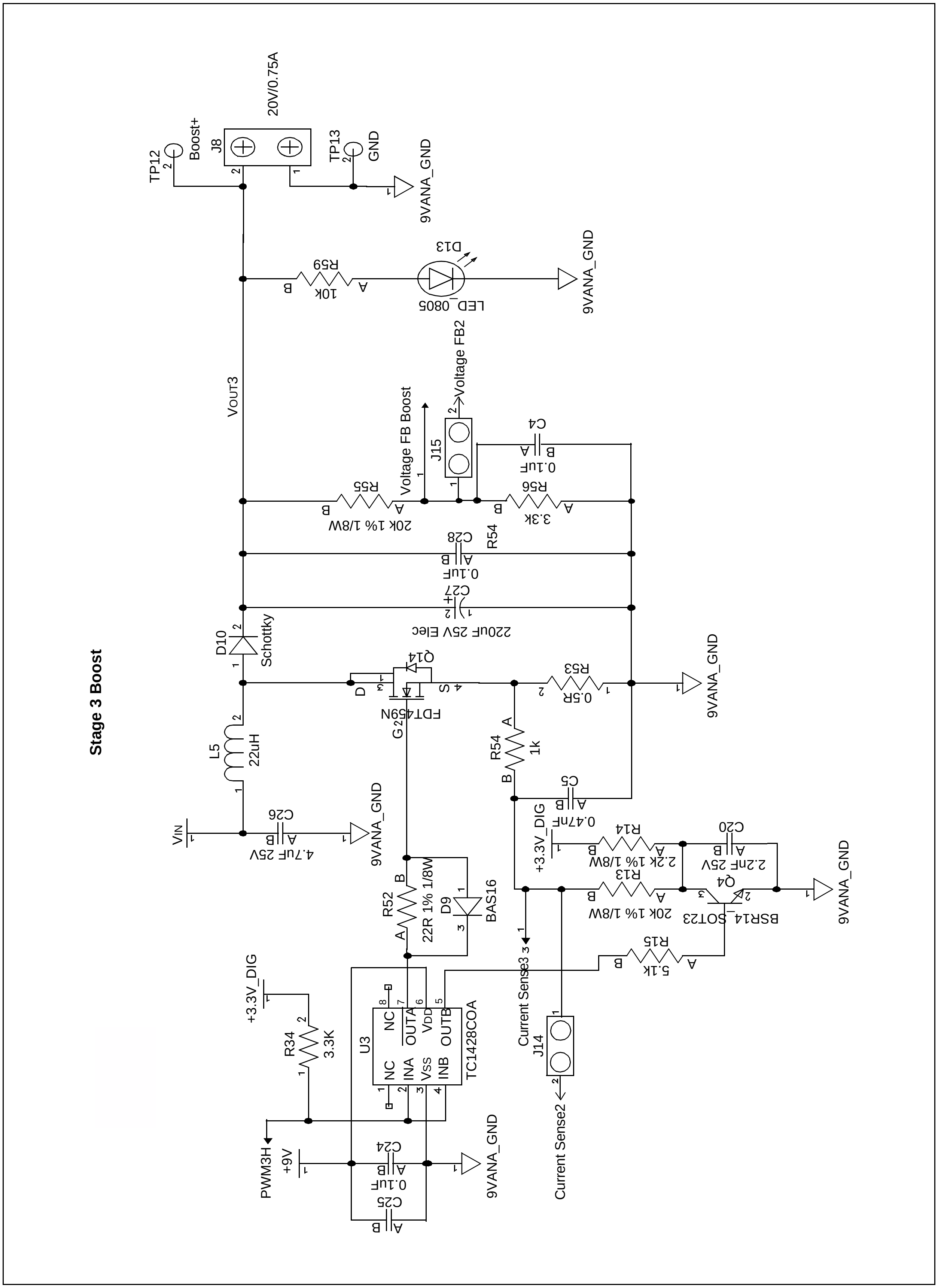


FIGURE 1-5: DAUGHTER BOARD SCHEMATIC 4 OF 5

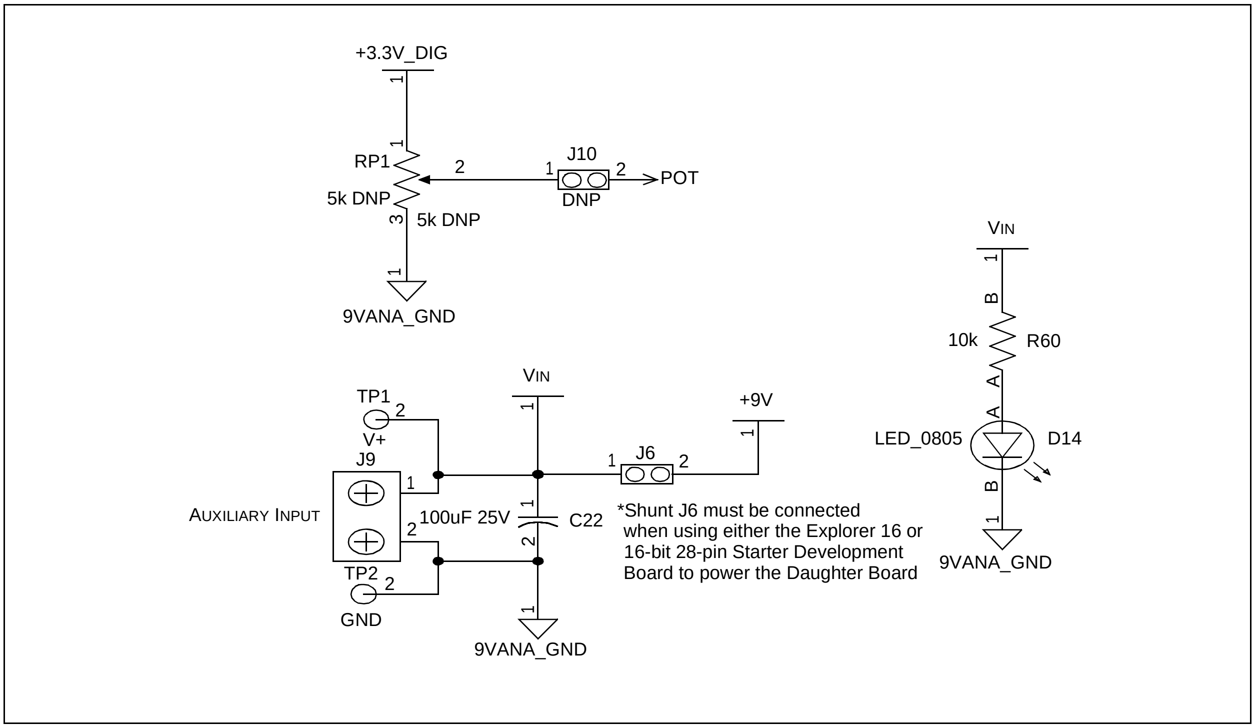
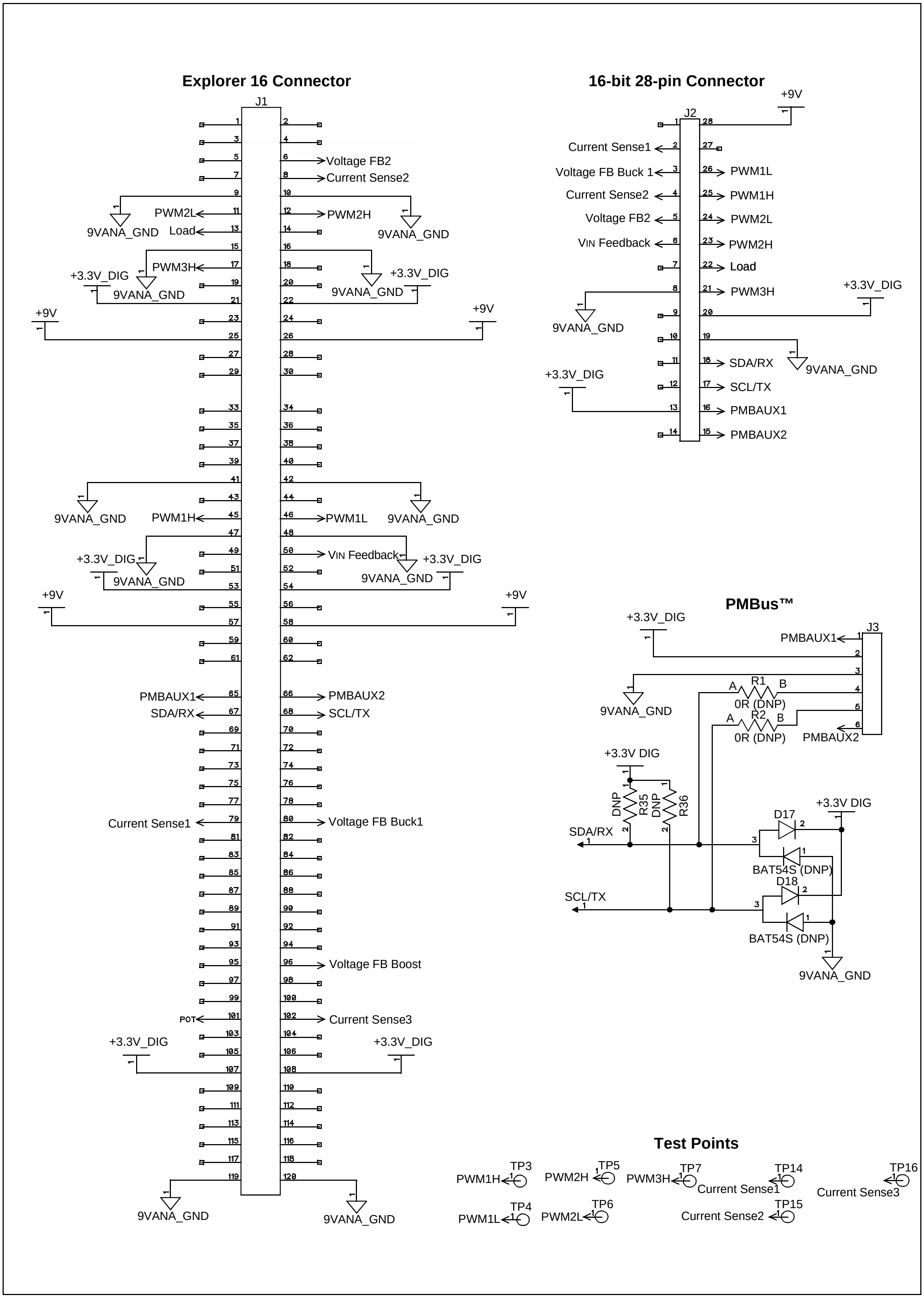


FIGURE 1-6: DAUGHTER BOARD SCHEMATIC 5 OF 5



Index

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01/02/08

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet

High-Performance,
16-bit Digital Signal Controllers

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

High-Performance, 16-Bit Digital Signal Controllers

Operating Range:

- Up to 40 MIPS Operation (at 3.0-3.6V):
  - Industrial temperature range (-40°C to +85°C)
  - Extended temperature range (-40°C to +125°C)

High-Performance DSC CPU:

- Modified Harvard Architecture
- C Compiler Optimized Instruction Set
- 16-Bit Wide Data Path
- 24-Bit Wide Instructions
- Linear Program Memory Addressing up to 4M Instruction Words
- Linear Data Memory Addressing up to 64 Kbytes
- 83 Base Instructions: Mostly 1 Word/1 Cycle
- Two 40-Bit Accumulators with Rounding and Saturation Options
- Flexible and Powerful Addressing modes:
  - Indirect
  - Modulo
  - Bit-Reversed
- Software Stack
- 16 x 16 Fractional/Integer Multiply Operations
- 32/16 and 16/16 Divide Operations
- Single-Cycle Multiply and Accumulate:
  - Accumulator write back for DSP operations
  - Dual data fetch
- Up to ±16-Bit Shifts for up to 40-Bit Data

Digital I/O:

- Peripheral Pin Select Functionality
- Up to 35 Programmable Digital I/O Pins
- Wake-up/Interrupt-on-Change for up to 30 Pins
- Output Pins can Drive Voltage from 3.0V to 3.6V
- Up to 5V Output with Open-Drain Configuration
- 5V Tolerant Digital Input Pins (except RB5)
- 16 mA Source/Sink on All PWM pins

On-Chip Flash and SRAM:

- Flash Program Memory (up to 16 Kbytes)
- Data SRAM (up to 2 Kbytes)
- Boot and General Security for Program Flash

Peripheral Features:

- Timer/Counters, up to Three 16-Bit Timers:
  - Can pair up to make one 32-bit timer
- Input Capture (up to two channels):
  - Capture on up, down or both edges
  - 16-bit capture input functions
  - 4-deep FIFO on each capture
- Output Compare (up to two channels):
  - Single or Dual 16-Bit Compare mode
  - 16-Bit Glitchless PWM mode
- 4-Wire SPI:
  - Framing supports I/O interface to simple codecs
  - 1-deep FIFO Buffer.
  - Supports 8-bit and 16-bit data
  - Supports all serial clock formats and sampling modes
- I^2C™:
  - Supports Full Multi-Master Slave mode
  - 7-bit and 10-bit addressing
  - Bus collision detection and arbitration
  - Integrated signal conditioning
  - Slave address masking
- UART:
  - Interrupt on address bit detect
  - Interrupt on UART error
  - Wake-up on Start bit from Sleep mode
  - 4-character TX and RX FIFO buffers
  - LIN bus support
  - IrDA® encoding and decoding in hardware
  - High-Speed Baud mode
  - Hardware Flow Control with CTS and RTS

Interrupt Controller:

- 5-Cycle Latency
- Up to 35 Available Interrupt Sources
- Up to Three External Interrupts
- Seven Programmable Priority Levels
- Four Processor Exceptions

High-Speed PWM Module Features:

- Up to Four PWM Generators with Four to Eight Outputs
- Individual Time Base and Duty Cycle for each of the Eight PWM Outputs
- Dead Time for Rising and Falling Edges
- Duty Cycle Resolution of 1.04 ns
- Dead-Time Resolution of 1.04 ns
- Phase Shift Resolution of 1.04 ns
- Frequency Resolution of 1.04 ns
- PWM modes Supported:
  - Standard Edge-Aligned
  - True Independent Output
  - Complementary
  - Center-Aligned
  - Push-Pull
  - Multi-Phase
  - Variable Phase
  - Fixed Off-Time
  - Current Reset
  - Current-Limit
- Independent Fault/Current-Limit Inputs for 8 PWM Outputs
- Output Override Control
- Special Event Trigger
- PWM Capture Feature
- Prescaler for Input Clock
- Dual Trigger from PWM to ADC
- PWMxL, PWMxH Output Pin Swapping
- PWM4H, PWM4L Pins Remappable
- On-the-Fly PWM Frequency, Duty Cycle and Phase Shift Changes
- Disabling of Individual PWM Generators
- Leading-Edge Blanking (LEB) Functionality

High-Speed Analog Comparator

- Up to Four Analog Comparators:
  - 20 ns response time
  - 10-bit DAC for each analog comparator
  - DACOUT pin to provide DAC output
  - Programmable output polarity
  - Selectable input source
  - ADC sample and convert capability
- PWM Module Interface:
  - PWM duty cycle control
  - PWM period control
  - PWM Fault detect

High-Speed 10-Bit ADC

- 10-Bit Resolution
- Up to 12 Input Channels Grouped into Six Conversion Pairs
- Two Internal Reference Monitoring Inputs Grouped into a Pair
- Successive Approximation Register (SAR) Converters for Parallel Conversions of Analog Pairs:
  - 4 Msps for devices with two SARs
  - 2 Msps for devices with one SAR
- Dedicated Result Buffer for each Analog Channel
- Independent Trigger Source Section for each Analog Input Conversion Pair

Power Management:

- On-Chip 2.5V Voltage Regulator
- Switch between Clock Sources in Real Time
- Idle, Sleep, and Doze modes with Fast Wake-up

CMOS Flash Technology:

- Low-Power, High-Speed Flash Technology
- Fully Static Design
- 3.3V (±10%) Operating Voltage
- Industrial and Extended Temperature
- Low-Power Consumption

System Management:

- Flexible Clock Options:
  - External, crystal, resonator, internal RC
  - Phase-Locked Loop (PLL) with 120 MHz VCO
  - Primary Crystal Oscillator (OSC) in the range of 3 MHz to 40 MHz
  - Internal Low-Power RC (LPRC) oscillator at a frequency of 32 kHz
  - Internal Fast RC (FRC) oscillator at a frequency of 7.37 MHz
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Watchdog Timer with its RC Oscillator
- Fail-Safe Clock Monitor (FSCM)
- Reset by Multiple Sources
- In-Circuit Serial Programming™ (ICSP™)
- Reference Oscillator Output

Application Examples

- AC-to-DC Converters
- Automotive HID
- Battery Chargers
- DC-to-DC Converters
- Digital Lighting
- Induction Cooking
- LED Ballast
- Renewable Power/Pure Sine Wave Inverters
- Uninterruptible Power Supply (UPS)

Packaging:

- 18-Pin SOIC
- 28-Pin SPDIP/SOIC/QFN-S
- 44-Pin TQFP/QFN

Note:	See the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families table for the exact peripheral features per device.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed below. The following pages show their pinout diagrams.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families

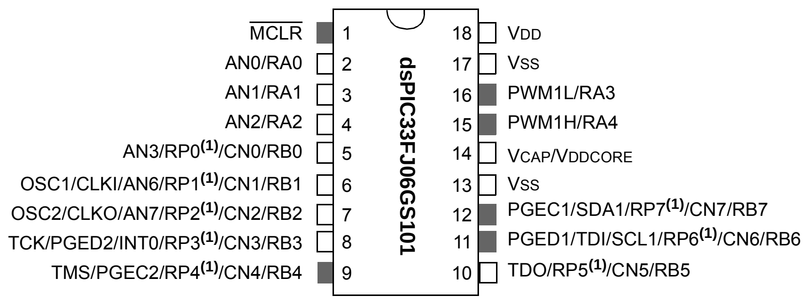
Device	Pins	Program Flash Memory (Kbytes)	RAM (Bytes)	Remappable Peripherals									DAC Output	I2C™	ADC			I/O Pins	Packages
				Remappable Pins	16-bit Timer	Input Capture	Output Compare	UART	SPI	PWM[2]	Analog Comparator	External Interrupts[3]			SARs	Sample and Hold (S&H) Circuit	Analog-to-Digital Inputs		
dsPIC33FJ06GS101	18	6	256	8	2	0	1	1	1	2x2[1]	0	3	0	1	1	3	6	13	SOIC
dsPIC33FJ06GS102	28	6	256	16	2	0	1	1	1	2x2	0	3	0	1	1	3	6	21	SPDIP SOIC QFN-S
dsPIC33FJ06GS202	28	6	1K	16	2	1	1	1	1	2x2	2	3	1	1	1	3	6	21	SPDIP SOIC QFN-S
dsPIC33FJ16GS402	28	16	2K	16	3	2	2	1	1	3x2	0	3	0	1	1	4	8	21	SPDIP SOIC QFN-S
dsPIC33FJ16GS404	44	16	2K	30	3	2	2	1	1	3x2	0	3	0	1	1	4	8	35	QFN TQFP
dsPIC33FJ16GS502	28	16	2K	16	3	2	2	1	1	4x2[1]	4	3	1	1	2	6	8	21	SPDIP SOIC QFN-S
dsPIC33FJ16GS504	44	16	2K	30	3	2	2	1	1	4x2[1]	4	3	1	1	2	6	12	35	QFN TQFP

Note 1: The PWM4H:PWM4L pins are remappable.
2: The PWM Fault pins and PWM synchronization pins are remappable.
3: Only two out of three interrupts are remappable.

Pin Diagrams

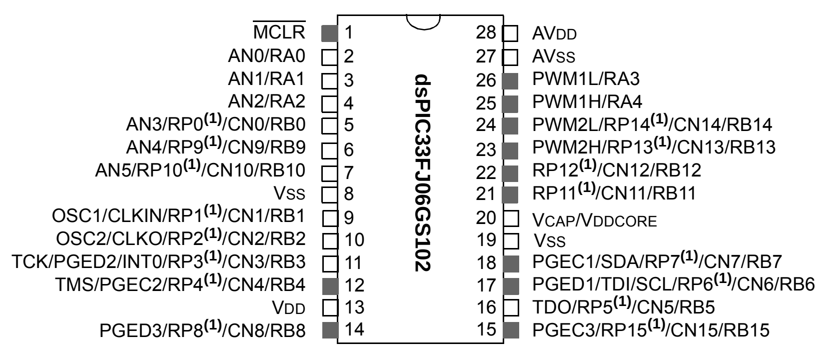
18-Pin SOIC

■ = Pins are up to 5V tolerant



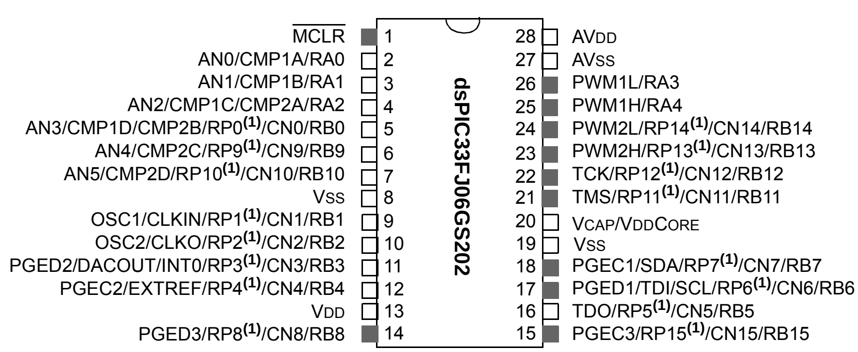
28-Pin SOIC, SPDIP

■ = Pins are up to 5V tolerant



28-Pin SPDIP, SOIC

■ = Pins are up to 5V tolerant

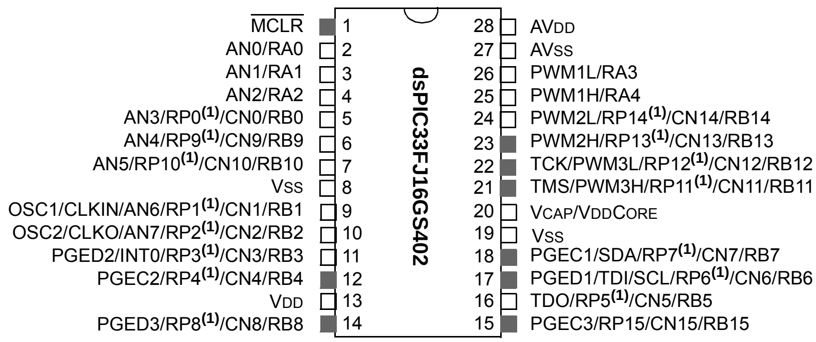


Note 1: The RPn pins can be used by any remappable peripheral. See the **“dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families”** table for the list of available peripherals

Pin Diagrams (Continued)

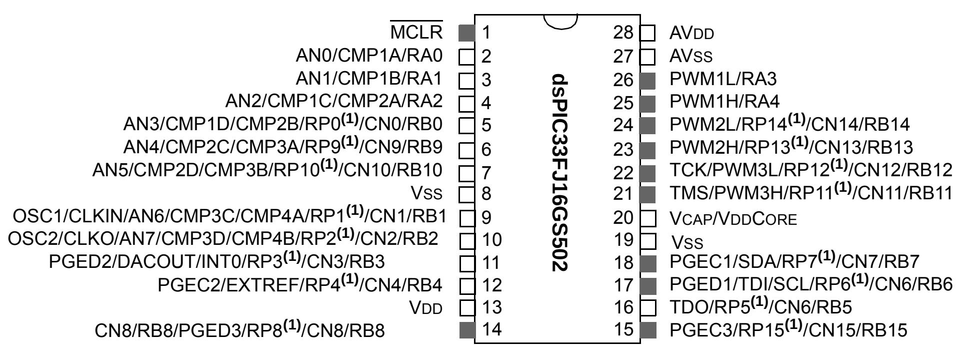
28-Pin SPDIP, SOIC

■ = Pins are up to 5V tolerant



28-Pin SPDIP, SOIC

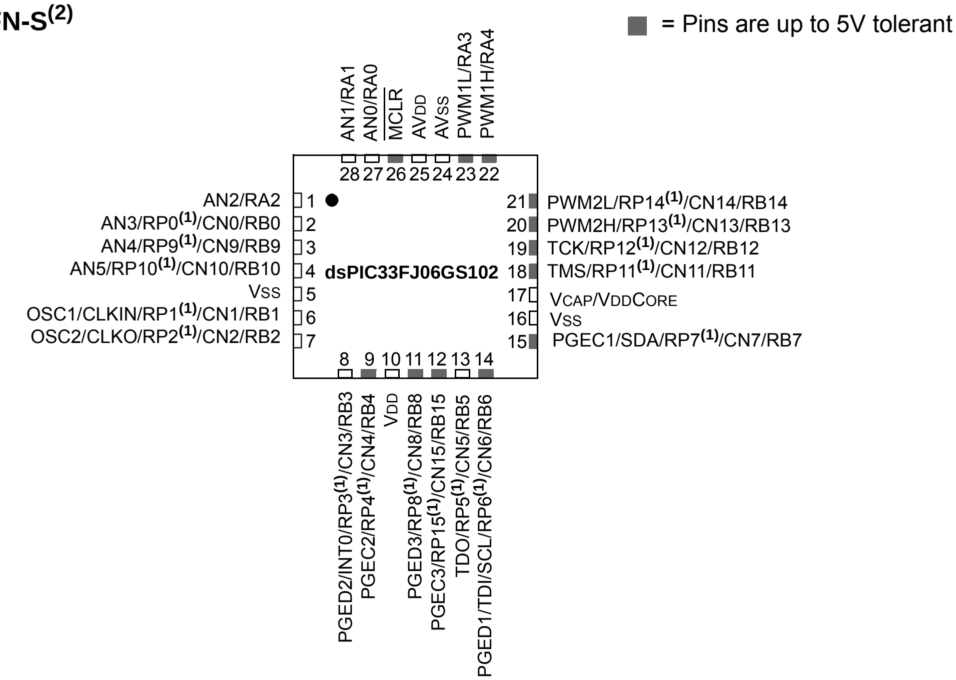
■ = Pins are up to 5V tolerant



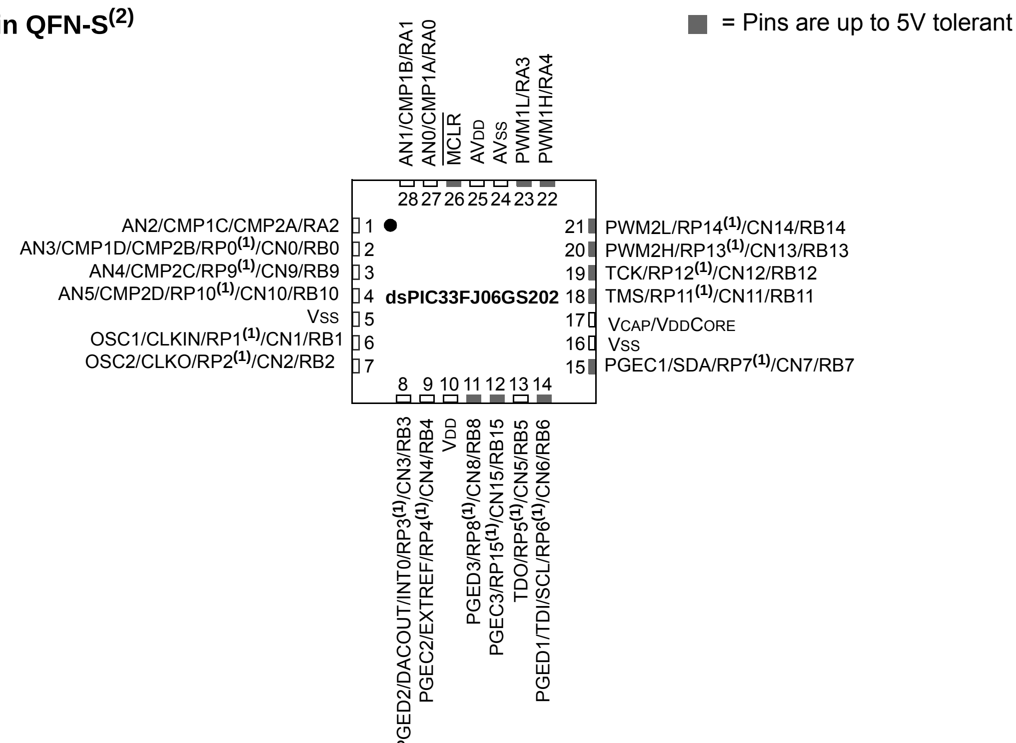
Note 1: The RPn pins can be used by any remappable peripheral. See the **"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families"** table for the list of available peripherals

Pin Diagrams (Continued)

28-Pin QFN-S(2)



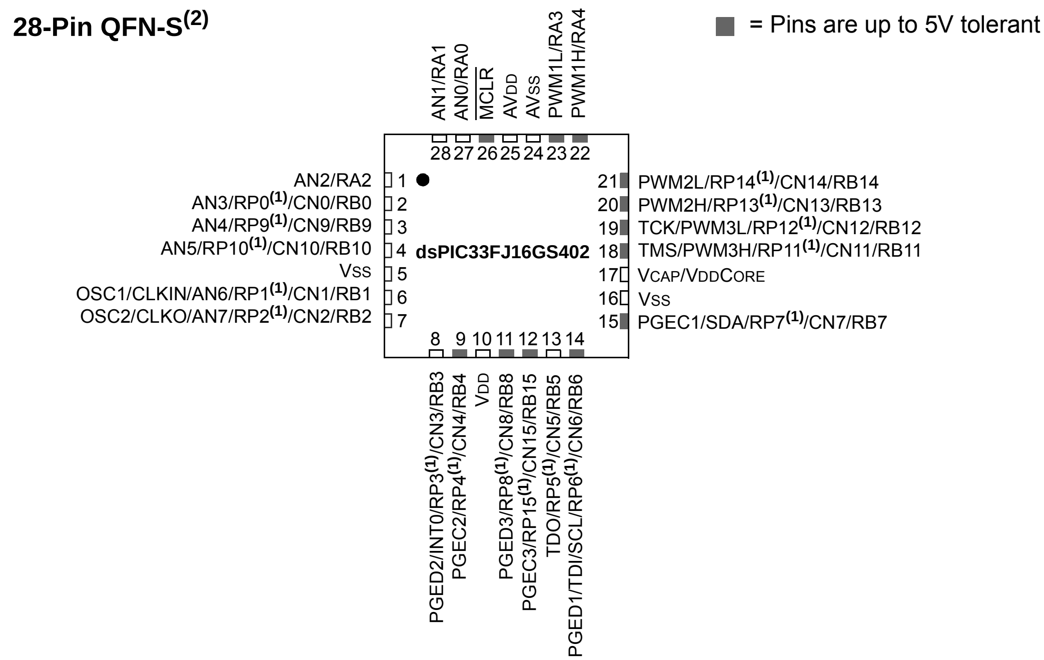
28-Pin QFN-S(2)

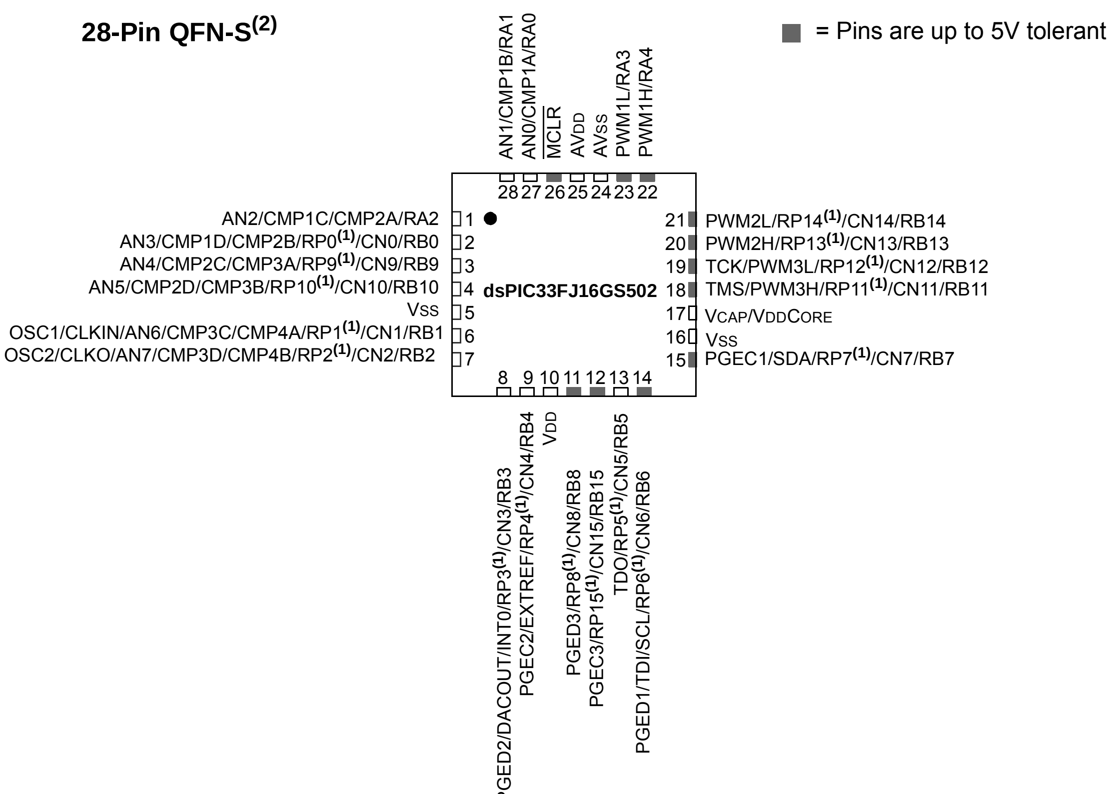


Note 1: The RPn pins can be used by any remappable peripheral. See the **"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families"** table for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)





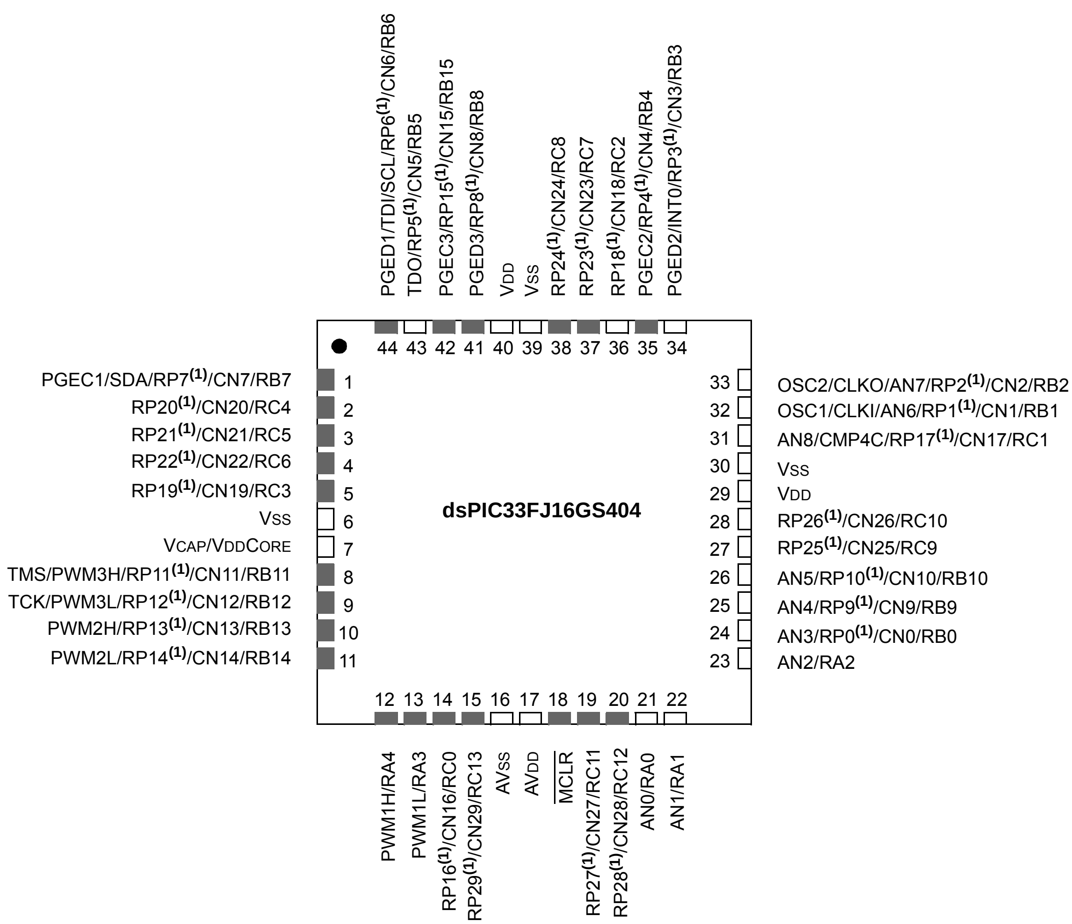
Note 1: The RPn pins can be used by any remappable peripheral. See the **"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families"** table for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

44-Pin QFN(2)

■ = Pins are up to 5V tolerant

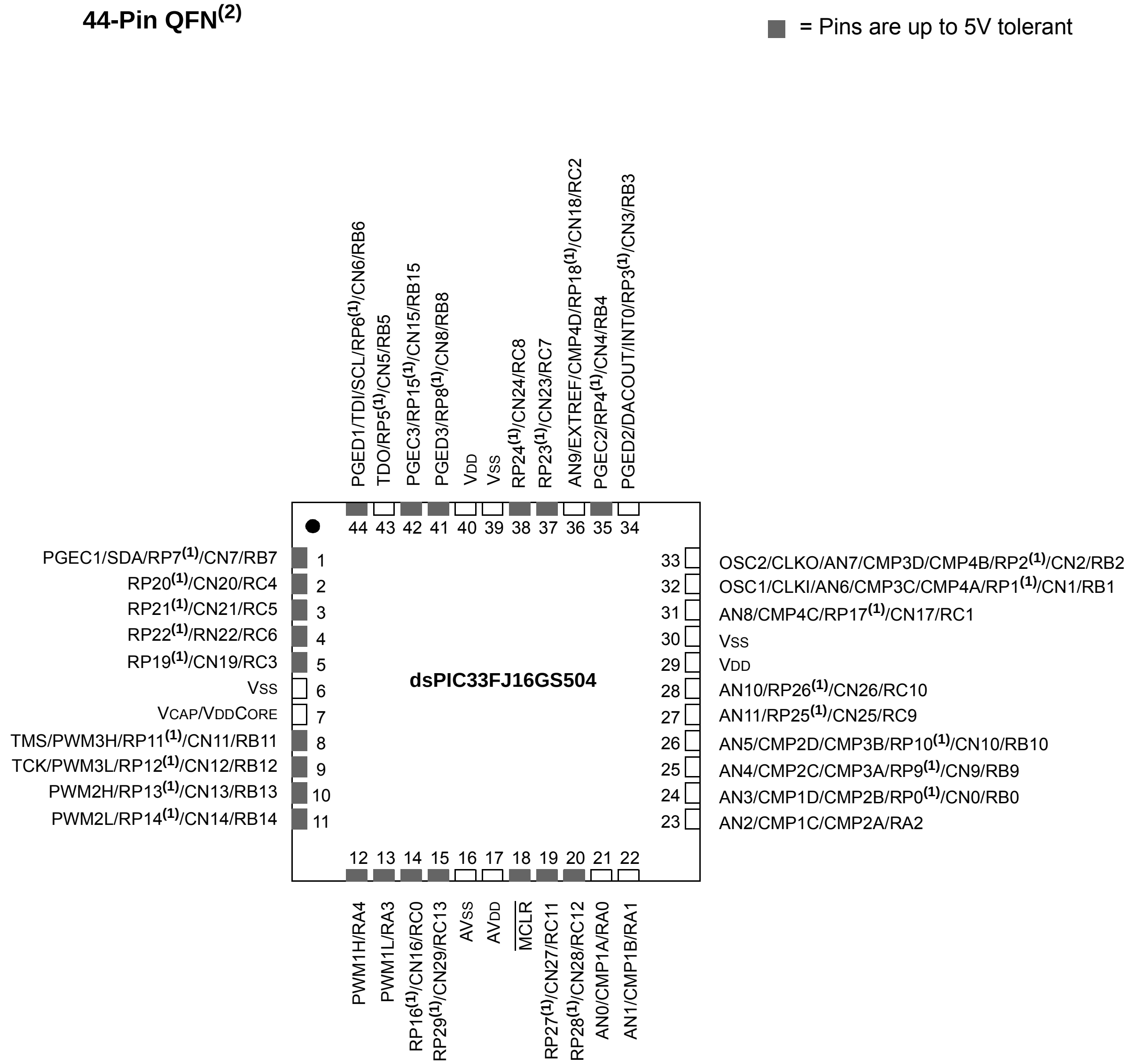


Note 1: The RPn pins can be used by any remappable peripheral. See the **"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families"** table for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

44-Pin QFN(2)

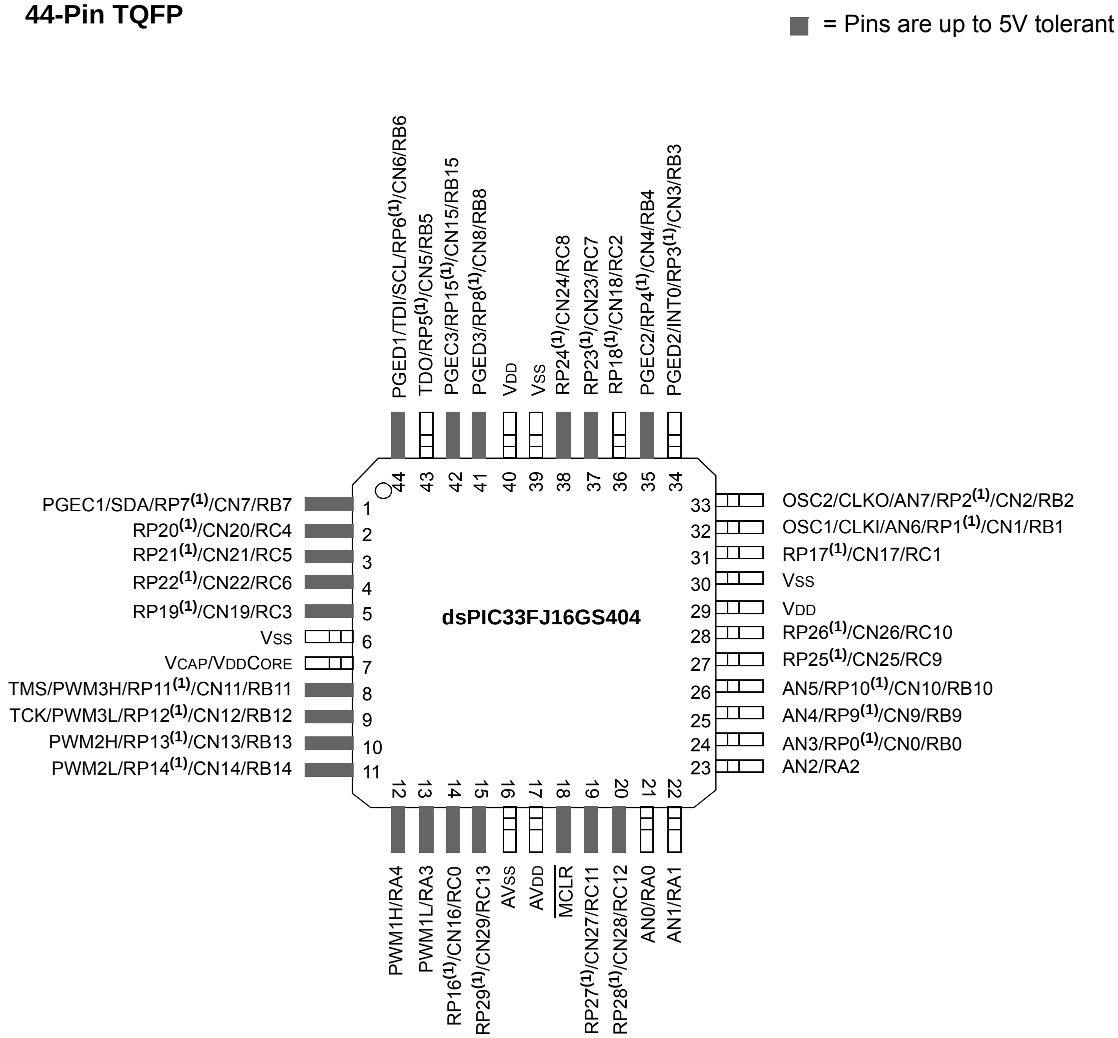


Note 1: The RPn pins can be used by any remappable peripheral. See the **"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families"** table for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to connect to VSS externally.

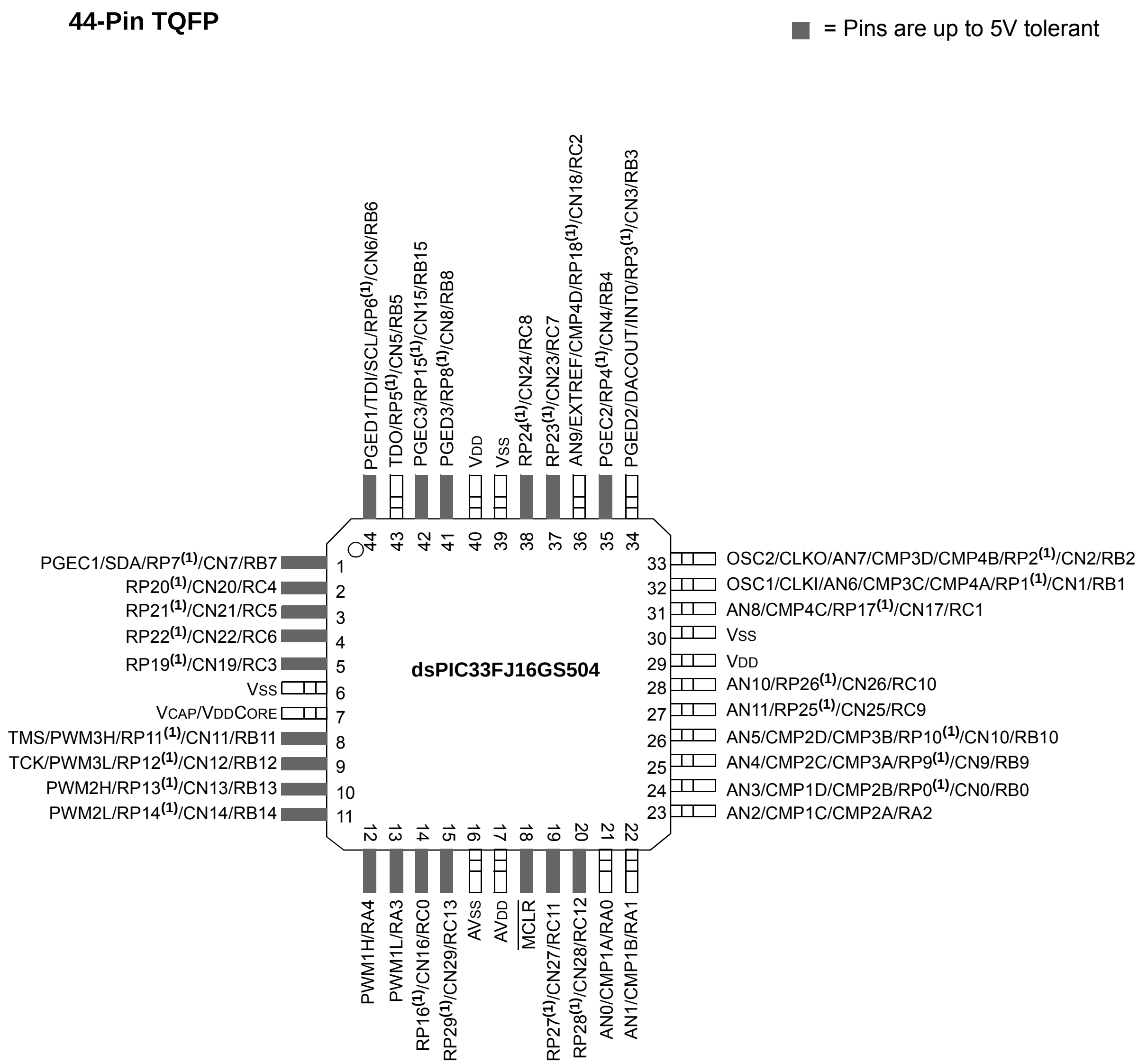
Pin Diagrams (Continued)

44-Pin TQFP



Note 1: The RPn pins can be used by any remappable peripheral. See the **"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families"** table for the list of available peripherals

Pin Diagrams (Continued)



Note 1: The RPn pins can be used by any remappable peripheral. See the **"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families"** table for the list of available peripherals

Table of Contents

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1.0 DEVICE OVERVIEW

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest *"dsPIC33F Family Reference Manual"* sections.

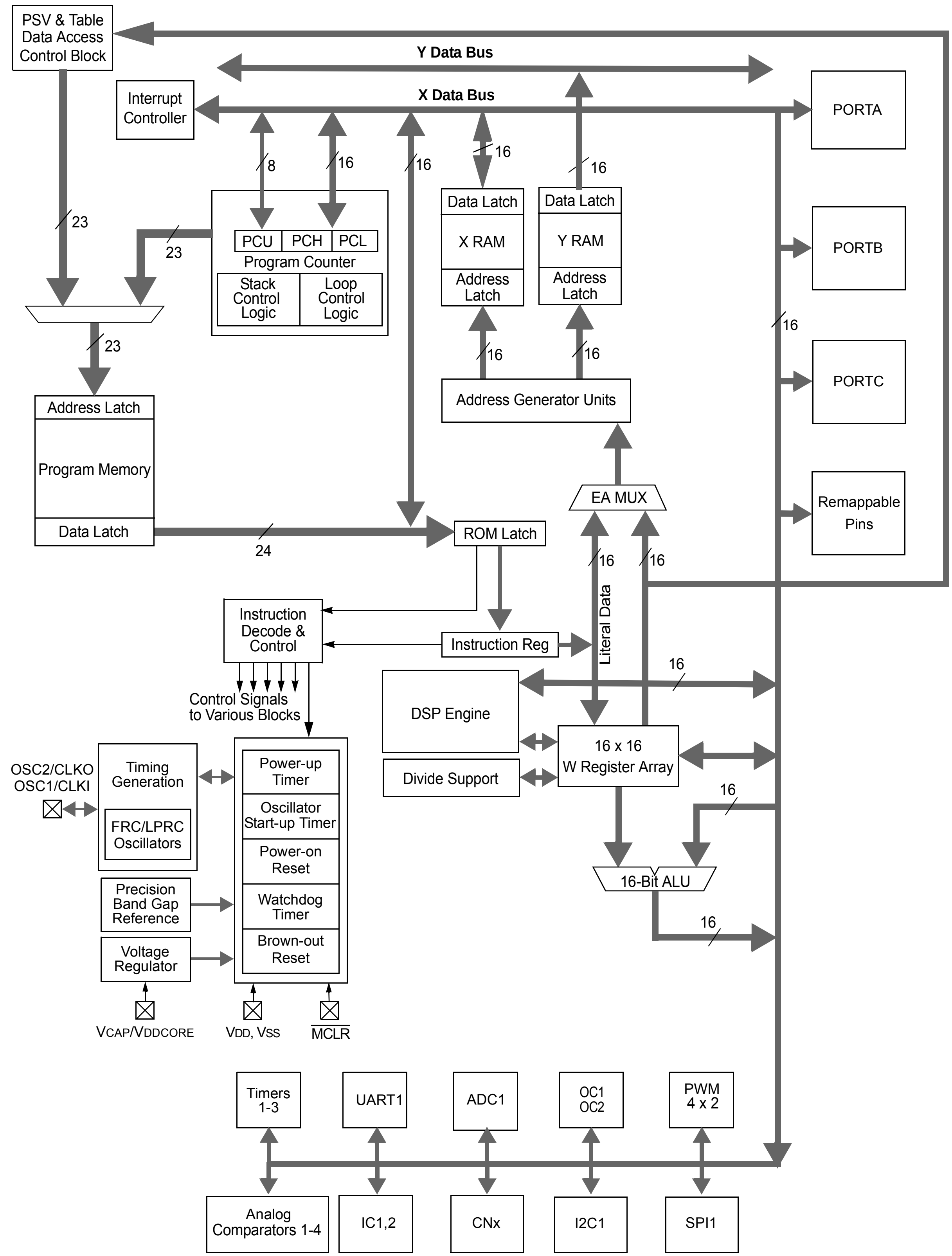
This document contains device-specific information for the following dsPIC33F Digital Signal Controller (DSC) devices:

- dsPIC33FJ06GS101
- dsPIC33FJ06GS102
- dsPIC33FJ06GS202
- dsPIC33FJ16GS402
- dsPIC33FJ16GS404
- dsPIC33FJ16GS502
- dsPIC33FJ16GS504

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit microcontroller (MCU) architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 BLOCK DIAGRAM



Note: Not all pins or features are implemented on all device pinout configurations. See pinout diagrams for the specific pins and features present on each device.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS Capable	Description
AN0-AN11	I	Analog	No	Analog input channels
CLKI	I	ST/CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
CN0-CN29	I	ST	No	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
IC1-IC2	I	ST	Yes	Capture inputs 1/2
OCFA	I	ST	Yes	Compare Fault A input (for Compare Channels 1 and 2)
OC1-OC2	O	—	Yes	Compare Outputs 1 through 2
INT0	I	ST	No	External Interrupt 0
INT1	I	ST	Yes	External Interrupt 1
INT2	I	ST	Yes	External Interrupt 2
RA0-RA4	I/O	ST	No	PORTA is a bidirectional I/O port
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port
RC0-RC13	I/O	ST	No	PORTC is a bidirectional I/O port
RP0-RP29	I/O	ST	No	Remappable I/O pins
T1CK	I	ST	Yes	Timer1 external clock input
T2CK	I	ST	Yes	Timer2 external clock input
T3CK	I	ST	Yes	Timer3 external clock input
$\overline{U1CTS}$	I	ST	Yes	UART1 clear to send
$\overline{U1RTS}$	O	—	Yes	UART1 ready to send
U1RX	I	ST	Yes	UART1 receive
U1TX	O	—	Yes	UART1 transmit
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1
SDI1	I	ST	Yes	SPI1 data in
SDO1	O	—	Yes	SPI1 data out
$\overline{SS1}$	I/O	ST	Yes	SPI1 slave synchronization or frame pulse I/O
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1
TMS	I	TTL	No	JTAG Test mode select pin
TCK	I	TTL	No	JTAG test clock input pin
TDI	I	TTL	No	JTAG test data input pin
TDO	O	—	No	JTAG test data output pin

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; I = Input
ST = Schmitt Trigger input with CMOS levels; P = Power; O = Output
TTL = Transistor-Transistor Logic; PPS = Peripheral Pin Select

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS Capable	Description
CMP1A	I	Analog	No	Comparator 1 Channel A
CMP1B	I	Analog	No	Comparator 1 Channel B
CMP1C	I	Analog	No	Comparator 1 Channel C
CMP1D	I	Analog	No	Comparator 1 Channel D
CMP2A	I	Analog	No	Comparator 2 Channel A
CMP2B	I	Analog	No	Comparator 2 Channel B
CMP2C	I	Analog	No	Comparator 2 Channel C
CMP2D	I	Analog	No	Comparator 2 Channel D
CMP3A	I	Analog	No	Comparator 3 Channel A
CMP3B	I	Analog	No	Comparator 3 Channel B
CMP3C	I	Analog	No	Comparator 3 Channel C
CMP3D	I	Analog	No	Comparator 3 Channel D
CMP4A	I	Analog	No	Comparator 4 Channel A
CMP4B	I	Analog	No	Comparator 4 Channel B
CMP4C	I	Analog	No	Comparator 4 Channel C
CMP4D	I	Analog	No	Comparator 4 Channel D
DACOUT	O	—	No	DAC output voltage
ACMP1-ACMP4	O	—	Yes	DAC trigger to PWM module
EXTREF	I	Analog	No	External voltage reference input for the reference DACs
REFCLKO	O	—	Yes	REFCLKO output signal is a postscaled derivative of the system clock
FLT1-FLT8	I	ST	Yes	Fault Inputs to PWM module
SYNCI1-SYNCI2	I	ST	Yes	External synchronization signal to PWM Master Time Base
SYNCO1	O	—	Yes	PWM master time base for external device synchronization
PWM1L	O	—	No	PWM1 low output
PWM1H	O	—	No	PWM1 high output
PWM2L	O	—	No	PWM2 low output
PWM2H	O	—	No	PWM2 high output
PWM3L	O	—	No	PWM3 low output
PWM3H	O	—	No	PWM3 high output
PWM4L	O	—	Yes	PWM4 low output
PWM4H	O	—	Yes	PWM4 high output
PGED1	I/O	ST	No	Data I/O pin for programming/debugging communication Channel 1
PGEC1	I	ST	No	Clock input pin for programming/debugging communication Channel 1
PGED2	I/O	ST	No	Data I/O pin for programming/debugging communication Channel 2
PGEC2	I	ST	No	Clock input pin for programming/debugging communication Channel 2
PGED3	I/O	ST	No	Data I/O pin for programming/debugging communication Channel 3
PGEC3	I	ST	No	Clock input pin for programming/debugging communication Channel 3
$\overline{\text{MCLR}}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules
VDD	P	—	No	Positive supply for peripheral logic and I/O pins
VCAP/VDDCORE	P	—	No	CPU logic filter capacitor connection
VSS	P	—	No	Ground reference for logic and I/O pins

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; I = Input
ST = Schmitt Trigger input with CMOS levels; P = Power; O = Output
TTL = Transistor-Transistor Logic; PPS = Peripheral Pin Select

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *dsPIC33F Family Reference Manual*, which is available from the Microchip website (www.microchip.com).

2.1 Basic Connection Requirements

Getting started with the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 family of 16-bit Digital Signal Controllers (DSC) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used) (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP/VDDCORE (see **Section 2.3 "Capacitor on Internal Voltage Regulator (VCAP/VDDCORE)"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used (see **Section 2.6 "External Oscillator Pins"**)

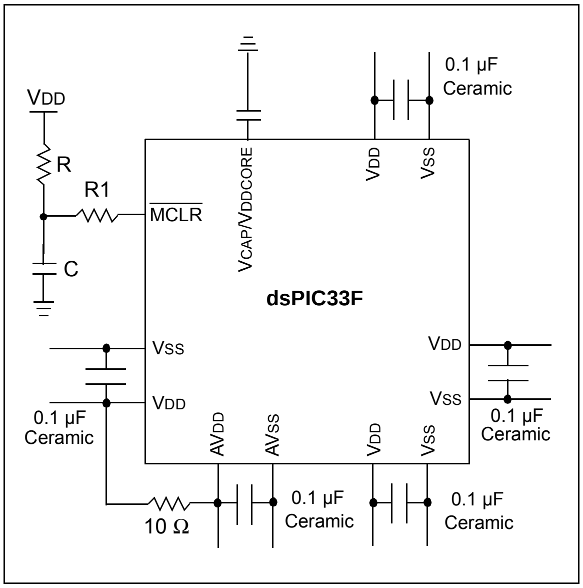
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 Capacitor on Internal Voltage Regulator (V_{CAP}/V_{DDCORE})

A low-ESR (< 5 Ohms) capacitor is required on the V_{CAP}/V_{DDCORE} pin, which is used to stabilize the voltage regulator output voltage. The V_{CAP}/V_{DDCORE} pin must not be connected to V_{DD}, and must have a capacitor between 4.7 µF and 10 µF, 16V connected to ground. The type can be ceramic or tantalum. Refer to **Section 24.0 “Electrical Characteristics”** for additional information.

The placement of this capacitor should be close to the V_{CAP}/V_{DDCORE}. It is recommended that the trace length not exceed one-quarter inch (6 mm). Refer to **Section 21.2 “On-Chip Voltage Regulator”** for details.

2.4 Master Clear ($\overline{\text{MCLR}}$) Pin

The $\overline{\text{MCLR}}$ pin provides for two specific device functions:

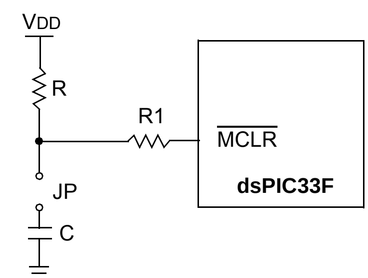
- Device Reset
- Device programming and debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor C, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations.

Place the components shown in Figure 2-2 within one-quarter inch (6 mm) from the $\overline{\text{MCLR}}$ pin.

FIGURE 2-2: EXAMPLE OF $\overline{\text{MCLR}}$ PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{\text{MCLR}}$ pin V_{IH} and V_{IL} specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into $\overline{\text{MCLR}}$ from the external capacitor C, in the event of $\overline{\text{MCLR}}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{\text{MCLR}}$ pin V_{IH} and V_{IL} specifications are met.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 2, MPLAB® ICD 3, or MPLAB® REAL ICE™.

For more information on ICD 2, ICD 3, and REAL ICE connection requirements, refer to the following documents that are available on the Microchip website.

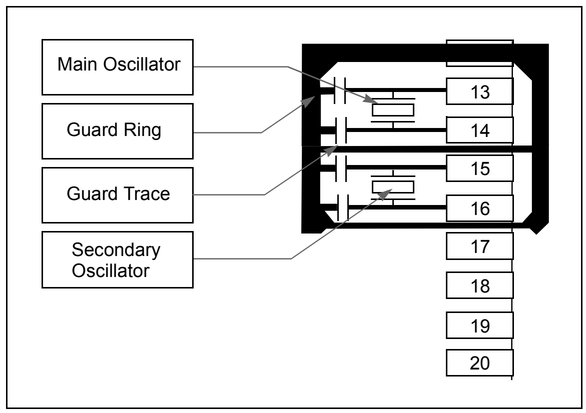
- “MPLAB® ICD 2 In-Circuit Debugger User's Guide” DS51331
- “Using MPLAB® ICD 2” (poster) DS51265
- “MPLAB® ICD 2 Design Advisory” DS51566
- “Using MPLAB® ICD 3” (poster) DS51765
- “MPLAB® ICD 3 Design Advisory” DS51764
- “MPLAB® REAL ICE™ In-Circuit Debugger User's Guide” DS51616
- “Using MPLAB® REAL ICE™” (poster) DS51749

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 “Oscillator Configuration”** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 4 MHz < F_{IN} < 8 MHz to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV, and PLLDBF to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration word.

2.8 Configuration of Analog and Digital Pins During ICSP Operations

If MPLAB ICD 2, ICD 3 or REAL ICE is selected as a debugger, it automatically initializes all of the A/D input pins (ANx) as "digital" pins, by setting all bits in the ADPCFG register.

The bits in the registers that correspond to the A/D pins that are initialized by MPLAB ICD 2, ICD 3, or REAL ICE, must not be cleared by the user application firmware; otherwise, communication errors will result between the debugger and the device.

If your application needs to use certain A/D pins as analog input pins during the debug session, the user application must clear the corresponding bits in the ADPCFG register during initialization of the ADC module.

When MPLAB ICD 2, ICD 3, or REAL ICE is used as a programmer, the user application firmware must correctly configure the ADPCFG register. Automatic initialization of these registers is only done during debugger operation. Failure to correctly configure the register(s) will result in all A/D pins being recognized as analog input pins, resulting in the port value being read as a logic '0', which may affect user application functionality.

2.9 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic-low state.

Alternatively, connect a 1k to 10k resistor to V_{SS} on unused pins and drive the output to logic low.

2.10 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-4 through Figure 2-11.

FIGURE 2-4: DIGITAL PFC

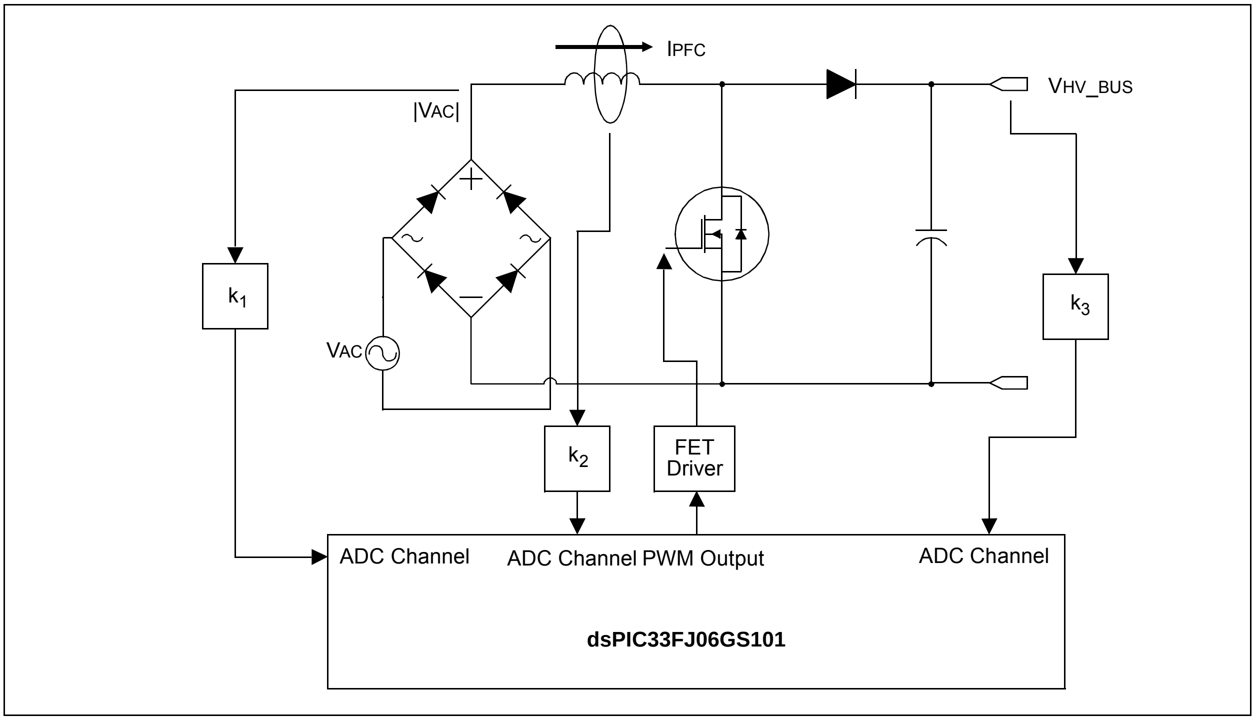


FIGURE 2-5: BOOST CONVERTER IMPLEMENTATION

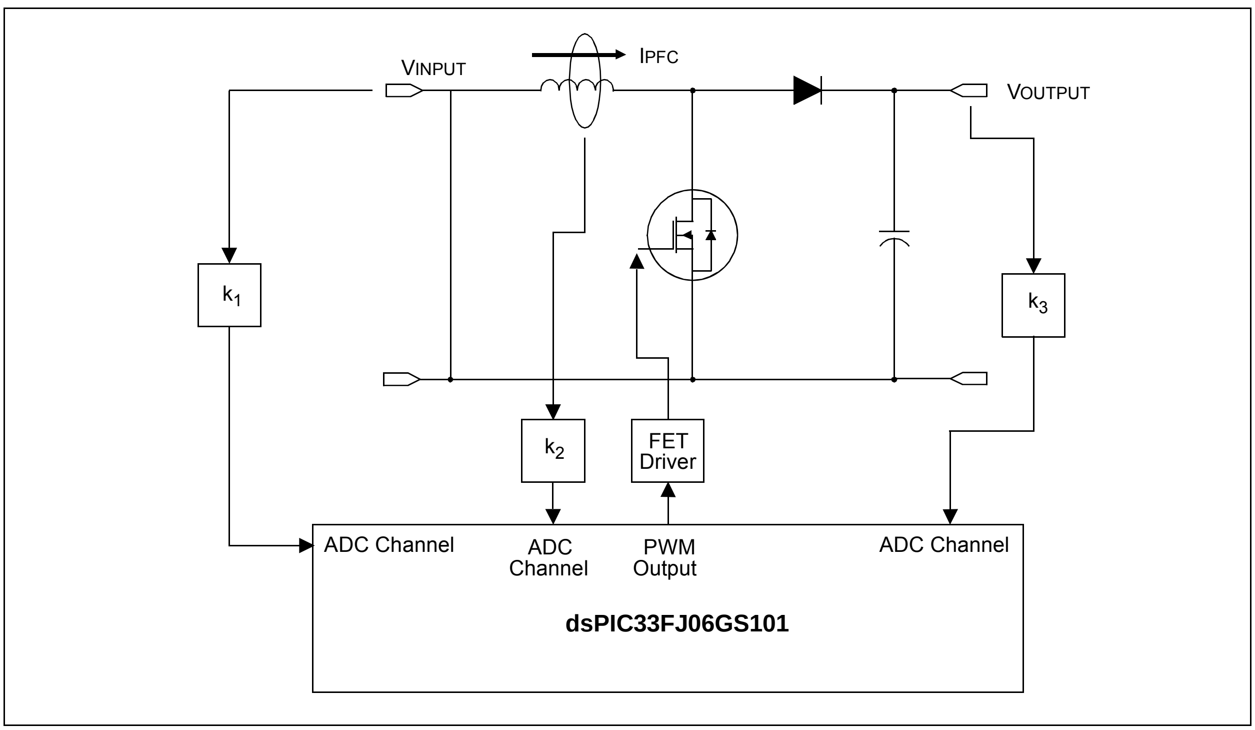


FIGURE 2-6: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER

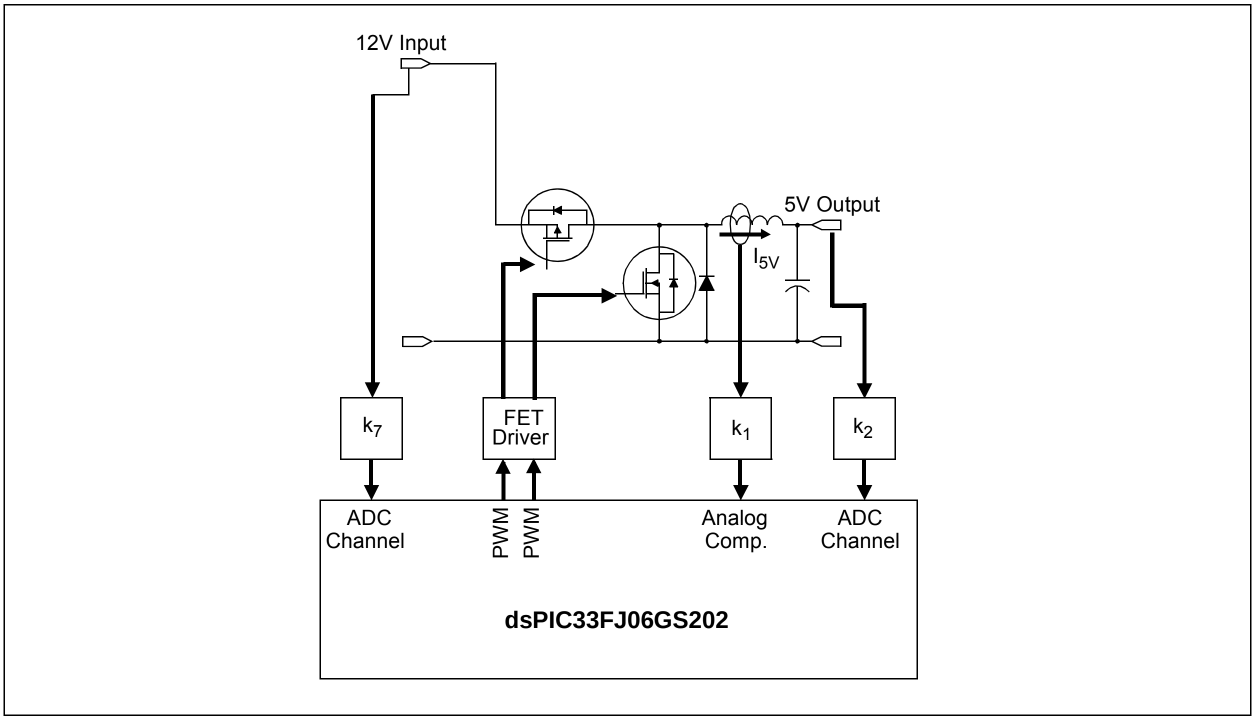
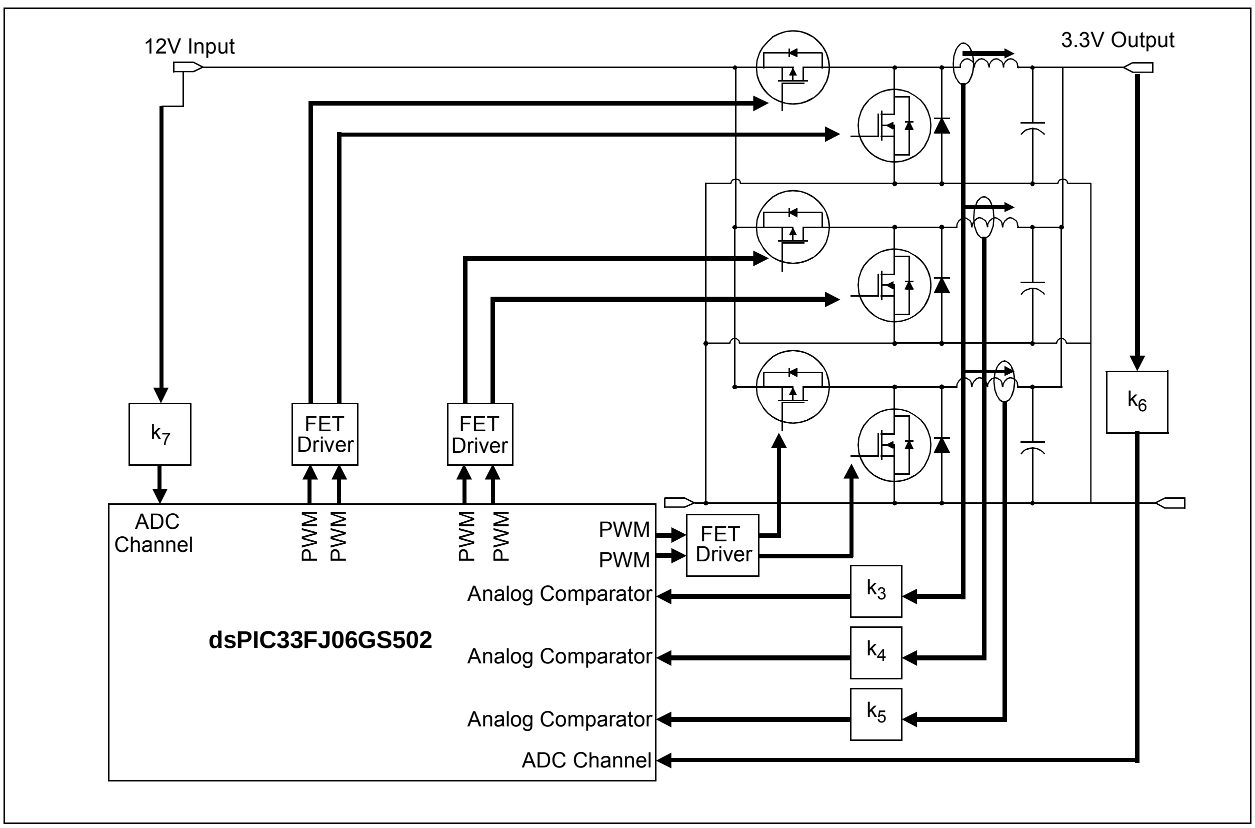


FIGURE 2-7: MULTI-PHASE SYNCHRONOUS BUCK CONVERTER



 Preliminary

FIGURE 2-8: OFF-LINE UPS

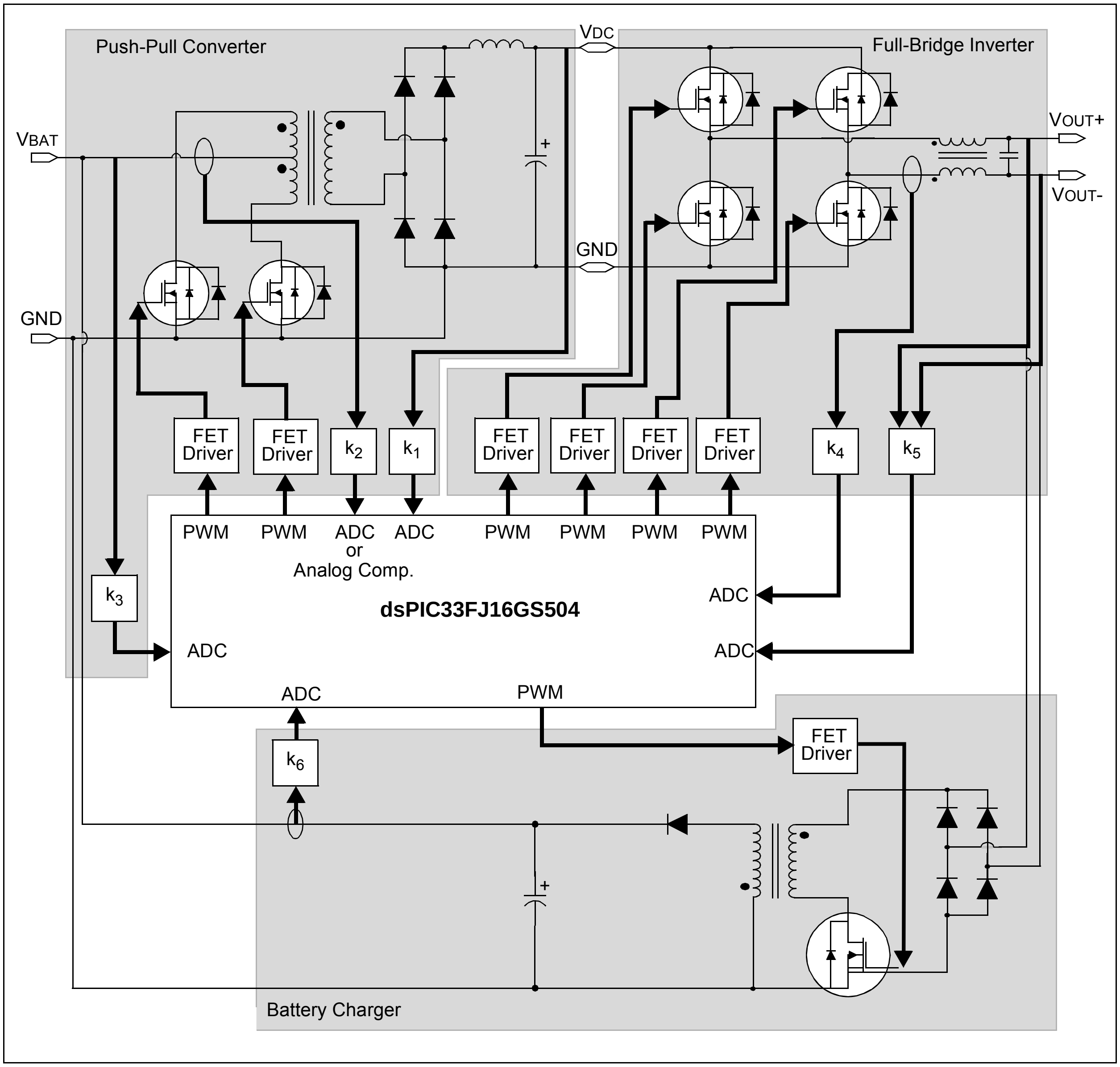


FIGURE 2-9: INTERLEAVED PFC

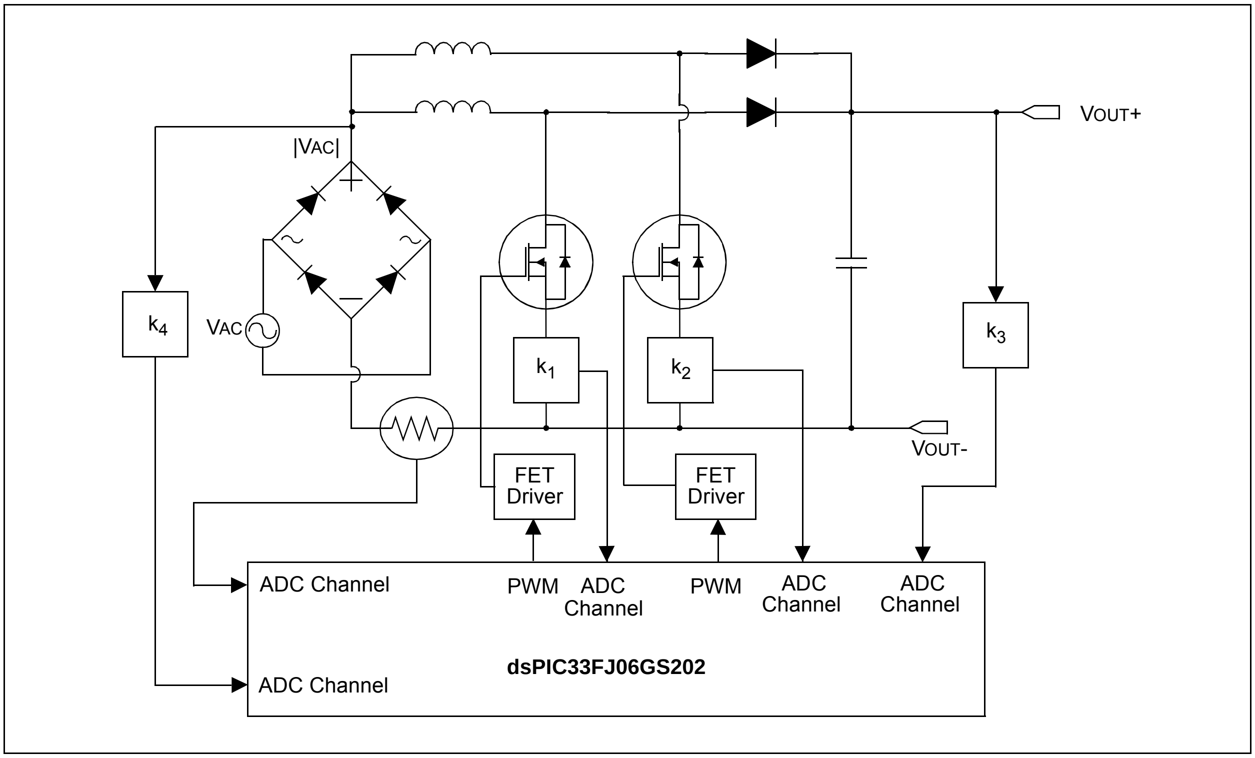


FIGURE 2-10: PHASE-SHIFTED FULL-BRIDGE CONVERTER

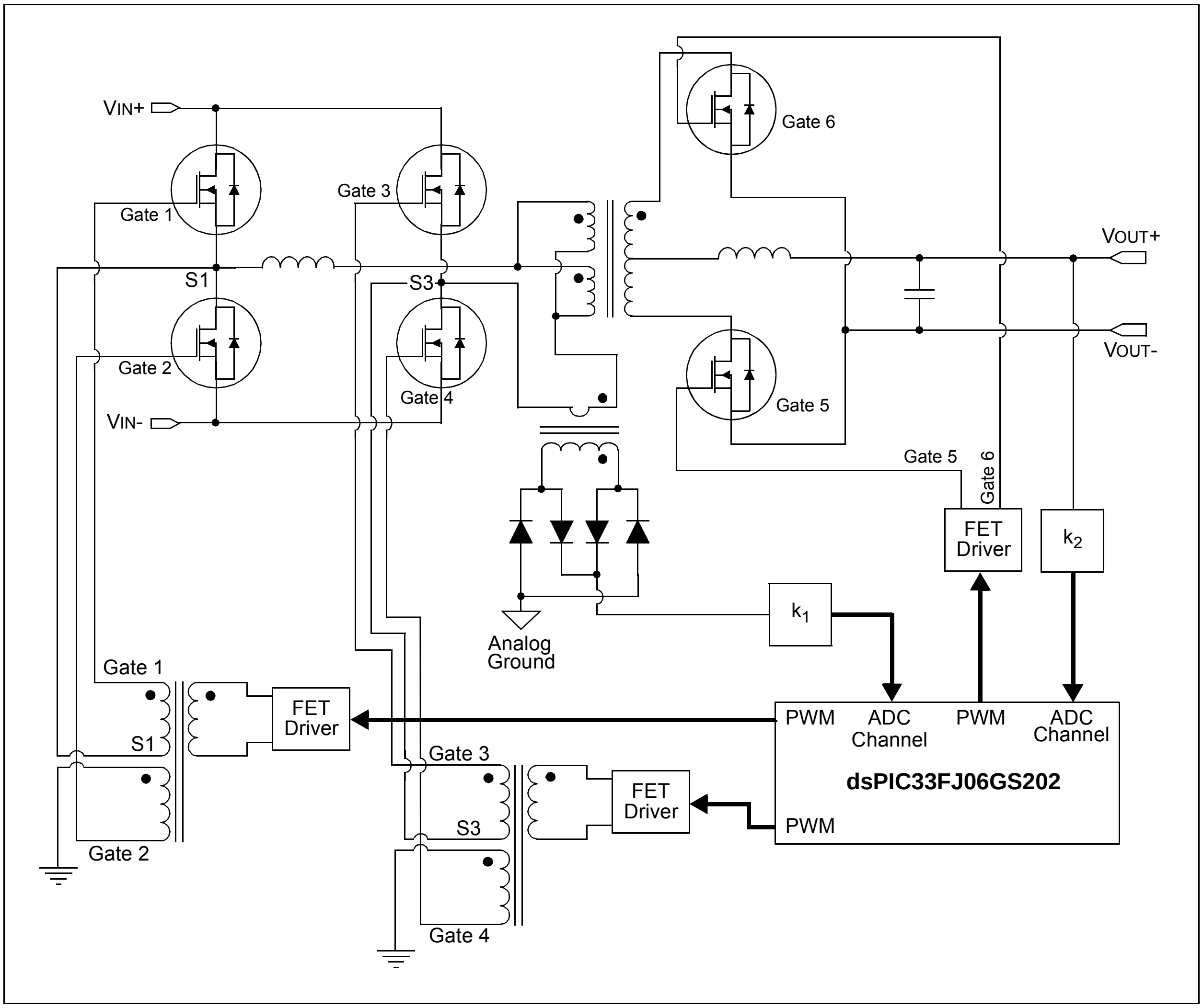
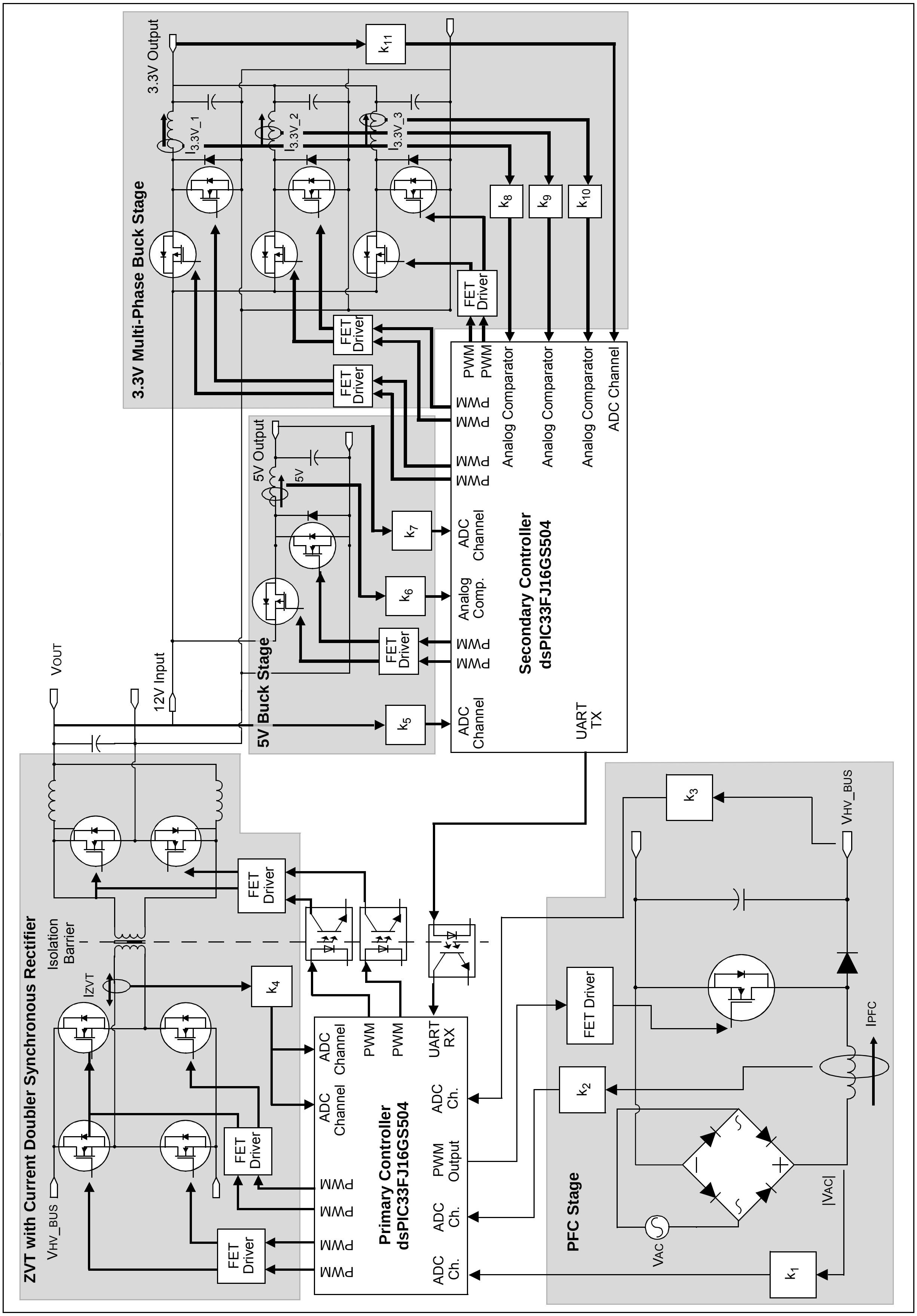


FIGURE 2-11: AC-TO-DC POWER SUPPLY WITH PFC AND THREE OUTPUTS (12V, 5V, AND 3.3V)



 Preliminary

3.0 CPU

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33F Family Reference Manual*", **Section 2. "CPU"** (DS70204), which is available from the Microchip web site (www.microchip.com).

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies from device to device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The sixteenth working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

There are two classes of instruction in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices: MCU and DSP. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1, and the programmer's model for the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 is shown in Figure 3-2.

3.1 Data Addressing Overview

The data space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

Overhead-free circular buffers (Modulo Addressing mode) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program-to-data space mapping feature lets any instruction access program space as if it were data space.

3.2 DSP Engine Overview

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value up to 16 bits, right or left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The `MAC` instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.

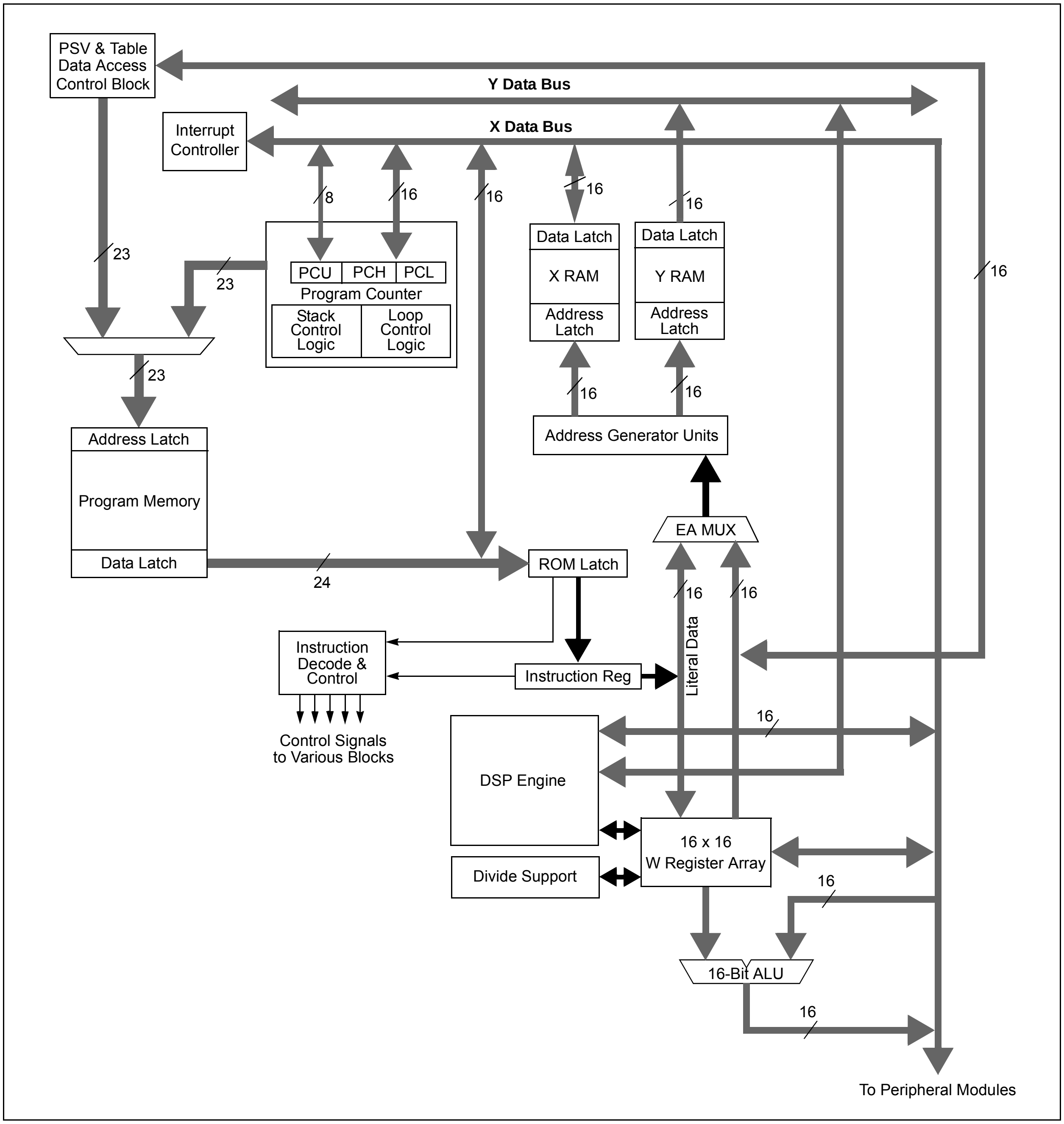
3.3 Special MCU Features

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 features a 17-bit by 17-bit single-cycle multiplier that is shared by both the MCU ALU and DSP engine. The multiplier can perform signed, unsigned and mixed sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication not only allows you to perform mixed sign multiplication, it also achieves accurate results for special operations, such as (-1.0) x (-1.0).

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 supports 16/16 and 32/16 divide operations, both fractional and integer. All divide instructions are iterative operations. They must be executed within a `REPEAT` loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data.

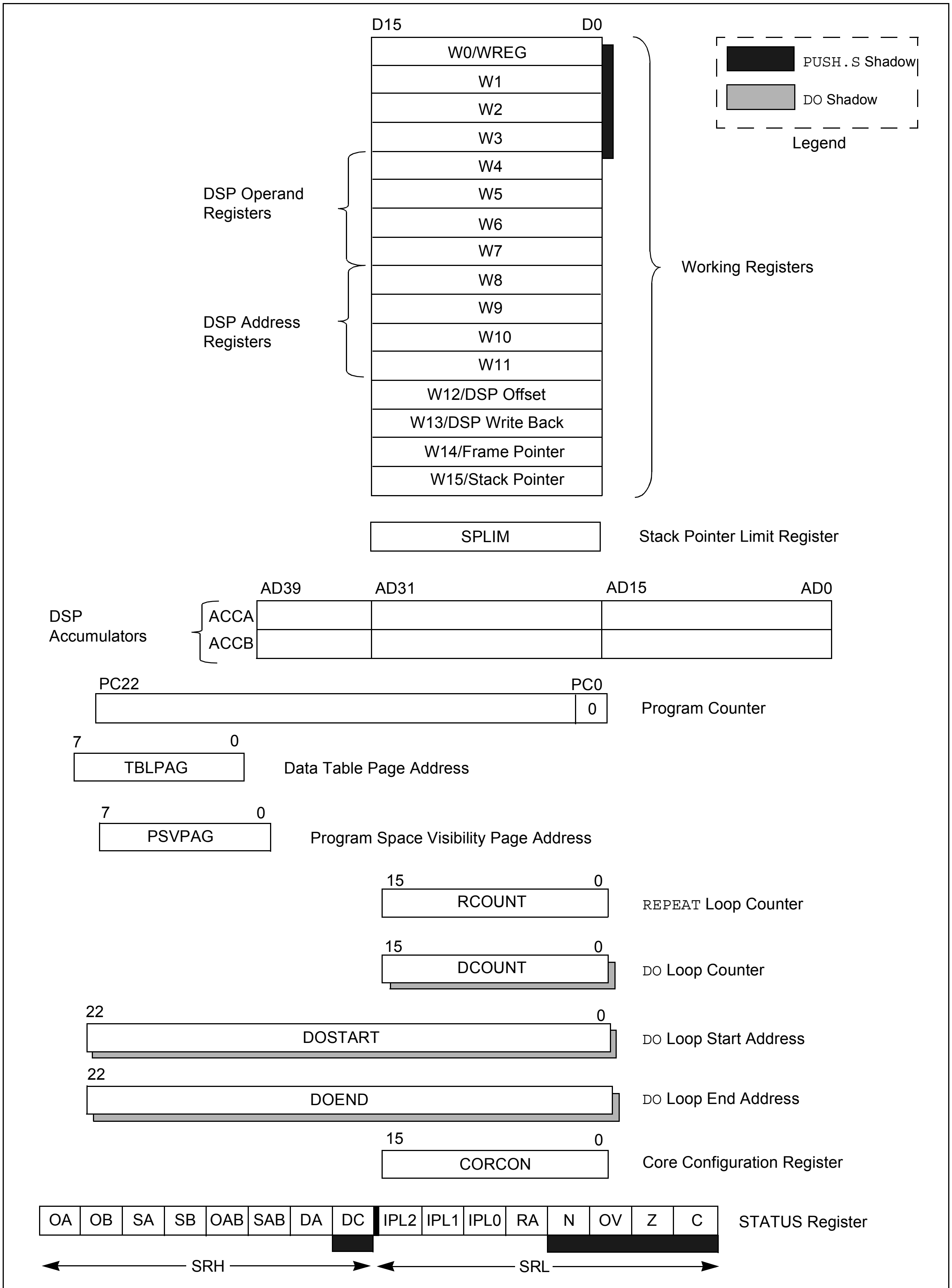
A 40-bit barrel shifter is used to perform up to a 16-bit left or right shift in a single cycle. The barrel shifter can be used by both MCU and DSP instructions.

FIGURE 3-1: dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CPU CORE BLOCK DIAGRAM



 Preliminary

FIGURE 3-2: dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 PROGRAMMER'S MODEL



3.4 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

R-0	R-0	R/C-0	R/C-0	R-0	R/C-0	R -0	R/W-0
OA	OB	SA(1)	SB(1)	OAB	SAB(1,4)	DA	DC
bit 15							bit 8

R/W-0(2)	R/W-0(3)	R/W-0(3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0>(2)			RA	N	OV	Z	C
bit 7							bit 0

Legend:		
C = Clearable bit	R = Readable bit	U = Unimplemented bit, read as ‘0’
S = Settable bit	W = Writable bit	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **OA:** Accumulator A Overflow Status bit
1 = Accumulator A overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit
1 = Accumulator B overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation ‘Sticky’ Status bit(1)
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

bit 12 **SB:** Accumulator B Saturation ‘Sticky’ Status bit(1)
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit
1 = Accumulators A or B have overflowed
0 = Neither Accumulators A or B have overflowed

bit 10 **SAB:** SA || SB Combined Accumulator ‘Sticky’ Status bit(1,4)
1 = Accumulators A or B are saturated or have been saturated at some time in the past
0 = Neither Accumulator A or B are saturated

bit 9 **DA:** DO Loop Active bit
1 = DO loop in progress
0 = DO loop not in progress

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

Note 1: This bit can be read or cleared (not set).

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

3: The IPL<2:0> Status bits are read-only when NSTDIS = 1 (INTCON1<15>).

4: Clearing this bit will clear SA and SB.

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits[2]

111 = CPU Interrupt Priority Level is 7 (15), user interrupts disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit

1 = REPEAT loop in progress
0 = REPEAT loop not in progress

bit 3 **N:** MCU ALU Negative bit

1 = Result was negative
0 = Result was non-negative (zero or positive)

bit 2 **OV:** MCU ALU Overflow bit

This bit is used for signed arithmetic (2's complement). It indicates an overflow of a magnitude that causes the sign bit to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = No overflow occurred

bit 1 **Z:** MCU ALU Zero bit

1 = An operation that affects the Z bit has set it at some time in the past
0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)

bit 0 **C:** MCU ALU Carry/$\overline{\text{Borrow}}$ bit

1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: This bit can be read or cleared (not set).

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

3: The IPL<2:0> Status bits are read-only when NSTDIS = 1 (INTCON1<15>).

4: Clearing this bit will clear SA and SB.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R-0	R-0	R-0
—	—	—	US	EDT(1)	DL<2:0>		
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3(2)	PSV	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	-n = Value at POR	'1' = Bit is set
0' = Bit is cleared	'x = Bit is unknown	U = Unimplemented bit, read as '0'	

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **US:** DSP Multiply Unsigned/Signed Control bit
1 = DSP engine multiplies are unsigned
0 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit(1)
1 = Terminate executing DO loop at end of current loop iteration
0 = No effect

bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits
111 = 7 DO loops active
•
•
•
001 = 1 DO loop active
000 = 0 DO loops active

bit 7 **SATA:** ACCA Saturation Enable bit
1 = Accumulator A saturation enabled
0 = Accumulator A saturation disabled

bit 6 **SATB:** ACCB Saturation Enable bit
1 = Accumulator B saturation enabled
0 = Accumulator B saturation disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit
1 = Data space write saturation enabled
0 = Data space write saturation disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit
1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **PSV:** Program Space Visibility in Data Space Enable bit
1 = Program space visible in data space
0 = Program space not visible in data space

bit 1 **RND:** Rounding Mode Select bit
1 = Biased (conventional) rounding enabled
0 = Unbiased (convergent) rounding enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit
1 = Integer mode enabled for DSP multiply ops
0 = Fractional mode enabled for DSP multiply ops

Note 1: This bit will always read as '0'.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

3.5 Arithmetic Logic Unit (ALU)

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as $\overline{\text{Borrow}}$ and $\overline{\text{Digit Borrow}}$ bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the "*dsPIC30F/33F Programmer's Reference Manual*" (DS70157) for information on the SR bits affected by each instruction.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit-divisor division.

3.5.1 MULTIPLIER

Using the high-speed, 17-bit x 17-bit multiplier of the DSP engine, the ALU supports unsigned, signed or mixed sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.5.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.6 DSP Engine

The DSP engine consists of a high-speed, 17-bit x 17-bit multiplier, a barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 is a single-cycle instruction flow architecture; therefore, concurrent operation of the DSP engine with MCU instruction flow is not possible. However, some MCU ALU and DSP engine resources can be used concurrently by the same instruction (for example, ED, EDAC).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are `ADD`, `SUB` and `NEG`.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

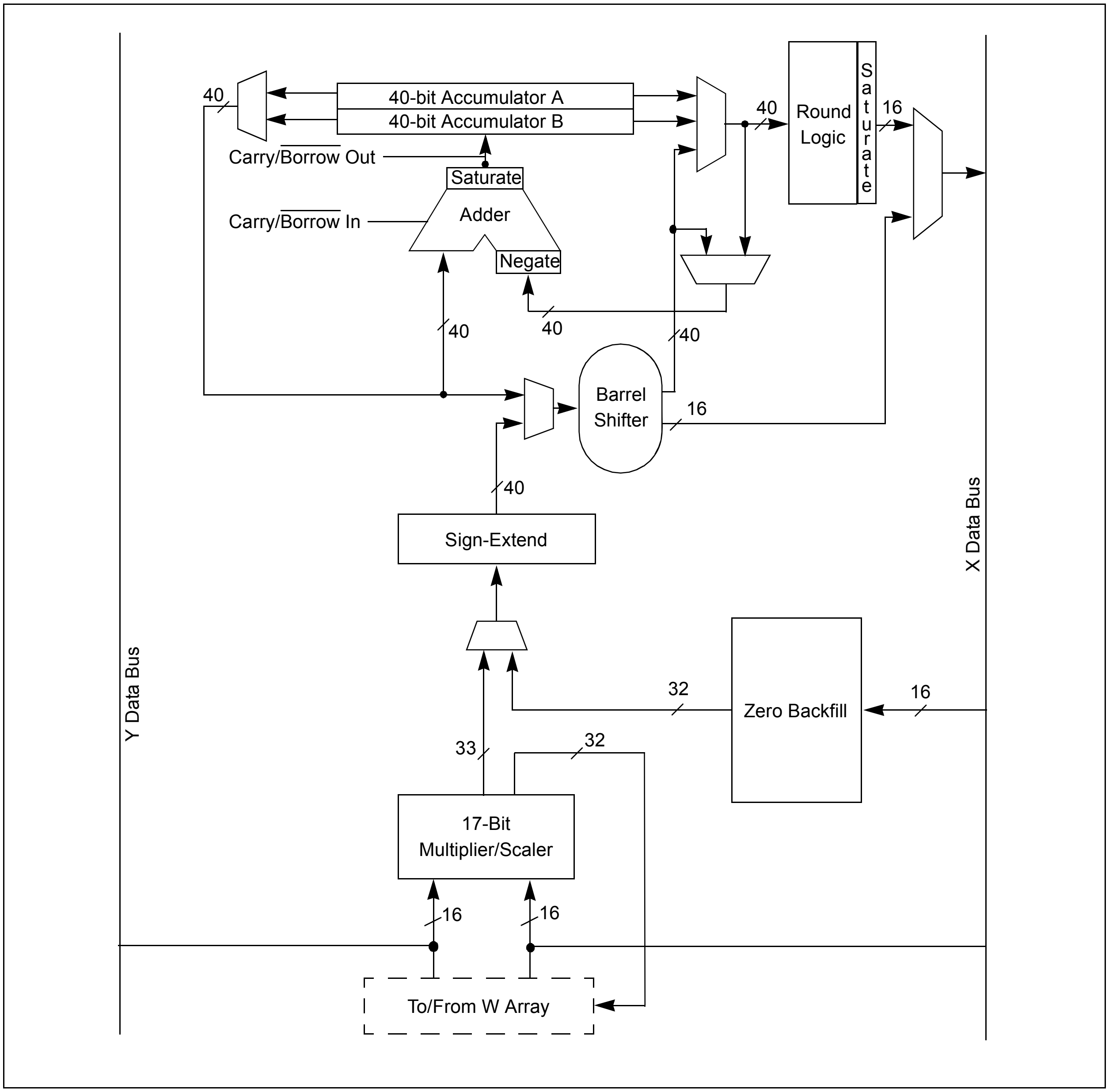
- Fractional or integer DSP multiply (IF)
- Signed or unsigned DSP multiply (US)
- Conventional or convergent rounding (RND)
- Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

A block diagram of the DSP engine is shown in Figure 3-3.

TABLE 3-1: DSP INSTRUCTIONS SUMMARY

Instruction	Algebraic Operation	ACC Write Back
CLR	$A = 0$	Yes
ED	$A = (x - y)2$	No
EDAC	$A = A + (x - y)2$	No
MAC	$A = A + (x * y)$	Yes
MAC	$A = A + x2$	No
MOVSAC	No change in A	Yes
MPY	$A = x * y$	No
MPY	$A = x\ 2$	No
MPY.N	$A = - x * y$	No
MSC	$A = A - x * y$	Yes

FIGURE 3-3: DSP ENGINE BLOCK DIAGRAM



 Preliminary

3.6.1 MULTIPLIER

The 17-bit x 17-bit multiplier is capable of signed or unsigned operation and can multiplex its output using a scaler to support either 1.31 fractional (Q31) or 32-bit integer results. Unsigned operands are zero-extended into the 17th bit of the multiplier input value. Signed operands are sign-extended into the 17th bit of the multiplier input value. The output of the 17-bit x 17-bit multiplier/scaler is a 33-bit value that is sign-extended to 40 bits. Integer data is inherently represented as a signed 2's complement value, where the Most Significant bit (MSb) is defined as a sign bit. The range of an N-bit 2's complement integer is -2^{N-1} to $2^{N-1} - 1$.

- For a 16-bit integer, the data range is -32768 (0x8000) to 32767 (0x7FFF) including 0.
- For a 32-bit integer, the data range is -2,147,483,648 (0x8000 0000) to 2,147,483,647 (0x7FFF FFFF).

When the multiplier is configured for fractional multiplication, the data is represented as a 2's complement fraction, where the MSb is defined as a sign bit and the radix point is implied to lie just after the sign bit (QX format). The range of an N-bit 2's complement fraction with this implied radix point is -1.0 to $(1 - 2^{1-N})$. For a 16-bit fraction, the Q15 data range is -1.0 (0x8000) to 0.999969482 (0x7FFF) including 0 and has a precision of 3.01518×10^{-5}. In Fractional mode, the 16 x 16 multiply operation generates a 1.31 product that has a precision of 4.65661×10^{-10}.

The same multiplier is used to support the MCU multiply instructions, which include integer 16-bit signed, unsigned and mixed sign multiply operations.

The `MUL` instruction can be directed to use byte or word-sized operands. Byte operands will direct a 16-bit result, and word operands will direct a 32-bit result to the specified register(s) in the W array.

3.6.2 DATA ACCUMULATORS AND ADDER/SUBTRACTER

The data accumulator consists of a 40-bit adder/subtracter with automatic sign extension logic. It can select one of two accumulators (A or B) as its pre-accumulation source and post-accumulation destination. For the `ADD` and `LAC` instructions, the data to be accumulated or loaded can be optionally scaled using the barrel shifter prior to accumulation.

3.6.2.1 Adder/Subtracter, Overflow and Saturation

The adder/subtracter is a 40-bit adder with an optional zero input into one side, and either true or complement data into the other input.

- In the case of addition, the Carry/$\overline{\text{Borrow}}$ input is active-high and the other input is true data (not complemented).
- In the case of subtraction, the Carry/$\overline{\text{Borrow}}$ input is active-low and the other input is complemented.

The adder/subtracter generates Overflow Status bits, SA/SB and OA/OB, which are latched and reflected in the STATUS register:

- Overflow from bit 39: this is a catastrophic overflow in which the sign of the accumulator is destroyed.
- Overflow into guard bits, 32 through 39: this is a recoverable overflow. This bit is set whenever all the guard bits are not identical to each other.

The adder has an additional saturation block that controls accumulator data saturation, if selected. It uses the result of the adder, the Overflow Status bits described previously and the SAT<A:B> (CORCON<7:6>) and ACCSAT (CORCON<4>) mode control bits to determine when and to what value to saturate.

Six STATUS register bits support saturation and overflow:

- OA: ACCA overflowed into guard bits
- OB: ACCB overflowed into guard bits
- SA: ACCA saturated (bit 31 overflow and saturation)
  or
  ACCA overflowed into guard bits and saturated (bit 39 overflow and saturation)
- SB: ACCB saturated (bit 31 overflow and saturation)
  or
  ACCB overflowed into guard bits and saturated (bit 39 overflow and saturation)
- OAB: Logical OR of OA and OB
- SAB: Logical OR of SA and SB

The OA and OB bits are modified each time data passes through the adder/subtracter. When set, they indicate that the most recent operation has overflowed into the accumulator guard bits (bits 32 through 39). The OA and OB bits can also optionally generate an arithmetic warning trap when set and the corresponding Overflow Trap Flag Enable bits (OVATE, OVBTE) in the INTCON1 register are set (refer to **Section 7.0 "Interrupt Controller"**). This allows the user application to take immediate action, for example, to correct system gain.

The SA and SB bits are modified each time data passes through the adder/subtracter, but can only be cleared by the user application. When set, they indicate that the accumulator has overflowed its maximum range (bit 31 for 32-bit saturation or bit 39 for 40-bit saturation) and will be saturated (if saturation is enabled). When saturation is not enabled, SA and SB default to bit 39 overflow and thus, indicate that a catastrophic overflow has occurred. If the COVTE bit in the INTCON1 register is set, SA and SB bits will generate an arithmetic warning trap when saturation is disabled.

The Overflow and Saturation Status bits can optionally be viewed in the STATUS Register (SR) as the logical OR of OA and OB (in bit OAB) and the logical OR of SA and SB (in bit SAB). Programmers can check one bit in the STATUS register to determine if either accumulator has overflowed, or one bit to determine if either accumulator has saturated. This is useful for complex number arithmetic, which typically uses both accumulators.

The device supports three Saturation and Overflow modes:

- Bit 39 Overflow and Saturation:
  When bit 39 overflow and saturation occurs, the saturation logic loads the maximally positive 9.31 (0x7FFFFFFFFF) or maximally negative 9.31 value (0x8000000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user application. This condition is referred to as ‘super saturation’ and provides protection against erroneous data or unexpected algorithm problems (such as gain calculations).
- Bit 31 Overflow and Saturation:
  When bit 31 overflow and saturation occurs, the saturation logic then loads the maximally positive 1.31 value (0x007FFFFFFF) or maximally negative 1.31 value (0x0080000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user application. When this Saturation mode is in effect, the guard bits are not used, so the OA, OB or OAB bits are never set.
- Bit 39 Catastrophic Overflow:
  The bit 39 Overflow Status bit from the adder is used to set the SA or SB bit, which remains set until cleared by the user application. No saturation operation is performed, and the accumulator is allowed to overflow, destroying its sign. If the COVTE bit in the INTCON1 register is set, a catastrophic overflow can initiate a trap exception.

3.6.3 ACCUMULATOR ‘WRITE BACK’

The `MAC` class of instructions (with the exception of `MPY`, `MPY.N`, `ED` and `EDAC`) can optionally write a rounded version of the high word (bits 31 through 16) of the accumulator that is not targeted by the instruction into data space memory. The write is performed across the X bus into combined X and Y address space. The following addressing modes are supported:

- W13, Register Direct:
  The rounded contents of the non-target accumulator are written into W13 as a 1.15 fraction.
- [W13] + = 2, Register Indirect with Post-Increment:
  The rounded contents of the non-target accumulator are written into the address pointed to by W13 as a 1.15 fraction. W13 is then incremented by 2 (for a word write).

3.6.3.1 Round Logic

The round logic is a combinational block that performs a conventional (biased) or convergent (unbiased) round function during an accumulator write (store). The Round mode is determined by the state of the RND bit in the CORCON register. It generates a 16-bit, 1.15 data value that is passed to the data space write saturation logic. If rounding is not indicated by the instruction, a truncated 1.15 data value is stored and the least significant word is simply discarded.

Conventional rounding zero-extends bit 15 of the accumulator and adds it to the ACCxH word (bits 16 through 31 of the accumulator).

- If the ACCxL word (bits 0 through 15 of the accumulator) is between 0x8000 and 0xFFFF (0x8000 included), ACCxH is incremented.
- If ACCxL is between 0x0000 and 0x7FFF, ACCxH is left unchanged.

A consequence of this algorithm is that over a succession of random rounding operations, the value tends to be biased slightly positive.

Convergent (or unbiased) rounding operates in the same manner as conventional rounding, except when ACCxL equals 0x8000. In this case, the Least Significant bit (bit 16 of the accumulator) of ACCxH is examined:

- If it is ‘`1`’, ACCxH is incremented.
- If it is ‘`0`’, ACCxH is not modified.

Assuming that bit 16 is effectively random in nature, this scheme removes any rounding bias that may accumulate.

The `SAC` and `SAC.R` instructions store either a truncated (`SAC`), or rounded (`SAC.R`) version of the contents of the target accumulator to data memory via the X bus, subject to data saturation (see **Section 3.6.3.2 “Data Space Write Saturation”**). For the `MAC` class of instructions, the accumulator write-back operation functions in the same manner, addressing combined MCU (X and Y) data space though the X bus. For this class of instructions, the data is always subject to rounding.

3.6.3.2 Data Space Write Saturation

In addition to adder/subtracter saturation, writes to data space can also be saturated, but without affecting the contents of the source accumulator. The data space write saturation logic block accepts a 16-bit, 1.15 fractional value from the round logic block as its input, together with overflow status from the original source (accumulator) and the 16-bit round adder. These inputs are combined and used to select the appropriate 1.15 fractional value as output to write to data space memory.

If the SATDW bit in the CORCON register is set, data (after rounding or truncation) is tested for overflow and adjusted accordingly:

- For input data greater than 0x007FFF, data written to memory is forced to the maximum positive 1.15 value, 0x7FFF.
- For input data less than 0xFF8000, data written to memory is forced to the maximum negative 1.15 value, 0x8000.

The Most Significant bit of the source (bit 39) is used to determine the sign of the operand being tested.

If the SATDW bit in the CORCON register is not set, the input data is always passed through unmodified under all conditions.

3.6.4 BARREL SHIFTER

The barrel shifter can perform up to 16-bit arithmetic or logic right shifts, or up to 16-bit left shifts in a single cycle. The source can be either of the two DSP accumulators or the X bus (to support multi-bit shifts of register or memory data).

The shifter requires a signed binary value to determine both the magnitude (number of bits) and direction of the shift operation. A positive value shifts the operand right. A negative value shifts the operand left. A value of '0' does not modify the operand.

The barrel shifter is 40 bits wide, thereby obtaining a 40-bit result for DSP shift operations and a 16-bit result for MCU shift operations. Data from the X bus is presented to the barrel shifter between bit positions 16 and 31 for right shifts, and between bit positions 0 and 16 for left shifts.

NOTES:

 Preliminary

4.0 MEMORY ORGANIZATION

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33F Family Reference Manual*", **Section 4. "Program Memory"** (DS70202), which is available from the Microchip web site (www.microchip.com).

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 architecture features separate program and data memory spaces and buses. This architecture also allows the direct access to program memory from the data space during code execution.

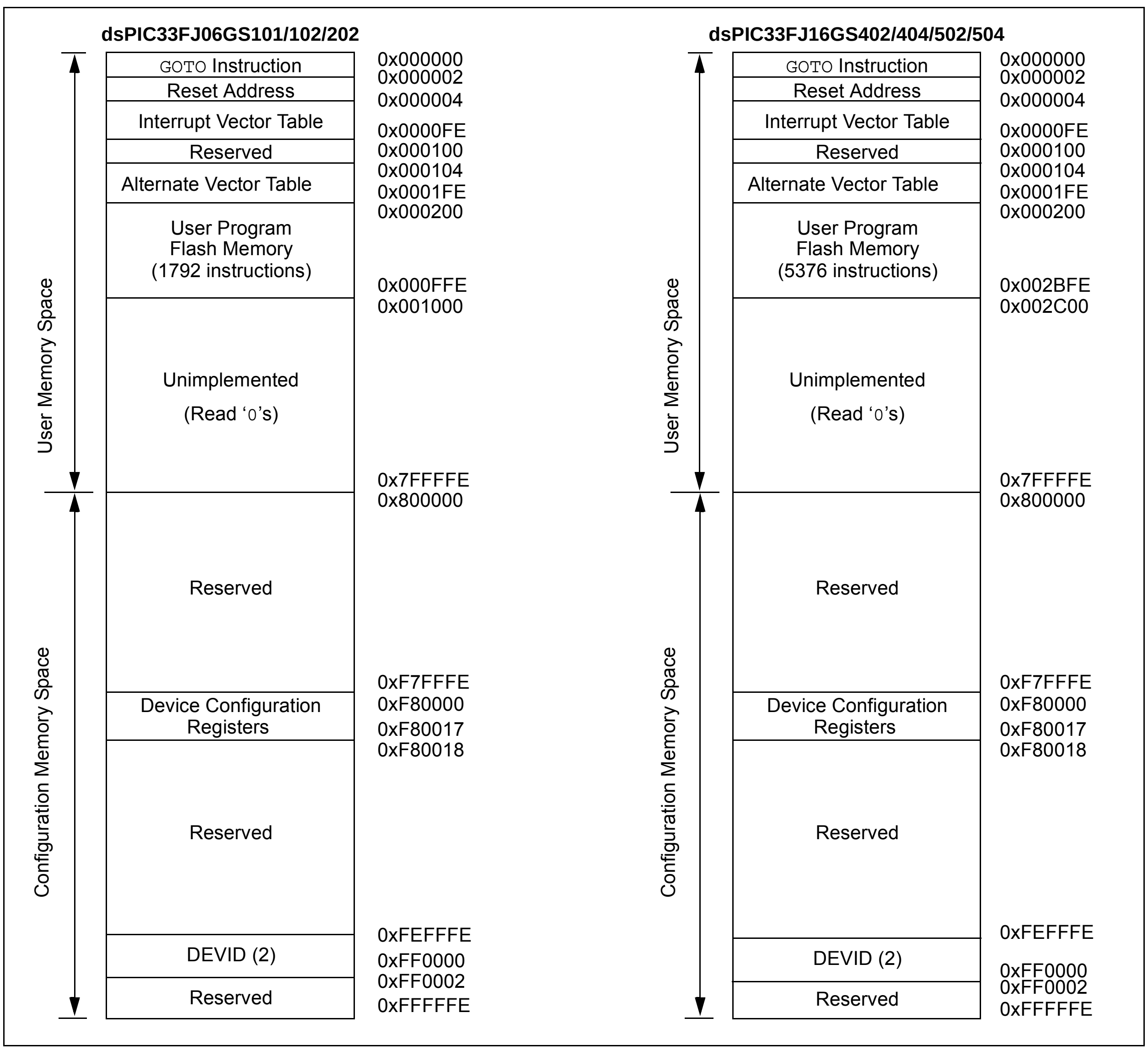
4.1 Program Address Space

The program address memory space of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit Program Counter (PC) during program execution, or from table operation or data space remapping as described in **Section 4.6 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

The memory maps for the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices are shown in Figure 4-1.

FIGURE 4-1: PROGRAM MEMORY MAPS FOR dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 DEVICES



4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (see Figure 4-2).

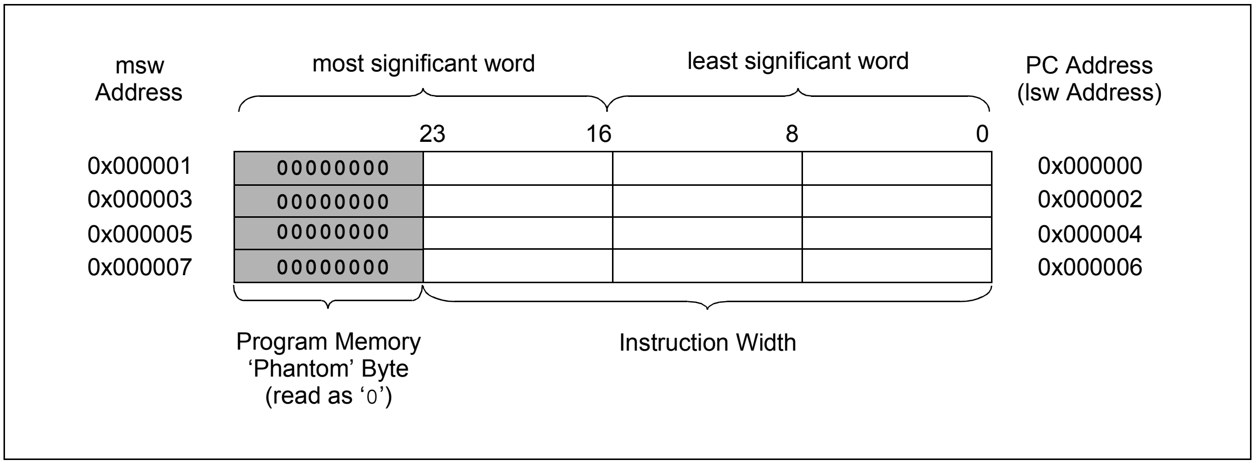
Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented by two during the code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices reserve the addresses between 0x00000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A `GOTO` instruction is programmed by the user application at 0x000000, with the actual address for the start of code at 0x000002.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices also have two interrupt vector tables, located from 0x000004 to 0x0000FF and 0x000100 to 0x0001FF. These vector tables allow each of the device interrupt sources to be handled by separate Interrupt Service Routines (ISRs). A more detailed discussion of the interrupt vector tables is provided in **Section 7.1 "Interrupt Vector Table"**.

FIGURE 4-2: PROGRAM MEMORY ORGANIZATION



4.2 Data Address Space

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CPU has a separate, 16-bit-wide data memory space. The data space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps is shown in Figure 4-3.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the data space. This arrangement gives a data space address range of 64 Kbytes or 32K words. The lower half of the data memory space (that is, when EA<15> = `0`) is used for implemented memory addresses, while the upper half (EA<15> = `1`) is reserved for the Program Space Visibility area (see **Section 4.6.3 "Reading Data From Program Memory Using Program Space Visibility"**).

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices implement up to 30 Kbytes of data memory. Should an EA point to a location outside of this area, an all-zero word or byte will be returned.

4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte addressable, 16-bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all data space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® MCU devices and improve data space memory usage efficiency, the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 instruction set supports both word and byte operations. As a consequence of byte accessibility, all effective address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] that results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word that contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the Least Significant Byte. The Most Significant Byte is not modified.

A sign-extend instruction (`SE`) is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a zero-extend (`ZE`) instruction on the appropriate address.

4.2.3 SFR SPACE

The first 2 Kbytes of the near data space, from 0x0000 to 0x07FF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control, and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '`0`'.

Note:	The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

4.2.4 NEAR DATA SPACE

The 8-Kbyte area between 0x0000 and 0x1FFF is referred to as the near data space. Locations in this space are directly addressable via a 13-bit absolute address field within all memory direct instructions. Additionally, the whole data space is addressable using `MOV` instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a working register as an Address Pointer.

FIGURE 4-3: DATA MEMORY MAP FOR dsPIC33FJ06GS101/102 DEVICES WITH 256 BYTES OF RAM

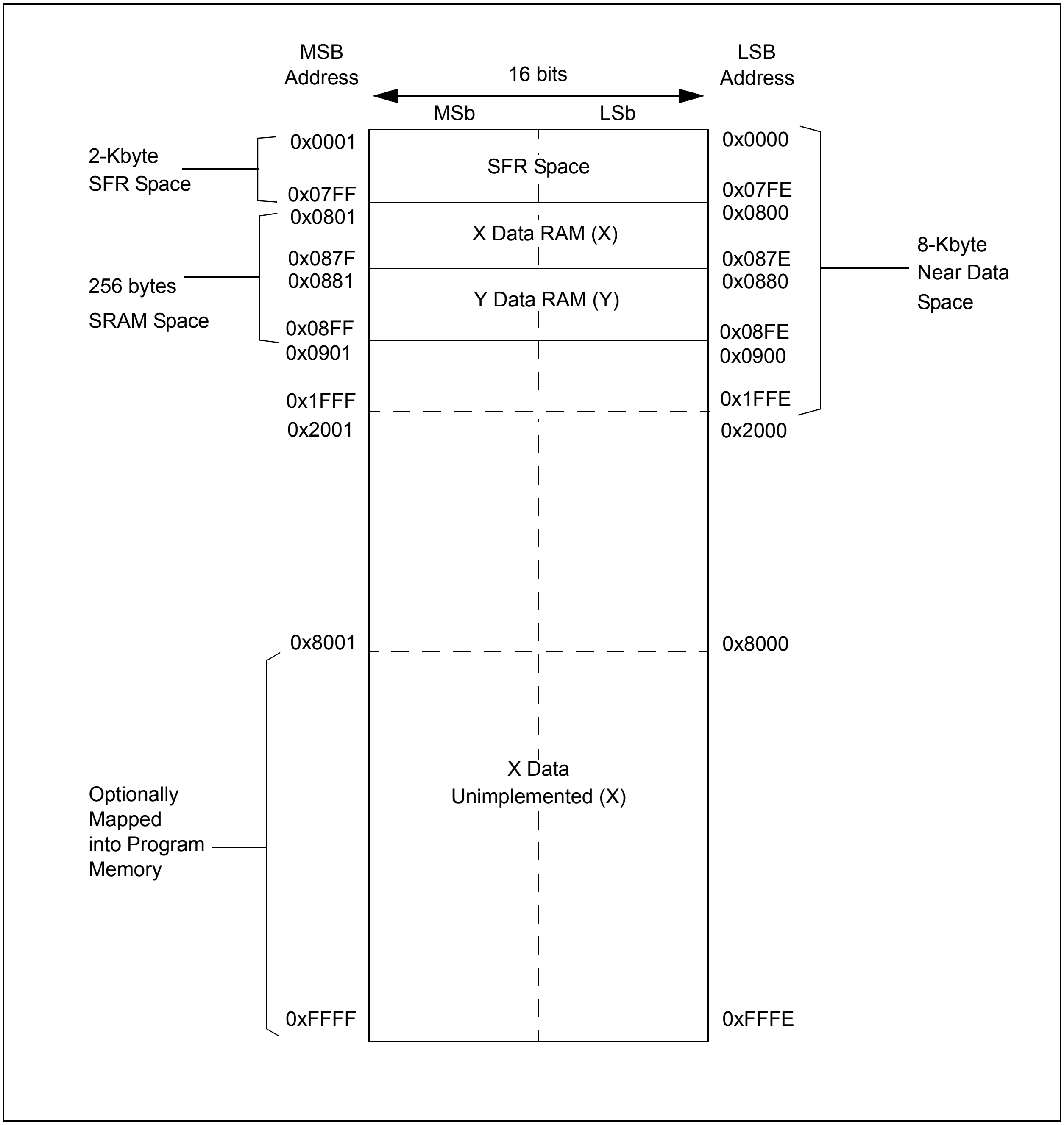


FIGURE 4-4: DATA MEMORY MAP FOR dsPIC33FJ06GS202 DEVICE WITH 1-Kbyte RAM

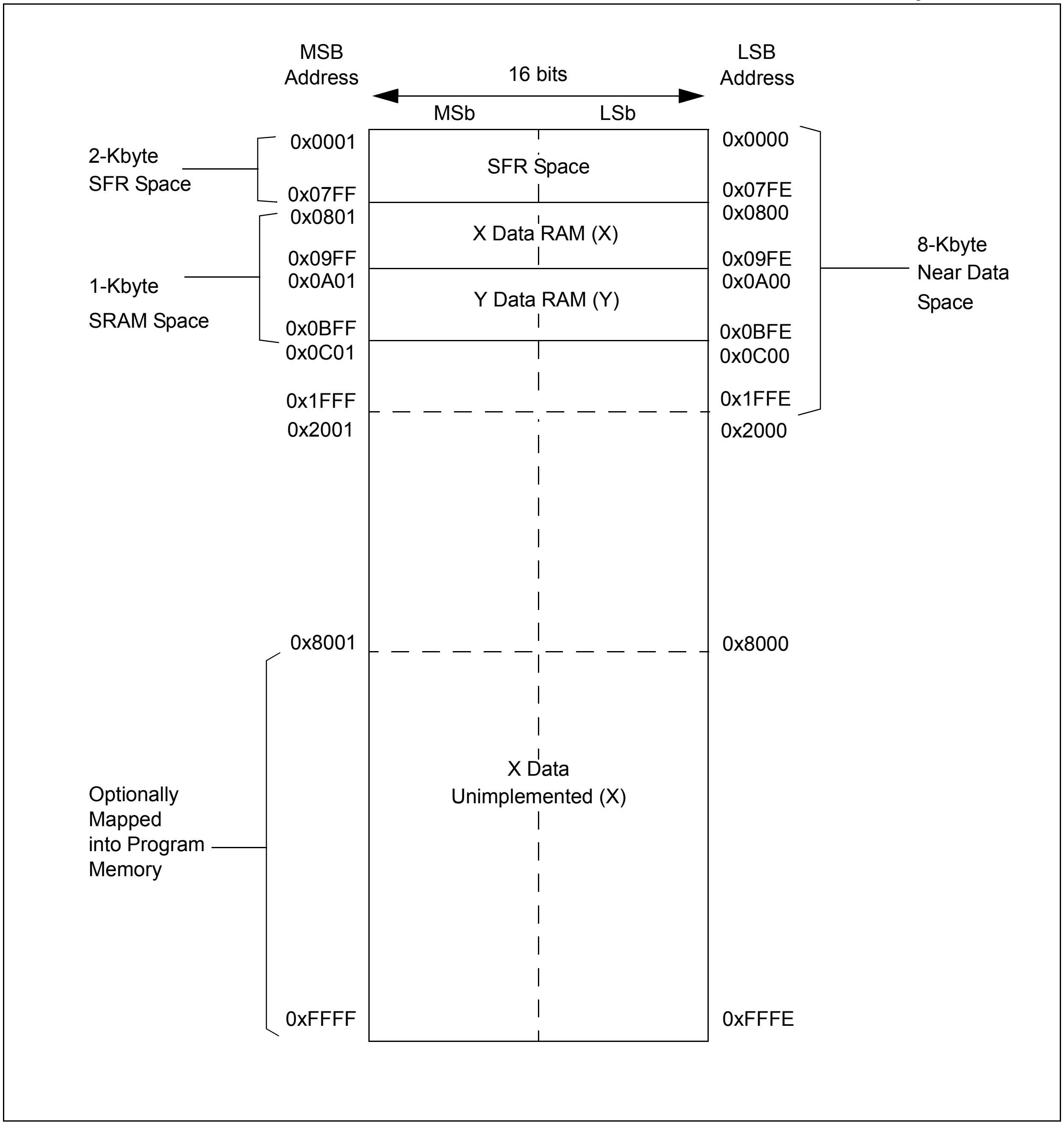
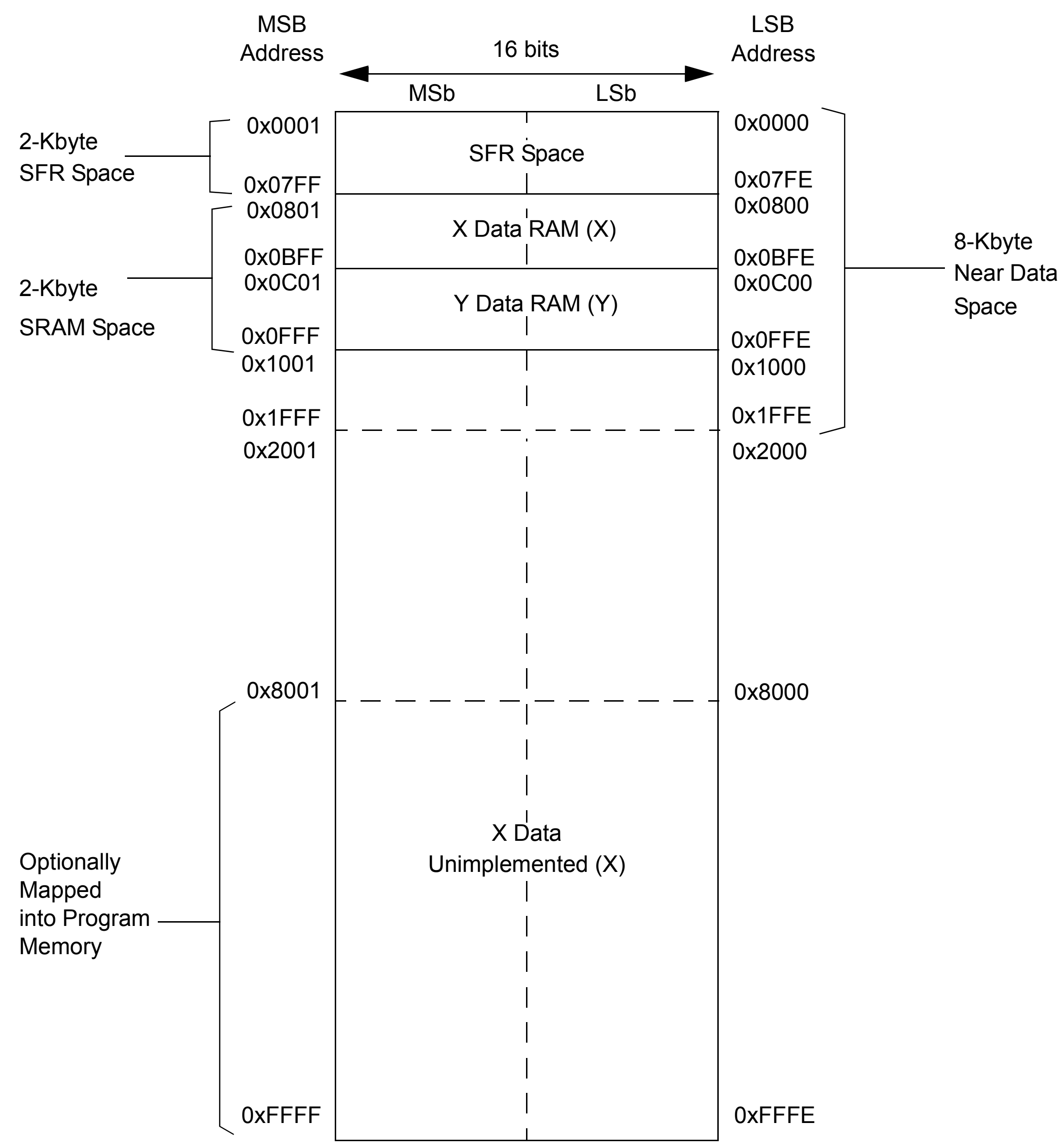


FIGURE 4-5: DATA MEMORY MAP FOR dsPIC33FJ16GS402/404/502/504 DEVICES WITH 2-Kbyte RAM



4.2.5 X AND Y DATA SPACES

The core has two data spaces, X and Y. These data spaces can be considered either separate (for some DSP instructions), or as one unified linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X data space is used by all instructions and supports all addressing modes. X data space has separate read and write data buses. The X read data bus is the read data path for all instructions that view data space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (`MAC` class).

The Y data space is used in concert with the X data space by the `MAC` class of instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MOVSAC`, `MPY`, `MPY.N` and `MSC`) to provide two concurrent data read paths.

Both the X and Y data spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X data space.

All data memory writes, including in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y data spaces is device-dependent and is not user-programmable.

All effective addresses are 16 bits wide and point to bytes within the data space. Therefore, the data space address range is 64 Kbytes, or 32K words, though the implemented memory locations vary by device.

TABLE 4-1: CPU CORE REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
WREG0	0000	Working Register 0																0000
WREG1	0002	Working Register 1																0000
WREG2	0004	Working Register 2																0000
WREG3	0006	Working Register 3																0000
WREG4	0008	Working Register 4																0000
WREG5	000A	Working Register 5																0000
WREG6	000C	Working Register 6																0000
WREG7	000E	Working Register 7																0000
WREG8	0010	Working Register 8																0000
WREG9	0012	Working Register 9																0000
WREG10	0014	Working Register 10																0000
WREG11	0016	Working Register 11																0000
WREG12	0018	Working Register 12																0000
WREG13	001A	Working Register 13																0000
WREG14	001C	Working Register 14																0000
WREG15	001E	Working Register 15																0800
SPLIM	0020	Stack Pointer Limit Register																xxxx
ACCAL	0022	ACCAL																xxxx
ACCAH	0024	ACCAH																xxxx
ACCAU	0026	ACCA<39>	ACCA<39>	ACCA<39>	ACCA<39>	ACCA<39>	ACCA<39>	ACCA<39>	ACCA<39>	ACCAU								xxxx
ACCBL	0028	ACCBL																xxxx
ACCBH	002A	ACCBH																xxxx
ACCBU	002C	ACCB<39>	ACCB<39>	ACCB<39>	ACCB<39>	ACCB<39>	ACCB<39>	ACCB<39>	ACCB<39>	ACCBU								xxxx
PCL	002E	Program Counter Low Word Register																0000
PCH	0030	—	—	—	—	—	—	—	—	Program Counter High Byte Register								0000
TBLPAG	0032	—	—	—	—	—	—	—	—	Table Page Address Pointer Register								0000
PSVPAG	0034	—	—	—	—	—	—	—	—	Program Memory Visibility Page Address Pointer Register								0000
RCOUNT	0036	Repeat Loop Counter Register																xxxx
DCOUNT	0038	DCOUNT<15:0>																xxxx
DOSTARTL	003A	DOSTARTL<15:1>															0	xxxx
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>						00xx
DOENDL	003E	DOENDL<15:1>															0	xxxx
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	DOENDH						00xx
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000
CORCON	0044	—	—	—	US	EDT	DL<2:0>			SATA	SATB	SATDW	ACCSAT	IPL3	PSV	RND	IF	0020
MODCON	0046	XMODEN	YMODEN	—	—	BWM<3:0>				YWM<3:0>				XWM<3:0>				0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-1: CPU CORE REGISTER MAP (CONTINUED)

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
XMODSRT	0048	XS<15:1>															0	xxxx
XMODEND	004A	XE<15:1>															1	xxxx
YMODSRT	004C	YS<15:1>															0	xxxx
YMODEND	004E	YE<15:1>															1	xxxx
XBREV	0050	BREN	XB<14:0>															xxxx
DISICNT	0052	—	—	Disable Interrupts Counter Register														xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-2: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJ06GS101

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	—	—	—	—	—	—	—	—	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNPU1	0068	—	—	—	—	—	—	—	—	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-3: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJ06GS102, dsPIC33FJ06GS202, dsPIC33FJ16GS402 AND dsPIC33FJ16GS502

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-4: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJ16GS404 AND dsPIC33FJ16GS504

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	—	CN29IE	CN28IE	CN27IE	CN26IE	CN25IE	CN24IE	CN23IE	CN22IE	CN21IE	CN20IE	CN19IE	CN18IE	CN17IE	CN16IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	—	CN29PUE	CN28PUE	CN27PUE	CN26PUE	CN25PUE	CN24PUE	CN23PUE	CN22PUE	CN21PUE	CN20PUE	CN19PUE	CN18PUE	CN17PUE	CN16PUE	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ06GS101 DEVICES ONLY

File Name	SFR Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	—	T2IF	—	—	—	T1IF	OC1IF	—	INT0IF	0000
IFS1	0086	—	—	INT2IF	—	—	—	—	—	—	—	—	INT1IF	CNIF	—	MI2C1IF	SI2C1IF	0000
IFS3	008A	—	—	—	—	—	—	PSEMIF	—	—	—	—	—	—	—	—	—	0000
IFS4	008C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIF	—	0000
IFS5	008E	—	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	0090	ADCP1IF	ADCP0IF	—	—	—	—	—	—	—	—	—	—	—	—	PWM4IF	—	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP3IF	—	0000
IEC0	0094	—	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	—	T2IE	—	—	—	T1IE	OC1IE	—	INT0IE	0000
IEC1	0096	—	—	INT2IE	—	—	—	—	—	—	—	—	INT1IE	CNIE	—	MI2C1IE	SI2C1IE	0000
IEC2	0098	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC3	009A	—	—	—	—	—	—	PSEMIE	—	—	—	—	—	—	—	—	—	0000
IEC4	009C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIE	—	0000
IEC5	009E	—	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	00A0	ADCP1IE	ADCP0IE	—	—	—	—	—	—	—	—	—	—	—	—	PWM4IE	—	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP3IE	—	0000
IPC0	00A4	—	T1IP<2:0>			—	OC1IP<2:0>			—	—	—	—	—	INT0IP<2:0>			4404
IPC1	00A6	—	T2IP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC2	00A8	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	—	—	—	4440
IPC3	00AA	—	—	—	—	—	—	—	—	—	ADIP<2:0>			—	U1TXIP<2:0>			0044
IPC4	00AC	—	CNIP<2:0>			—	—	—	—	—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4044
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC7	00B2	—	—	—	—	—	—	—	—	—	INT2IP<2:0>			—	—	—	—	0040
IPC14	00C0	—	—	—	—	—	—	—	—	—	PSEMIP<2:0>			—	—	—	—	0040
IPC16	00C4	—	—	—	—	—	—	—	—	—	U1EIP<2:0>			—	—	—	—	0400
IPC23	00D2	—	—	—	—	—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	0040
IPC24	00D4	—	—	—	—	—	—	—	—	—	PWM4IP<2:0>			—	—	—	—	4400
IPC27	00DA	—	ADCP1IP<2:0>			—	ADCP0IP<2:0>			—	—	—	—	—	—	—	—	0040
IPC28	00DC	—	—	—	—	—	—	—	—	—	ADCP3IP<2:0>			—	—	—	—	0000
INTTREG	00E0	—	—	—	—	ILR<3:0>				—	VECNUM<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ06GS102 DEVICES ONLY

File Name	SFR Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	—	T2IF	—	—	—	T1IF	OC1IF	—	INT0IF	0000
IFS1	0086	—	—	INT2IF	—	—	—	—	—	—	—	—	INT1IF	CNIF	—	MI2C1IF	SI2C1IF	0000
IFS3	008A	—	—	—	—	—	—	PSEMIF	—	—	—	—	—	—	—	—	—	0000
IFS4	008C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIF	—	0000
IFS5	008E	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	0090	ADCP1IF	ADCP0IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IF	0000
IEC0	0094	—	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	—	T2IE	—	—	—	T1IE	OC1IE	—	INT0IE	0000
IEC1	0096	—	—	INT2IE	—	—	—	—	—	—	—	—	INT1IE	CNIE	—	MI2C1IE	SI2C1IE	0000
IEC3	009A	—	—	—	—	—	—	PSEMIE	—	—	—	—	—	—	—	—	—	0000
IEC4	009C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIE	—	0000
IEC5	009E	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	00A0	ADCP1IE	ADCP0IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IE	0000
IPC0	00A4	—	T1IP<2:0>			—	OC1IP<2:0>			—	—	—	—	—	INT0IP<2:0>			4404
IPC1	00A6	—	T2IP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC2	00A8	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	—	—	—	4440
IPC3	00AA	—	—	—	—	—	—	—	—	—	ADIP<2:0>			—	U1TXIP<2:0>			0044
IPC4	00AC	—	CNIP<2:0>			—	—	—	—	—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4044
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC7	00B2	—	—	—	—	—	—	—	—	—	INT2IP<2:0>			—	—	—	—	0040
IPC14	00C0	—	—	—	—	—	—	—	—	—	PSEMIP<2:0>			—	—	—	—	0040
IPC16	00C4	—	—	—	—	—	—	—	—	—	U1EIP<2:0>			—	—	—	—	0040
IPC23	00D2	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC27	00DA	—	ADCP1IP<2:0>			—	ADCP0IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC28	00DC	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IP<2:0>			0004
INTTREG	00E0	—	—	—	—	ILR<3:0>				—	VECNUM<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ06G202 DEVICES ONLY

File Name	SFR Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	—	T2IF	—	—	—	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0086	—	—	INT2IF	—	—	—	—	—	—	—	—	INT1IF	CNIF	AC1IF	MI2C1IF	SI2C1IF	0000
IFS3	008A	—	—	—	—	—	—	PSEMIF	—	—	—	—	—	—	—	—	—	0000
IFS4	008C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIF	—	0000
IFS5	008E	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	0090	ADCP1IF	ADCP0IF	—	—	—	—	—	—	AC2IF	—	—	—	—	—	—	—	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	—	ADCP6IF	—	—	—	ADCP2IF	0000
IEC0	0094	—	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	—	T2IE	—	—	—	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	—	—	INT2IE	—	—	—	—	—	—	—	—	INT1IE	CNIE	AC1IE	MI2C1IE	SI2C1IE	0000
IEC3	009A	—	—	—	—	—	—	PSEMIE	—	—	—	—	—	—	—	—	—	0000
IEC4	009C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIE	—	0000
IEC5	009E	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	00A0	ADCP1IE	ADCP0IE	—	—	—	—	—	—	AC2IE	—	—	—	—	—	—	—	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	—	ADCP6IE	—	—	—	ADCP2IE	0000
IPC0	00A4	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	00A6	—	T2IP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC2	00A8	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	—	—	—	4440
IPC3	00AA	—	—	—	—	—	—	—	—	—	ADIP<2:0>			—	U1TXIP<2:0>			0044
IPC4	00AC	—	CNIP<2:0>			—	AC1IP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC7	00B2	—	—	—	—	—	—	—	—	—	INT2IP<2:0>			—	—	—	—	0040
IPC14	00C0	—	—	—	—	—	—	—	—	—	PSEMIP<2:0>			—	—	—	—	0040
IPC16	00C4	—	—	—	—	—	—	—	—	—	U1EIP<2:0>			—	—	—	—	0040
IPC23	00D2	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC25	00D6	—	AC2IP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC27	00DA	—	ADCP1IP<2:0>			—	ADCP0IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC28	00DC	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IP<2:0>			0004
IPC29	00DE	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP6IP<2:0>			0004
INTTREG	00E0	—	—	—	—	ILR<3:0>				—	VECNUM<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

 Preliminary

TABLE 4-8: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ16GS402/404 DEVICES ONLY

File Name	SFR Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	—	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0086	—	—	INT2IF	—	—	—	—	—	—	—	—	INT1IF	CNIF	—	MI2C1IF	SI2C1IF	0000
IFS3	008A	—	—	—	—	—	—	PSEMIF	—	—	—	—	—	—	—	—	—	0000
IFS4	008C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIF	—	0000
IFS5	008E	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	0090	ADCP1IF	ADCP0IF	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP3IF	ADCP2IF	0000
IEC0	0094	—	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	—	—	INT2IE	—	—	—	—	—	—	—	—	INT1IE	CNIE	—	MI2C1IE	SI2C1IE	0000
IEC3	009A	—	—	—	—	—	—	PSEMIE	—	—	—	—	—	—	—	—	—	0000
IEC4	009C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIE	—	0000
IEC5	009E	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	00A0	ADCP1IE	ADCP0IE	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IE	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP3IE	ADCP2IE	0000
IPC0	00A4	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	00A6	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	—	—	—	4440
IPC2	00A8	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	00AA	—	—	—	—	—	—	—	—	—	ADIP<2:0>			—	U1TXIP<2:0>			0044
IPC4	00AC	—	CNIP<2:0>			—	—	—	—	—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4044
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC7	00B2	—	—	—	—	—	—	—	—	—	INT2IP<2:0>			—	—	—	—	0040
IPC14	00C0	—	—	—	—	—	—	—	—	—	PSEMIP<2:0>			—	—	—	—	0040
IPC16	00C4	—	—	—	—	—	—	—	—	—	U1EIP<2:0>			—	—	—	—	0040
IPC23	00D2	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—			—	—	—	—	4400
IPC24	00D4	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IP<2:0>			0004
IPC27	00DA	—	ADCP1IP<2:0>			—	ADCP0IP<2:0>			—	—			—	—	—	—	4400
IPC28	00DC	—	—	—	—	—	—	—	—	—	ADCP3IP<2:0>			—	ADCP2IP<2:0>			0044
INTTREG	00E0	—	—	—	—	ILR<3:0>				—	VECNUM<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-9: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ16GS502 DEVICES ONLY

File Name	SFR Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	—	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0086	—	—	INT2IF	—	—	—	—	—	—	—	—	INT1IF	CNIF	AC1IF	MI2C1IF	SI2C1IF	0000
IFS3	008A	—	—	—	—	—	—	PSEMIF	—	—	—	—	—	—	—	—	—	0000
IFS4	008C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIF	—	0000
IFS5	008E	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	0090	ADCP1IF	ADCP0IF	—	—	—	—	AC4IF	AC3IF	AC2IF	—	—	—	—	—	PWM4IF	PWM3IF	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	—	ADCP6IF	—	—	ADCP3IF	ADCP2IF	0000
IEC0	0094	—	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	—	—	INT2IE	—	—	—	—	—	—	—	—	INT1IE	CNIE	AC1IE	MI2C1IE	SI2C1IE	0000
IEC3	009A	—	—	—	—	—	—	PSEMIE	—	—	—	—	—	—	—	—	—	0000
IEC4	009C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIE	—	0000
IEC5	009E	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	00A0	ADCP1IE	ADCP0IE	—	—	—	—	AC4IE	AC3IE	AC2IE	—	—	—	—	—	PWM4IE	PWM3IE	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	—	ADCP6IE	—	—	ADCP3IE	ADCP2IE	0000
IPC0	00A4	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	00A6	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	—	—	—	4440
IPC2	00A8	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	00AA	—	—	—	—	—	—			—	ADIP<2:0>			—	U1TXIP<2:0>			0044
IPC4	00AC	—	CNIP<2:0>			—	AC1IP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC7	00B2	—	—	—	—	—	—	—	—	—	INT2IP<2:0>			—	—	—	—	0040
IPC14	00C0	—	—	—	—	—	—	—	—	—	PSEMIP<2:0>			—	—	—	—	0040
IPC16	00C4	—	—	—	—	—	—	—	—	—	U1EIP<2:0>			—	—	—	—	0040
IPC23	00D2	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC24	00D4	—	—	—	—	—	—	—	—	—	PWM4IP<2:0>			—	PWM3IP<2:0>			0044
IPC25	00D6	—	AC2IP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC26	00D8	—	—	—	—	—	—	—	—	—	AC4IP<2:0>			—	AC3IP<2:0>			0044
IPC27	00DA	—	ADCP1IP<2:0>			—	ADCP0IP<2:0>			—	—			—	—	—	—	4400
IPC28	00DC	—	—	—	—	—	—	—	—	—	ADCP3IP<2:0>			—	ADCP2IP<2:0>			0044
IPC29	00DE	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP6IP<2:0>			0004
INTTREG	00E0	—	—	—	—	ILR<3:0>				—	VECNUM<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-10: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ16GS504 DEVICES ONLY

File Name	SFR Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	—	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0086	—	—	INT2IF	—	—	—	—	—	—	—	—	INT1IF	CNIF	AC1IF	MI2C1IF	SI2C1IF	0000
IFS3	008A	—	—	—	—	—	—	PSEMIF	—	—	—	—	—	—	—	—	—	0000
IFS4	008C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIF	—	0000
IFS5	008E	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	0090	ADCP1IF	ADCP0IF	—	—	—	—	AC4IF	AC3IF	AC2IF	—	—	—	—	—	PWM4IF	PWM3IF	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	—	ADCP6IF	ADCP5IF	ADCP4IF	ADCP3IF	ADCP2IF	0000
IEC0	0094	—	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	—	—	INT2IE	—	—	—	—	—	—	—	—	INT1IE	CNIE	AC1IE	MI2C1IE	SI2C1IE	0000
IEC3	009A	—	—	—	—	—	—	PSEMIE	—	—	—	—	—	—	—	—	—	0000
IEC4	009C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIE	—	0000
IEC5	009E	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	00A0	ADCP1IE	ADCP0IE	—	—	—	—	AC4IE	AC3IE	AC2IE	—	—	—	—	—	PWM4IE	PWM3IE	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	—	ADCP6IE	ADCP5IE	ADCP4IE	ADCP3IE	ADCP2IE	0000
IPC0	00A4	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	00A6	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	—	—	—	4440
IPC2	00A8	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	00AA	—	—	—	—	—	—	—	—	—	ADIP<2:0>			—	U1TXIP<2:0>			0044
IPC4	00AC	—	CNIP<2:0>			—	AC1IP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC7	00B2	—	—	—	—	—	—	—	—	—	INT2IP<2:0>			—	—	—	—	0040
IPC14	00C0	—	—	—	—	—	—	—	—	—	PSEMIP<2:0>			—	—	—	—	0040
IPC16	00C4	—	—	—	—	—	—	—	—	—	U1EIP<2:0>			—	—	—	—	0040
IPC23	00D2	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC24	00D4	—	—	—	—	—	—	—	—	—	PWM4IP<2:0>			—	PWM3IP<2:0>			0044
IPC25	00D6	—	AC2IP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC26	00D8	—	—	—	—	—	—	—	—	—	AC4IP<2:0>			—	AC3IP<2:0>			0440
IPC27	00DA	—	ADCP1IP<2:0>			—	ADCP0IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC28	00DC	—	ADCP5IP<2:0>			—	ADCP4IP<2:0>			—	ADCP3IP<2:0>			—	ADCP2IP<2:0>			4444
IPC29	00DE	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP6IP<2:0>			0004
INTTREG	00E0	—	—	—	—	ILR<3:0>				—	VECNUM<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-11: TIMER REGISTER MAP FOR dsPIC33FJ06GS101 AND dsPIC33FJ06GSX02

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																xxxx
PR1	0102	Period Register 1																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	TSYNC	TCS	—	0000
TMR2	0106	Timer2 Register																xxxx
PR2	010C	Period Register 2																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	—	TCS	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-12: TIMER REGISTER MAP FOR dsPIC33FJ16GSX02 AND dsPIC33FJ16GSX04

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																xxxx
PR1	0102	Period Register 1																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	TSYNC	TCS	—	0000
TMR2	0106	Timer2 Register																xxxx
TMR3HLD	0108	Timer3 Holding Register (for 32-bit timer operations only)																xxxx
TMR3	010A	Timer3 Register																xxxx
PR2	010C	Period Register 2																FFFF
PR3	010E	Period Register 3																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		T32	—	TCS	—	0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	—	TCS	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-13: INPUT CAPTURE REGISTER MAP FOR dsPIC33FJ06GS202

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1BUF	0140	Input Capture 1 Register																xxxx
IC1CON	0142	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-14: INPUT CAPTURE REGISTER MAP FOR dsPIC33FJ16GSX02 AND dsPIC33FJ16GSX04

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1BUF	0140	Input Capture 1 Register																xxxx
IC1CON	0142	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC2BUF	0144	Input Capture 2 Register																xxxx
IC2CON	0146	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-15: OUTPUT COMPARE REGISTER MAP dsPIC33FJ06GS101 AND dsPIC33FJ06GSX02

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1RS	0180	Output Compare 1 Secondary Register																xxxx
OC1R	0182	Output Compare 1 Register																xxxx
OC1CON	0184	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-16: OUTPUT COMPARE REGISTER MAP dsPIC33FJ16GSX02 AND dsPIC33FJ06GSX04

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1RS	0180	Output Compare 1 Secondary Register																xxxx
OC1R	0182	Output Compare 1 Register																xxxx
OC1CON	0184	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000
OC2RS	0186	Output Compare 2 Secondary Register																xxxx
OC2R	0188	Output Compare 2 Register																xxxxx
OC2CON	018A	—	—	OCSIDL	—	—	—	—	—	—	—	—	OCFLT	OCTSEL	OCM<2:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-17: HIGH-SPEED PWM REGISTER MAP

File Name	Addr Offset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0400	PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	—	SYNCSRC<1:0>		SEVTPS<3:0>				0000
PTCON2	0402	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
PTPER	0404	PTPER<15:0>																FFF8
SEVTCMP	0406	SEVTCMP<15:3>													—	—	—	0000
MDC	040A	MDC<15:0>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-18: HIGH-SPEED PWM GENERATOR 1 REGISTER MAP

File Name	Addr Offset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0420	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<1:0>		—	—	—	CAM	XPRES	IUE	0000
IOCON1	0422	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
FCLCON1	0424	IFLTMOD	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>		0000
PDC1	0426	PDC1<15:0>																0000
PHASE1	0428	PHASE1<15:0>																0000
DTR1	042A	—	—	DTR1<13:0>														0000
ALTDTR1	042C	—	—	ALTDTR1<13:0>														0000
SDC1	042E	SDC1<15:0>																0000
SPHASE1	0430	SPHASE1<15:0>																0000
TRIG1	0432	TRGCMP<15:3>													—	—	—	0000
TRGCON1	0434	TRGDIV<3:0>				—	—	—	—	DTM	—	TRGSTRT<5:0>						0000
STRIG1	0436	STRGCMP<15:3>													—	—	—	0000
PWMCAP1	0438	PWMCAP1<15:3>													—	—	—	0000
LEBCON1	043A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	LEB<9:3>							—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-19: HIGH-SPEED PWM GENERATOR 2 REGISTER MAP FOR dsPIC33FJ06GS102/202 AND dsPIC33FJ16GSX02/X04 DEVICES ONLY

File Name	Addr Offset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON2	0440	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<1:0>		—	—	—	CAM	XPRES	IUE	0000
IOCON2	0442	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
FCLCON2	0444	IFLTMOD	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>		0000
PDC2	0446	PDC2<15:0>																0000
PHASE2	0448	PHASE2<15:0>																0000
DTR2	044A	—	—	DTR2<13:0>														0000
ALTDTR2	044C	—	—	ALTDTR2<13:0>														0000
SDC2	044E	SDC2<15:0>																0000
SPHASE2	0450	SPHASE2<15:0>																0000
TRIG2	0452	TRGCMP<15:3>													—	—	—	0000
TRGCON2	0454	TRGDIV<3:0>				—	—	—	—	DTM	—	TRGSTRT<5:0>						0000
STRIG2	0456	STRGCMP<15:3>													—	—	—	0000
PWMCAP2	0458	PWMCAP2<15:3>													—	—	—	0000
LEBCON2	045A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	LEB<9:3>							—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-20: HIGH-SPEED PWM GENERATOR 3 REGISTER MAP FOR dsPIC33FJ16GSX02/X04 DEVICES ONLY

File Name	Addr Offset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON3	0460	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<1:0>		—	—	—	CAM	XPRES	IUE	0000
IOCON3	0462	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
FCLCON3	0464	IFLTMOD	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>		0000
PDC3	0466	PDC3<15:0>																0000
PHASE3	0468	PHASE3<15:0>																0000
DTR3	046C	—	—	DTR3<13:0>														0000
ALTDTR3	046C	—	—	ALTDTR3<13:0>														0000
SDC3	046E	SDC3<15:0>																0000
SPHASE3	0470	SPHASE3<15:0>																0000
TRIG3	0472	TRGCMP<15:3>													—	—	—	0000
TRGCON3	0474	TRGDIV<3:0>				—	—	—	—	DTM	—	TRGSTRT<5:0>						0000
STRIG3	0476	STRGCMP<15:3>													—	—	—	0000
PWMCAP3	0478	PWMCAP3<15:3>													—	—	—	0000
LEBCON3	047A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	LEB<9:3>							—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-21: HIGH-SPEED PWM GENERATOR 4 REGISTER MAP FOR dsPIC33FJ06GS101 AND dsPIC33FJ16GS50X DEVICES ONLY

File Name	Addr Offset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON4	0480	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<1:0>		—	—	—	CAM	XPRES	IUE	0000
IOCON4	0482	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
FCLCON4	0484	IFLTMOD	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>		0000
PDC4	0486	PDC4<15:0>																0000
PHASE4	0488	PHASE4<15:0>																0000
DTR4	048A	—	—	DTR4<13:0>														0000
ALTDTR4	048A	—	—	ALTDTR4<13:0>														0000
SDC4	048E	SDC4<15:0>																0000
SPHASE4	0490	SPHASE4<15:0>																0000
TRIG4	0492	TRGCMP<15:3>													—	—	—	0000
TRGCON4	0494	TRGDIV<3:0>				—	—	—	—	DTM	—	TRGSTRT<5:0>						0000
STRIG4	0496	STRGCMP<15:3>													—	—	—	0000
PWMCAP4	0498	PWMCAP4<15:3>													—	—	—	0000
LEBCON4	049A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	LEB<9:3>							—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: I2C1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	—	—	—	—	—	Receive Register								0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	Transmit Register								00FF
I2C1BRG	0204	—	—	—	—	—	—	—	Baud Rate Generator Register									0000
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	—	—	—	—	—	Address Register										0000
I2C1MSK	020C	—	—	—	—	—	—	AMSK<9:0>										0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-23: UART1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: SPI1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	—	—	—	—	SPIROV	—	—	—	—	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE<2:0>			PPRE<1:0>		0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	—	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-25: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ06GS101 DEVICES ONLY

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADCON	0300	ADON	—	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS<2:0>			0003
ADPCFG	0302	—	—	—	—	—	—	—	—	PCFG7	PCFG6	—	—	PCFG3	PCFG2	PCFG1	PCFG0	0000
ADSTAT	0306	—	—	—	—	—	—	—	—	—	—	—	—	P3RDY	—	P1RDY	P0RDY	0000
ADBASE	0308	ADBASE<15:1>															—	0000
ADCPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC1<4:0>					IRQEN0	PEND0	SWTRG0	TRGSRC0<4:0>					0000
ADCPC1	030C	IRQEN3	PEND3	SWTRG3	TRGSRC3<4:0>					—	—	—	—	—	—	—	—	0000
ADCBUF0	0320	ADC Data Buffer 0																xxxx
ADCBUF1	0322	ADC Data Buffer 1																xxxx
ADCBUF2	0324	ADC Data Buffer 2																xxxx
ADCBUF3	0326	ADC Data Buffer 3																xxxx
ADCBUF6	032C	ADC Data Buffer 6																xxxx
ADCBUF7	032E	ADC Data Buffer 7																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ06GS102 DEVICES ONLY

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADCON	0300	ADON	—	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS<2:0>			0003
ADPCFG	0302	—	—	—	—	—	—	—	—	—	—	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
ADSTAT	0306	—	—	—	—	—	—	—	—	—	—	—	—	—	P2RDY	P1RDY	P0RDY	0000
ADBASE	0308	ADBASE<15:1>															—	0000
ADCPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC1<4:0>					IRQEN0	PEND0	SWTRG0	TRGSRC0<4:0>					0000
ADCPC1	030C	—	—	—	—	—	—	—	—	IRQEN2	PEND2	SWTRG2	TRGSRC2<4:0>					0000
ADCBUF0	0320	ADC Data Buffer 0																xxxx
ADCBUF1	0322	ADC Data Buffer 1																xxxx
ADCBUF2	0324	ADC Data Buffer 2																xxxx
ADCBUF3	0326	ADC Data Buffer 3																xxxx
ADCBUF4	0328	ADC Data Buffer 4																xxxx
ADCBUF5	032A	ADC Data Buffer 5																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-27: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ06GS202 DEVICES ONLY

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADCON	0300	ADON	—	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS<2:0>			0003
ADPCFG	0302	—	—	—	—	—	—	—	—	—	—	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
ADSTAT	0306	—	—	—	—	—	—	—	—	—	P6RDY	—	—	—	P2RDY	P1RDY	P0RDY	0000
ADBASE	0308	ADBASE<15:1>															—	0000
ADCPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC1<4:0>					IRQEN0	PEND0	SWTRG0	TRGSRC0<4:0>					0000
ADCPC1	030C	—	—	—	—	—	—	—	—	IRQEN2	PEND2	SWTRG2	TRGSRC2<4:0>					0000
ADCPC3	0310	—	—	—	—	—	—	—	—	IRQEN6	PEND6	SWTRG6	TRGSRC6<4:0>					0000
ADCBUF0	0320	ADC Data Buffer 0																xxxx
ADCBUF1	0322	ADC Data Buffer 1																xxxx
ADCBUF2	0324	ADC Data Buffer 2																xxxx
ADCBUF3	0326	ADC Data Buffer 3																xxxx
ADCBUF4	0328	ADC Data Buffer 4																xxxx
ADCBUF5	032A	ADC Data Buffer 5																xxxx
ADCBUF12	0338	ADC Data Buffer 12																xxxx
ADCBUF13	033A	ADC Data Buffer13																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-28: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ16GS402/404 DEVICES ONLY

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADCON	0300	ADON	—	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS<2:0>			0003
ADPCFG	0302	—	—	—	—	—	—	—	—	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
ADSTAT	0306	—	—	—	—	—	—	—	—	—	—	—	—	P3RDY	P2RDY	P1RDY	P0RDY	0000
ADBASE	0308	ADBASE<15:1>															—	0000
ADCPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC1<4:0>					IRQEN0	PEND0	SWTRG0	TRGSRC0<4:0>					0000
ADCPC1	030C	IRQEN3	PEND3	SWTRG3	TRGSRC3<4:0>					IRQEN2	PEND2	SWTRG2	TRGSRC2<4:0>					0000
ADCBUF0	0320	ADC Data Buffer 0																xxxx
ADCBUF1	0322	ADC Data Buffer 1																xxxx
ADCBUF2	0324	ADC Data Buffer 2																xxxx
ADCBUF3	0326	ADC Data Buffer 3																xxxx
ADCBUF4	0328	ADC Data Buffer 4																xxxx
ADCBUF5	032A	ADC Data Buffer 5																xxxx
ADCBUF6	032C	ADC Data Buffer 6																xxxx
ADCBUF7	032E	ADC Data Buffer 7																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-29: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ16GS502 DEVICES ONLY

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADCON	0300	ADON	—	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS<2:0>			0003
ADPCFG	0302	—	—	—	—	—	—	—	—	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
ADSTAT	0306	—	—	—	—	—	—	—	—	—	P6RDY	—	—	P3RDY	P2RDY	P1RDY	P0RDY	0000
ADBASE	0308	ADBASE<15:1>															—	0000
ADCPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC1<4:0>					IRQEN0	PEND0	SWTRG0	TRGSRC0<4:0>					0000
ADCPC1	030C	IRQEN3	PEND3	SWTRG3	TRGSRC3<4:0>					IRQEN2	PEND2	SWTRG2	TRGSRC2<4:0>					0000
ADCPC3	0310	—	—	—	—	—	—	—	—	IRQEN6	PEND6	SWTRG6	TRGSRC6<4:0>					0000
ADCBUF0	0320	ADC Data Buffer 0																xxxx
ADCBUF1	0322	ADC Data Buffer 1																xxxx
ADCBUF2	0324	ADC Data Buffer 2																xxxx
ADCBUF3	0326	ADC Data Buffer 3																xxxx
ADCBUF4	0328	ADC Data Buffer 4																xxxx
ADCBUF5	032A	ADC Data Buffer 5																xxxx
ADCBUF6	032C	ADC Data Buffer 6																xxxx
ADCBUF7	032E	ADC Data Buffer 7																xxxx
ADCBUF12	0338	ADC Data Buffer 12																xxxx
ADCBUF13	033A	ADC Data Buffer 13																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-30: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ16GS504 DEVICES ONLY

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADCON	0300	ADON	—	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS<2:0>			0003
ADPCFG	0302	—	—	—	—	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
ADSTAT	0306	—	—	—	—	—	—	—	—	—	P6RDY	P5RDY	P4RDY	P3RDY	P2RDY	P1RDY	P0RDY	0000
ADBASE	0308	ADBASE<15:1>															—	0000
ADCPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC1<4:0>					IRQEN0	PEND0	SWTRG0	TRGSRC0<4:0>					0000
ADCPC1	030C	IRQEN3	PEND3	SWTRG3	TRGSRC3<4:0>					IRQEN2	PEND2	SWTRG2	TRGSRC2<4:0>					0000
ADCPC2	030E	IRQEN5	PEND5	SWTRG5	TRGSRC5<4:0>					IRQEN4	PEND4	SWTRG4	TRGSRC4<4:0>					0000
ADCPC3	0310	—	—	—	—	—	—	—	—	IRQEN6	PEND6	SWTRG6	TRGSRC6<4:0>					0000
ADCBUF0	0320	ADC Data Buffer 0																xxxx
ADCBUF1	0322	ADC Data Buffer 1																xxxx
ADCBUF2	0324	ADC Data Buffer 2																xxxx
ADCBUF3	0326	ADC Data Buffer 3																xxxx
ADCBUF4	0328	ADC Data Buffer 4																xxxx
ADCBUF5	032A	ADC Data Buffer 5																xxxx
ADCBUF6	032C	ADC Data Buffer 6																xxxx
ADCBUF7	032E	ADC Data Buffer 7																xxxx
ADCBUF8	0330	ADC Data Buffer 8																xxxx
ADCBUF9	0332	ADC Data Buffer 9																xxxx
ADCBUF10	0334	ADC Data Buffer 10																xxxx
ADCBUF11	0336	ADC Data Buffer 11																xxxx
ADCBUF12	0338	ADC Data Buffer 12																xxxx
ADCBUF13	033A	ADC Data Buffer 13																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-31: ANALOG COMPARATOR CONTROL REGISTER MAP FOR dsPIC33FJ06GS202 DEVICES ONLY

File Name	ADR	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMPCON1	0540	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL<1:0>		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC1	0542	—	—	—	—	—	—	CMREF<9:0>										0000
CMPCON2	0544	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL<1:0>		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC2	0546	—	—	—	—	—	—	CMREF<9:0>										0000

TABLE 4-32: ANALOG COMPARATOR CONTROL REGISTER MAP dsPIC33FJ16GS502/504 DEVICES ONLY

File Name	ADR	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMPCON1	0540	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL<1:0>		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC1	0542	—	—	-	—	—	—	CMREF<9:0>										0000
CMPCON2	0544	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL<1:0>		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC2	0546	—	—	-	—	—	—	CMREF<9:0>										0000
CMPCON3	0548	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL<1:0>		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC3	054A	—	—	-	—	—	—	CMREF<9:0>										0000
CMPCON4	054C	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL<1:0>		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC4	054E	—	—	—	—	—	—	CMREF<9:0>										0000

TABLE 4-33: PERIPHERAL PIN SELECT INPUT REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	0680	—	—	INT1R<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR1	0682	—	—	—	—	—	—	—	—	—	—	INT2R<5:0>						003F
RPINR2	0684	—	—	T1CKR<5:0>						—	—	—	—	—	—	—	—	0000
RPINR3	0686	—	—	T3CKR<5:0>						—	—	T2CKR<5:0>						3F3F
RPINR7	068E	—	—	IC2R<5:0>						—	—	IC1R<5:0>						3F3F
RPINR11	0696	—	—	—	—	—	—	—	—	—	—	OCFAR<5:0>						3F3F
RPINR18	06A4	—	—	U1CTSR<5:0>						—	—	U1RXR<5:0>						003F
RPINR20	06A8	—	—	SCK1R<5:0>						—	—	SDI1R<5:0>						3F3F
RPINR21	06AA	—	—	—	—	—	—	—	—	—	—	SS1R<5:0>						0000
RPINR29	06BA	—	—	FLT1R<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR30	06BC	—	—	FLT3R<5:0>						—	—	FLT2R<5:0>						3F3F
RPINR31	06BE	—	—	FLT5R<5:0>						—	—	FLT4R<5:0>						3F3F
RPINR32	06C0	—	—	FLT7R<5:0>						—	—	FLT6R<5:0>						3F3F
RPINR33	06C2	—	—	SYNCI1R<5:0>						—	—	FLT8R<5:0>						3F3F
RPINR34	06C4	—	—	—	—	—	—	—	—	—	—	SYNCI2R<5:0>						3F3F

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-34: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33FJ06GS101

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	06D0	—	—	RP1R<5:0>						—	—	RP0R<5:0>						0000
RPOR1	06D2	—	—	RP3R<5:0>						—	—	RP2R<5:0>						0000
RPOR2	06D4	—	—	RP5R<5:0>						—	—	RP4R<5:0>						0000
RPOR3	06D6	—	—	RP7R<5:0>						—	—	RP6R<5:0>						0000
RPOR16	06F0	—	—	RP33<5:0>						—	—	RP32<5:0>						0000
RPOR17	06F2	—	—	RP35<5:0>						—	—	RP34<5:0>						0000

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-35: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33FJ06GS102, dsPIC33FJ06GS202, dsPIC33FJ16GS402 AND dsPIC33FJ16GS502

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	06D0	—	—	RP1R<5:0>						—	—	RP0R<5:0>						0000
RPOR1	06D2	—	—	RP3R<5:0>						—	—	RP2R<5:0>						0000
RPOR2	06D4	—	—	RP5R<5:0>						—	—	RP4R<5:0>						0000
RPOR3	06D6	—	—	RP7R<5:0>						—	—	RP6R<5:0>						0000
RPOR4	06D8	—	—	RP9R<5:0>						—	—	RP8R<5:0>						0000
RPOR5	06DA	—	—	RP11R<5:0>						—	—	RP10R<5:0>						0000
RPOR6	06DC	—	—	RP13R<5:0>						—	—	RP12R<5:0>						0000
RPOR7	06DE	—	—	RP15R<5:0>						—	—	RP14R<5:0>						0000
RPOR16	06F0	—	—	RP33<5:0>						—	—	RP32<5:0>						0000
RPOR17	06F2	—	—	RP35<5:0>						—	—	RP34<5:0>						0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-36: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33FJ16GS404 AND dsPIC33FJ16GS504

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	06D0	—	—	RP1R<5:0>						—	—	RP0R<5:0>						0000
RPOR1	06D2	—	—	RP3R<5:0>						—	—	RP2R<5:0>						0000
RPOR2	06D4	—	—	RP5R<5:0>						—	—	RP4R<5:0>						0000
RPOR3	06D6	—	—	RP7R<5:0>						—	—	RP6R<5:0>						0000
RPOR4	06D8	—	—	RP9R<5:0>						—	—	RP8R<5:0>						0000
RPOR5	06DA	—	—	RP11R<5:0>						—	—	RP10R<5:0>						0000
RPOR6	06DC	—	—	RP13R<5:0>						—	—	RP12R<5:0>						0000
RPOR7	06DE	—	—	RP15R<5:0>						—	—	RP14R<5:0>						0000
RPOR8	06E0	—	—	RP17R<5:0>						—	—	RP16R<5:0>						0000
RPOR9	06E2	—	—	RP19R<5:0>						—	—	RP18R<5:0>						0000
RPOR10	06E4	—	—	RP21R<5:0>						—	—	RP20R<5:0>						0000
RPOR11	06E6	—	—	RP23R<5:0>						—	—	RP22R<5:0>						0000
RPOR12	06E8	—	—	RP25R<5:0>						—	—	RP24R<5:0>						0000
RPOR13	06EA	—	—	RP27R<5:0>						—	—	RP26R<5:0>						0000
RPOR14	06EC	—	—	RP29R<5:0>						—	—	RP28R<5:0>						0000
RPOR16	06F0	—	—	RP33<5:0>						—	—	RP32<5:0>						0000
RPOR17	06F2	—	—	RP35<5:0>						—	—	RP34<5:0>						0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-37: PORTA REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	02C0	—	—	—	—	—	—	—	—	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	001F
PORTA	02C2	—	—	—	—	—	—	—	—	—	—	—	RA4	RA3	RA2	RA1	RA0	xxxx
LATA	02C4	—	—	—	—	—	—	—	—	—	—	—	LATA4	LATA3	LATA2	LATA1	LATA0	0000
ODCA	02C6	—	—	—	—	—	—	—	—	—	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-38: PORTB REGISTER MAP FOR dsPIC33FJ06GS101

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	—	—	—	—	—	—	—	—	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	00FF
PORTB	02CA	—	—	—	—	—	—	—	—	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	02CC	—	—	—	—	—	—	—	—	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	0000
ODCB	02CE	—	—	—	—	—	—	—	—	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-39: PORTB REGISTER MAP FOR dsPIC33FJ06GS102, dsPIC33FJ06GS202, dsPIC33FJ16GS402, dsPIC33FJ16GS404, dsPIC33FJ16GS502 AND dsPIC33FJ16GS504

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	02CA	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	02CC	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	0000
ODCB	02CE	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-40: PORTC REGISTER MAP FOR dsPIC33FJ16GS404 AND dsPIC33FJ16GS504

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	02D0	—	—	TRISC13	TRISC12	TRISC11	TRISC10	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	3FFF
PORTC	02D2	—	—	RC13	RC12	RC11	RC10	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	02D4	—	—	LATC13	LATC12	LATC11	LATC10	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	0000
ODCC	02D6	—	—	ODCC13	ODCC12	ODCC11	ODCC10	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-41: SYSTEM CONTROL REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	—	—	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	xxxx(1)
OSCCON	0742	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	IOLOCK	LOCK	—	CF	—	—	OSWEN	0300(2)
CLKDIV	0744	ROI	DOZE<2:0>			DOZEN	FRCDIV<2:0>			PLLPOST<1:0>		—	PLLPRE<4:0>					3040
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV<8:0>									0030
REFOCON	074E	ROON	—	ROSIDL	ROSEL	RODIV<3:0>				—	—	—	—	—	—	—	—	0000
OSCTUN	0748											TUN<5:0>						0000
ACLKCON	0750	ENAPLL	APLLCK	SELACLK	—	—	APSTSCLR<2:0>			ASRCSEL	FRCSEL	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The RCON register Reset values are dependent on type of Reset.

2: The OSCCON register Reset values are dependent on the FOSC Configuration bits and on type of Reset.

TABLE 4-42: NVM REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0760	WR	WREN	WRERR	—	—	—	—	—	—	ERASE	—	—	NVMOP<3:0>				0000(1)
NVMKEY	0766	—	—	—	—	—	—	—	—	NVMKEY<7:0>								0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset value shown is for POR only. Value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

TABLE 4-43: PMD REGISTER MAP FOR dsPIC33FJ06GS101 DEVICES ONLY

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	—	—	—	T2MD	T1MD	—	PWMMD	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	—	—	IC2MD	IC1MD	—	—	—	—	—	—	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	—	—	PWM4MD	—	—	PWM1MD	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-44: PMD REGISTER MAP FOR dsPIC33FJ06GS102 DEVICES ONLY

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	—	—	—	T2MD	T1MD	—	PWMMD	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	—	—	IC2MD	IC1MD	—	—	—	—	—	—	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	—	—	—	—	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-45: PMD REGISTER MAP FOR dsPIC33FJ06GS202 DEVICES ONLY

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	—	—	—	T2MD	T1MD	—	PWMMD	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	—	—	—	IC1MD	—	—	—	—	—	—	—	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	—	—	—	—	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	077C	—	—	—	—	—	—	CMP2MD	CMP1MD	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-46: PMD REGISTER MAP FOR dsPIC33FJ16GS402 AND dsPIC33FJ16GS404 DEVICES ONLY

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	—	—	T3MD	T2MD	T1MD	—	PWMMD	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	—	—	IC2MD	IC1MD	—	—	—	—	—	—	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	—	—	—	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	077C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-47: PMD REGISTER MAP FOR dsPIC33FJ16GS502 AND dsPIC33FJ16GS504 DEVICES ONLY

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	—	—	T3MD	T2MD	T1MD	—	PWMMD	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	—	—	IC2MD	IC1MD	—	—	—	—	—	—	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	—	—	PWM4MD	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	077C	—	—	—	—	CMP4MD	CMP3MD	CMP2MD	CMP1MD	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.2.6 SOFTWARE STACK

In addition to its use as a working register, the W15 register in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices is also used as a software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It predecrements for stack pops and post-increments for stack pushes, as shown in Figure 4-6. For a PC push during any `CALL` instruction, the MSb of the PC is zero-extended before the push, ensuring that the MSb is always clear.

Note:	A PC push during exception processing concatenates the SRL register to the MSb of the PC prior to the push.

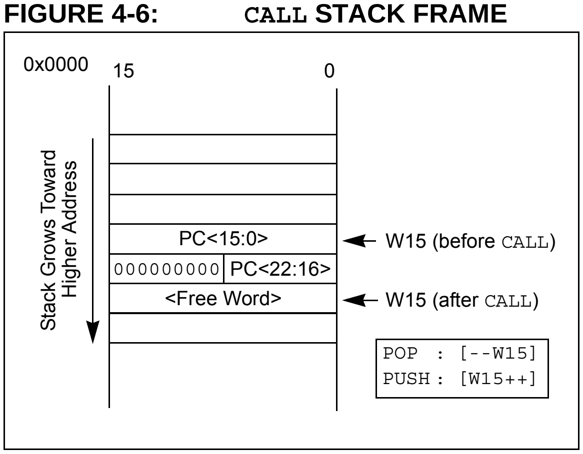
The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to ‘`0`’ because all stack operations must be word-aligned.

Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation. For example, to cause a stack error trap when the stack grows beyond address 0x1000 in RAM, initialize the SPLIM with the value 0x0FFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-6: `CALL` STACK FRAME



4.3 Instruction Addressing Modes

The addressing modes shown in Table 4-48 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the `MAC` class of instructions differ from those in the other instruction types.

4.3.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (near data space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the `MUL` instruction), which writes the result to a register or register pair. The `MOV` instruction allows additional flexibility and can access the entire data space.

4.3.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be register direct), which is referred to as Wb. Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note:	Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-48: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn forms the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn forms the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

4.3.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions and the DSP accumulator class of instructions provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

> **Note:** For the `MOV` instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (register offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

> **Note:** Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.3.4 `MAC` INSTRUCTIONS

The dual source operand DSP instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MPY`, `MPY.N`, `MOVSAC` and `MSC`), also referred to as `MAC` instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the data pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The effective addresses generated (before and after modification) must, therefore, be valid addresses within X data space for W8 and W9 and Y data space for W10 and W11.

> **Note:** Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the `MAC` class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.3.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, `BRA` (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the `DISI` instruction uses a 14-bit unsigned literal field. In some instructions, such as `ADD Acc`, the source of an operand or result is implied by the opcode itself. Certain operations, such as `NOP`, do not have any operands.

4.4 Modulo Addressing

Modulo Addressing mode is a method used to provide an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either data or program space (since the data pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into program space) and Y data spaces. Modulo Addressing can operate on any W register pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction as there are certain restrictions on the buffer start address (for incrementing buffers), or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.4.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.4.2 W ADDRESS REGISTER SELECTION

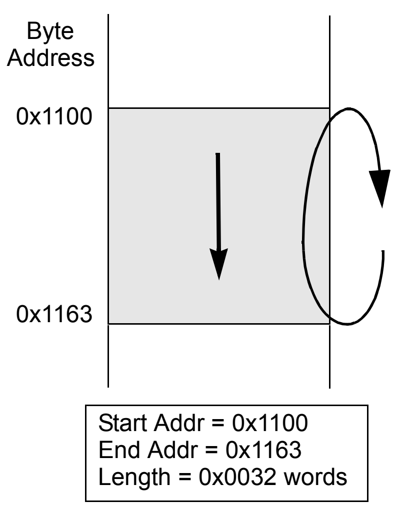
The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that will operate with Modulo Addressing:

- If XWM = `15`, X RAGU and X WAGU Modulo Addressing is disabled.
- If YWM = `15`, Y AGU Modulo Addressing is disabled.

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X data space when XWM is set to any value other than '15' and the XMODEN bit is set at MODCON<15>.

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y data space when YWM is set to any value other than '15' and the YMODEN bit is set at MODCON<14>.

FIGURE 4-7: MODULO ADDRESSING OPERATION EXAMPLE




```
MOV     #0x1100, W0
MOV     W0, XMODSRT    ;set modulo start address
MOV     #0x1163, W0
MOV     W0, MODEND     ;set modulo end address
MOV     #0x8001, W0
MOV     W0, MODCON     ;enable W1, X AGU for modulo

MOV     #0x0000, W0    ;W0 holds buffer fill value

MOV     #0x1110, W1    ;point W1 to buffer

DO      AGAIN, #0x31   ;fill the 50 buffer locations
MOV     W0, [W1++]     ;fill the next location
AGAIN:  INC W0, W0     ;increment the fill value
```

4.4.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

> **Note:** The modulo corrected effective address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the effective address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed but the contents of the register remain unchanged.

4.5 Bit-Reversed Addressing

Bit-Reversed Addressing mode is intended to simplify data re-ordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.5.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled in any of these situations:

- BWM bits (W register selection) in the MODCON register are any value other than 15 (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is $M = 2^N$ bytes, the last 'N' bits of the data buffer start address must be zeros.

XB<14:0> is the Bit-Reversed Address modifier, or 'pivot point,' which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

> **Note:** All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It will not function for any other addressing mode or for byte-sized data, and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB), and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

> **Note:** Modulo Addressing and Bit-Reversed Addressing should not be enabled together. If an application attempts to do so, Bit-Reversed Addressing will assume priority when active for the X WAGU and X WAGU; Modulo Addressing will be disabled. However, Modulo Addressing will continue to function in the X RAGU.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

FIGURE 4-8: BIT-REVERSED ADDRESS EXAMPLE

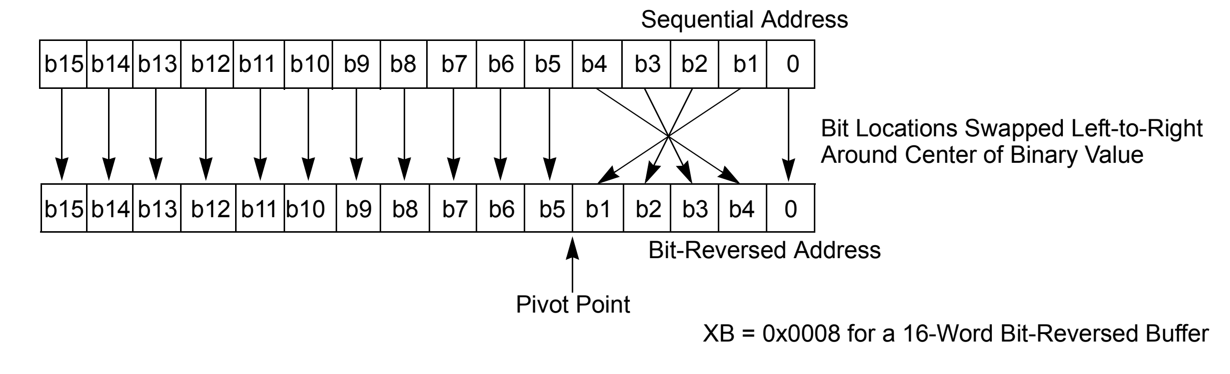


TABLE 4-49: BIT-REVERSED ADDRESS SEQUENCE (16-ENTRY)

Normal Address					Bit-Reversed Address				
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

4.6 Interfacing Program and Data Memory Spaces

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 architecture uses a 24-bit-wide program space and a 16-bit-wide data space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 architecture provides two methods by which program space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the program space
- Remapping a portion of the program space into the data space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look ups from a large table of static data. The application can only access the least significant word of the program word.

4.6.1 ADDRESSING PROGRAM SPACE

Since the address ranges for the data and program spaces are 16 and 24 bits, respectively, a method is needed to create a 23-bit or 24-bit program address from 16-bit data registers. The solution depends on the interface method to be used.

For table operations, the 8-bit Table Page register (TBLPAG) is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full 24-bit program space address. In this format, the Most Significant bit of TBLPAG is used to determine if the operation occurs in the user memory (TBLPAG<7> = `0`) or the configuration memory (TBLPAG<7> = `1`).

For remapping operations, the 8-bit Program Space Visibility Register (PSVPAG) is used to define a 16K word page in the program space. When the Most Significant bit of the EA is '`1`', PSVPAG is concatenated with the lower 15 bits of the EA to form a 23-bit program space address. Unlike table operations, this limits remapping operations strictly to the user memory area.

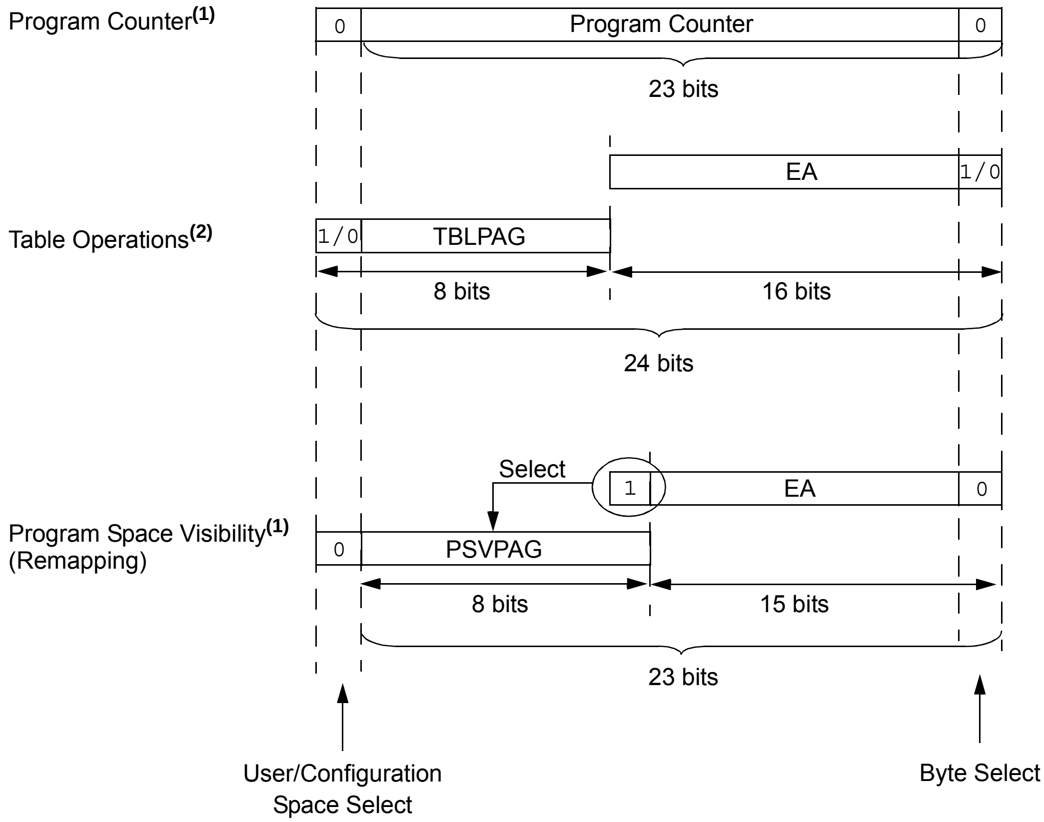
Table 4-50 and Figure 4-9 show how the program EA is created for table operations and remapping accesses from the data EA. Here, P<23:0> refers to a program space word, and D<15:0> refers to a data space word.

TABLE 4-50: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx		xxxx xxxx xxxx xxxx		
Program Space Visibility (Block Remap/Read)	User	0	PSVPAG<7:0>		Data EA<14:0>(1)	
		0	xxxx xxxx		xxx xxxx xxxx xxxx	

Note 1: Data EA<15> is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is PSVPAG<0>.

FIGURE 4-9: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Note 1: The Least Significant bit (LSb) of program space addresses is always fixed as '0' to maintain word alignment of data in the program and data spaces.

2: Table operations are not required to be word-aligned. Table read operations are permitted in the configuration memory space.

4.6.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

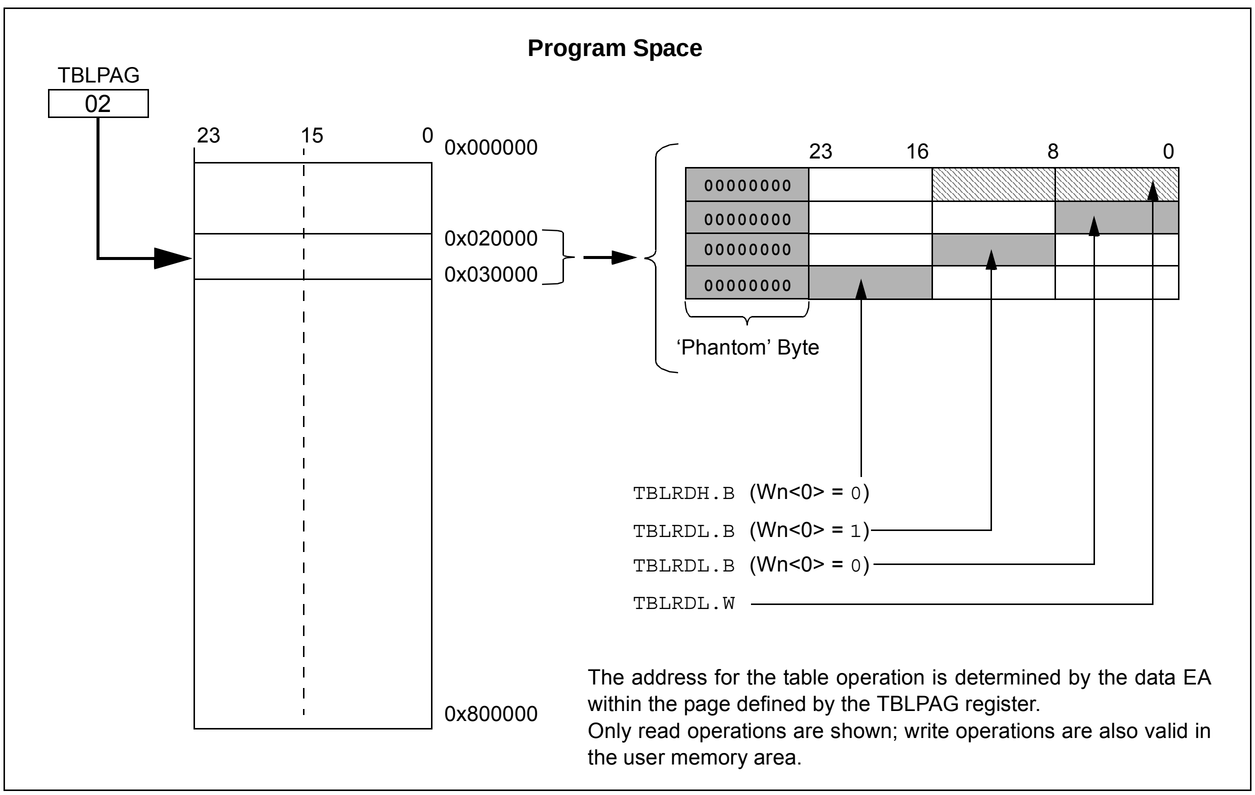
Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
  - In Word mode, this instruction maps the lower word of the program space location (P<15:0>) to a data address (D<15:0>).
  - In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is ‘1’; the lower byte is selected when it is ‘0’.
- TBLRDH (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. Note that D<15:8>, the ‘phantom byte’, will always be ‘0’.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to D<7:0> of the data address, in the TBLRDL instruction. The data is always ‘0’ when the upper ‘phantom’ byte is selected (Byte Select = 1).

Similarly, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are explained in **Section 5.0 “Flash Program Memory”**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

FIGURE 4-10: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



4.6.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into any 16K word page of the program space. This option provides transparent access to stored constant data from the data space without the need to use special instructions (such as TBLRDL/H).

Program space access through the data space occurs if the Most Significant bit of the data space EA is '1' and program space visibility is enabled by setting the PSV bit in the Core Control register (CORCON<2>). The location of the program memory space to be mapped into the data space is determined by the Program Space Visibility Page register (PSVPAG). This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, PSVPAG functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits. By incrementing the PC by 2 for each program memory word, the lower 15 bits of data space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads to this area add a cycle to the instruction being executed, since two program memory fetches are required.

Although each data space address 8000h and higher maps directly into a corresponding program memory address (see Figure 4-11), only the lower 16 bits of the 24-bit program word are used to contain the data. The upper 8 bits of any program space location used as data should be programmed with '1111 1111' or '0000 0000' to force a NOP. This prevents possible issues should the area of code ever be accidentally executed.

Note:	PSV access is temporarily disabled during table reads/writes.

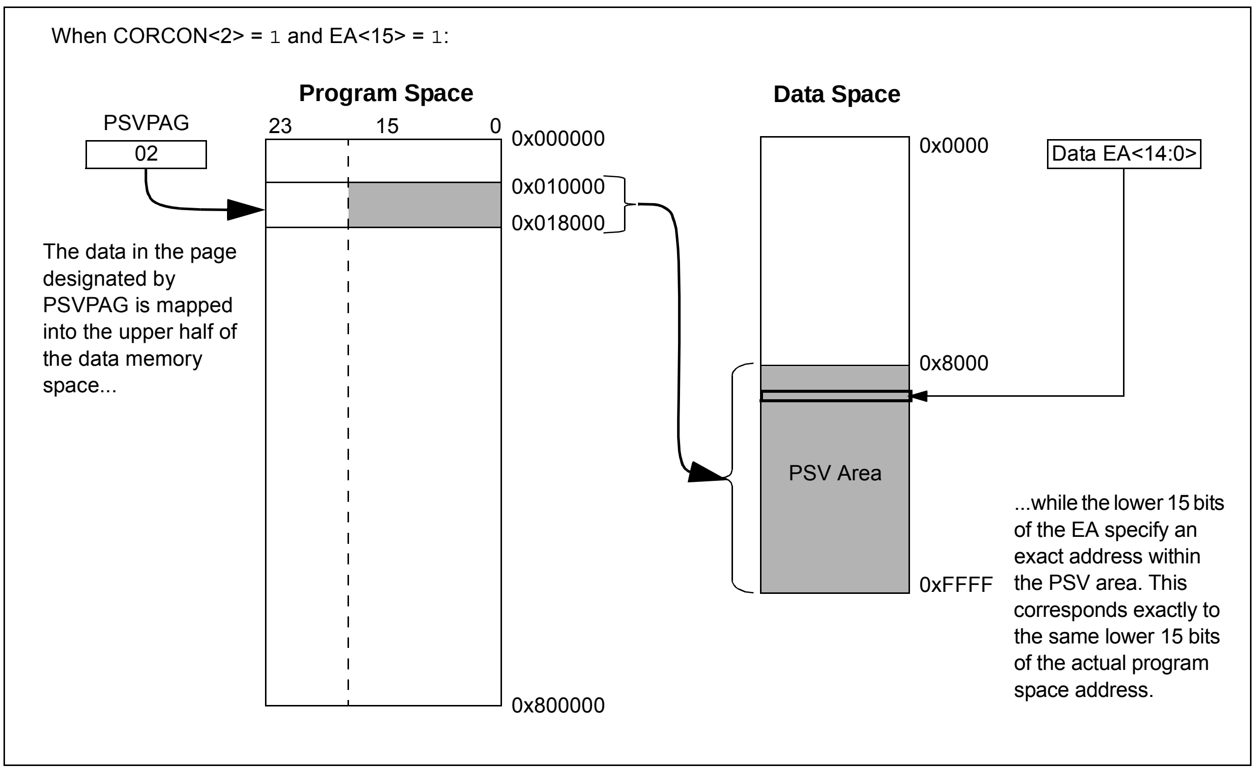
For operations that use PSV and are executed outside a REPEAT loop, the MOV and MOV.D instructions require one instruction cycle in addition to the specified execution time. All other instructions require two instruction cycles in addition to the specified execution time.

For operations that use PSV, and are executed inside a REPEAT loop, these instances require two instruction cycles in addition to the specified execution time of the instruction:

- Execution in the first iteration
- Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the REPEAT loop will allow the instruction using PSV to access data, to execute in a single cycle.

FIGURE 4-11: PROGRAM SPACE VISIBILITY OPERATION



NOTES:

5.0 FLASH PROGRAM MEMORY

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33F Family Reference Manual*", **Section 5. "Flash Programming"** (DS70191), which is available from the Microchip web site (www.microchip.com).

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows a dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx, and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the digital signal controller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using `TBLRD` (table read) and `TBLWT` (table write) instructions. With RTSP, the user application can write program memory data, either in blocks or 'rows' of 64 instructions (192 bytes) at a time, or a single program memory word, and erase program memory in blocks or 'pages' of 512 instructions (1536 bytes) at a time.

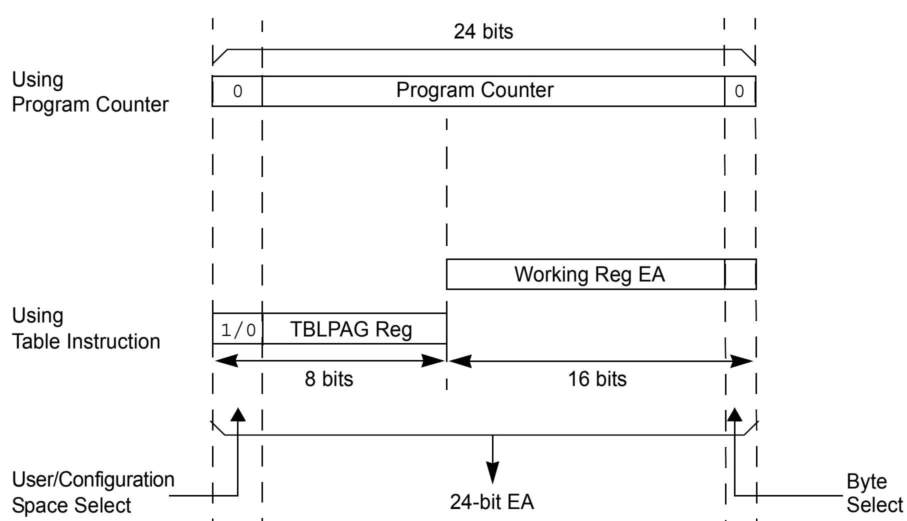
5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the table read and table write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 5-1.

The `TBLRDL` and the `TBLWTL` instructions are used to read or write to bits<15:0> of program memory. `TBLRDL` and `TBLWTL` can access program memory in both Word and Byte modes.

The `TBLRDH` and `TBLWTH` instructions are used to read or write to bits<23:16> of program memory. `TBLRDH` and `TBLWTH` can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



5.2 RTSP Operation

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of memory, which consists of eight rows (512 instructions) at a time, and to program one row or one word at a time. Table 24-12 shows typical erase and programming times. The 8-row erase pages and single row write rows are edge-aligned from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

The program memory implements holding buffers that can contain 64 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the buffers sequentially. The instruction words loaded must always be from a group of 64 boundary.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of `TBLWT` instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register. A total of 64 `TBLWTL` and `TBLWTH` instructions are required to load the instructions.

All of the table write operations are single-word writes (two instruction cycles) because only the buffers are written. A programming cycle is required for programming each row.

5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

The programming time depends on the FRC accuracy (see Table 24-20) and the value of the FRC Oscillator Tuning register (see Register 8-4). Use the following formula to calculate the minimum and maximum values for the Row Write Time, Page Erase Time, and Word Write Cycle Time parameters (see Table 24-12).

EQUATION 5-1: PROGRAMMING TIME

$$\frac{T}{7.37\ MHz \times (FRC\ Accuracy)\% \times (FRC\ Tuning)\%}$$

For example, if the device is operating at +125°C, the FRC accuracy will be ±5%. If the TUN<5:0> bits (see Register 8-4) are set to `'b111111`, the Minimum Row Write Time is:

$$T_{RW} = \frac{11064\ Cycles}{7.37\ MHz \times (1 + 0.05) \times (1 - 0.00375)} = 1.435ms$$

and, the Maximum Row Write Time is:

$$T_{RW} = \frac{11064\ Cycles}{7.37\ MHz \times (1 - 0.05) \times (1 - 0.00375)} = 1.586ms$$

Setting the WR bit (NVMCON<15>) starts the operation, and the WR bit is automatically cleared when the operation is finished.

5.4 Control Registers

Two SFRs are used to read and write the program Flash memory: NVMCON and NVMKEY.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to **Section 5.3 "Programming Operations"** for further details.

REGISTER 5-1: NVMCON: FLASH MEMORY CONTROL REGISTER

R/SO-0(1)	R/W-0(1)	R/W-0(1)	U-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0(1)	U-0	U-0	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)
—	ERASE	—	—	NVMOP<3:0>(2)			
bit 7							bit 0

Legend:	SO = Settable Only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **WR:** Write Control bit
1 = Initiates a Flash memory program or erase operation. The operation is self-timed and the bit is cleared by hardware once operation is complete.
0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit
1 = Enable Flash program/erase operations
0 = Inhibit Flash program/erase operations

bit 13 **WRERR:** Write Sequence Error Flag bit
1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
0 = The program or erase operation completed normally

bit 12-7 **Unimplemented:** Read as ‘0’

bit 6 **ERASE:** Erase/Program Enable bit
1 = Perform the erase operation specified by NVMOP<3:0> on the next WR command
0 = Perform the program operation specified by NVMOP<3:0> on the next WR command

bit 5-4 **Unimplemented:** Read as ‘0’

bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits(2)

If ERASE = 1:
1111 = Memory bulk erase operation
1101 = Erase general segment
0011 = No operation
0010 = Memory page erase operation
0001 = No operation
0000 = Erase a single Configuration register byte

If ERASE = 0:
1111 = No operation
1101 = No operation
0011 = Memory word program operation
0010 = No operation
0001 = Memory row program operation
0000 = Program a single Configuration register byte

Note 1: These bits can only be Reset on POR.
2: All other combinations of NVMOP<3:0> are unimplemented.

REGISTER 5-2: NVMKEY: NONVOLATILE MEMORY KEY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **NVMKEY<7:0>:** Key Register bits (write-only)

5.4.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

One row of program Flash memory can be programmed at a time. To achieve this, it is necessary to erase the 8-row erase page that contains the desired row. The general process is:

1. Read eight rows of program memory (512 instructions) and store in data RAM.
2. Update the program data in RAM with the desired new data.
3. Erase the block (see Example 5-1):
   a) Set the NVMOP bits (NVMCON<3:0>) to '`0010`' to configure for block erase. Set the ERASE (NVMCON<6>) and WREN (NVMCON<14>) bits.
   b) Write the starting address of the page to be erased into the TBLPAG and W registers.
   c) Write 0x55 to NVMKEY.
   d) Write 0xAA to NVMKEY.
   e) Set the WR bit (NVMCON<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.
4. Write the first 64 instructions from data RAM into the program memory buffers (see Example 5-2).
5. Write the program block to Flash memory:
   a) Set the NVMOP bits to '`0001`' to configure for row programming. Clear the ERASE bit and set the WREN bit.
   b) Write 0x55 to NVMKEY.
   c) Write 0xAA to NVMKEY.
   d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.
6. Repeat steps 4 and 5, using the next available 64 instructions from the block in data RAM by incrementing the value in TBLPAG, until all 512 instructions are written back to Flash memory.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be `NOP`s, as shown in Example 5-3.

EXAMPLE 5-1: ERASING A PROGRAM MEMORY PAGE

```
; Set up NVMCON for block erase operation
       MOV     #0x4042, W0                  ;
       MOV     W0, NVMCON                   ; Initialize NVMCON
; Init pointer to row to be ERASED
       MOV     #tblpage(PROG_ADDR), W0      ;
       MOV     W0, TBLPAG                   ; Initialize PM Page Boundary SFR
       MOV     #tbloffset(PROG_ADDR), W0    ; Initialize in-page EA[15:0] pointer
       TBLWTL  W0, [W0]                     ; Set base address of erase block
       DISI    #5                           ; Block all interrupts with priority <7
                                            ; for next 5 instructions
       MOV     #0x55, W0
       MOV     W0, NVMKEY                   ; Write the 55 key
       MOV     #0xAA, W1                    ;
       MOV     W1, NVMKEY                   ; Write the AA key
       BSET    NVMCON, #WR                  ; Start the erase sequence
       NOP                                  ; Insert two NOPs after the erase
       NOP                                  ; command is asserted
```

EXAMPLE 5-2: LOADING THE WRITE BUFFERS

```
; Set up NVMCON for row programming operations
       MOV     #0x4001, W0                ;
       MOV     W0, NVMCON                 ; Initialize NVMCON
; Set up a pointer to the first program memory location to be written
; program memory selected, and writes enabled
       MOV     #0x0000, W0                ;
       MOV     W0, TBLPAG                 ; Initialize PM Page Boundary SFR
       MOV     #0x6000, W0                ; An example program memory address
; Perform the TBLWT instructions to write the latches
; 0th_program_word
       MOV     #LOW_WORD_0, W2            ;
       MOV     #HIGH_BYTE_0, W3           ;
       TBLWTL  W2, [W0]                   ; Write PM low word into program latch
       TBLWTH  W3, [W0++]                 ; Write PM high byte into program latch
; 1st_program_word
       MOV     #LOW_WORD_1, W2            ;
       MOV     #HIGH_BYTE_1, W3           ;
       TBLWTL  W2, [W0]                   ; Write PM low word into program latch
       TBLWTH  W3, [W0++]                 ; Write PM high byte into program latch
;  2nd_program_word
       MOV     #LOW_WORD_2, W2            ;
       MOV     #HIGH_BYTE_2, W3           ;
       TBLWTL  W2, [W0]                   ; Write PM low word into program latch
       TBLWTH  W3, [W0++]                 ; Write PM high byte into program latch
       •
       •
       •
; 63rd_program_word
       MOV     #LOW_WORD_31, W2           ;
       MOV     #HIGH_BYTE_31, W3          ;
       TBLWTL  W2, [W0]                   ; Write PM low word into program latch
       TBLWTH  W3, [W0++]                 ; Write PM high byte into program latch
```

EXAMPLE 5-3: INITIATING A PROGRAMMING SEQUENCE

```
       DISI    #5                         ; Block all interrupts with priority <7
                                          ; for next 5 instructions
       MOV     #0x55, W0
       MOV     W0, NVMKEY                 ; Write the 55 key
       MOV     #0xAA, W1                  ;
       MOV     W1, NVMKEY                 ; Write the AA key
       BSET    NVMCON, #WR                ; Start the erase sequence
       NOP                                ; Insert two NOPs after the
       NOP                                ; erase command is asserted
```


6.0 RESETS

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33F Family Reference Manual*", **Section 8. "Reset"** (DS70192), which is available from the Microchip web site (www.microchip.com).

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- $\overline{\text{MCLR}}$: Master Clear Pin Reset
- SWR: Software `RESET` Instruction
- WDTO: Watchdog Timer Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
  - Illegal Opcode Reset
  - Uninitialized W Register Reset
  - Security Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of reset will make the $\overline{\text{SYSRST}}$ signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

Note:	Refer to the specific peripheral section or **Section 3.0 "CPU"** of this data sheet for register Reset states.

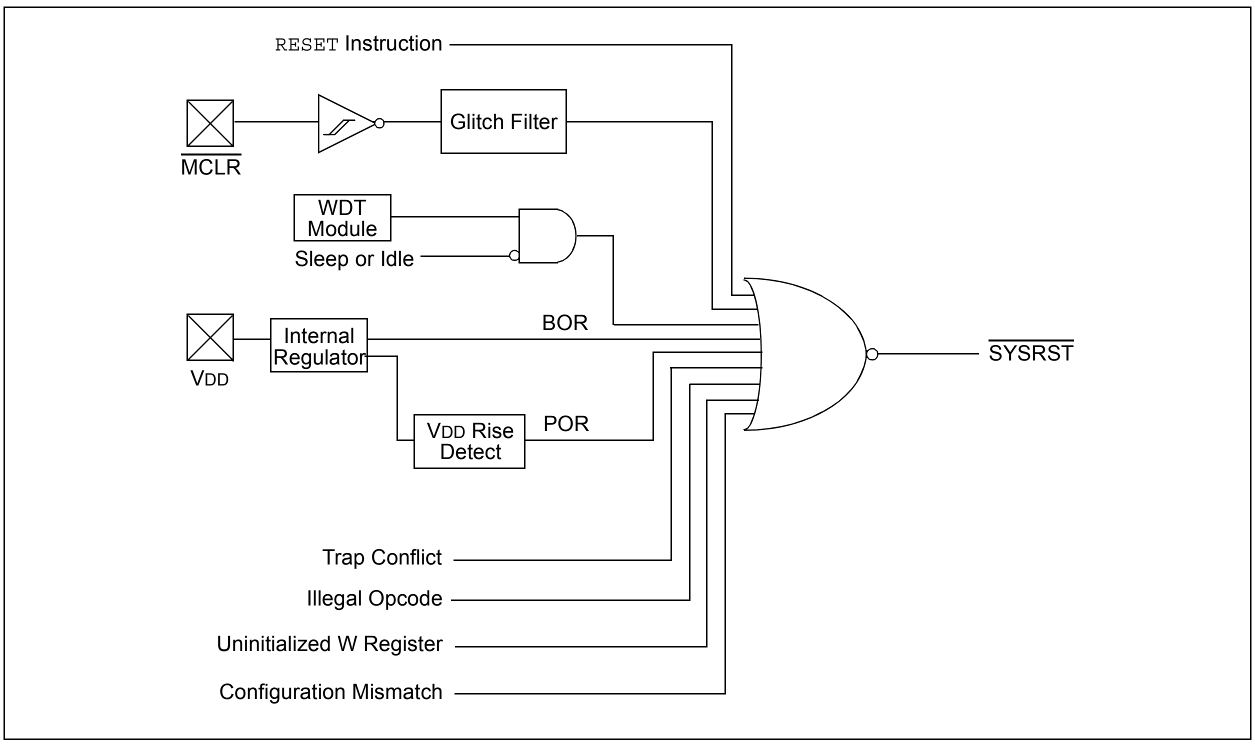
All types of device Reset sets a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits, except for the POR bit (RCON<0>), that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note:	The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM



REGISTER 6-1: RCON: RESET CONTROL REGISTER(1)

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	—	—	—	—	CM	VREGS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN(2)	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or uninitialized W Reset has not occurred

bit 13-10 **Unimplemented:** Read as ‘0’

bit 9 **CM:** Configuration Mismatch Flag bit
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has NOT occurred

bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset Pin ($\overline{\text{MCLR}}$) bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag (Instruction) bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(2)
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is ‘1’ (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

REGISTER 6-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)

bit 1	**BOR:** Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred
bit 0	**POR:** Power-on Reset Flag bit 1 = A Power-up Reset has occurred 0 = A Power-up Reset has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is ‘1’ (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

6.1 System Reset

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices have two types of Reset:

- Cold Reset
- Warm Reset

A cold Reset is the result of a Power-on Reset (POR) or a Brown-out Reset (BOR). On a cold Reset, the FNOSC Configuration bits in the FOSC Configuration register select the device clock source.

A warm Reset is the result of all the other Reset sources, including the `RESET` instruction. On warm Reset, the device will continue to operate from the current clock source as indicated by the Current Oscillator Selection (COSC<2:0>) bits in the Oscillator Control (OSCCON<14:12>) register.

The device is kept in a Reset state until the system power supplies have stabilized at appropriate levels and the oscillator clock is ready. The sequence in which this occurs is detailed below and is shown in Figure 6-2.

1. **POR Reset:** A POR circuit holds the device in Reset when the power supply is turned on. The POR circuit is active until VDD crosses the VPOR threshold and the delay, TPOR, has elapsed.
2. **BOR Reset:** The on-chip voltage regulator has a BOR circuit that keeps the device in Reset until VDD crosses the VBOR threshold and the delay, TBOR, has elapsed. The delay, TBOR, ensures that the voltage regulator output becomes stable.
3. **PWRT Timer:** The programmable power-up timer continues to hold the processor in Reset for a specific period of time (TPWRT) after a BOR. The delay TPWRT ensures that the system power supplies have stabilized at the appropriate level for full-speed operation. After the delay, TPWRT, has elapsed, the $\overline{\text{SYSRST}}$ becomes inactive, which in turn enables the selected oscillator to start generating clock cycles.
4. **Oscillator Delay:** The total delay for the clock to be ready for various clock source selections is given in Table 6-1. Refer to **Section 8.0 "Oscillator Configuration"** for more information.
5. When the oscillator clock is ready, the processor begins execution from location 0x000000. The user application programs a `GOTO` instruction at the Reset address, which redirects program execution to the appropriate start-up routine.
6. The Fail-Safe Clock Monitor (FSCM), if enabled, begins to monitor the system clock when the system clock is ready and the delay, TFSCM, elapsed.

TABLE 6-1: OSCILLATOR DELAY

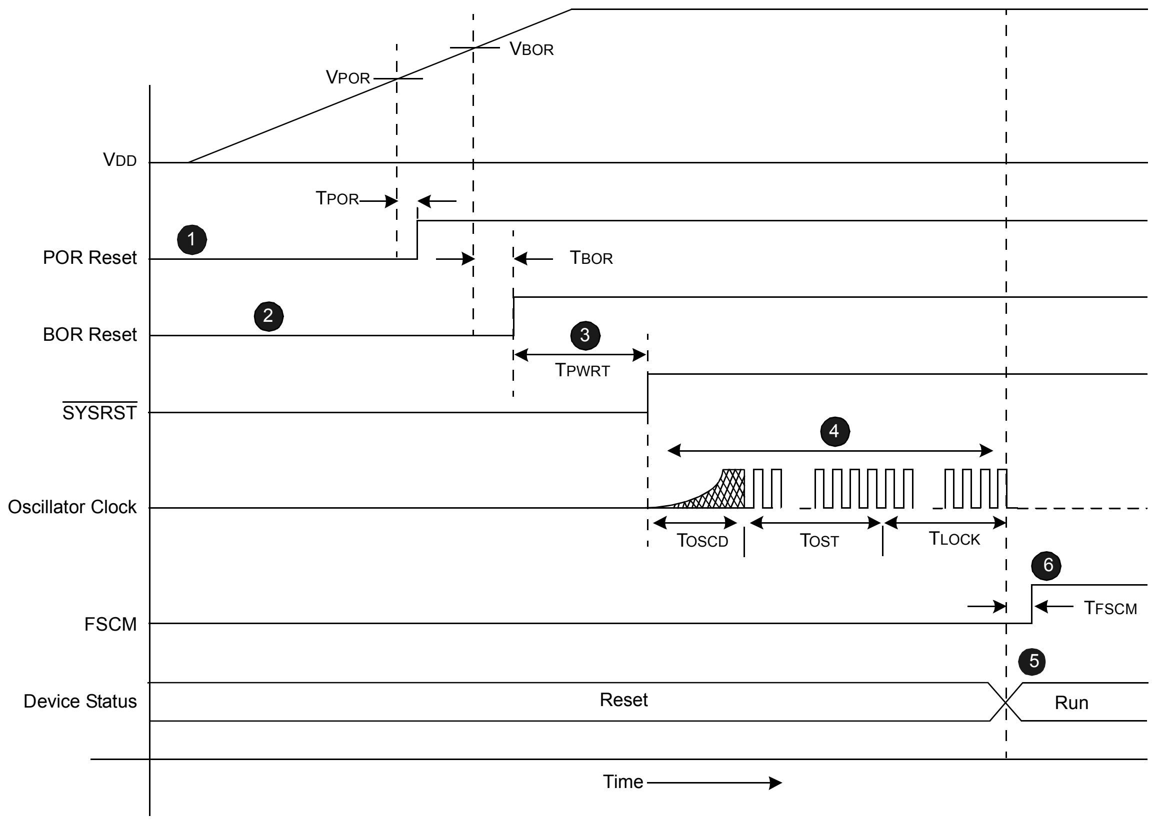
Oscillator Mode	Oscillator Startup Delay	Oscillator Startup Timer	PLL Lock Time	Total Delay
FRC, FRCDIV16, FRCDIVN	TOSCD(1)	—	—	TOSCD(1)
FRCPLL	TOSCD(1)	—	TLOCK(3)	TOSCD + TLOCK(1,3)
XT	TOSCD(1)	TOST(2)	—	TOSCD + TOST(1,2)
HS	TOSCD(1)	TOST(2)	—	TOSCD + TOST(1,2)
EC	—	—	—	—
XTPLL	TOSCD(1)	TOST(2)	TLOCK(3)	TOSCD + TOST + TLOCK(1,2,3)
HSPLL	TOSCD(1)	TOST(2)	TLOCK(3)	TOSCD + TOST + TLOCK(1,2,3)
ECPLL	—	—	TLOCK(3)	TLOCK(3)
LPRC	TOSCD(1)	—	—	TOSCD(1)

Note 1: TOSCD = Oscillator start-up delay (1.1 μs max for FRC, 70 μs max for LPRC). Crystal oscillator start-up times vary with crystal characteristics, load capacitance, etc.

2: TOST = Oscillator start-up timer delay (1024 oscillator clock period). For example, TOST = 102.4 μs for a 10 MHz crystal and TOST = 32 ms for a 32 kHz crystal.

3: TLOCK = PLL lock time (1.5 ms nominal) if PLL is enabled.

FIGURE 6-2: SYSTEM RESET TIMING



Note 1: POR Reset: A POR circuit holds the device in Reset when the power supply is turned on. The POR circuit is active until VDD crosses the VPOR threshold and the delay, TPOR, has elapsed.

2: BOR Reset: The on-chip voltage regulator has a BOR circuit that keeps the device in Reset until VDD crosses the VBOR threshold and the delay, TBOR, has elapsed. The delay, TBOR, ensures the voltage regulator output becomes stable.

3: PWRT Timer: The programmable power-up timer continues to hold the processor in Reset for a specific period of time (TPWRT) after a BOR. The delay, TPWRT, ensures that the system power supplies have stabilized at the appropriate level for full-speed operation. After the delay, TPWRT has elapsed and the SYSRST becomes inactive, which in turn, enables the selected oscillator to start generating clock cycles.

4: Oscillator Delay: The total delay for the clock to be ready for various clock source selections is given in Table 6-1. Refer to **Section 8.0 "Oscillator Configuration"** for more information.

5: When the oscillator clock is ready, the processor begins execution from location 0x000000. The user application programs a `GOTO` instruction at the Reset address, which redirects program execution to the appropriate start-up routine.

6: If the Fail-Safe Clock Monitor (FSCM) is enabled, it begins to monitor the system clock when the system clock is ready and the delay, TFSCM, has elapsed.

TABLE 6-2: OSCILLATOR DELAY

Symbol	Parameter	Value
V_{POR}	POR threshold	1.8V nominal
T_{POR}	POR extension time	30 µs maximum
V_{BOR}	BOR threshold	2.5V nominal
T_{BOR}	BOR extension time	100 µs maximum
T_{PWRT}	Programmable power-up time delay	0-128 ms nominal
T_{FSCM}	Fail-Safe Clock Monitor delay	900 µs maximum

> **Note:** When the device exits the Reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges; otherwise, the device may not function correctly. The user application must ensure that the delay between the time power is first applied, and the time $\overline{SYSRST}$ becomes inactive, is long enough to get all operating parameters within specification.

6.2 Power-on Reset (POR)

A Power-on Reset (POR) circuit ensures the device is reset from power-on. The POR circuit is active until V_{DD} crosses the V_{POR} threshold and the delay, T_{POR}, has elapsed. The delay, T_{POR}, ensures the internal device bias circuits become stable.

The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR. Refer to **Section 24.0 “Electrical Characteristics”** for details.

The POR status (POR) bit in the Reset Control (RCON<0>) register is set to indicate the Power-on Reset.

6.2.1 Brown-out Reset (BOR) and Power-up Timer (PWRT)

The on-chip regulator has a Brown-out Reset (BOR) circuit that resets the device when the V_{DD} is too low ($V_{DD} < V_{BOR}$) for proper device operation. The BOR circuit keeps the device in Reset until V_{DD} crosses the V_{BOR} threshold and the delay, T_{BOR}, has elapsed. The delay, T_{BOR}, ensures the voltage regulator output becomes stable.

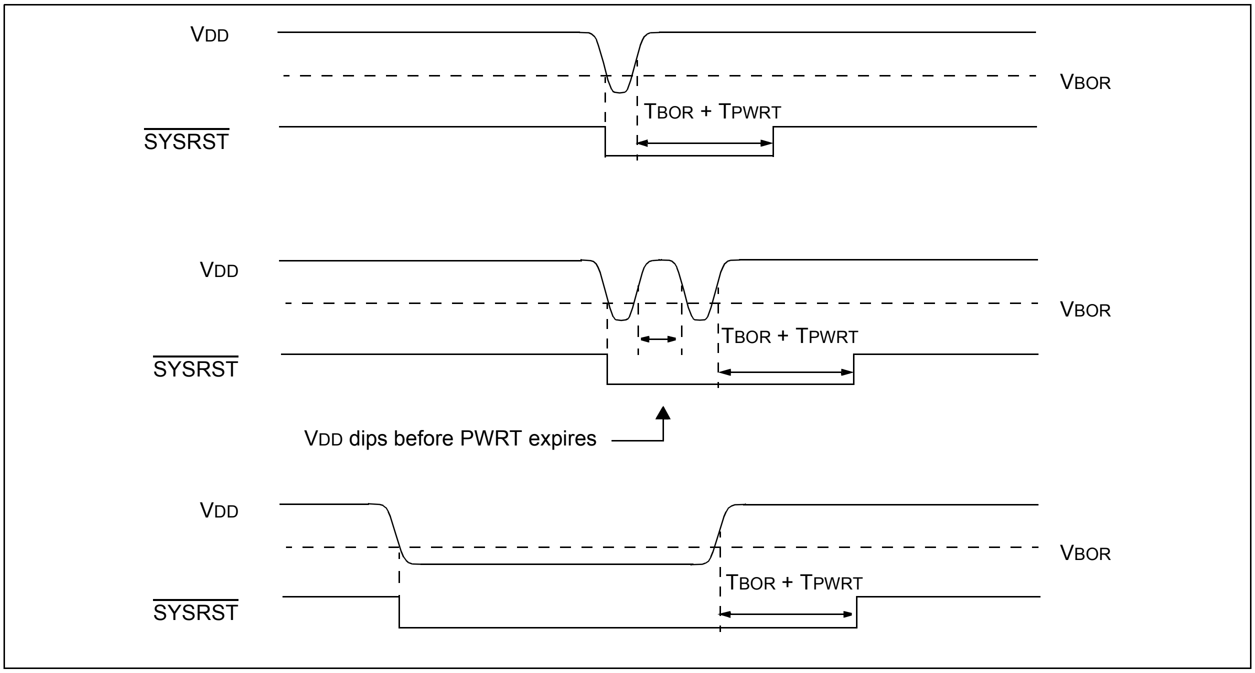
The BOR status (BOR) bit in the Reset Control (RCON<1>) register is set to indicate the Brown-out Reset.

The device will not run at full speed after a BOR as the V_{DD} should rise to acceptable levels for full-speed operation. The PWRT provides power-up time delay (T_{PWRT}) to ensure that the system power supplies have stabilized at the appropriate levels for full-speed operation before the $\overline{SYSRST}$ is released.

The power-up timer delay (T_{PWRT}) is programmed by the Power-on Reset Timer Value Select (FPWRT<2:0>) bits in the POR Configuration (FPOR<2:0>) register, which provides eight settings (from 0 ms to 128 ms). Refer to **Section 21.0 “Special Features”** for further details.

Figure 6-3 shows the typical brown-out scenarios. The reset delay ($T_{BOR} + T_{PWRT}$) is initiated each time V_{DD} rises above the V_{BOR} trip point

FIGURE 6-3: BROWN-OUT SITUATIONS



6.3 External Reset (EXTR)

The external Reset is generated by driving the $\overline{\text{MCLR}}$ pin low. The $\overline{\text{MCLR}}$ pin is a Schmitt trigger input with an additional glitch filter. Reset pulses that are longer than the minimum pulse width will generate a Reset. Refer to **Section 24.0 "Electrical Characteristics"** for minimum pulse width specifications. The external Reset ($\overline{\text{MCLR}}$) pin (EXTR) bit in the Reset Control (RCON) register is set to indicate the $\overline{\text{MCLR}}$ Reset.

6.3.0.1 EXTERNAL SUPERVISORY CIRCUIT

Many systems have external supervisory circuits that generate Reset signals to reset multiple devices in the system. This external Reset signal can be directly connected to the $\overline{\text{MCLR}}$ pin to reset the device when the rest of system is reset.

6.3.0.2 INTERNAL SUPERVISORY CIRCUIT

When using the internal power supervisory circuit to reset the device, the external Reset pin ($\overline{\text{MCLR}}$) should be tied directly or resistively to VDD. In this case, the $\overline{\text{MCLR}}$ pin will not be used to generate a Reset. The external Reset pin ($\overline{\text{MCLR}}$) does not have an internal pull-up and must not be left unconnected.

6.4 Software `RESET` Instruction (SWR)

Whenever the `RESET` instruction is executed, the device will assert $\overline{\text{SYSRST}}$, placing the device in a special Reset state. This Reset state will not re-initialize the clock. The clock source in effect prior to the `RESET` instruction will remain. $\overline{\text{SYSRST}}$ is released at the next instruction cycle and the Reset vector fetch will commence.

The Software Reset (SWR) flag (instruction) in the Reset Control (RCON<6>) register is set to indicate the software Reset.

6.5 Watchdog Time-out Reset (WDTO)

Whenever a Watchdog time-out occurs, the device will asynchronously assert $\overline{\text{SYSRST}}$. The clock source will remain unchanged. A WDT time-out during Sleep or Idle mode will wake-up the processor, but will not reset the processor.

The Watchdog Timer Time-out (WDTO) flag in the Reset Control (RCON<4>) register is set to indicate the Watchdog Reset. Refer to **Section 21.4 "Watchdog Timer (WDT)"** for more information on Watchdog Reset.

6.6 Trap Conflict Reset

If a lower priority hard trap occurs while a higher priority trap is being processed, a hard Trap Conflict Reset occurs. The hard traps include exceptions of priority level 13 through level 15, inclusive. The address error (level 13) and oscillator error (level 14) traps fall into this category.

The Trap Reset (TRAPR) flag in the Reset Control (RCON<15>) register is set to indicate the Trap Conflict Reset. Refer to **Section 7.0 "Interrupt Controller"** for more information on Trap Conflict Resets.

6.7 Configuration Mismatch Reset

To maintain the integrity of the Peripheral Pin Select Control registers, they are constantly monitored with shadow registers in hardware. If an unexpected change in any of the registers occur (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset occurs.

The Configuration Mismatch (CM) flag in the Reset Control (RCON<9>) register is set to indicate the Configuration Mismatch Reset. Refer to **Section 10.0 "I/O Ports"** for more information on the Configuration Mismatch Reset.

> **Note:** The Configuration Mismatch Reset feature and associated Reset flag are not available on all devices.

6.8 Illegal Condition Device Reset

An illegal condition device Reset occurs due to the following sources:

- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

The Illegal Opcode or Uninitialized W Access Reset (IOPUWR) flag in the Reset Control (RCON<14>) register is set to indicate the illegal condition device Reset.

6.8.1 ILLEGAL OPCODE RESET

A device Reset is generated if the device attempts to execute an illegal opcode value that is fetched from program memory.

The Illegal Opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the Illegal Opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 3Fh, which is an illegal opcode value.

6.8.2 UNINITIALIZED W REGISTER RESET

Any attempt to use the uninitialized W register as an Address Pointer will Reset the device. The W register array (with the exception of W15) is cleared during all Resets and is considered uninitialized until written to.

6.8.3 SECURITY RESET

If a Program Flow Change (PFC) or Vector Flow Change (VFC) targets a restricted location in a protected segment (boot and secure segment), that operation will cause a Security Reset.

The PFC occurs when the program counter is reloaded as a result of a call, jump, computed jump, return, return from subroutine or other form of branch instruction.

The VFC occurs when the program counter is reloaded with an interrupt or trap vector.

Refer to **Section 21.8 "Code Protection and CodeGuard™ Security"** for more information on Security Reset.

6.9 Using the RCON Status Bits

The user application can read the Reset Control (RCON) register after any device Reset to determine the cause of the Reset.

> **Note:** The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

Table 6-3 provides a summary of the Reset flag bit operation.

TABLE 6-3: RESET FLAG BIT OPERATION

Flag Bit	Set by:	Cleared by:
TRAPR (RCON<15>)	Trap conflict event	POR,BOR
IOPWR (RCON<14>)	Illegal opcode or uninitialized W register access or Security Reset	POR,BOR
CM (RCON<9>)	Configuration Mismatch	POR,BOR
EXTR (RCON<7>)	$\overline{\text{MCLR}}$ Reset	POR
SWR (RCON<6>)	`RESET` instruction	POR,BOR
WDTO (RCON<4>)	WDT time-out	`PWRSAV` instruction, `CLRWDT` instruction, POR,BOR
SLEEP (RCON<3>)	`PWRSAV #SLEEP` instruction	POR,BOR
IDLE (RCON<2>)	`PWRSAV #IDLE` instruction	POR,BOR
BOR (RCON<1>)	POR, BOR	
POR (RCON<0>)	POR	

Note: All Reset flag bits can be set or cleared by user software.

7.0 INTERRUPT CONTROLLER

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33F Family Reference Manual*", **Section 41. "Interrupts (Part IV)"** (DS70300), which is available on the Microchip web site (www.microchip.com).

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CPU. It has the following features:

- Up to eight processor exceptions and software traps
- Seven user-selectable priority levels
- Interrupt Vector Table (IVT) with up to 118 vectors
- A unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Alternate Interrupt Vector Table (AIVT) for debug support
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The Interrupt Vector Table (IVT) is shown in Figure 7-1. The IVT resides in program memory, starting at location 000004h. The IVT contains 126 vectors, consisting of eight nonmaskable trap vectors, plus up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit-wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with vector 0 will take priority over interrupts at any other vector address.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices implement up to 35 unique interrupts and 4 non-maskable traps. These are summarized in Table 7-1.

7.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 7-1. Access to the AIVT is provided by the ALTIVT control bit (INTCON2<15>). If the ALTIVT bit is set, all interrupt and exception processes use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 device clears its registers in response to a Reset, which forces the PC to zero. The digital signal controller then begins program execution at location 0x000000. A `GOTO` instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note:	Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a `RESET` instruction.

FIGURE 7-1: dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 INTERRUPT VECTOR TABLE

Decreasing Natural Order Priority

Reset – GOTO Instruction	0x000000
Reset – GOTO Address	0x000002
Reserved	0x000004
Oscillator Fail Trap Vector	
Address Error Trap Vector	
Stack Error Trap Vector	
Math Error Trap Vector	
Reserved	
Reserved	
Reserved	
Interrupt Vector 0	0x000014
Interrupt Vector 1	
~	
~	
~	
Interrupt Vector 52	0x00007C
Interrupt Vector 53	0x00007E
Interrupt Vector 54	0x000080
~	
~	
~	
Interrupt Vector 116	0x0000FC
Interrupt Vector 117	0x0000FE
Reserved	0x000100
Reserved	0x000102
Reserved	
Oscillator Fail Trap Vector	
Address Error Trap Vector	
Stack Error Trap Vector	
Math Error Trap Vector	
Reserved	
Reserved	
Reserved	
Interrupt Vector 0	0x000114
Interrupt Vector 1	
~	
~	
~	
Interrupt Vector 52	0x00017C
Interrupt Vector 53	0x00017E
Interrupt Vector 54	0x000180
~	
~	
~	
Interrupt Vector 116	
Interrupt Vector 117	0x0001FE
Start of Code	0x000200

Interrupt Vector Table (IVT)(1) (0x000014 – 0x0000FC)

Alternate Interrupt Vector Table (AIVT)(1)

Note 1: See Table 7-1 for the list of implemented interrupt vectors.

TABLE 7-1: INTERRUPT VECTORS

Vector Number	Interrupt Request (IQR)	IVT Address	AIVT Address	Interrupt Source
Highest Natural Order Priority				
8	0	0x000014	0x000114	INT0 – External Interrupt 0
9	1	0x000016	0x000116	IC1 – Input Capture 1
10	2	0x000018	0x000118	OC1 – Output Compare 1
11	3	0x00001A	0x00011A	T1 – Timer1
12	4	0x00001C	0x00011C	Reserved
13	5	0x00001E	0x00011E	IC2 – Input Capture 2
14	6	0x000020	0x000120	OC2 – Output Compare 2
15	7	0x000022	0x000122	T2 – Timer2
16	8	0x000024	0x000124	T3 – Timer3
17	9	0x000026	0x000126	SPI1E – SPI1 Fault
18	10	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	11	0x00002A	0x00012A	U1RX – UART1 Receiver
20	12	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	13	0x00002E	0x00012E	ADC – ADC Group Convert Done
22	14	0x000030	0x000130	Reserved
23	15	0x000032	0x000132	Reserved
24	16	0x000034	0x000134	SI2C1 – I2C1 Slave Event
25	17	0x000036	0x000136	MI2C1 – I2C1 Master Event
26	18	0x000038	0x000138	CMP1 – Analog Comparator 1 Interrupt
27	19	0x00003A	0x00013A	CN – Input Change Notification Interrupt
28	20	0x00003C	0x00013C	INT1 – External Interrupt 1
29	21	0x00003E	0x00013E	Reserved
30	22	0x000040	0x000140	Reserved
31	23	0x000042	0x000142	Reserved
32	24	0x000044	0x000144	Reserved
33	25	0x000046	0x000146	Reserved
34	26	0x000048	0x000148	Reserved
35	27	0x00004A	0x00014A	Reserved
36	28	0x00004C	0x00014C	Reserved
37	29	0x00004E	0x00014E	INT2 – External Interrupt 2
38-64	30-56			Reserved
65	57	0x000086	0x000186	PWM PSEM Special Event Match
66-72	58-64			Reserved
73	65	0x000096	0x000196	U1E – UART1 Error Interrupt
74-101	66-93			Reserved
102	94	0x0000D0	0x0001D0	PWM1 – PWM1 Interrupt
103	95	0x0000D2	0x0001D2	PWM2 – PWM2 Interrupt
104	96	0x0000D4	0x0001D4	PWM3 – PWM3 Interrupt
105	97	0x0000D6	0x0001D6	PWM4 – PWM4 Interrupt
106	98	0x0000D8	0x0001D8	Reserved
107	99	0x0000DA	0x0001DA	Reserved
108	100	0x0000DC	0x0001DC	Reserved
109	101	0x0000DE	0x0001DE	Reserved
110	102	0x0000E0	0x0001E0	Reserved
111	103	0x0000E2	0x00001E2	CMP2 – Analog Comparator 2

TABLE 7-1: INTERRUPT VECTORS (CONTINUED)

Vector Number	Interrupt Request (IQR)	IVT Address	AIVT Address	Interrupt Source
112	104	0x0000E4	0x0001E4	CMP3 – Analog Comparator 3
113	105	0x0000E6	0x0001E6	CMP4 – Analog Comparator 4
114	106	0x0000E8	0x0001E8	Reserved
115	107	0x0000EA	0x0001EA	Reserved
116	108	0x0000EC	0x0001EC	Reserved
117	109	0x0000EE	0x0001EE	Reserved
118	110	0x0000F0	0x0001F0	ADC Pair 0 Convert Done
119	111	0x0000F2	0x0001F2	ADC Pair 1 Convert Done
120	112	0x0000F4	0x0001F4	ADC Pair 2 Convert Done
121	113	0x0000F6	0x0001F6	ADC Pair 3 Convert Done
122	114	0x0000F8	0x0001F8	ADC Pair 4 Convert Done
123	115	0x0000FA	0x0001FA	ADC Pair 5 Convert Done
124	116	0x0000FC	0x0001FC	ADC Pair 6 Convert Done
125	117	0x0000FE	0x0001FE	Reserved
Lowest Natural Order Priority				

 Preliminary

7.3 Interrupt Control and Status Registers

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices implement 27 registers for the interrupt controller:

- INTCON1
- INTCON2
- IFSx
- IECx
- IPCx
- INTTREG

7.3.1 INTCON1 AND INTCON2

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit as well as the control and status flags for the processor trap sources. The INTCON2 register controls the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table.

7.3.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

7.3.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.3.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

7.3.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt priority Level, which are latched into the Vector Number (VECNUM<6:0>) and Interrupt Level (ILR<3:0>) bit fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence that they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having vector number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit is found in IEC0<0> and the INT0IP bits are found in the first position of IPC0 (IPC0<2:0>).

7.3.6 STATUS/CONTROL REGISTERS

Although they are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality.

- The CPU STATUS register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU interrupt Priority Level. The user can change the current CPU priority level by writing to the IPL bits.
- The CORCON register contains the IPL3 bit, which together with IPL<2:0>, indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-1 through Register 7-35 in the following pages.

REGISTER 7-1: SR: CPU STATUS REGISTER(1)

R-0	R-0	R/C-0	R/C-0	R-0	R/C-0	R -0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0(3)	R/W-0(3)	R/W-0(3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(2)	IPL1(2)	IPL0(2)	RA	N	OV	Z	C
bit 7							bit 0

Legend:		
C = Clearable bit	R = Readable bit	U = Unimplemented bit, read as '0'
S = Settable bit	W = Writable bit	-n = Value at POR
'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(2)

`111` = CPU Interrupt Priority Level is 7 (15), user interrupts disabled
`110` = CPU Interrupt Priority Level is 6 (14)
`101` = CPU Interrupt Priority Level is 5 (13)
`100` = CPU Interrupt Priority Level is 4 (12)
`011` = CPU Interrupt Priority Level is 3 (11)
`010` = CPU Interrupt Priority Level is 2 (10)
`001` = CPU Interrupt Priority Level is 1 (9)
`000` = CPU Interrupt Priority Level is 0 (8)

Note 1: For complete register details, see Register 3-1.

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = `1`. User interrupts are disabled when IPL<3> = `1`.

3: The IPL<2:0> status bits are read-only when NSTDIS (INTCON1<15>) = `1`.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER(1)

U-0	U-0	U-0	U-0	R/W-0	R-0	R-0	R-0
—	—	—	US	EDT	DL<2:0>		
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3(2)	PSV	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	-n = Value at POR	'1' = Bit is set
0' = Bit is cleared	'x = Bit is unknown	U = Unimplemented bit, read as '0'	

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)

`1` = CPU Interrupt Priority Level is greater than 7
`0` = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see Register 3-2.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit
1 = Trap was caused by overflow of Accumulator A
0 = Trap was not caused by overflow of Accumulator A

bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit
1 = Trap was caused by overflow of Accumulator B
0 = Trap was not caused by overflow of Accumulator B

bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit
1 = Trap was caused by catastrophic overflow of Accumulator A
0 = Trap was not caused by catastrophic overflow of Accumulator A

bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit
1 = Trap was caused by catastrophic overflow of Accumulator B
0 = Trap was not caused by catastrophic overflow of Accumulator B

bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit
1 = Trap overflow of Accumulator A
0 = Trap disabled

bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit
1 = Trap overflow of Accumulator B
0 = Trap disabled

bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit
1 = Trap on catastrophic overflow of Accumulator A or B enabled
0 = Trap disabled

bit 7 **SFTACERR:** Shift Accumulator Error Status bit
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift

bit 6 **DIV0ERR:** Arithmetic Error Status bit
1 = Math error trap was caused by a divide by zero
0 = Math error trap was not caused by a divide by zero

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **MATHERR:** Arithmetic Error Status bit
1 = Math error trap has occurred
0 = Math error trap has not occurred

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 2	**STKERR:** Stack Error Trap Status bit 1 = Stack error trap has occurred 0 = Stack error trap has not occurred
bit 1	**OSCFAIL:** Oscillator Failure Trap Status bit 1 = Oscillator failure trap has occurred 0 = Oscillator failure trap has not occurred
bit 0	**Unimplemented:** Read as '0'

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
1 = Use alternate vector table
0 = Use standard (default) vector table

bit 14 **DISI:** `DISI` Instruction Status bit
1 = `DISI` instruction is active
0 = `DISI` instruction is not active

bit 13-3 **Unimplemented:** Read as ‘0’

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF(1,2)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IF(1,2)	OC2IF(1,2)	IC2IF	—	T1IF	OC1IF	IC1IF(1)	INT0IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **ADIF:** ADC Group Conversion Complete Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12 **U1TXIF:** UART1 Transmitter Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 11 **U1RXIF:** UART1 Receiver Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10 **SPI1IF:** SPI1 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 9 **SPI1EIF:** SPI1 Fault Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8 **T3IF:** Timer3 Interrupt Flag Status bit(1,2)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **T2IF:** Timer2 Interrupt Flag Status bit(1,2)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **OC2IF:** Output Compare Channel 2 Interrupt Flag Status bit(1,2)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **IC2IF:** Input Capture Channel 2 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **T1IF:** Timer1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

Note 1: This bit is not implemented in dsPIC33FJ06GS101/102 devices.
2: These bits are not implemented in dsPIC33FJ06GS202 devices.

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0 (CONTINUED)

bit 2	**OC1IF:** Output Compare Channel 1 Interrupt Flag Status bit `1` = Interrupt request has occurred `0` = Interrupt request has not occurred
bit 1	**IC1IF:** Input Capture Channel 1 Interrupt Flag Status bit(1) `1` = Interrupt request has occurred `0` = Interrupt request has not occurred
bit 0	**INT0IF:** External Interrupt 0 Flag Status bit `1` = Interrupt request has occurred `0` = Interrupt request has not occurred

Note 1: This bit is not implemented in dsPIC33FJ06GS101/102 devices.

2: These bits are not implemented in dsPIC33FJ06GS202 devices.

REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	INT2IF	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT1IF	CNIF	AC1IF(1)	MI2C1IF	SI2C1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **INT2IF:** External Interrupt 2 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12-5 **Unimplemented:** Read as ‘0’

bit 4 **INT1IF:** External Interrupt 1 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **CNIF:** Input Change Notification Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **AC1IF:** Analog Comparator 1 Interrupt Flag Status bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **MI2C1IF:** I2C1 Master Events Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **SI2C1IF:** I2C1 Slave Events Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

Note 1: This bit is not implemented in dsPIC33FJ16GS402/404 and dsPIC33FJ06GS101/102 devices.

REGISTER 7-7: IFS3: INTERRUPT FLAG STATUS REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	PSEMIF	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as ‘0’

bit 9 **PSEMIF:** PWM Special Event Match Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8-0 **Unimplemented:** Read as ‘0’

REGISTER 7-8: IFS4: INTERRUPT FLAG STATUS REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	U1EIF	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as ‘0’

bit 1 **U1EIF:** UART1 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **Unimplemented:** Read as ‘0’

REGISTER 7-9: IFS5: INTERRUPT FLAG STATUS REGISTER 5

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
PWM2IF(1)	PWM1IF	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PWM2IF:** PWM2 Interrupt Flag Status bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **PWM1IF:** PWM1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13-0 **Unimplemented:** Read as ‘0’

Note 1: This bit is not implemented in dsPIC33FJ06GS101/102 devices.

REGISTER 7-10: IFS6: INTERRUPT FLAG STATUS REGISTER 6

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
ADCP1IF	ADCP0IF	—	—	—	—	AC4IF[1,2]	AC3IF[1,2]
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
AC2IF[2]	—	—	—	—	—	PWM4IF[1,3]	PWM3IF[4]
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ADCP1IF:** ADC Pair 1 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **ADCP0IF:** ADC Pair 0 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13-10 **Unimplemented:** Read as ‘0’

bit 9 **AC4IF:** Analog Comparator 4 Interrupt Flag Status bit[1,2]
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8 **AC3IF:** Analog Comparator 3 Interrupt Flag Status bit[1,2]
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **AC2IF:** Analog Comparator 2 Interrupt Flag Status bit[2]
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6-2 **Unimplemented:** Read as ‘0’

bit 1 **PWM4IF:** PWM4 Interrupt Flag Status bit[1,3]
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **PWM3IF:** PWM3 Interrupt Flag Status bit[4]
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

Note 1: These bits are unimplemented in dsPIC33FJ06GS202 devices.
2: These bits are unimplemented in dsPIC33FJ06GS101 and dsPIC33FJ16GS502 devices.
3: These bits are unimplemented in dsPIC33FJ16GS402/404/502 devices.
4: These bits are unimplemented in dsPIC33FJ06101/102/202 devices.

REGISTER 7-11: IFS7: INTERRUPT FLAG STATUS REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	ADCP6IF	ADCP5IF(1)	ADCP4IF(1)	ADCP3IF(2)	ADCP2IF(3)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4 **ADCP6IF:** ADC Pair 6 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **ADCP5IF:** ADC Pair 5 Conversion Done Interrupt Flag Status bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **ADCP4IF:** ADC Pair 4 Conversion Done Interrupt Flag Status bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **ADCP3IF:** ADC Pair 3 Conversion Done Interrupt Flag Status bit(2)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **ADCP2IF:** ADC Pair 2 Conversion Done Interrupt Flag Status bit(3)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

Note 1: These bits are not implemented in dsPIC33FJ06GS101/102/202 and dsPIC33FJ16GS402/402/502 devices.

2: This bit is not implemented in dsPIC33FJ06GS102/202 devices.

3: This bit is not implemented in dsPIC33FJ06GS101 devices.

REGISTER 7-12: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE(1,2)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IE	OC2IE(1,2)	IC2IE(1,2)	—	T1IE	OC1IE	IC1IE(1)	INT0IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **ADIE:** ADC1 Conversion Complete Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 12 **U1TXIE:** UART1 Transmitter Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 11 **U1RXIE:** UART1 Receiver Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 10 **SPI1IE:** SPI1 Event Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 9 **SPI1EIE:** SPI1 Event Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 8 **T3IE:** Timer3 Interrupt Enable bit(1,2)
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 7 **T2IE:** Timer2 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 6 **OC2IE:** Output Compare Channel 2 Interrupt Enable bit(1,2)
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 5 **IC2IE:** Input Capture Channel 2 Interrupt Enable bit(1,2)
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **T1IE:** Timer1 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

Note 1: These bits are unimplemented in dsPIC33FJ06GS101/102 devices.
2: These bits are unimplemented in dsPIC33FJ06GS202 devices.

REGISTER 7-12: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0 (CONTINUED)

bit 2 **OC1IE:** Output Compare Channel 1 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 1 **IC1IE:** Input Capture Channel 1 Interrupt Enable bit(1)
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 0 **INT0IE:** External Interrupt 0 Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

Note 1: These bits are unimplemented in dsPIC33FJ06GS101/102 devices.
2: These bits are unimplemented in dsPIC33FJ06GS202 devices.

REGISTER 7-13: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	INT2IE	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT1IE	CNIE	AC1IE(1)	MI2C1IE	SI2C1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **INT2IE:** External Interrupt 2 Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 12-5 **Unimplemented:** Read as ‘0’

bit 4 **INT1IE:** External Interrupt 1 Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 3 **CNIE:** Input Change Notification Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 2 **AC1IE:** Analog Comparator 1 Interrupt Enable bit(1)
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 1 **MI2C1IE:** I2C1 Master Events Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 0 **SI2C1IE:** I2C1 Slave Events Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

Note 1: This bit is not implemented in dsPIC33FJ06GS101/102 and dsPIC33FJ16GS402/404 devices.

REGISTER 7-14: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	PSEMIE	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **PSEMIE:** PWM Special Event Match Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 8-0 **Unimplemented:** Read as '0'

REGISTER 7-15: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	U1EIE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **U1EIE:** UART1 Error Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 7-16: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
PWM2IE[1]	PWM1IE	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PWM2IE:** PWM2 Interrupt Enable bit[1]
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **PWM1IE:** PWM1 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13-0 **Unimplemented:** Read as ‘0’

Note 1: This bit is unimplemented in dsPIC33FJ06GS101/102 devices.

REGISTER 7-17: IEC6: INTERRUPT ENABLE CONTROL REGISTER 6

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
ADCP1IE	ADCP0IE	—	—	—	—	AC4IE(1,2)	AC3IE(1,2)
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
AC2IE(2)	—	—	—	—	—	PWM4IE(1,3)	PWM3IE(4)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ADCP1IE:** ADC Pair 1 Conversion Done Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **ADCP0IE:** ADC Pair 0 Conversion Done Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13-10 **Unimplemented:** Read as ‘0

bit 9 **AC4IE:** Analog Comparator 4 Interrupt Enable bit(1,2)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 8 **AC3IE:** Analog Comparator 3 Interrupt Enable bit(1,2)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7 **AC2IE:** Analog Comparator 2 Interrupt Enable bit(2)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6-2 **Unimplemented:** Read as ‘0’

bit 1 **PWM4IE:** PWM4 Interrupt Enable bit(1,3)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **PWM3IE:** PWM3 Interrupt Enable bit(4)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

Note 1: These bits are unimplemented in dsPIC33FJ06GS202 devices.
2: These bits are unimplemented in dsPIC33FJ06GS101 and dsPIC33FJ16GS502 devices.
3: These bits are unimplemented in dsPIC33FJ16GS402/404/502 devices.
4: These bits are unimplemented in dsPIC33FJ06101/102/202 devices.

REGISTER 7-18: IEC7: INTERRUPT ENABLE CONTROL REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	ADCP6IE(3)	ADCP5IE(1)	ADCP4IE(1)	ADCP3IE(2)	ADCP2IE(3)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4 **ADCP6IE:** ADC Pair 6 Conversion Done Interrupt Enable bit(3)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit **ADCP5IE:** ADC Pair 5 Conversion Done Interrupt Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit **ADCP4IE:** ADC Pair 4 Conversion Done Interrupt Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit **ADCP3IE:** ADC Pair 3 Conversion Done Interrupt Enable bit(2)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit **ADCP2IE:** ADC Pair 2 Conversion Done Interrupt Enable bit(3)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

Note 1: These bits are not implemented in dsPIC33FJ06GS101/102/202 and dsPIC33FJ16GS402/402/502 devices.

2: This bit is not implemented in dsPIC33FJ06GS102/202 devices.

3: This bit is not implemented in dsPIC33FJ06GS101 devices.

REGISTER 7-19: IPC0: INTERRUPT PRIORITY CONTROL REGISTER 0

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T1IP<2:0>			—	OC1IP<2:0>		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC1IP<2:0>(1)			—	INT0IP<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **T1IP<2:0>:** Timer1 Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **OC1IP<2:0>:** Output Compare Channel 1 Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **IC1IP<2:0>:** Input Capture Channel 1 Interrupt Priority bits(1)
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **INT0IP<2:0>:** External Interrupt 0 Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

Note 1: These bits are unimplemented in dsPIC33FJ06GS101/102 devices.

REGISTER 7-20: IPC1: INTERRUPT PRIORITY CONTROL REGISTER 1

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T2IP<2:0>			—	OC2IP<2:0>(1)		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	IC2IP<2:0>(1,2)			—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **T2IP<2:0>:** Timer2 Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **OC2IP<2:0>:** Output Compare Channel 2 Interrupt Priority bits(1)
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **IC2IP<2:0>:** Input Capture Channel 2 Interrupt Priority bits(1,2)
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

Note 1: These bits are not implemented in dsPIC33FJ06GS101/202 devices.
2: These bits are not implemented in dsPIC33FJ06GS102 devices.

REGISTER 7-21: IPC2: INTERRUPT PRIORITY CONTROL REGISTER 2

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U1RXIP<2:0>			—	SPI1IP<2:0>		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI1EIP<2:0>			—	T3IP<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U1RXIP<2:0>:** UART1 Receiver Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **SPI1IP<2:0>:** SPI1 Event Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SPI1EIP<2:0>:** SPI1 Error Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **T3IP<2:0>:** Timer3 Interrupt Priority bits(1)
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

Note 1: These bits are not implemented in dsPIC33FJ06GS101/102/202 devices.

REGISTER 7-22: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	ADIP<2:0>			—	U1TXIP<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **ADIP<2:0>:** ADC1 Conversion Complete Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **U1TXIP<2:0>:** UART1 Transmitter Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

REGISTER 7-23: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP<2:0>			—	AC1IP<2:0>(1)		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	MI2C1IP<2:0>			—	SI2C1IP<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **CNIP<2:0>:** Change Notification Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **AC1IP<2:0>:** Analog Comparator 1 Interrupt Priority bits(1)
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MI2C1IP<2:0>:** I2C1 Master Events Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **SI2C1IP<2:0>:** I2C1 Slave Events Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

Note 1: These bits are not implemented in dsPIC33FJ06GS101/102 and dsPIC33FJ16GS402/404 devices.

REGISTER 7-24: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT1IP<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **INT1IP<2:0>:** External Interrupt 1 Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

REGISTER 7-25: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

U-0	U-1	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	INT2IP<2:0>			—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **INT2IP<2:0>:** External Interrupt 2 Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 7-26: IPC14: INTERRUPT PRIORITY CONTROL REGISTER 14

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	PSEMIP<2:0>			—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **PSEMIP<2:0>:** PWM Special Event Match Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 7-27: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U1EIP<2:0>			—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **U1EIP<2:0>:** UART1 Error Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 7-28: IPC23: INTERRUPT PRIORITY CONTROL REGISTER 23

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	PWM2IP(1)			—	PWM1IP<2:0>		
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **PWM2IP<2:0>:** PWM2 Interrupt Priority bits(1)
111 = Interrupt is priority 7 (highest priority)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **PWM1IP<2:0>:** PWM1 Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7-0 **Unimplemented:** Read as '0'

Note 1: These bits are not implemented in dsPIC33FJ06GS101/102 devices.

REGISTER 7-29: IPC24: INTERRUPT PRIORITY CONTROL REGISTER 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	PWM4IP(1)			—	PWM3IP<2:0>(2)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **PWM4IP<2:0>:** PWM4 Interrupt Priority bits(1)

`111` = Interrupt is priority 7 (highest priority)
•
•
•
`001` = Interrupt is priority 1
`000` = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **PWM3IP<2:0>:** PWM3 Interrupt Priority bits(2)

`111` = Interrupt is priority 7 (highest priority)
•
•
•
`001` = Interrupt is priority 1
`000` = Interrupt source is disabled

Note 1: These bits are not implemented in dsPIC33FJ06GS202 and dsPIC33FJ16GS402/404 devices.

2: These bits are not implemented in dsPIC33FJ06101/102/202 devices.

REGISTER 7-30: IPC25: INTERRUPT PRIORITY CONTROL REGISTER 25

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	AC2IP<2:0>(1)			—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **AC2IP<2:0>:** Analog Comparator 2 Interrupt Priority bits(1)
111 = Interrupt is priority 7 (highest priority)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11-01 **Unimplemented:** Read as ‘0’

Note 1: These bits are not implemented in dsPIC33FJ06GS101/102 and dsPIC33FJ16GS402/404 devices.

REGISTER 7-31: IPC26: INTERRUPT PRIORITY CONTROL REGISTER 26

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	AC4IP<2:0>(1)			—	AC3IP<2:0>(1,2)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **AC4IP<2:0>:** Analog Comparator 4 Interrupt Priority bits(1)
`111` = Interrupt is priority 7 (highest priority)
•
•
•
`001` = Interrupt is priority 1
`000` = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **AC3IP<2:0>:** Analog Comparator 3 Interrupt Priority bits(1,2)
`111` = Interrupt is priority 7 (highest priority)
•
•
•
`001` = Interrupt is priority 1
`000` = Interrupt source is disabled

Note 1: These bits are not implemented in dsPIC33FJ06GS202 and dsPIC33FJ16GS402/404 devices.
2: These bits are not implemented in dsPIC33FJ06GS101/102 devices.

REGISTER 7-32: IPC27: INTERRUPT PRIORITY CONTROL REGISTER 27

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	ADCP1IP<2:0>			—	ADCP0IP<2:0>		
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **ADCP1IP<2:0>:** ADC Pair 1 Conversion Done Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **ADCP0IP<2:0>:** ADC Pair 0 Conversion Done Interrupt Priority bits(1)
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 7-33: IPC28: INTERRUPT PRIORITY CONTROL REGISTER 28

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	ADCP5IP<2:0>(4)			—	ADCP4IP<2:0>(4)		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	ADCP3IP<2:0>(2,3)			—	ADCP2IP<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **ADCP5IP<2:0>:** ADC Pair 5 Conversion Done Interrupt Priority bits(4)
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **ADCP4IP<2:0>:** ADC Pair 4 Conversion Done Interrupt Priority bits(4)
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **ADCP3IP<2:0>:** ADC Pair 3 Conversion Done Interrupt Priority bits(2,3)
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **ADCP2IP<2:0>:** ADC Pair 2 Conversion Done Interrupt Priority bits(1)
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

Note 1: These bits are not implemented in dsPIC33FJ06GS101 devices.
2: These bits are not implemented in dsPIC33FJ06GS102 devices.
3: These bits are not implemented in dsPIC33FJ06GS202 devices.
4: These bits are implemented in dsPIC33FJ16GS504 devices only.

REGISTER 7-34: IPC29: INTERRUPT PRIORITY CONTROL REGISTER 29

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	ADCP6IP<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **ADCP6IP<2:0>:** ADC Pair 6 Conversion Done Interrupt 1 Priority bits(1)
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

Note 1: These bits are not implemented in dsPIC33FJ06GS202 devices.

REGISTER 7-35: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ILR<3:0>			
bit 15							bit 8

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	VECNUM<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-8 **ILR<3:0>:** New CPU Interrupt Priority Level bits
1111 = CPU Interrupt Priority Level is 15
•
•
•
0001 = CPU Interrupt Priority Level is 1
0000 = CPU Interrupt Priority Level is 0

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **VECNUM<6:0>:** Vector Number of Pending Interrupt bits
0111111 = Interrupt vector pending is number 135
•
•
•
0000001 = Interrupt vector pending is number 9
0000000 = Interrupt vector pending is number 8

7.4 Interrupt Setup Procedures

7.4.1 INITIALIZATION

Complete the following steps to configure an interrupt source at initialization:

1. Set the NSTDIS bit (INTCON1<15>) if nested interrupts are not desired.
2. Select the user-assigned priority level for the interrupt source by writing the control bits in the appropriate IPCx register. The priority level will depend on the specific application and type of interrupt source. If multiple priority levels are not desired, the IPCx register control bits for all enabled interrupt sources can be programmed to the same non-zero value.

Note:	At a device Reset, the IPCx registers are initialized such that all user interrupt sources are assigned to priority level 4.

3. Clear the interrupt flag status bit associated with the peripheral in the associated IFSx register.
4. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate IECx register.

7.4.2 INTERRUPT SERVICE ROUTINE

The method used to declare an ISR and initialize the IVT with the correct vector address depends on the programming language (C or assembler) and the language development toolsuite used to develop the application.

In general, the user application must clear the interrupt flag in the appropriate IFSx register for the source of interrupt that the ISR handles. Otherwise, program will re-enter the ISR immediately after exiting the routine. If the ISR is coded in assembly language, it must be terminated using a `RETFIE` instruction to unstack the saved PC value, SRL value and old CPU priority level.

7.4.3 TRAP SERVICE ROUTINE

A Trap Service Routine (TSR) is coded like an ISR, except that the appropriate trap status flag in the INTCON1 register must be cleared to avoid re-entry into the TSR.

7.4.4 INTERRUPT DISABLE

The following steps outline the procedure to disable all user interrupts:

1. Push the current SR value onto the software stack using the `PUSH` instruction.
2. Force the CPU to priority level 7 by inclusive ORing the value EOh with SRL.

To enable user interrupts, the `POP` instruction can be used to restore the previous SR value.

Note:	Only user interrupts with a priority level of 7 or lower can be disabled. Trap sources (level 8-level 15) cannot be disabled.

The `DISI` instruction provides a convenient way to disable interrupts of priority levels 1-6 for a fixed period of time. Level 7 interrupt sources are not disabled by the `DISI` instruction.

NOTES:

8.0 OSCILLATOR CONFIGURATION

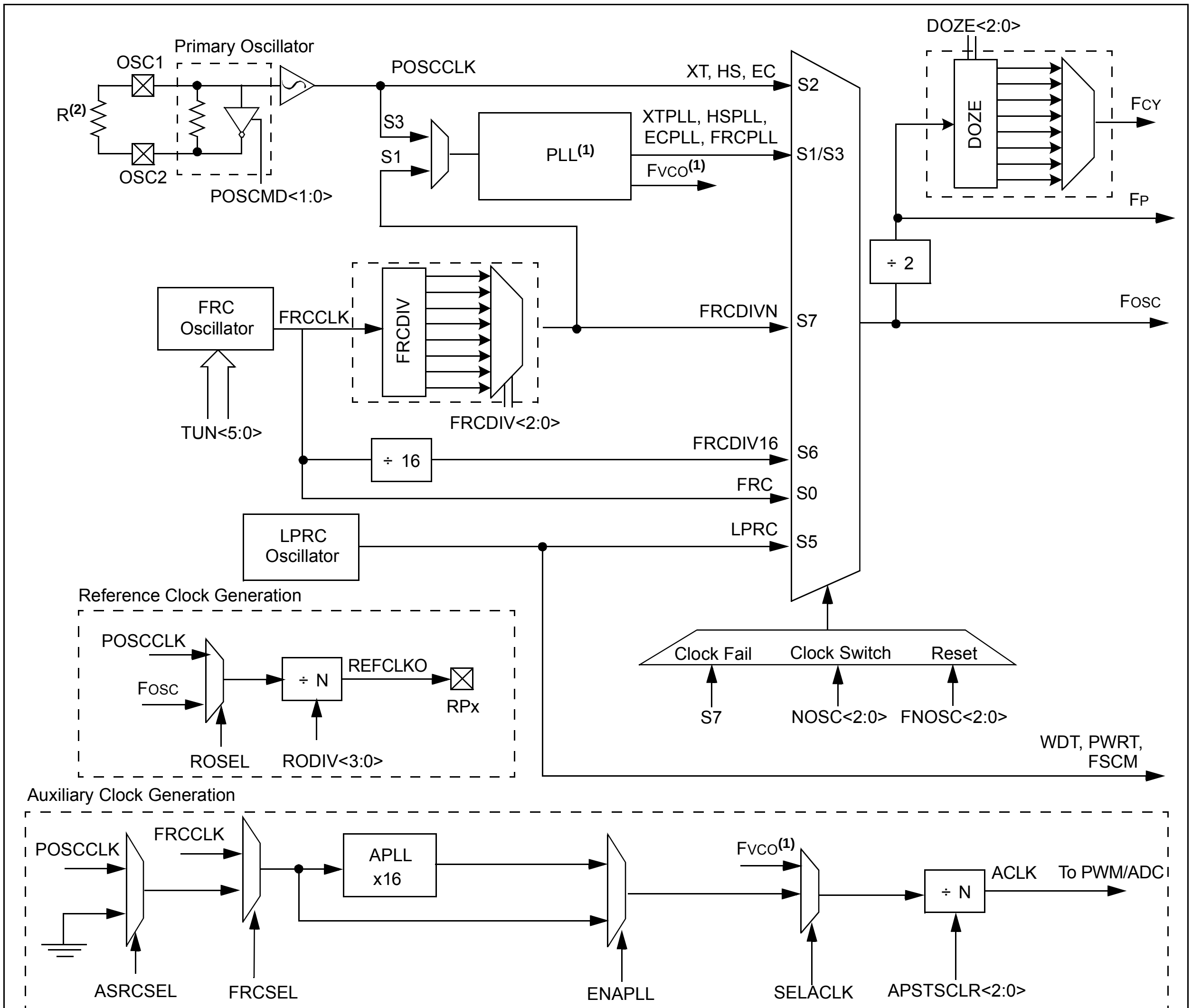
Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*, **Section 42. "Oscillator (Part IV)"** (DS70307), which is available from the Microchip web site (www.microchip.com).

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 oscillator system provides:

- External and internal oscillator options as clock sources
- An on-chip Phase-Locked Loop (PLL) to scale the internal operating frequency to the required system clock frequency
- An internal FRC oscillator that can also be used with the PLL, thereby allowing full-speed operation without any external clock generation hardware
- Clock switching between various clock sources
- Programmable clock postscaler for system power savings
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and takes fail-safe measures
- A Clock Control register (OSCCON)
- Nonvolatile Configuration bits for main oscillator selection.
- Auxiliary PLL for ADC and PWM

A simplified diagram of the oscillator system is shown in Figure 8-1.

FIGURE 8-1: dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 OSCILLATOR SYSTEM DIAGRAM



Note 1: See **Section 8.1.3 "PLL Configuration"** and **Section 8.2 "Auxiliary Clock Generation"** for FVCO values.

2: If the Oscillator is used with XT or HS modes, an external parallel resistor with the value of 1 MΩ must be connected.

8.1 CPU Clocking System

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices provide six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with PLL
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator
- FRC Oscillator with Postscaler

8.1.1 SYSTEM CLOCK SOURCES

The Fast RC (FRC) internal oscillator runs at a nominal frequency of 7.37 MHz. User software can tune the FRC frequency. User software can optionally specify a factor (ranging from 1:2 to 1:256) by which the FRC clock frequency is divided. This factor is selected using the FRCDIV<2:0> (CLKDIV<10:8>) bits.

The primary oscillator can use one of the following as its clock source:

- XT (Crystal): Crystals and ceramic resonators in the range of 3 MHz to 10 MHz. The crystal is connected to the OSC1 and OSC2 pins.
- HS (High-Speed Crystal): Crystals in the range of 10 MHz to 40 MHz. The crystal is connected to the OSC1 and OSC2 pins.
- EC (External Clock): The external clock signal is directly applied to the OSC1 pin.

The LPRC internal oscIllator runs at a nominal frequency of 32.768 kHz. It is also used as a reference clock by the Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The clock signals generated by the FRC and primary oscillators can be optionally applied to an on-chip Phase-Locked Loop (PLL) to provide a wide range of output frequencies for device operation. PLL configuration is described in **Section 8.1.3 “PLL Configuration”**.

The FRC frequency depends on the FRC accuracy (see Table 24-20) and the value of the FRC Oscillator Tuning register (see Register 8-4).

8.1.2 SYSTEM CLOCK SELECTION

The oscillator source used at a device Power-on Reset event is selected using Configuration bit settings. The oscillator Configuration bit settings are located in the Configuration registers in the program memory. (Refer to **Section 21.1 “Configuration Bits”** for further details.) The Initial Oscillator Selection Configuration bits, FNOSC<2:0> (FOSCSEL<2:0>), and the Primary Oscillator Mode Select Configuration bits, POSCMD<1:0> (FOSC<1:0>), select the oscillator source that is used at a Power-on Reset. The FRC primary oscillator is the default (unprogrammed) selection.

The Configuration bits allow users to choose among 12 different clock modes, shown in Table 8-1.

The output of the oscillator (or the output of the PLL if a PLL mode has been selected), FOSC, is divided by 2 to generate the device instruction clock (FCY) and the peripheral clock time base (FP). FCY defines the operating speed of the device and speeds up to 40 MHz are supported by the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 architecture.

Instruction execution speed or device operating frequency, FCY, is given by Equation 8-1.

EQUATION 8-1: DEVICE OPERATING FREQUENCY

$$F_{CY} = F_{OSC}/2$$

TABLE 8-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	Note
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	**1, 2**
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	**1**
Low-Power RC Oscillator (LPRC)	Internal	xx	101	**1**
Reserved	Reserved	xx	100	—
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	—
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	—
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	**1**
Primary Oscillator (HS)	Primary	10	010	—
Primary Oscillator (XT)	Primary	01	010	—
Primary Oscillator (EC)	Primary	00	010	**1**
Fast RC Oscillator with PLL (FRCPLL)	Internal	xx	001	**1**
Fast RC Oscillator (FRC)	Internal	xx	000	**1**

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.
2: This is the default oscillator mode for an unprogrammed (erased) device.

8.1.3 PLL CONFIGURATION

The primary oscillator and internal FRC oscillator can optionally use an on-chip PLL to obtain higher speeds of operation. The PLL provides significant flexibility in selecting the device operating speed. A block diagram of the PLL is shown in Figure 8-2.

The output of the primary oscillator or FRC, denoted as 'FIN', is divided down by a prescale factor (N1) of 2, 3, ... or 33 before being provided to the PLL's Voltage Controlled Oscillator (VCO). The input to the VCO must be selected in the range of 0.8 MHz to 8 MHz. The prescale factor 'N1' is selected using the PLLPRE<4:0> bits (CLKDIV<4:0>).

The PLL Feedback Divisor, selected using the PLLDIV<8:0> bits (PLLFBD<8:0>), provides a factor, 'M', by which the input to the VCO is multiplied. This factor must be selected such that the resulting VCO output frequency is in the range of 100 MHz to 200 MHz.

The VCO output is further divided by a postscale factor, 'N2'. This factor is selected using the PLLPOST<1:0> bits (CLKDIV<7:6>). 'N2' can be either 2, 4, or 8, and must be selected such that the PLL output frequency (FOSC) is in the range of 12.5 MHz to 80 MHz, which generates device operating speeds of 6.25-40 MIPS.

For a primary oscillator or FRC oscillator, output 'FIN', the PLL output 'FOSC' is given by Equation 8-2.

EQUATION 8-2: FOSC CALCULATION

$$F_{OSC} = F_{IN} * \left(\frac{M}{N1*N2}\right)$$

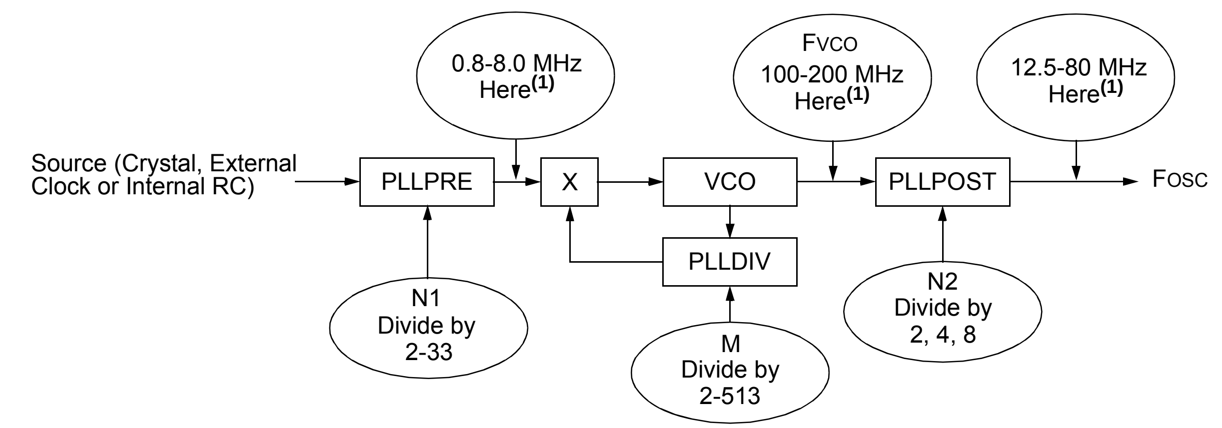
For example, suppose a 10 MHz crystal is being used with the selected oscillator mode of XT with PLL (see Equation 8-3).

- If PLLPRE<4:0> = 0, then N1 = 2. This yields a VCO input of 10/2 = 5 MHz, which is within the acceptable range of 0.8-8 MHz.
- If PLLDIV<8:0> = 0x1E, then M = 32. This yields a VCO output of 5 x 32 = 160 MHz, which is within the 100-200 MHz ranged needed.
- If PLLPOST<1:0> = 0, then N2 = 2. This provides a Fosc of 160/2 = 80 MHz. The resultant device operating speed is 80/2 = 40 MIPS.

EQUATION 8-3: XT WITH PLL MODE EXAMPLE

$$F_{CY} = \frac{F_{OSC}}{2} = \frac{1}{2}\left(\frac{10000000 * 32}{2 * 2}\right) = 40 \text{ MIPS}$$

FIGURE 8-2: dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 PLL BLOCK DIAGRAM



Note 1: This frequency range must be satisfied at all times.

8.2 Auxiliary Clock Generation

The auxiliary clock generation is used for a peripherals that need to operate at a frequency unrelated to the system clock such as a PWM or ADC.

Note:	To achieve 1.04 ns PWM resolution, the auxiliary clock must be set up for 120 MHz.

The primary oscillator and internal FRC oscillator sources can be used with an auxiliary PLL to obtain the auxiliary clock. The auxiliary PLL has a fixed 16x multiplication factor.

Note:	If the primary PLL is used as a source for the auxiliary clock, then the primary PLL should be configured up to a maximum operation of 30 MIPS or less.

8.3 Reference Clock Generation

The reference clock output logic provides the user with the ability to output a clock signal based on the system clock or the crystal oscillator on a device pin. The user application can specify a wide range of clock scaling prior to outputting the reference clock.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER[1]

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC<2:0>			—	NOSC<2:0>[2]		
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/C-0	U-0	U-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF	—	—	OSWEN
bit 7							bit 0

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)
- 000 = Fast RC oscillator (FRC)
- 001 = Fast RC oscillator (FRC) with PLL
- 010 = Primary oscillator (XT, HS, EC)
- 011 = Primary oscillator (XT, HS, EC) with PLL
- 100 = Reserved
- 101 = Low-Power RC oscillator (LPRC)
- 110 = Fast RC oscillator (FRC) with divide-by-16
- 111 = Fast RC oscillator (FRC) with divide-by-n

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits[2]
- 000 = Fast RC oscillator (FRC)
- 001 = Fast RC oscillator (FRC) with PLL
- 010 = Primary oscillator (XT, HS, EC)
- 011 = Primary oscillator (XT, HS, EC) with PLL
- 100 = Reserved
- 101 = Low-Power RC oscillator (LPRC)
- 110 = Fast RC oscillator (FRC) with divide-by-16
- 111 = Fast RC oscillator (FRC) with divide-by-n

bit 7 **CLKLOCK:** Clock Lock Enable bit

If clock switching is enabled and FSCM is disabled, (FOSC<FCKSM> = 0b01):
- 1 = Clock switching is disabled, system clock source is locked
- 0 = Clock switching is enabled, system clock source can be modified by clock switching

bit 6 **IOLOCK:** Peripheral Pin Select Lock bit
- 1 = Peripherial pin select is locked, write to Peripheral Pin Select registers not allowed
- 0 = Peripherial pin select is not locked, write to Peripheral Pin Select registers allowed

bit 5 **LOCK:** PLL Lock Status bit (read-only)
- 1 = Indicates that PLL is in lock, or PLL start-up timer is satisfied
- 0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

bit 4 **Unimplemented:** Read as ‘0’

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. “Oscillator (Part IV)”** (DS70307) in the *“dsPIC33F Family Reference Manual”* (available from the Microchip website) for details.

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER(1) (CONTINUED)

bit 3	**CF:** Clock Fail Detect bit (read/clear by application) 1 = FSCM has detected clock failure 0 = FSCM has not detected clock failure
bit 2-1	**Unimplemented:** Read as '0'
bit 0	**OSWEN:** Oscillator Switch Enable bit 1 = Request oscillator switch to selection specified by NOSC<2:0> bits 0 = Oscillator switch is complete

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillator (Part IV)"** (DS70307) in the *"dsPIC33F Family Reference Manual"* (available from the Microchip website) for details.

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

REGISTER 8-2: CLKDIV: CLOCK DIVISOR REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE<2:0>			DOZEN(1)	FRCDIV<2:0>		
bit 15							bit 8

R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPOST<1:0>		—	PLLPRE<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts will clear the DOZEN bit and the processor clock/peripheral clock ratio is set to 1:1
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** Processor Clock Reduction Select bits
000 = FCY/1
001 = FCY/2
010 = FCY/4
011 = FCY/8 (default)
100 = FCY/16
101 = FCY/32
110 = FCY/64
111 = FCY/128

bit 11 **DOZEN:** Doze Mode Enable bit(1)
1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks
0 = Processor clock/peripheral clock ratio forced to 1:1

bit 10-8 **FRCDIV<2:0>:** Internal Fast RC Oscillator Postscaler bits
000 = FRC divide by 1 (default)
001 = FRC divide by 2
010 = FRC divide by 4
011 = FRC divide by 8
100 = FRC divide by 16
101 = FRC divide by 32
110 = FRC divide by 64
111 = FRC divide by 256

bit 7-6 **PLLPOST<1:0>:** PLL VCO Output Divider Select bits (also denoted as ‘N2’, PLL postscaler)
00 = Output/2
01 = Output/4 (default)
10 = Reserved
11 = Output/8

bit 5 **Unimplemented:** Read as ‘0’

bit 4-0 **PLLPRE<4:0>:** PLL Phase Detector Input Divider bits (also denoted as ‘N1’, PLL prescaler)
00000 = Input/2 (default)
00001 = Input/3
•
•
•
11111 = Input/33

Note 1: This bit is cleared when the ROI bit is set and an interrupt occurs.

REGISTER 8-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PLLDIV<8>
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as ‘0’

bit 8-0 **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as ‘M’, PLL multiplier)

000000000 = 2
000000001 = 3
000000010 = 4
•
•
•
000110000 = 50 (default)
•
•
•
111111111 = 513

REGISTER 8-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN<5:0>(1)					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

011111 = Center frequency + 11.625% (8.23 MHz)
011110 = Center frequency + 11.25% (8.20 MHz)
•
•
•
000001 = Center frequency + 0.375% (7.40 MHz)
000000 = Center frequency (7.37 MHz nominal)
111111 = Center frequency -0.375% (7.345 MHz)
•
•
•
100001 = Center frequency -11.625% (6.52 MHz)
100000 = Center frequency -12% (6.49 MHz)

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation and is neither characterized nor tested

REGISTER 8-5: ACLKCON: AUXILIARY CLOCK DIVISOR CONTROL REGISTER

R/W-0	R-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
ENAPLL	APLLCK	SELACLK	—	—	APSTSCLR<2:0>		
bit 15							bit 0

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
ASRCSEL	FRCSEL	—	—	—	—	—	—
bit 7							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ENAPLL:** Auxiliary PLL Enable bit
1 = APLL is enabled
0 = APLL is disabled

bit 14 **APLLCK:** APLL Locked Status bit (read-only)
1 = Indicates that auxiliary PLL is in lock
0 = Indicates that auxiliary PLL is not in lock

bit 13 **SELACLK:** Select Auxiliary Clock Source for Auxiliary Clock Divider bit
1 = Auxiliary Oscillators provides the source clock for auxiliary clock divider
0 = Primary PLL (F_{VCO}) provides the source clock for auxiliary clock divider

bit 12-11 **Unimplemented:** Read as ‘0’

bit 10-8 **APSTSCLR<2:0>:** Auxiliary Clock Output Divider bits
111 = Divided by 1
110 = Divided by 2
101 = Divided by 4
100 = Divided by 8
011 = Divided by 16
010 = Divided by 32
001 = Divided by 64
000 = Divided by 256

bit 7 **ASRCSEL:** Select Reference Clock Source for Auxiliary Clock bit
1 = Primary oscillator is the clock source
0 = No clock input is selected

bit 6 **FRCSEL:** Select Reference Clock Source for Auxiliary PLL bit
1 = Select FRC clock for auxiliary PLL
0 = Input clock source is determined by ASRCSEL bit setting

bit 5-0 **Unimplemented:** Read as ‘0’

REGISTER 8-6: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSIDL	ROSEL	RODIV<3:0>(1)			
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ROON:** Reference Oscillator Output Enable bit
1 = Reference oscillator output enabled on REFCLK0(2) pin
0 = Reference oscillator output disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **ROSIDL:** Reference Oscillator Run in Sleep bit
1 = Reference oscillator output continues to run in Sleep
0 = Reference oscillator output is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Oscillator crystal used as the reference clock
0 = System clock used as the reference clock

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divider bits(1)
1111 = Reference clock divided by 32,768
1110 = Reference clock divided by 16,384
1101 = Reference clock divided by 8,192
1100 = Reference clock divided by 4,096
1011 = Reference clock divided by 2,048
1010 = Reference clock divided by 1,024
1001 = Reference clock divided by 512
1000 = Reference clock divided by 256
0111 = Reference clock divided by 128
0110 = Reference clock divided by 64
0101 = Reference clock divided by 32
0100 = Reference clock divided by 16
0011 = Reference clock divided by 8
0010 = Reference clock divided by 4
0001 = Reference clock divided by 2
0000 = Reference clock

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
2: This pin is remappable. Refer to **Section 10.4 “Peripheral Pin Select”** for more information.

8.4 Clock Switching Operation

Applications are free to switch among any of the four clock sources (primary, LP, FRC and LPRC) under software control at any time. To limit the possible side effects of this flexibility, dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices have a safeguard lock built into the switch process.

Note:	Primary oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMD<1:0> Configuration bits. While an application can switch to and from primary oscillator mode in software, it cannot switch among the different primary submodes without reprogramming the device.

8.4.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the Configuration register must be programmed to '0'. (Refer to **Section 21.1 "Configuration Bits"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and Fail-Safe Clock Monitor function are disabled. This is the default setting.

The NOSC control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC bits (OSCCON<14:12>) reflect the clock source selected by the FNOSC Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled. It is held at '0' at all times.

8.4.2 OSCILLATOR SWITCHING SEQUENCE

To perform a clock switch, the following basic sequence is required:

1. If desired, read the COSC bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSC control bits (OSCCON<10:8>) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit (OSCCON<0>) to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically as follows:

1. The clock switching hardware compares the COSC status bits with the new value of the NOSC control bits. If they are the same, the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
2. If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and the CF (OSCCON<3>) status bits are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware waits until the Oscillator Start-up Timer (OST) expires. If the new source is using the PLL, the hardware waits until a PLL lock is detected (LOCK = 1).
4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSC bit values are transferred to the COSC status bits.
6. The old clock source is turned off at this time, with the exception of LPRC (if WDT or FSCM are enabled).

Note 1:	The processor continues to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.
2:	Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
3:	Refer to **Section 42. "Oscillator (Part IV)"** (DS70307) in the *"dsPIC33F Family Reference Manual"* for details.

8.5 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by programming. If the FSCM function is enabled, the LPRC internal oscillator runs at all times (except during Sleep mode) and is not subject to control by the Watchdog Timer.

In the event of an oscillator failure, the FSCM generates a clock failure trap event and switches the system clock over to the FRC oscillator. Then, the application program can either attempt to restart the oscillator or execute a controlled shutdown. The trap can be treated as a warm Reset by simply loading the Reset address into the oscillator fail trap vector.

If the PLL multiplier is used to scale the system clock, the internal FRC is also multiplied by the same factor on clock failure. Essentially, the device switches to FRC with PLL on a clock failure.

NOTES:

9.0 POWER-SAVING FEATURES

> **Note:** This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*, **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70196), which is available from the Microchip web site (www.microchip.com).

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices can manage power consumption in four different ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

9.1 Clock Frequency and Clock Switching

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 8.0 "Oscillator Configuration"**.

9.2 Instruction-Based Power-Saving Modes

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices have two special power-saving modes that are entered through the execution of a special `PWRSAV` instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the `PWRSAV` instruction is shown in Example 9-1.

> **Note:** `SLEEP_MODE` and `IDLE_MODE` are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to wake-up.

9.2.1 SLEEP MODE

The following occur in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals may continue to operate. This includes the items such as the input change notification on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device will wake-up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

EXAMPLE 9-1: `PWRSAV` INSTRUCTION SYNTAX

```
PWRSAV  #SLEEP_MODE    ; Put the device into SLEEP mode
PWRSAV  #IDLE_MODE     ; Put the device into IDLE mode
```

9.2.2 IDLE MODE

The following occur in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 9.4 “Peripheral Module Disable”**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device will wake-up from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution begins immediately, starting with the instruction following the `PWRSAV` instruction, or the first instruction in the ISR.

9.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a `PWRSAV` instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

9.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this may not be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the CAN module has been configured for 500 kbps based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the CAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

9.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers will have no effect and read values will be invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

 Preliminary

REGISTER 9-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	—	T3MD	T2MD	T1MD	—	PWMMD	—
bit 15							bit 8

R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0
I2C1MD	—	U1MD	—	SPI1MD	—	—	ADCMD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **T3MD**: Timer3 Module Disable bit
1 = Timer3 module is disabled
0 = Timer3 module is enabled

bit 12 **T2MD**: Timer2 Module Disable bit
1 = Timer2 module is disabled
0 = Timer2 module is enabled

bit 11 **T1MD**: Timer1 Module Disable bit
1 = Timer1 module is disabled
0 = Timer1 module is enabled

bit 10 **Unimplemented:** Read as ‘0’

bit 9 **PWMMD**: PWM Module Disable bit
1 = PWM module is disabled
0 = PWM module is enabled

bit 8 **Unimplemented:** Read as ‘0’

bit 7 **I2C1MD**: I2C1 Module Disable bit
1 = I2C1 module is disabled
0 = I2C1 module is enabled

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **U1MD**: UART1 Module Disable bit
1 = UART1 module is disabled
0 = UART1 module is enabled

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **SPI1MD**: SPI1 Module Disable bit
1 = SPI1 module is disabled
0 = SPI1 module is enabled

bit 2-1 **Unimplemented:** Read as ‘0’

bit 0 **ADCMD**: ADC Module Disable bit
1 = ADC module is disabled
0 = ADC module is enabled

REGISTER 9-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	IC2MD	IC1MD
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	OC2MD	OC1MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as ‘0’

bit 9 **IC2MD**: Input Capture 2 Module Disable bit
1 = Input Capture 2 module is disabled
0 = Input Capture 2 module is enabled

bit 8 **IC1MD**: Input Capture 1 Module Disable bit
1 = Input Capture 1 module is disabled
0 = Input Capture 1 module is enabled

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **OC2MD**: Output Compare 2 Module Disable bit
1 = Output Compare 2 module is disabled
0 = Output Compare 2 module is enabled

bit 0 **OC1MD**: Output Compare 1 Module Disable bit
1 = Output Compare 1 module is disabled
0 = Output Compare 1 module is enabled

REGISTER 9-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	—	—	—	—	CMPMD	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10 **CMPMD**: Analog Comparator Module Disable bit
1 = Analog comparator module is disabled
0 = Analog comparator module is enabled

bit 9-0 **Unimplemented:** Read as ‘0’

REGISTER 9-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	REFOMD	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **REFOMD**: Reference Clock Generator Module Disable bit
1 = Reference clock generator module is disabled
0 = Reference clock generator module is enabled

bit 2-0 **Unimplemented:** Read as ‘0’

REGISTER 9-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	PWM4MD	PWM3MD	PWM2MD	PWM1MD
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11 **PWM4MD**: PWM Generator 4 Module Disable bit
1 = PWM Generator 4 module is disabled
0 = PWM Generator 4 module is enabled

bit 10 **PWM3MD**: PWM Generator 3 Module Disable bit
1 = PWM Generator 3 module is disabled
0 = PWM Generator 3 module is enabled

bit 9 **PWM2MD**: PWM Generator 2 Module Disable bit
1 = PWM Generator 2 module is disabled
0 = PWM Generator 2 module is enabled

bit 8 **PWM1MD**: PWM Generator 1 Module Disable bit
1 = PWM Generator 1 module is disabled
0 = PWM Generator 1 module is enabled

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 9-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	CMP4MD	CMP3MD	CMP2MD	CMP1MD
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11 **CMP4MD**: Analog Comparator 4 Module Disable bit
1 = Analog Comparator 4 module is disabled
0 = Analog Comparator 4 module is enabled

bit 10 **CMP3MD**: Analog Comparator 3 Module Disable bit
1 = Analog Comparator 3 module is disabled
0 = Analog Comparator 3 module is enabled

bit 9 **CMP2MD**: Analog Comparator 2 Module Disable bit
1 = Analog Comparator 2 module is disabled
0 = Analog Comparator 2 module is enabled

bit 8 **CMP1MD**: Analog Comparator 1 Module Disable bit
1 = Analog Comparator 1 module is disabled
0 = Analog Comparator 1 module is enabled

bit 7-0 **Unimplemented:** Read as ‘0’

NOTES:

10.0 I/O PORTS

Note: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*, **Section 10. "I/O Ports"** (DS70193), which is available on Microchip web site (www.microchip.com).

All of the device pins (except VDD, VSS, $\overline{MCLR}$ and OSC1/CLKI) are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

10.1 Parallel I/O (PIO) Ports

Generally a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 10-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected.

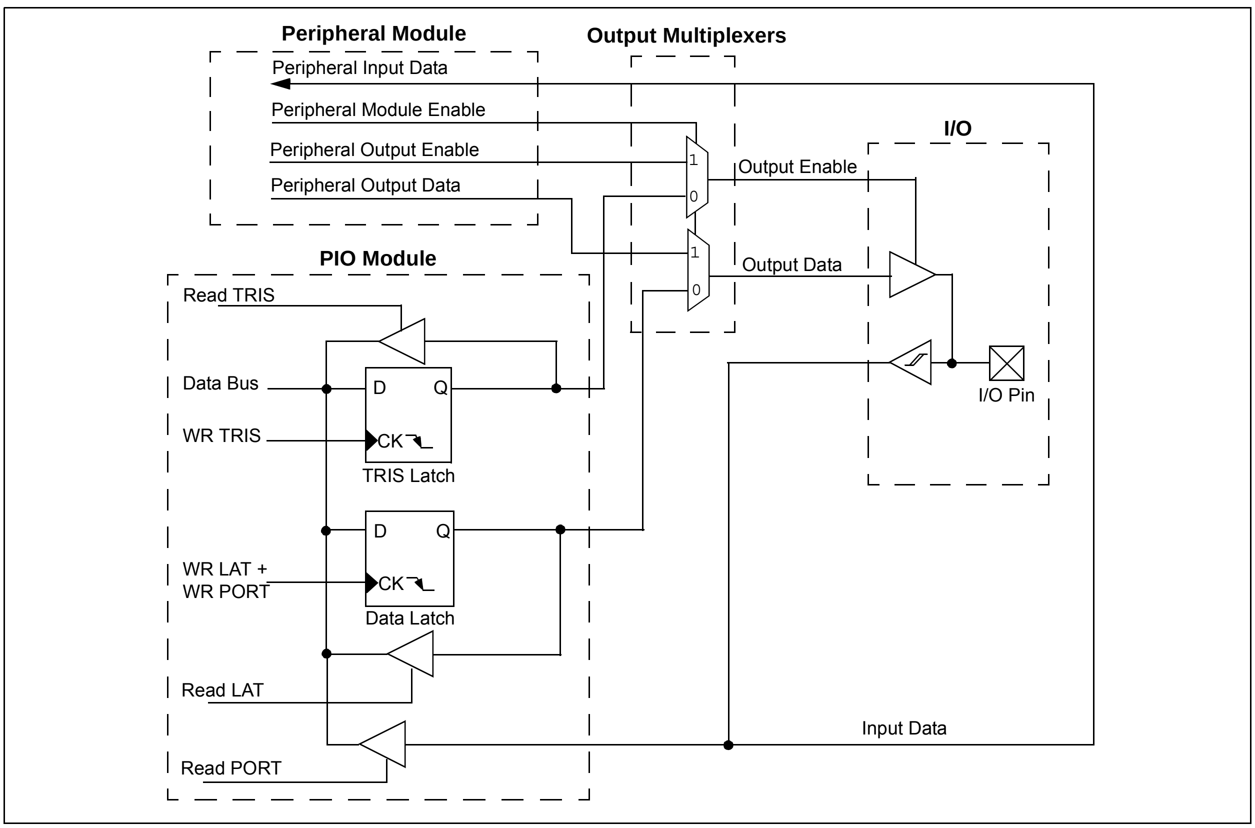
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

FIGURE 10-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



10.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, some digital-only port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (for example, 5V) on any desired digital only pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

Refer to **"Pin Diagrams"** for the available pins and their functionality.

10.2 Configuring Analog Port Pins

The ADPCFG and TRIS registers control the operation of the Analog-to-Digital (A/D) port pins. The port pins that are to function as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The ADPCFG register has a default value of 0x0000; therefore, all pins that share ANx functions are analog (not digital) by default.

When the PORT register is read, all pins configured as analog input channels will read as cleared (a low level).

Pins configured as digital inputs will not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

10.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a `NOP`. An example is shown in Example 10-1.

10.3 Input Change Notification

The input change notification function of the I/O ports allows the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices to generate interrupt requests to the processor in response to a Change-Of-State (COS) on selected input pins. This feature can detect input Change-Of-States even in Sleep mode, when the clocks are disabled. Depending on the device pin count, up to 30 external signals (CNx pin) can be selected (enabled) for generating an interrupt request on a Change-Of-State.

Four control registers are associated with the CN module. The CNEN1 and CNEN2 registers contain the interrupt enable control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up connected to it. The pull-ups act as a current source connected to the pin, and eliminate the need for external resistors when the push button or keypad devices are connected. The pull-ups are enabled separately using the CNPU1 and CNPU2 registers, which contain the control bits for each of the CN pins. Setting any of the control bits enables the weak pull-ups for the corresponding pins.

Note:	Pull-ups on change notification pins should always be disabled when the port pin is configured as a digital output.

EQUATION 10-1: PORT WRITE/READ EXAMPLE

```
MOV   0xFF00, W0          ; Configure PORTB<15:8> as inputs
MOV   W0, TRISBB          ; and PORTB<7:0> as outputs
NOP                       ; Delay 1 cycle
BTSS  PORTB, #13          ; Next Instruction
```


10.4 Peripheral Pin Select

Peripheral pin select configuration enables peripheral set selection and placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, programmers can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The peripheral pin select configuration feature operates over a fixed subset of digital I/O pins. Programmers can independently map the input and/or output of most digital peripherals to any one of these I/O pins. Peripheral pin select is performed in software, and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping, once it has been established.

10.4.1 AVAILABLE PINS

The peripheral pin select feature is used with a range of up to 30 pins. The number of available pins depends on the particular device and its pin count. Pins that support the peripheral pin select feature include the designation “RPn” in their full pin designation, where “RP” designates a remappable peripheral and “n” is the remappable pin number.

10.4.2 CONTROLLING PERIPHERAL PIN SELECT

Peripheral pin select features are controlled through two sets of Special Function Registers: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

10.4.2.1 Input Mapping

The inputs of the peripheral pin select options are mapped on the basis of the peripheral. A control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 10-1 through Register 10-14). Each register contains sets of 6-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral’s bit field with an appropriate 6-bit value maps the RPn pin with that value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of peripheral pin selections supported by the device.

Figure 10-2 Illustrates remappable pin selection for U1RX input.

Note:	For input mapping only, the Peripheral Pin Select (PPS) functionality does not have priority over the TRISx settings. Therefore, when configuring the RPx pin for input, the corresponding bit in the TRISx register must also be configured for input (i.e., set to ‘1’).

FIGURE 10-2: REMAPPABLE MUX INPUT FOR U1RX

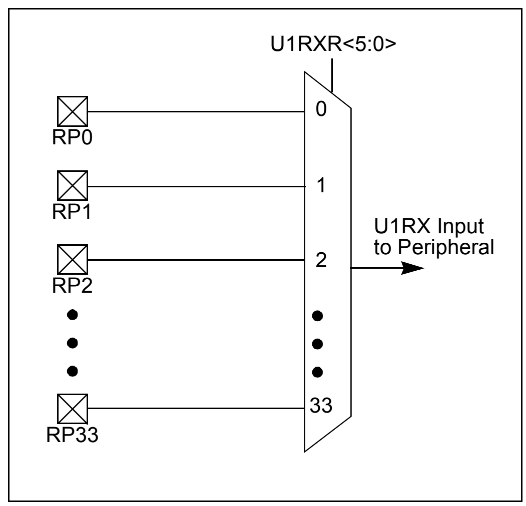


TABLE 10-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<5:0>
External Interrupt 2	INT2	RPINR1	INT2R<5:0>
Timer1 External Clock	T1CK	RPINR2	T1CKR<5:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<5:0>
Timer3 External Clock	T3CK	RPINR3	T3CKR<5:0>
Input Capture 1	IC1	RPINR7	IC1R<5:0>
Input Capture 2	IC2	RPINR7	IC2R<5:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<5:0>
UART1 Receive	U1RX	RPINR18	U1RXR<5:0>
UART1 Clear To Send	$\overline{\text{U1CTS}}$	RPINR18	U1CTSR<5:0>
SPI Data Input 1	SDI1	RPINR20	SDI1R<5:0>
SPI Clock Input 1	SCK1	RPINR20	SCK1R<5:0>
SPI Slave Select Input 1	$\overline{\text{SS1}}$	RPINR21	SS1R<5:0>
PWM Fault Input PWM1	FLT1	RPINR29	FLT1R<5:0>
PWM Fault Input PWM2	FLT2	RPINR30	FLT2R<5:0>
PWM Fault Input PWM3	FLT3	RPINR30	FLT3R<5:0>
PWM Fault Input PWM4	FLT4	RPINR31	FLT4R<5:0>
PWM Fault Input PWM5	FLT5	RPINR31	FLT5R<5:0>
PWM Fault Input PWM6	FLT6	RPINR32	FLT6R<5:0>
PWM Fault Input PWM7	FLT7	RPINR32	FLT7R<5:0>
PWM Fault Input PWM8	FLT8	RPINR33	FLT8R<5:0>
External Synchronization signal to PWM Master Time Base	SYNCI1	RPINR33	SYNCI1R<5:0>
External Synchronization signal to PWM Master Time Base	SYNCI2	RPINR34	SYNCI2R<5:0>

10.4.2.2 Output Mapping

In contrast to inputs, the outputs of the peripheral pin select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 10-15 through Register 10-31). The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 10-2 and Figure 10-3).

The list of peripherals for output mapping also includes a null value of '`00000`' because of the mapping technique. This permits any given pin to remain unconnected from the output of any of the pin selectable peripherals.

FIGURE 10-3: MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPn

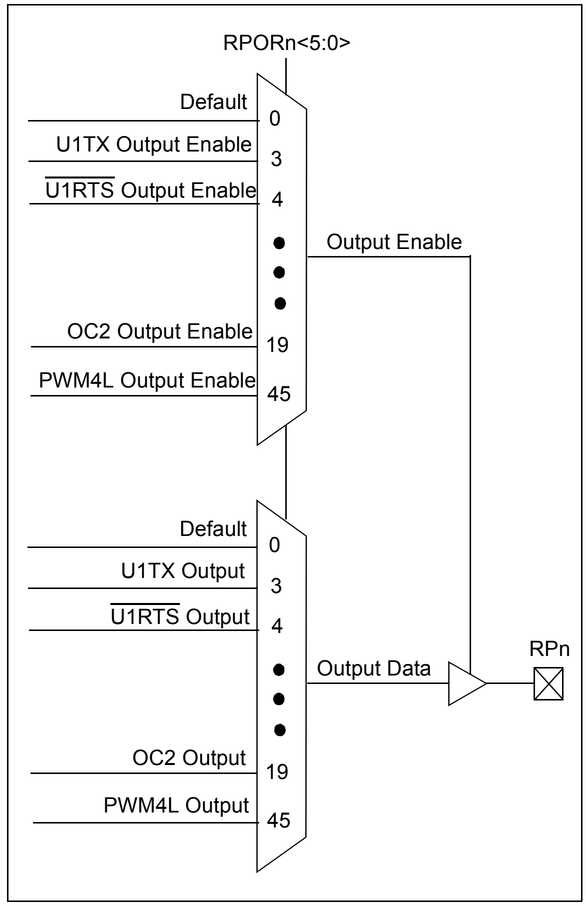


TABLE 10-2: OUTPUT SELECTION FOR REMAPPABLE PIN (RPn)

Function	RPORn<5:0>	Output Name
NULL	`000000`	RPn tied to default port pin
U1TX	`000011`	RPn tied to UART1 transmit
$\overline{\text{U1RTS}}$	`000100`	RPn tied to UART1 ready to send
SDO1	`000111`	RPn tied to SPI1 data output
SCK1	`001000`	RPn tied to SPI1 clock output
$\overline{\text{SS1}}$	`001001`	RPn tied to SPI1 slave select output
OC1	`010010`	RPn tied to Output Compare 1
OC2	`010011`	RPn tied to Output Compare 2
SYNCO1	`100101`	RPn tied to external device synchronization signal via PWM master time base
REFCLKO	`100110`	REFCLK output signal
ACMP1	`100111`	RPn tied to Analog Comparator Output 1
ACMP2	`101000`	RPn tied to Analog Comparator Output 2
ACMP3	`101001`	RPn tied to Analog Comparator Output 3
ACMP4	`101010`	RPn tied to Analog Comparator Output 4
PWM4H	`101100`	RPn tied to PWM output pins associated with PWM Generator 4
PWM4L	`101101`	RPn tied to PWM output pins associated with PWM Generator 4

10.4.2.3 Virtual Pins

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices support four virtual RPn pins (RP32, RP33, RP34 and RP35), which are identical in functionality to all other RPn pins, with the exception of pinouts. These four pins are internal to the devices and are not connected to a physical device pin.

These pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example, the output of the analog comparator can be connected to RP32 and the PWM Fault input can be configured for RP32 as well. This configuration allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

10.4.3 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. dsPIC33F devices include three features to prevent alterations to the peripheral map:

- Control register lock sequence
- Continuous state monitoring
- Configuration bit pin select lock

10.4.3.1 Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

1. Write 0x46 to OSCCON<7:0>.
2. Write 0x57 to OSCCON<7:0>.
3. Clear (or set) IOLOCK as a single operation.

> **Note:** MPLAB® C30 provides built-in C language functions for unlocking the OSCCON register:
>
> ```
> __builtin_write_OSCCONL(value)
> __builtin_write_OSCCONH(value)
> ```
>
> See MPLAB C30 Help files for more information.

Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the peripheral pin selects to be configured with a single unlock sequence followed by an update to all control registers, then locked with a second lock sequence.

10.4.3.2 Continuous State Monitoring

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset will be triggered.

10.4.3.3 Configuration Bit Pin Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY (FOSC<5>) Configuration bit blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure will not execute and the Peripheral Pin Select Control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows user applications unlimited access (with the proper use of the unlock sequence) to the Peripheral Pin Select registers.

10.5 Peripheral Pin Select Registers

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices implement 34 registers for remappable peripheral configuration:

- 15 Input Remappable Peripheral Registers
- 19 Output Remappable Peripheral Registers

Note:	Input and output register values can only be changed if OSCCON<IOLOCK> = 0. See **Section 10.4.3.1 “Control Register Lock”** for a specific command sequence.

Not all output remappable peripheral registers are implemented on all devices. See the register description of the specific register for further details.

REGISTER 10-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT1R<5:0>					
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **INT1R<5:0>:** Assign External Interrupt 1 (INTR1) to the Corresponding RPn Pin bits
111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 10-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT2R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **INT2R<5:0>:** Assign External Interrupt 2 (INTR2) to the Corresponding RPn Pin bits

111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

REGISTER 10-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T3CKR<5:0>					
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T2CKR<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **T3CKR<5:0>:** Assign Timer3 External Clock (T3CK) to the Corresponding RPn Pin bits

111111 = Input tied to Vss
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **T2CKR<5:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn Pin bits

111111 = Input tied to Vss
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

REGISTER 10-4: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	IC2R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	IC1R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **IC2R<5:0>:** Assign Input Capture 2 (IC2) to the Corresponding RPn Pin bits
111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **IC1R<5:0>:** Assign Input Capture 1 (IC1) to the Corresponding RPn Pin bits
111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

REGISTER 10-5: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	OCFAR<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **OCFAR<5:0>:** Assign Output Capture A (OCFA) to the Corresponding RPn Pin bits

111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

REGISTER 10-6: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U1CTSR<5:0>					
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U1RXR<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **U1CTSR<5:0>:** Assign UART1 Clear to Send ($\overline{\text{U1CTS}}$) to the Corresponding RPn Pin bits

111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **U1RXR<5:0>:** Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits

111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

REGISTER 10-7: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SCK1R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SDI1R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **SCK1R<5:0>:** Assign SPI1 Clock Input (SCK1IN) to the Corresponding RPn Pin bits

111111 = Input tied to Vss
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SDI1R<5:0>:** Assign SPI1 Data Input (SDI1) to the Corresponding RPn Pin bits

111111 = Input tied to Vss
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

REGISTER 10-8: RPINR21: PERIPHERAL PIN SELECT INPUT REGISTER 21

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SS1R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SS1R<5:0>:** Assign SPI1 Slave Select Input (SS1IN) to the Corresponding RPn Pin bits

111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

REGISTER 10-9: RPINR29: PERIPHERAL PIN SELECT INPUT REGISTER 29

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	FLT1R<5:0>					
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **FLT1R<5:0>:** Assign PWM Fault Input 1 (FLT1) to the Corresponding RPn Pin bits

111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 10-10: RPINR30: PERIPHERAL PIN SELECT INPUT REGISTER 30

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	FLT3R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	FLT2R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **FLT3R<5:0>:** Assign PWM Fault Input 3 (FLT3) to the Corresponding RPn Pin bits

111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **FLT2R<5:0>:** Assign PWM Fault Input 2 (FLT2) to the Corresponding RPn Pin bits

111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

REGISTER 10-11: RPINR31: PERIPHERAL PIN SELECT INPUT REGISTER 31

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	FLT5R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	FLT4R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **FLT5R<5:0>:** Assign PWM Fault Input 5 (FLT5) to the Corresponding RPn Pin bits

`111111` = Input tied to VSS
`100011` = Input tied to RP35
`100010` = Input tied to RP34
`100001` = Input tied to RP33
`100000` = Input tied to RP32
•
•
•
`00000` = Input tied to RP0

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **FLT4R<5:0>:** Assign PWM Fault Input 4 (FLT4) to the Corresponding RPn Pin bits

`111111` = Input tied to VSS
`100011` = Input tied to RP35
`100010` = Input tied to RP34
`100001` = Input tied to RP33
`100000` = Input tied to RP32
•
•
•
`00000` = Input tied to RP0

REGISTER 10-12: RPINR32: PERIPHERAL PIN SELECT INPUT REGISTER 32

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	FLT7R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	FLT6R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **FLT7R<5:0>:** Assign PWM Fault Input 7 (FLT7) to the Corresponding RPn Pin bits

111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **FLT6R<5:0>:** Assign PWM Fault Input 6 (FLT6) to the Corresponding RPn Pin bits

111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

REGISTER 10-13: RPINR33: PERIPHERAL PIN SELECT INPUT REGISTER 33

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SYNCI1R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	FLT8R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **SYNCI1R<5:0>:** Assign PWM Master Time Base External Synchronization Signal to the Corresponding RPn Pin bits

111111 = Input tied to Vss
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **FLT8R<5:0>:** Assign PWM Fault Input 8 (FLT8) to the Corresponding RPn Pin bits

111111 = Input tied to Vss
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

REGISTER 10-14: RPINR34: PERIPHERAL PIN SELECT INPUT REGISTER 34

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SYNCI2R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SYNCI2R<5:0>:** Assign PWM Master Time Base External Synchronization Signal to the Corresponding RPn Pin bits

111111 = Input tied to VSS
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

REGISTER 10-15: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP1R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP0R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP1R<5:0>:** Peripheral Output Function is Assigned to RP1 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP0R<5:0>:** Peripheral Output Function is Assigned to RP0 Output Pin bits (see Table 10-2 for peripheral function numbers)

REGISTER 10-16: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP3R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP2R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP3R<5:0>:** Peripheral Output Function is Assigned to RP3 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP2R<5:0>:** Peripheral Output Function is Assigned to RP2 Output Pin bits (see Table 10-2 for peripheral function numbers)

REGISTER 10-17: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP5R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP4R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP5R<5:0>:** Peripheral Output Function is Assigned to RP5 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP4R<5:0>:** Peripheral Output Function is Assigned to RP4 Output Pin bits (see Table 10-2 for peripheral function numbers)

REGISTER 10-18: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP7R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP6R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP7R<5:0>:** Peripheral Output Function is Assigned to RP7 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP6R<5:0>:** Peripheral Output Function is Assigned to RP6 Output Pin bits (see Table 10-2 for peripheral function numbers)

REGISTER 10-19: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP9R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP8R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP9R<5:0>:** Peripheral Output Function is Assigned to RP9 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP8R<5:0>:** Peripheral Output Function is Assigned to RP8 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is not implemented in the dsPIC33FJ06GS101 device.

REGISTER 10-20: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP11R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP10R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP11R<5:0>:** Peripheral Output Function is Assigned to RP11 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP10R<5:0>:** Peripheral Output Function is Assigned to RP10 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is not implemented in the dsPIC33FJ06GS101 device.

REGISTER 10-21: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP13R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP12R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP13R<5:0>:** Peripheral Output Function is Assigned to RP13 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP12R<5:0>:** Peripheral Output Function is Assigned to RP12 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is not implemented in the dsPIC33FJ06GS101 device.

REGISTER 10-22: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP15R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP14R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP15R<5:0>:** Peripheral Output Function is Assigned to RP15 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP14R<5:0>:** Peripheral Output Function is Assigned to RP14 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is not implemented in the dsPIC33FJ06GS101 device.

REGISTER 10-23: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP17R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP16R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP17R<5:0>:** Peripheral Output Function is Assigned to RP17 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP16R<5:0>:** Peripheral Output Function is Assigned to RP16 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is implemented in dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices only.

REGISTER 10-24: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP19R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP18R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP19R<5:0>:** Peripheral Output Function is Assigned to RP19 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP18R<5:0>:** Peripheral Output Function is Assigned to RP18 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is implemented in dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices only.

REGISTER 10-25: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP21R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP20R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP21R<5:0>:** Peripheral Output Function is Assigned to RP21 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP20R<5:0>:** Peripheral Output Function is Assigned to RP20 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is implemented in dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices only.

REGISTER 10-26: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP23R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP22R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP23R<5:0>:** Peripheral Output Function is Assigned to RP23 Output Pin bits
(see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP22R<5:0>:** Peripheral Output Function is Assigned to RP22 Output Pin bits
(see Table 10-2 for peripheral function numbers)

Note 1: This register is implemented in dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices only.

REGISTER 10-27: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP25R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP24R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP25R<5:0>:** Peripheral Output Function is Assigned to RP25 Output Pin bits
(see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP24R<5:0>:** Peripheral Output Function is Assigned to RP24 Output Pin bits
(see Table 10-2 for peripheral function numbers)

Note 1: This register is implemented in dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices only.

REGISTER 10-28: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP27R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP26R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP27R<5:0>:** Peripheral Output Function is Assigned to RP27 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP26R<5:0>:** Peripheral Output Function is Assigned to RP26 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is implemented in dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices only.

REGISTER 10-29: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP29R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP28R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP29R<5:0>:** Peripheral Output Function is Assigned to RP29 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP28R<5:0>:** Peripheral Output Function is Assigned to RP28 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is implemented in dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices only.

REGISTER 10-30: RPOR16: PERIPHERAL PIN SELECT OUTPUT REGISTER 16

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP33R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP32R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP33R<5:0>:** Peripheral Output Function is Assigned to RP33 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP32R<5:0>:** Peripheral Output Function is Assigned to RP32 Output Pin bits (see Table 10-2 for peripheral function numbers)

REGISTER 10-31: RPOR17: PERIPHERAL PIN SELECT OUTPUT REGISTER 17

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP35R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP34R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP35R<5:0>:** Peripheral Output Function is Assigned to RP35 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP34R<5:0>:** Peripheral Output Function is Assigned to RP34 Output Pin bits (see Table 10-2 for peripheral function numbers)

11.0 TIMER1

> **Note:** This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*, **Section 11. "Timers"** (DS70205), which is available from the Microchip web site (www.microchip.com).

The Timer1 module is a 16-bit timer, which can serve as a time counter for the Real-Time Clock (RTC), or operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated from the low-power 32 kHz crystal oscillator available on the device
- Can be operated in Asynchronous Counter mode from an external clock source.
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and the clock synchronization is performed after the prescaler.

The unique features of Timer1 allow it to be used for Real-Time Clock (RTC) applications. A block diagram of Timer1 is shown in Figure 11-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (F_{CY}). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

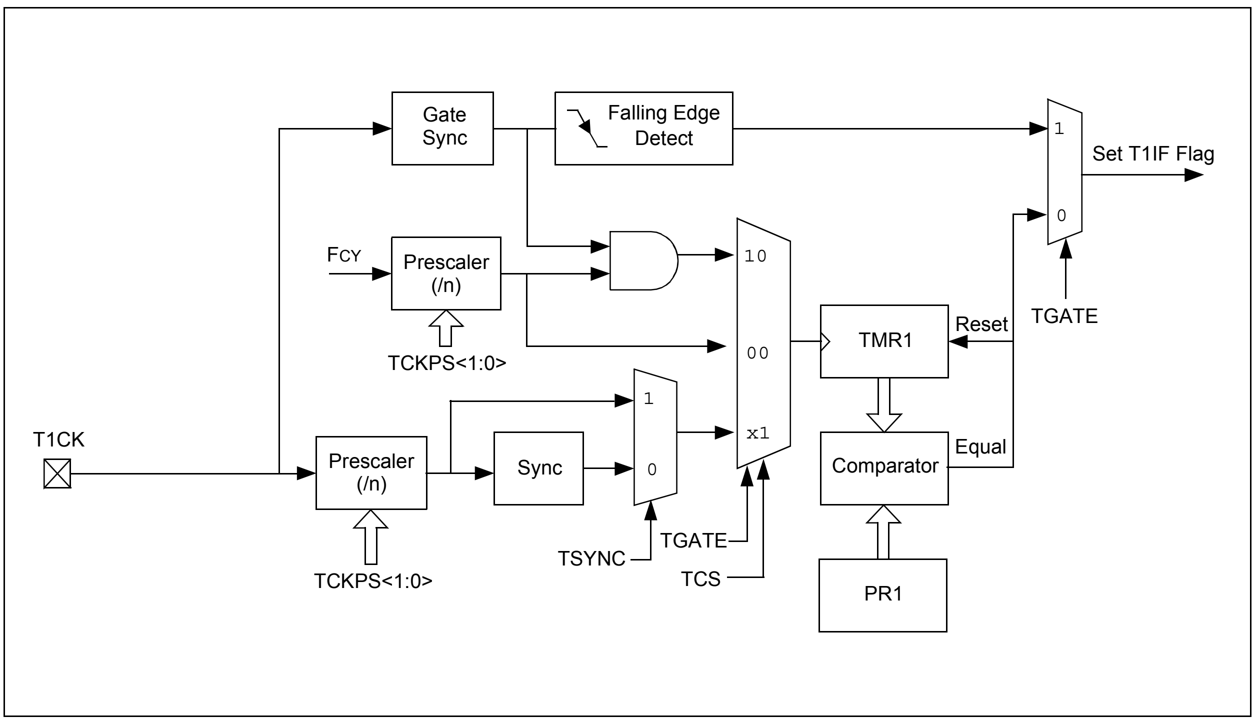
- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

The timer control bit settings for different operating modes are given in the Table 11-1.

TABLE 11-1: TIMER MODE SETTINGS

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated Timer	0	1	x
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

FIGURE 11-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



REGISTER 11-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
—	TGATE	TCKPS<1:0>		—	TSYNC	TCS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer1 On bit
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **TSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-7 **Unimplemented:** Read as ‘0’

bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When T1CS = 1:
This bit is ignored.
When T1CS = 0:
1 = Gated time accumulation enabled
0 = Gated time accumulation disabled

bit 5-4 **TCKPS<1:0>** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit
When TCS = 1:
1 = Synchronize external clock input
0 = Do not synchronize external clock input
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit
1 = External clock from T1CK pin (on the rising edge)
0 = Internal clock (FCY)

bit 0 **Unimplemented:** Read as ‘0’

12.0 TIMER2/3 FEATURES

> **Note:** This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*, **Section 11. "Timers"** (DS70205), which is available on the Microchip web site (www.microchip.com).

Timer2 is a Type B timer that offers the following major features:

- A Type B timer can be concatenated with a Type C timer to form a 32-bit timer
- External clock input (TxCK) is always synchronized to the internal device clock and the clock synchronization is performed after the prescaler.

Figure 12-1 shows a block diagram of the Type B timer.

Timer3 is a Type C timer that offers the following major features:

- A Type C timer can be concatenated with a Type B timer to form a 32-bit timer
- The external clock input (TxCK) is always synchronized to the internal device clock and the clock synchronization is performed before the prescaler

A block diagram of the Type C timer is shown in Figure 12-2.

> **Note:** Timer3 is not available on all devices.

FIGURE 12-1: TYPE B TIMER BLOCK DIAGRAM (x = 2)

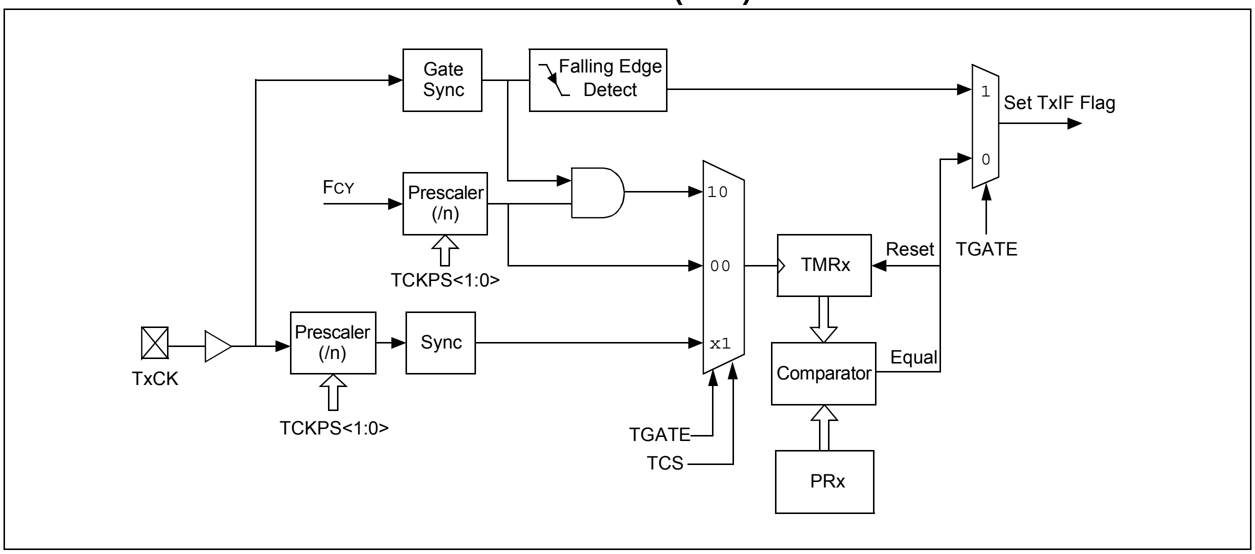
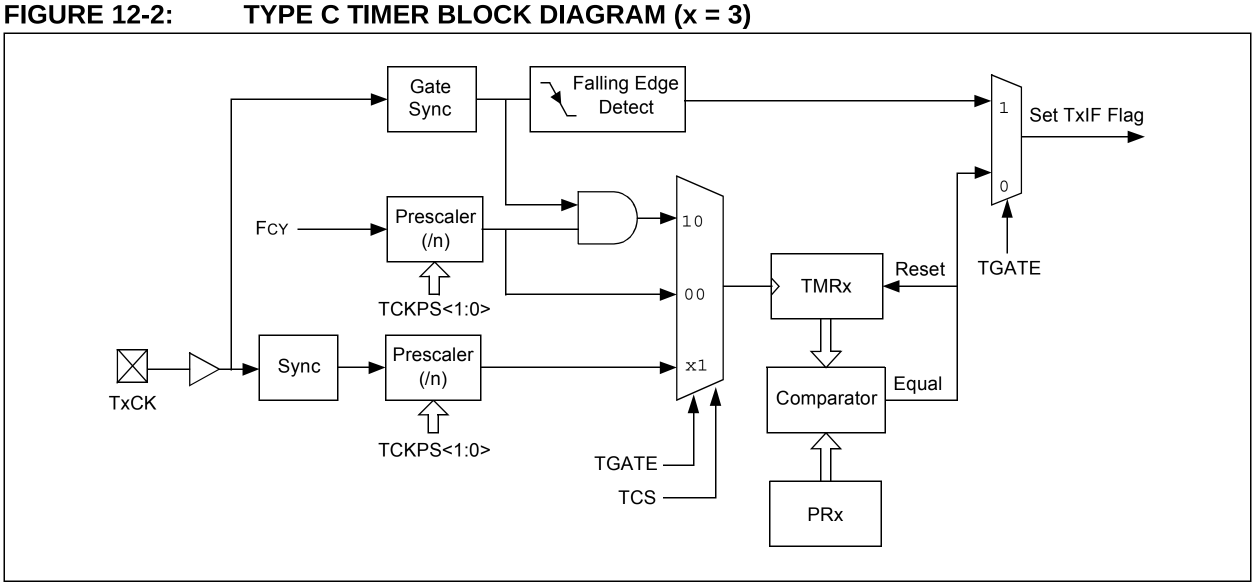


FIGURE 12-2: TYPE C TIMER BLOCK DIAGRAM (x = 3)



The Timer2/3 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous Counter mode, the input clock is derived from the external clock input at the TxCK pin.

The timer modes are determined by the following bits:

- TCS (TxCON<1>): Timer Clock Source Control bit
- TGATE (TxCON<6>): Timer Gate Control bit

Timer control bit settings for different operating modes are given in the Table 12-1.

TABLE 12-1: TIMER MODE SETTINGS

Mode	TCS	TGATE
Timer	0	0
Gated Timer	0	1
Synchronous Counter	1	x

12.1 16-Bit Operation

To configure any of the timers for individual 16-bit operation:

1. Clear the T32 bit corresponding to that timer.
2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits.
4. Load the timer period value into the PRx register.
5. If interrupts are required, set the interrupt enable bit, TxIE. Use the priority bits, TxIP<2:0>, to set the interrupt priority.
6. Set the TON bit.

12.2 32-Bit Operation

A 32-bit timer module can be formed by combining a Type B and a Type C 16-bit timer module. For 32-bit timer operation, the T32 control bit in the Type B Timer Control (TxCON<3>) register must be set. The Type C timer holds the most significant word (msw) and the Type B timer holds the least significant word (lsw) for 32-bit operation.

When configured for 32-bit operation, only the Type B Timer Control (TxCON) register bits are required for setup and control while the Type C Timer Control register bits are ignored (except the TSIDL bit).

For interrupt control, the combined 32-bit timer uses the interrupt enable, interrupt flag and interrupt priority control bits of the Type C timer. The interrupt control and status bits for the Type B timer are ignored during 32-bit timer operation.

The Timer2 and Timer 3 that can be combined to form a 32-bit timer are listed in Table 12-2.

TABLE 12-2: 32-BIT TIMER

Type B Timer (lsw)	Type C Timer (msw)
Timer2	Timer3

A block diagram representation of the 32-bit timer module is shown in Figure 12-3. The 32-timer module can operate in one of the following modes:

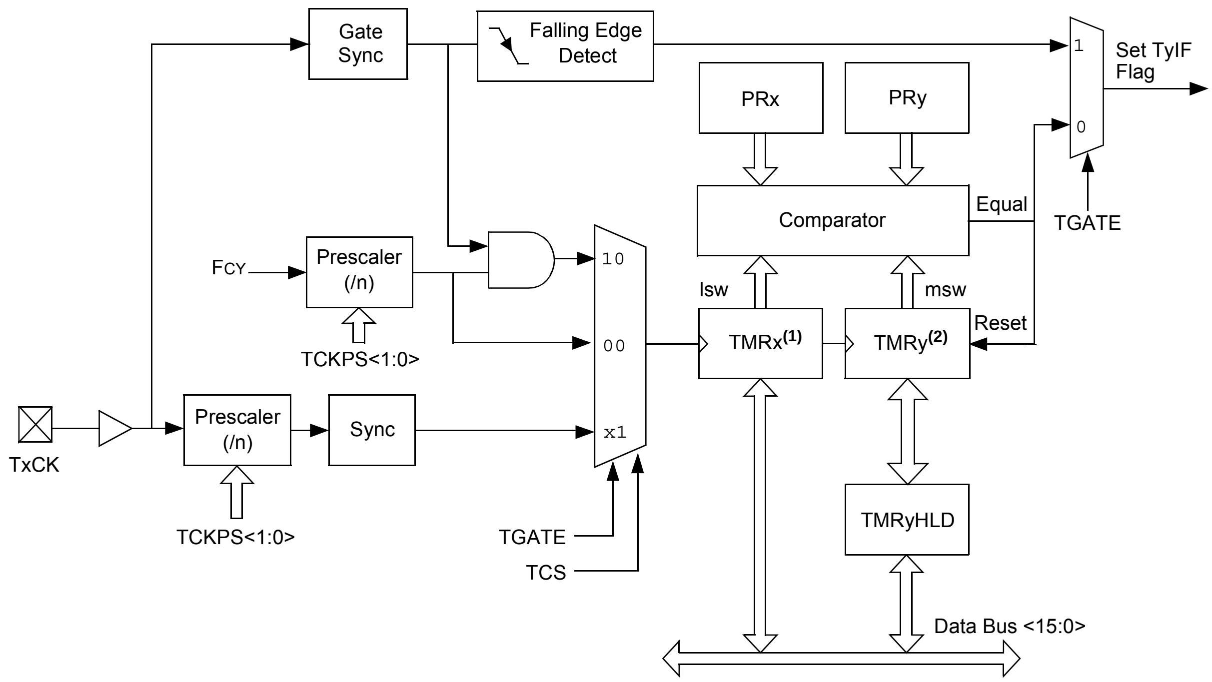
- Timer mode
- Gated Timer mode
- Synchronous Counter mode

To configure the features of Timer2/3 for 32-bit operation:

1. Set the T32 control bit.
2. Select the prescaler ratio for Timer2 using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the corresponding TCS and TGATE bits.
4. Load the timer period value. PR3 contains the most significant word of the value, while PR2 contains the least significant word.
5. If interrupts are required, set the interrupt enable bit, T3IE. Use the priority bits, T3IP<2:0>, to set the interrupt priority. While Timer2 controls the timer, the interrupt appears as a Timer3 interrupt.
6. Set the corresponding TON bit.

The timer value at any point is stored in the register pair, TMR3:TMR2, which always contains the most significant word of the count, while TMR2 contains the least significant word.

FIGURE 12-3: 32-BIT TIMER BLOCK DIAGRAM



Note 1: Timerx is a Type B Timer (x = 2).

2: Timery is a Type C Timer (y = 3).

REGISTER 12-1: TxCON: TIMER CONTROL REGISTER (x = 2)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS<1:0>		T32[(1)]	—	TCS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timerx On bit

When T32 = 1 (in 32-Bit Timer mode):
1 = Starts 32-bit TMRx:TMRy timer pair
0 = Stops 32-bit TMRx:TMRy timer pair

When T32 = 0 (in 16-Bit Timer mode):
1 = Starts 16-bit timer
0 = Stops 16-bit timer

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Stop in Idle Mode bit
1 = Discontinue timer operation when device enters Idle mode
0 = Continue timer operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit

When TCS = 1:
This bit is ignored.

When TCS = 0:
1 = Gated time accumulation enabled
0 = Gated time accumulation disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

bit 3 **T32:** 32-Bit Timerx Mode Select bit
1 = TMRx and TMRy form a 32-bit timer
0 = TMRx and TMRy form separate 16-bit timer

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit
1 = External clock from TxCK pin
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

REGISTER 12-2: TyCON: TIMER CONTROL REGISTER (y = 3)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(2)	—	TSIDL(1)	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(2)	TCKPS<1:0>(2)		—	—	TCS(2)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timery On bit(2)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **TSIDL:** Stop in Idle Mode bit(1)
1 = Discontinue timer operation when device enters Idle mode
0 = Continue timer operation in Idle mode

bit 12-7 **Unimplemented:** Read as ‘0’

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(2)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation enabled
0 = Gated time accumulation disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits(2)
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **TCS:** Timery Clock Source Select bit(2)
1 = External clock from TxCK pin
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as ‘0’

Note 1: When 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

2: When the 32-bit timer operation is enabled (T32 = 1) in the Timer Control (TxCON<3>) register, these bits have no effect.

NOTES:

13.0 INPUT CAPTURE

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *“dsPIC33F Family Reference Manual”*, **Section 12. “Input Capture”** (DS70198), which is available on the Microchip web site (www.microchip.com).

The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices support up to two input capture channels.

The input capture module captures the 16-bit value of the selected Time Base register when an event occurs at the ICx pin. The events that cause a capture event are listed below in three categories:

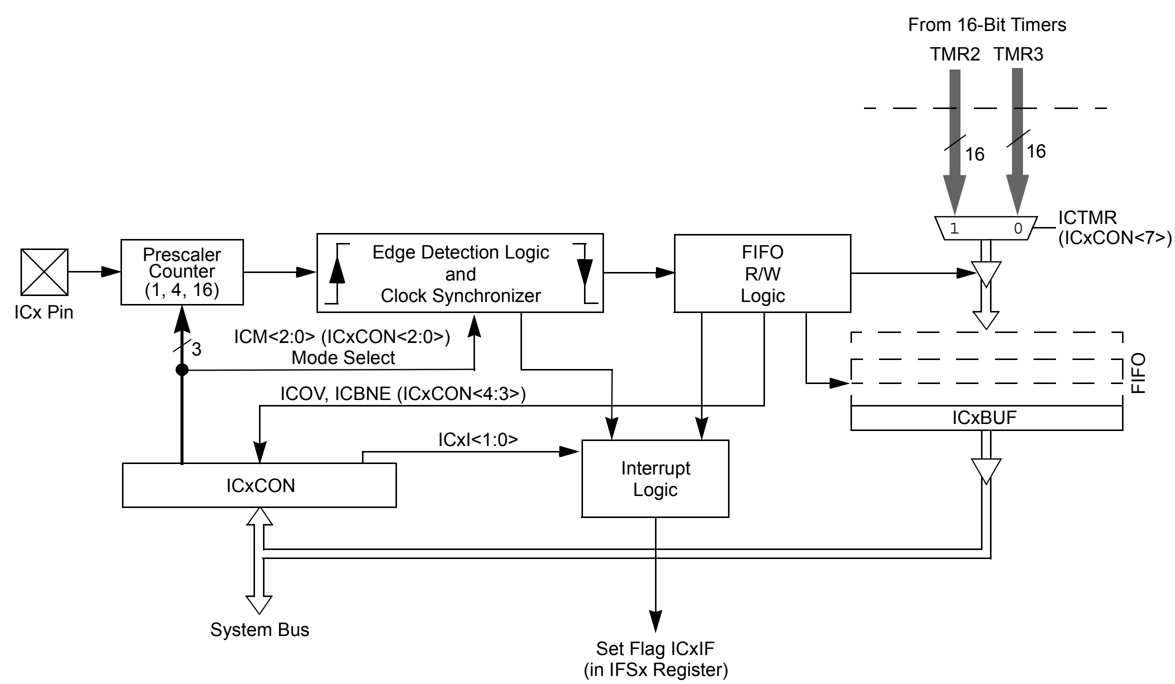
- Simple Capture Event modes:
  - Capture timer value on every falling edge of input at ICx pin
  - Capture timer value on every rising edge of input at ICx pin
- Capture timer value on every edge (rising and falling)
- Prescaler Capture Event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select one of the two 16-bit timers (Timer2 or Timer3) for the time base. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values
  - Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
- Use of input capture to provide additional sources of external interrupts

FIGURE 13-1: INPUT CAPTURE BLOCK DIAGRAM



Note 1: An ‘x’ in a signal, register or bit name denotes the number of the capture channel.

13.1 Input Capture Registers

REGISTER 13-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER (x = 1, 2)

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **ICSIDL:** Input Capture Module Stop in Idle Control bit
1 = Input capture module halts in CPU Idle mode
0 = Input capture module continues to operate in CPU Idle mode

bit 12-8 **Unimplemented:** Read as ‘0’

bit 7 **ICTMR:** Input Capture Timer Select bits
1 = TMR2 contents are captured on capture event
0 = TMR3 contents are captured on capture event

bit 6-5 **ICI<1:0>:** Select Number of Captures per Interrupt bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
1 = Input capture overflow occurred
0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Empty Status bit (read-only)
1 = Input capture buffer is not empty, at least one more capture value can be read
0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode. Rising edge detect-only, all other control bits are not applicable.
110 = Unused (module disabled)
101 = Capture mode, every 16th rising edge
100 = Capture mode, every 4th rising edge
011 = Capture mode, every rising edge
010 = Capture mode, every falling edge
001 = Capture mode, every edge (rising and falling). ICI<1:0> bits do not control interrupt generation for this mode.
000 = Input capture module turned off

14.0 OUTPUT COMPARE

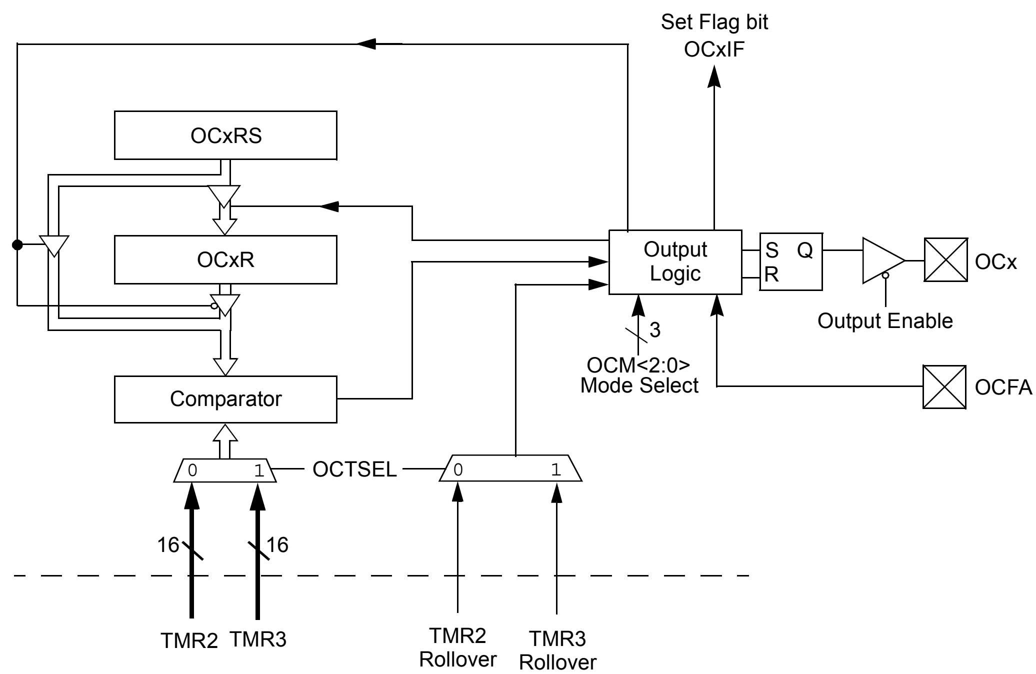
Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*, **Section 13. "Output Compare"** (DS70209), which is available on the Microchip web site (www.microchip.com).

The output compare module can select either Timer2 or Timer3 for its time base. The module compares the value of the timer with the value of one or two Compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the Compare register value. The output compare module generates either a single output pulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events.

The output compare module has multiple operating modes:

- Active-Low One-Shot mode
- Active-High One-Shot mode
- Toggle mode
- Delayed One-Shot mode
- Continuous Pulse mode
- PWM mode without Fault Protection
- PWM mode with Fault Protection

FIGURE 14-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



Note: An 'x' in a signal, register or bit name denotes the number of the output compare channels.

14.1 Output Compare Modes

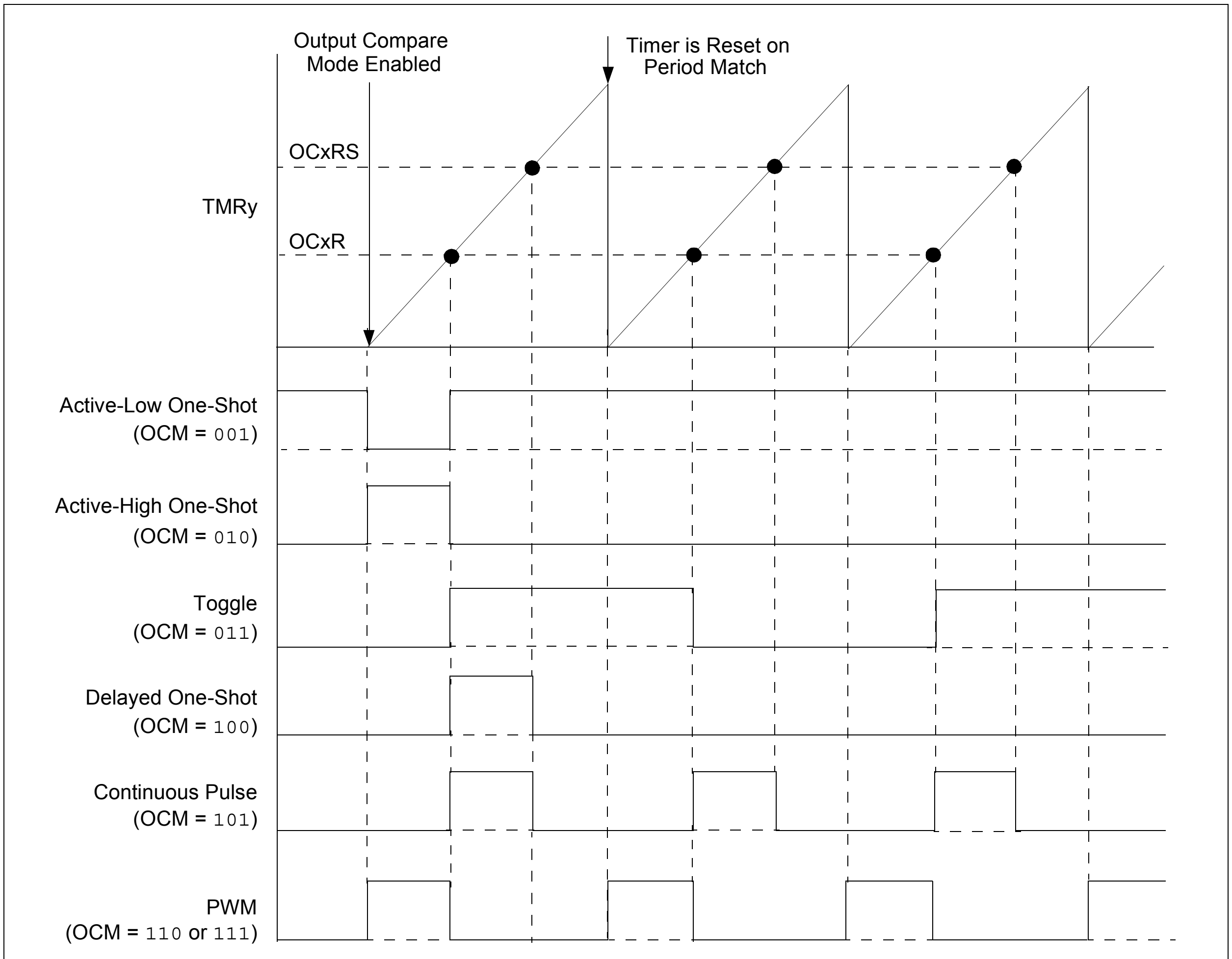
Configure the Output Compare modes by setting the appropriate Output Compare Mode (OCM<2:0>) bits in the Output Compare Control (OCxCON<2:0>) register. Table 14-1 lists the different bit settings for the Output Compare modes. Figure 14-2 illustrates the output compare operation for various modes. The user application must disable the associated timer when writing to the Output Compare Control registers to avoid malfunctions.

Note: Refer to **Section 13. "Output Compare"** in the *"dsPIC33F Family Reference Manual"* (DS7029) for OCxR and OCxRS register restrictions.

TABLE 14-1: OUTPUT COMPARE MODES

OCM<2:0>	Mode	OCx Pin Initial State	OCx Interrupt Generation
000	Module Disabled	Controlled by GPIO register	—
001	Active-Low One-Shot	0	OCx rising edge
010	Active-High One-Shot	1	OCx falling edge
011	Toggle	Current output is maintained	OCx rising and falling edge
100	Delayed One-Shot	0	OCx falling edge
101	Continuous Pulse	0	OCx falling edge
110	PWM without Fault Protection	'0', if OCxR is zero '1', if OCxR is non-zero	No interrupt
111	PWM with Fault Protection	'0', if OCxR is zero '1', if OCxR is non-zero	OCFA falling edge for OC1 to OC4

FIGURE 14-2: OUTPUT COMPARE OPERATION



 Preliminary

REGISTER 14-1: OCxCON: OUTPUT COMPARE x CONTROL REGISTER (x = 1, 2)

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	OCSIDL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R-0, HC	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OCFLT	OCTSEL	OCM<2:0>		
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **OCSIDL:** Stop Output Compare in Idle Mode Control bit
1 = Output Compare x halts in CPU Idle mode
0 = Output Compare x continues to operate in CPU Idle mode

bit 12-5 **Unimplemented:** Read as ‘0’

bit 4 **OCFLT:** PWM Fault Condition Status bit
1 = PWM Fault condition has occurred (cleared in hardware only)
0 = No PWM Fault condition has occurred (this bit is only used when OCM<2:0> = 111)

bit 3 **OCTSEL:** Output Compare Timer Select bit
1 = Timer3 is the clock source for Compare x
0 = Timer2 is the clock source for Compare x

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
111 = PWM mode on OCx, Fault pin enabled
110 = PWM mode on OCx, Fault pin disabled
101 = Initialize OCx pin low, generate continuous output pulses on OCx pin
100 = Initialize OCx pin low, generate single output pulse on OCx pin
011 = Compare event toggles OCx pin
010 = Initialize OCx pin high, compare event forces OCx pin low
001 = Initialize OCx pin low, compare event forces OCx pin high
000 = Output compare channel is disabled

NOTES:

15.0 HIGH-SPEED PWM

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *“dsPIC33F Family Reference Manual”*, **Section 43. “High- Speed PWM”** (DS70323), which is available on the Microchip web site (www.microchip.com).

The high-speed PWM module on the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices supports a wide variety of PWM modes and output formats. This PWM module is ideal for power conversion applications, such as:

- AC/DC Converters
- DC/DC Converters
- Power Factor Correction(PFC)
- Uninterruptible Power Supply (UPS)
- Inverters
- Battery Chargers
- Digital Lighting

15.1 Features Overview

The high-speed PWM module incorporates the following features:

- 2-4 PWM generators with 4-8 outputs
- Individual time base and duty cycle for each of the eight PWM outputs
- Dead time for rising and falling edges:
- Duty cycle resolution of 1.04 ns at 40 MIPS
- Dead-time resolution of 1.04 ns at 40 MIPS
- Phase shift resolution of 1.04 ns at 40 MIPS
- Frequency resolution of 1.04 ns at 40 MIPS
- PWM modes supported:
  - Standard Edge-Aligned
  - True Independent Output
  - Complementary
  - Center-Aligned
  - Push-Pull
  - Multiphase
  - Variable Phase
  - Fixed Off-Time
  - Current Reset
  - Current-Limit
- Independent Fault/Current-Limit inputs for each of the eight PWM outputs
- Output override control
- Special Event Trigger
- PWM capture feature
- Prescaler for input clock
- Dual trigger from PWM to ADC
- PWMxH, PWMxL output pin swapping
- PWM4H, PWM4L pins remappable
- On-the-fly PWM frequency, duty cycle and phase shift changes
- Disabling of Individual PWM generators to reduce power consumption
- Leading-Edge Blanking (LEB) functionality

Note:	Duty cycle, dead-time, phase shift and frequency resolution is 8.32 ns in Center-Aligned PWM mode.

Figure 15-1 conceptualizes the PWM module in a simplified block diagram. Figure 15-2 illustrates how the module hardware is partitioned for each PWM output pair for the Complementary PWM mode. Each functional unit of the PWM module is discussed in subsequent sections.

The PWM module contains four PWM generators. The module has up to eight PWM output pins: PWM1H, PWM1L, PWM2H, PWM2L, PWM3H, PWM3L, PWM4H and PWM4L. For complementary outputs, these eight I/O pins are grouped into H/L pairs.

15.2 Feature Description

The PWM module is designed for applications that require:

- High-resolution at high PWM frequencies
- The ability to drive Standard, Edge-Aligned, Center-Aligned Complementary mode, and Push-Pull mode outputs
- The ability to create multiphase PWM outputs

For Center-Aligned mode, the duty cycle, period phase and dead-time resolutions will be 8 ns.

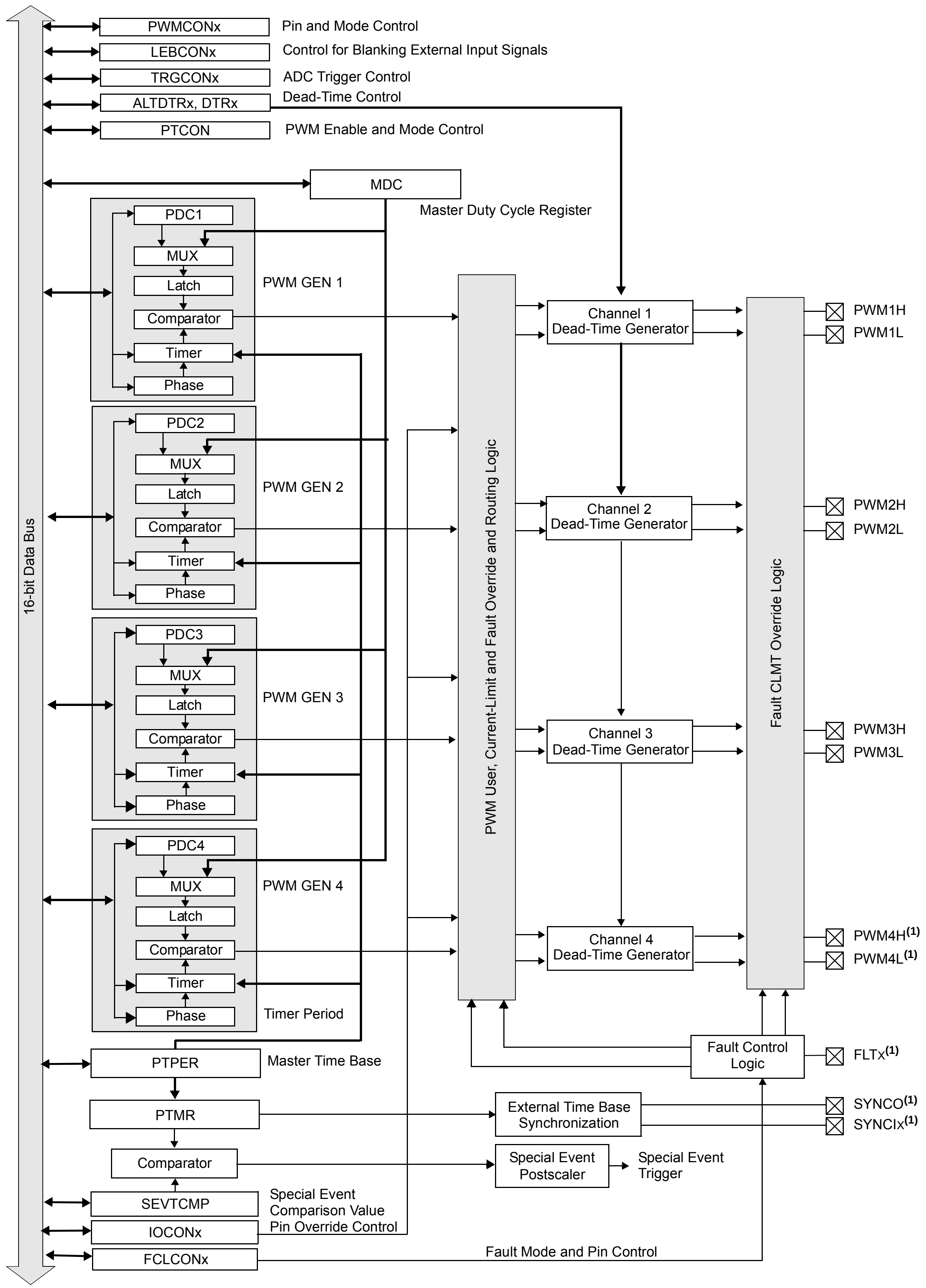
Two common, medium power converter topologies are push-pull and half-bridge. These designs require the PWM output signal to be switched between alternate pins, as provided by the Push-Pull PWM mode.

Phase-shifted PWM describes the situation where each PWM generator provides outputs, but the phase relationship between the generator outputs is specifiable and changeable.

Multiphase PWM is often used to improve DC/DC converter load transient response, and reduce the size of output filter capacitors and inductors. Multiple DC/DC converters are often operated in parallel, but phase-shifted in time. A single PWM output operating at 250 kHz has a period of 4 µs, but an array of four PWM channels, staggered by 1 µs each, yields an effective switching frequency of 1 MHz. Multiphase PWM applications typically use a fixed-phase relationship.

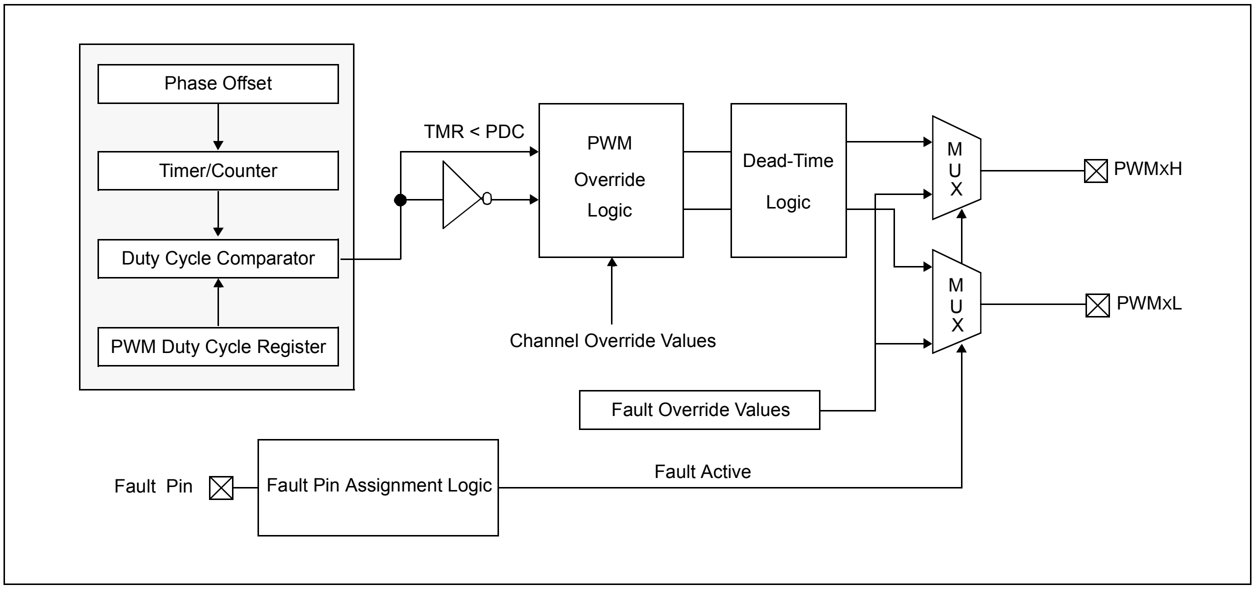
Variable phase PWM is useful in Zero Voltage Transition (ZVT) power converters. Here, the PWM duty cycle is always 50%, and the power flow is controlled by varying the relative phase shift between the two PWM generators.

FIGURE 15-1: SIMPLIFIED CONCEPTUAL BLOCK DIAGRAM OF HIGH-SPEED PWM



Note 1: These pins are remappable.

FIGURE 15-2: PARTITIONED OUTPUT PAIR, COMPLEMENTARY PWM MODE



15.3 Control Registers

The following registers control the operation of the high-speed PWM module.

- PTCON: PWM Time Base Control Register
- PTCON2: PWM Clock Divider Select Register
- PTPER: PWM Master Time Base Register(1)
- SEVTCMP: PWM Special Event Compare Register
- MDC: PWM Master Duty Cycle Register
- PWMCONx: PWMx Control Register
- PDCx: PWMx Generator Duty Cycle Register
- PHASEx: PWMx Primary Phase Shift Register (PHASEx Register provides the local time base period for PWMxH)
- DTRx: PWMx Dead-Time Register
- ALTDTRx: PWMx Alternate Dead-Time Register
- SDCx: PWMx Secondary Duty Cycle Register
- SPHASEx: PWMx Secondary Phase Shift Register (Provides the local time base for PWMxL)
- TRGCONx: PWMx Trigger Control Register
- IOCONx: PWMx I/O Control Register
- FCLCONx: PWMx Fault Current-Limit Control Register
- TRIGx: PWMx Primary Trigger Compare Value Register
- STRIGx: PWMx Secondary Trigger Compare Value Register
- LEBCONx: Leading-Edge Blanking Control Register
- PWMCAPx: Primary PWMx Time Base Capture Register

REGISTER 15-1: PTCON: PWM TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU(1)	SYNCPOL(1)	SYNCOEN(1)
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN(1)	—	SYNCSRC<1:0>(1)		SEVTPS<3:0>(1)			
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PTEN:** PWM Module Enable bit
1 = PWM module is enabled
0 = PWM module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **PTSIDL:** PWM Time Base Stop in Idle Mode bit
1 = PWM time base halts in CPU Idle mode
0 = PWM time base runs in CPU Idle mode

bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled

bit 10 **EIPU:** Enable Immediate Period Updates bit(1)
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWM cycle boundaries

bit 9 **SYNCPOL:** Synchronization Input/Output Polarity bit(1)
1 = SYNCIx and SYNCO polarity is inverted (active-low)
0 = SYNCIx and SYNCO are active-high

bit 8 **SYNCOEN:** Primary Time Base Sync Enable bit(1)
1 = SYNCO output is enabled
0 = SYNCO output is disabled

bit 7 **SYNCEN:** External Time Base Synchronization Enable bit(1)
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

bit 6 **Unimplemented:** Read as ‘0’

bit 5-4 **SYNCSRC<1:0>:** Synchronous Source Selection bits(1)
00 = SYNCI1
01 = SYNCI2
10 = Reserved
11 = Reserved

bit 3-0 **SEVTPS<3:0>:** PWM Special Event Trigger Output Postscaler Select bits(1)
0000 = 1:1 Postscaler generates a Special Event Trigger on every compare match event
0001 = 1:2 Postscaler generates a Special Event Trigger on every second compare match event
•
•
•
1111 = 1:16 Postscaler generates a Special Event Trigger trigger on every sixteenth compare match event

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCIx feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.

REGISTER 15-2: PTCON2: PWM CLOCK DIVIDER SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCLKDIV<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **PCLKDIV<2:0>:** PWM Input Clock Prescaler (Divider) Select bits(1)

000 = Divide by 1, maximum PWM timing resolution (power-on default)
001 = Divide by 2, maximum PWM timing resolution
010 = Divide by 4, maximum PWM timing resolution
011 = Divide by 8, maximum PWM timing resolution
100 = Divide by 16, maximum PWM timing resolution
101 = Divide by 32, maximum PWM timing resolution
110 = Divide by 64, maximum PWM timing resolution
111 = Reserved

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 15-3: PTPER: PWM MASTER TIME BASE REGISTER(1)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PTPER <15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
PTPER <7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **PTPER<15:0>:** PWM Master Time Base (PMTMR) Period Value bits

Note 1: The minimum value that can be loaded into the PTPER register is 0x0010 and the maximum value is 0xFFF8.

REGISTER 15-4: SEVTCMP: PWM SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP <15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
SEVTCMP <7:3>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **SEVTCMP<15:3>**: Special Event Compare Count Value bits

bit 2-0 **Unimplemented:** Read as ‘0’

REGISTER 15-5: MDC: PWM MASTER DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MDC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MDC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **MDC<15:0>:** Master PWM Duty Cycle Value bits

Note 1: The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of Period – 0x0008.

2: As the duty cycle gets closer to 0% or 100% of the PWM period (0 ns-40 ns, depending on the mode of operation), the PWM duty cycle resolution will degrade from 1 LSB to 3 LSB.

REGISTER 15-6: PWMCONx: PWMx CONTROL REGISTER

HS/HC-0	HS/HC-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTSTAT(1)	CLSTAT(1)	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB(3)	MDCS(3)
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
DTC<1:0>		—	—	—	CAM(2,3)	XPRES(4)	IUE
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
1 = Fault interrupt is pending
0 = No Fault interrupt is pending. This bit is cleared by setting FLTIEN = 0.

bit 14 **CLSTAT:** Current-Limit Interrupt Status bit(1)
1 = Current-limit interrupt is pending
0 = No current-limit interrupt is pending. This bit is cleared by setting CLIEN = 0.

bit 13 **TRGSTAT:** Trigger Interrupt Status bit
1 = Trigger interrupt is pending
0 = No trigger interrupt is pending. This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit
1 = Fault interrupt is enabled
0 = Fault interrupt is disabled and the FLTSTAT bit is cleared

bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
1 = Current-limit interrupt enabled
0 = Current-limit interrupt disabled and the CLSTAT bit is cleared

bit 10 **TRGIEN:** Trigger Interrupt Enable bit
1 = A trigger event generates an interrupt request
0 = Trigger event interrupts are disabled and the TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit(3)
1 = PHASEx/SPHASEx register provides time base period for this PWM generator
0 = PTPER register provides timing for this PWM generator

bit 8 **MDCS:** Master Duty Cycle Register Select bit(3)
1 = MDC register provides duty cycle information for this PWM generator
0 = PDCx/SDCx register provides duty cycle information for this PWM generator

bit 7-6 **DTC<1:0>:** Dead-Time Control bits
00 = Positive dead time actively applied for all output modes
01 = Negative dead time actively applied for all output modes
10 = Dead-time function is disabled
11 = Reserved

bit 5-3 **Unimplemented:** Read as '0'

Note 1: Software must clear the interrupt status here and the corresponding IFS bit in the interrupt controller.
2: The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
3: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.
4: To operate in External Period Reset mode, configure FCLCONx<CLMOD> = 0 and PWMCONx<ITB> = 1.

REGISTER 15-6: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

bit 2	**CAM:** Center-Aligned Mode Enable bit[2,3] 1 = Center-Aligned mode is enabled 0 = Center-Aligned mode is disabled
bit 1	**XPRES:** External PWM Reset Control bit[4] 1 = Current-limit source resets time base for this PWM generator if it is in Independent Time Base mode 0 = External pins do not affect PWM time base
bit 0	**IUE:** Immediate Update Enable bit 1 = Updates to the active MDC/PDCx/SDCx registers are immediate 0 = Updates to the active MDC/PDCx/SDCx registers are synchronized to the PWM time base

Note 1: Software must clear the interrupt status here and the corresponding IFS bit in the interrupt controller.

2: The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.

3: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

4: To operate in External Period Reset mode, configure FCLCONx<CLMOD> = 0 and PWMCONx<ITB> = 1.

 Preliminary

REGISTER 15-7: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **PDCx<15:0>:** PWM Generator # Duty Cycle Value bits

Note 1: In Independent PWM mode, the PDCx register controls the PWMxH duty cycle only. In Complementary, Redundant and Push-Pull PWM modes, the PDCx register controls the duty cycle of both the PWMxH and PWMxL. The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of 0xFFEF.

2: As the duty cycle gets closer to 0% or 100% of the PWM period (0 ns-40 ns, depending on the mode of operation), the PWM duty cycle resolution will degrade from 1 LSB to 3 LSB.

REGISTER 15-8: SDCx: PWMx SECONDARY DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDCx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDCx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **SDCx<15:0>:** Secondary Duty Cycle for PWMxL Output Pin bits

Note 1: The SDCx register is used in Independent PWM mode only. When used in Independent PWM mode, the SDCx register controls the PWMxL duty cycle. The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of 0xFFEF.

2: As the duty cycle gets closer to 0% or 100% of the PWM period (0 ns-40 ns, depending on the mode of operation), the PWM duty cycle resolution will degrade from 1 LSB to 3 LSB.

REGISTER 15-9: PHASEx: PWMx PRIMARY PHASE SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **PHASEx<15:0>:** PWM Phase Shift Value or Independent Time Base Period for this PWM Generator bits

Note 1: If PWMCONx<ITB> = `0`, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (IOCONx<PMOD> = `00`, `01`, or `10`) PHASEx<15:0> = Phase shift value for PWMxH and PWMxL outputs
- True Independent Output mode (IOCONx<PMOD> = `11`) PHASEx<15:0> = Phase shift value for PWMxL only

2: If PWMCONx<ITB> = `1`, the following applies based on the mode of operation:
- Complementary, Redundant, and Push-Pull Output mode (IOCONx<PMOD> = `00`, `01`, or `10`) PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL
- True Independent Output mode (IOCONx<PMOD> = `11`) PHASEx<15:0> = Independent time base period value for PWMxL only
- The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of Period - 0x0008.

REGISTER 15-10: SPHASEx: PWMx SECONDARY PHASE SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPHASEx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPHASEx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **SPHASEx<15:0>:** Secondary Phase Offset for PWMxL Output Pin bits (used in Independent PWM mode only)

Note 1: If PWMCONx<ITB> = `0`, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (IOCONx<PMOD> = `00`, `01`, or `10`) SPHASEx<15:0> = Not used
- True Independent Output mode (IOCONx<PMOD> = `11`) PHASEx<15:0> = Phase shift value for PWMxL only

2: If PWMCONx<ITB> = `1`, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (IOCONx<PMOD> = `00`, `01`, or `10`) SPHASEx<15:0> = Not used
- True Independent Output mode (IOCONx<PMOD> = `11`) PHASEx<15:0> = Independent time base period value for PWMxL only

REGISTER 15-11: DTRx: PWMx DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **DTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 15-12: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ALTDTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALTDTR <7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **ALTDTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 15-13: TRGCONx: PWMx TRIGGER CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
TRGDIV<3:0>				—	—	—	—
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTM(1)	—	TRGSTRT<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **TRGDIV<3:0>**: Trigger # Output Divider bits
0000 = Trigger output for every trigger event
0001 = Trigger output for every 2nd trigger event
0010 = Trigger output for every 3rd trigger event
0011 = Trigger output for every 4th trigger event
0100 = Trigger output for every 5th trigger event
0101 = Trigger output for every 6th trigger event
0110 = Trigger output for every 7th trigger event
0111 = Trigger output for every 8th trigger event
1000 = Trigger output for every 9th trigger event
1001 = Trigger output for every 10th trigger event
1010 = Trigger output for every 11th trigger event
1011 = Trigger output for every 12th trigger event
1100 = Trigger output for every 13th trigger event
1101 = Trigger output for every 14th trigger event
1110 = Trigger output for every 15th trigger event
1111 = Trigger output for every 16th trigger event

bit 11-8 **Unimplemented:** Read as ‘0’

bit 7 **DTM:** Dual Trigger Mode bit(1)
1 = Secondary trigger event is combined with the primary trigger event to create the PWM trigger.
0 = Secondary trigger event is not combined with the primary trigger event to create the PWM trigger. Two separate PWM triggers are generated.

bit 6 **Unimplemented:** Read as ‘0’

bit 5-0 **TRGSTRT<5:0>:** Trigger Postscaler Start Enable Select bits
000000 = Wait 0 PWM cycles before generating the first trigger event after the module is enabled
000001 = Wait 1 PWM cycles before generating the first trigger event after the module is enabled
000010 = Wait 1 PWM cycles before generating the first trigger event after the module is enabled
•
•
•
111111 = Wait 63 PWM cycles before generating the first trigger event after the module is enabled

Note 1: The secondary generator cannot generate PWM trigger interrupts.

REGISTER 15-14: IOCONx: PWMx I/O CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD<1:0>(1)		OVRENH	OVRENL
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PENH:** PWMH Output Pin Ownership bit
1 = PWM module controls PWMxH pin
0 = GPIO module controls PWMxH pin

bit 14 **PENL:** PWML Output Pin Ownership bit
1 = PWM module controls PWMxL pin
0 = GPIO module controls PWMxL pin

bit 13 **POLH:** PWMH Output Pin Polarity bit
1 = PWMxH pin is active-low
0 = PWMxH pin is active-high

bit 12 **POLL:** PWML Output Pin Polarity bit
1 = PWMxL pin is active-low
0 = PWMxL pin is active-high

bit 11-10 **PMOD<1:0>:** PWM # I/O Pin Mode bits(1)
00 = PWM I/O pin pair is in the Complementary Output mode
01 = PWM I/O pin pair is in the Redundant Output mode
10 = PWM I/O pin pair is in the Push-Pull Output mode
11 = PWM I/O pin pair is in the True Independent Output mode

bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
1 = OVRDAT<1> provides data for output on PWMxH pin
0 = PWM generator provides data for PWMxH pin

bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
1 = OVRDAT<0> provides data for output on PWMxL pin
0 = PWM generator provides data for PWMxL pin

bit 7-6 **OVRDAT<1:0>:** Data for PWMxH and PWMxL Pins if Override is Enabled bits
If OVERENH = 1 then OVRDAT<1> provides data for PWMxH.
If OVERENL = 1 then OVRDAT<0> provides data for PWMxL.

bit 5-4 **FLTDAT<1:0>:** Data for PWMxH and PWMxL Pins if FLTMOD is Enabled bits
FCLCONx<IFLTMOD> = 0: Normal Fault mode:
If Fault active, then FLTDAT<1> provides data for PWMxH.
If Fault active, then FLTDAT<0> provides data for PWMxL.
FCLCONx<IFLTMOD> = 1: Independent Fault mode:
If current-limit active, then FLTDAT<1> provides data for PWMxH.
If Fault active, then FLTDAT<0> provides data for PWMxL.

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 15-14: IOCONx: PWMx I/O CONTROL REGISTER (CONTINUED)

bit 3-2	**CLDAT<1:0>:** Data for PWMxH and PWMxL Pins if CLMODE is Enabled bits FCLCONx<IFLTMOD> = 0: Normal Fault mode: If current-limit active, then CLDAT<1> provides data for PWMxH. If current-limit active, then CLDAT<0> provides data for PWMxL. FCLCONx<IFLTMOD> = 1: Independent Fault mode: CLDAT<1:0> is ignored.
bit 1	**SWAP<1:0>:** SWAP PWMxH and PWMxL pins 1 = PWMxH output signal is connected to PWMxL pin and PWMxL signal is connected to PWMxH pins 0 = PWMxH and PWMxL pins are mapped to their respective pins
bit 0	**OSYNC:** Output Override Synchronization bit 1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWM time base 0 = Output overrides via the OVDDAT<1:0> bits occur on next CPU clock boundary

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 15-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IFLTMOD	CLSRC<4:0>(2,3)					CLPOL(1)	CLMOD
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTSRC<4:0>(2,3)					FLTPOL(1)	FLTMOD<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IFLTMOD:** Independent Fault Mode Enable bit

1 = Independent Fault mode: Current-limit input maps FLTDAT<1> to PWMxH output and Fault input maps FLTDAT<0> to PWMxL output. The CLDAT<1:0> bits are not used for override functions.

0 = Normal Fault mode: Current-limit feature maps CLDAT<1:0> bits to the PWMxH and PWMxL outputs. The PWM Fault feature maps FLTDAT<1:0> to the PWMxH and PWMxL outputs.

bit 14-10 **CLSRC<4:0>:** Current-Limit Control Signal Source Select for PWM # Generator bits(2,3)

00000 = Fault 1
00001 = Fault 2
00010 = Fault 3
00011 = Fault 4
00100 = Fault 5
00101 = Fault 6
00110 = Fault 7
00111 = Fault 8

01000 = Reserved
•
•
•
11111 = Reserved

bit 9 **CLPOL:** Current-Limit Polarity for PWM Generator # bit(1)

1 = The selected current-limit source is active-low
0 = The selected current-limit source is active-high

bit 8 **CLMOD:** Current-Limit Mode Enable bit for PWM Generator # bit

1 = Current-limit function is enabled
0 = Current-limit function is disabled

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

2: When Independent Fault mode is enabled (IFLTMOD = 1), and Fault 1 is used for Current-Limit mode (CLSRC<4:0> = b0000), the Fault Control Source Select bits (FLTSRC<4:0>) should be set to an unused Fault source to prevent Fault 1 from disabling both the PWMxL and PWMxH outputs.

3: When Independent Fault mode is enabled (IFLTMOD = 1) and Fault 1 is used for Fault mode (FLTSRC<4:0> = b0000), the Current-Limit Control Source Select bits (CLSRC<4:0>) should be set to an unused current-limit source to prevent the current-limit source from disabling both the PWMxH and PWMxL outputs.

REGISTER 15-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER (CONTINUED)

bit 7-3 **FLTSRC<4:0>:** Fault Control Signal Source Select for PWM Generator # bits(2,3)
00000 = Fault 1
00001 = Fault 2
00010 = Fault 3
00011 = Fault 4
00100 = Fault 5
00101 = Fault 6
00110 = Fault 7
00111 = Fault 8

01000 = Reserved
•
•
•
11111 = Reserved

bit 2 **FLTPOL:** Fault Polarity for PWM Generator # bit(1)
1 = The selected Fault source is active-low
0 = The selected Fault source is active-high

bit 1-0 **FLTMOD<1:0>:** Fault Mode for PWM Generator # bits
00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)
01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
10 = Reserved
11 = Fault input is disabled

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

2: When Independent Fault mode is enabled (IFLTMOD = 1), and Fault 1 is used for Current-Limit mode (CLSRC<4:0> = b0000), the Fault Control Source Select bits (FLTSRC<4:0>) should be set to an unused Fault source to prevent Fault 1 from disabling both the PWMxL and PWMxH outputs.

3: When Independent Fault mode is enabled (IFLTMOD = 1) and Fault 1 is used for Fault mode (FLTSRC<4:0> = b0000), the Current-Limit Control Source Select bits (CLSRC<4:0>) should be set to an unused current-limit source to prevent the current-limit source from disabling both the PWMxH and PWMxL outputs.

REGISTER 15-16: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
TRGCMP<7:3>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **TRGCMP<15:3>:** Trigger Control Value bits
When primary PWM functions in local time base, this register contains the compare values that can trigger the ADC module.

bit 2-0 **Unimplemented:** Read as ‘0’

REGISTER 15-17: STRIGx: PWMx SECONDARY TRIGGER COMPARE VALUE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STRGCMP<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
STRGCMP<7:3>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **STRGCMP<15:3>:** Secondary Trigger Control Value bits
When secondary PWM functions in local time base, this register contains the compare values that can trigger the ADC module.

bit 2-0 **Unimplemented:** Read as ‘0’

REGISTER 15-18: LEBCONx: LEADING-EDGE BLANKING CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	LEB<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
LEB<7:3>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
1 = Rising edge of PWMxH will trigger LEB counter
0 = LEB ignores rising edge of PWMxH

bit 14 **PHF:** PWMH Falling Edge Trigger Enable bit
1 = Falling edge of PWMxH will trigger LEB counter
0 = LEB ignores falling edge of PWMxH

bit 13 **PLR:** PWML Rising Edge Trigger Enable bit
1 = Rising edge of PWMxL will trigger LEB counter
0 = LEB ignores rising edge of PWMxL

bit 12 **PLF:** PWML Falling Edge Trigger Enable bit
1 = Falling edge of PWMxL will trigger LEB counter
0 = LEB ignores falling edge of PWMxL

bit 11 **FLTLEBEN:** Fault Input LEB Enable bit
1 = Leading-edge blanking is applied to selected Fault input
0 = Leading-edge blanking is not applied to selected Fault input

bit 10 **CLLEBEN:** Current-Limit LEB Enable bit
1 = Leading-edge blanking is applied to selected current-limit input
0 = Leading-edge blanking is not applied to selected current-limit input

bit 9-3 **LEB:** Leading-Edge Blanking for Current-Limit and Fault Inputs bits
Value is 8 nsec increments.

bit 2-0 **Unimplemented:** Read as ‘0’

REGISTER 15-19: PWMCAPx: PRIMARY PWMx TIME BASE CAPTURE REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PWMCAP<15:8>(1,2)							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	U-0	U-0	U-0
PWMCAP<7:3>(1,2)					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **PWMCAP<15:3>:** Captured PWM Time Base Value bits(1,2)
The value in this register represents the captured PWM time base value when a leading edge is detected on the current-limit input.

bit 2-0 **Unimplemented:** Read as ‘0’

Note 1: The capture feature is only available on primary output (PWMxH).

2: This feature is active only after LEB processing on the current-limit input signal is complete.

16.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*, **Section 18. "Serial Peripheral Interface (SPI)"** (DS70206), which is available on the Microchip web site (www.microchip.com).

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, analog-to-digital converters and so on. The SPI module is compatible with SPI and SIOP from Motorola®.

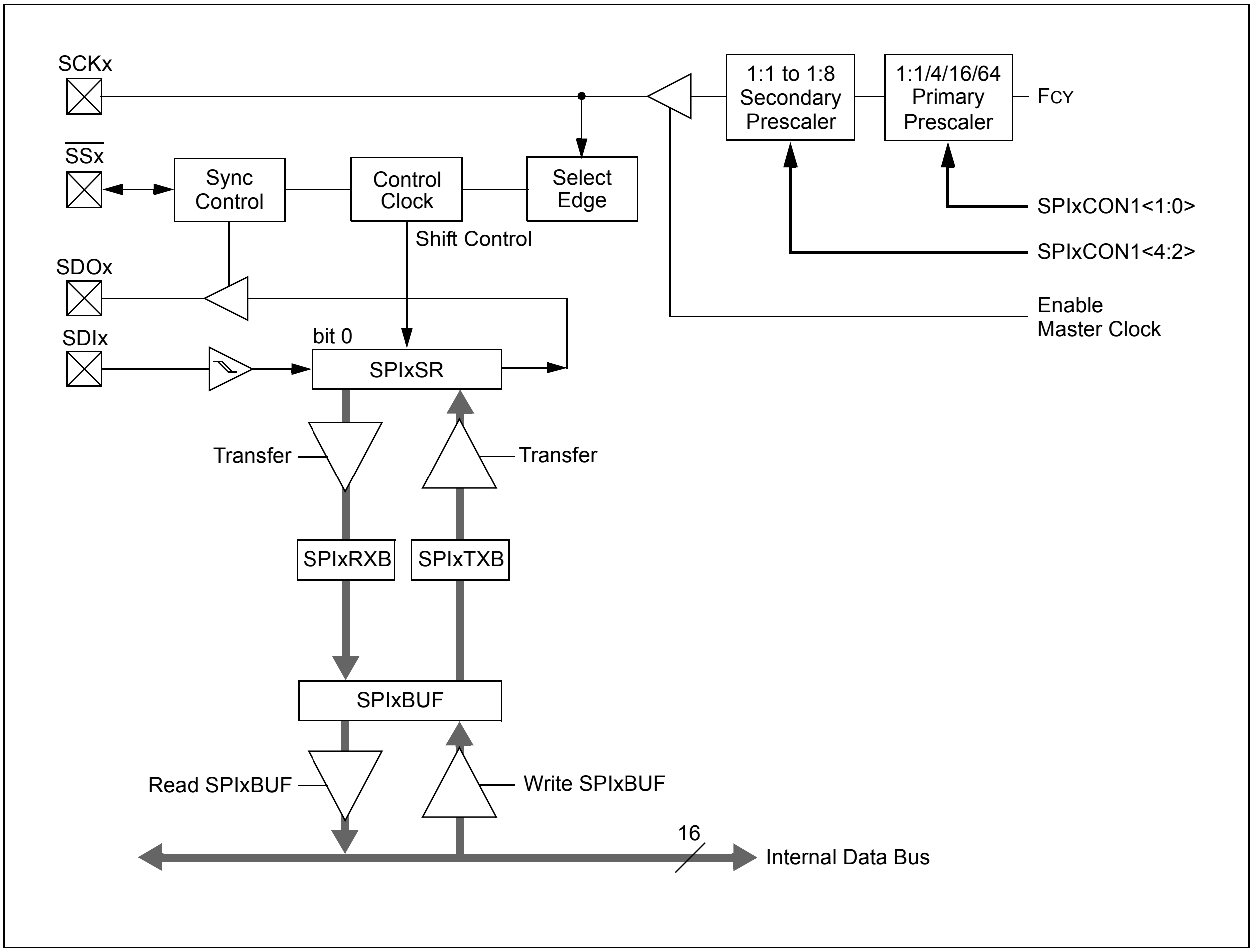
The SPI module consists of a 16-bit shift register, SPIxSR (where x = 1), used for shifting data in and out, and a buffer register, SPIxBUF. A control register, SPIxCON, configures the module. Additionally, a status register, SPIxSTAT, indicates status conditions.

The serial interface consists of the following four pins:

- SDIx (Serial Data Input)
- SDOx (Serial Data Output)
- $\overline{\text{SCKx}}$ (Shift Clock Input Or Output)
- $\overline{\text{SSx}}$ (Active-Low Slave Select).

In Master mode operation, SCK is a clock output; in Slave mode, it is a clock input.

FIGURE 16-1: SPI MODULE BLOCK DIAGRAM



REGISTER 16-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
SPIEN	—	SPISIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/C-0	U-0	U-0	U-0	U-0	R-0	R-0
—	SPIROV	—	—	—	—	SPITBF	SPIRBF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **SPIEN:** SPIx Enable bit
1 = Enables module and configures SCKx, SDOx, SDIx and $\overline{SSx}$ as serial port pins
0 = Disables module

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SPISIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-7 **Unimplemented:** Read as ‘0’

bit 6 **SPIROV:** Receive Overflow Flag bit
1 = A new byte/word is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
0 = No overflow has occurred

bit 5-2 **Unimplemented:** Read as ‘0’

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit
1 = Transmit not yet started, SPIxTXB is full
0 = Transmit started, SPIxTXB is empty. Automatically set in hardware when CPU writes SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit
1 = Receive complete, SPIxRXB is full
0 = Receive is not complete, SPIxRXB is empty. Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when core reads SPIxBUF location, reading SPIxRXB.

REGISTER 16-2: SPIxCON1: SPIx CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE[1]
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN[3]	CKP	MSTEN	SPRE<2:0>[2]			PPRE<1:0>[2]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **DISSCK:** Disable SCKx pin bit (SPI Master modes only)
1 = Internal SPI clock is disabled; pin functions as I/O
0 = Internal SPI clock is enabled

bit 11 **DISSDO:** Disable SDOx pin bit
1 = SDOx pin is not used by module; pin functions as I/O
0 = SDOx pin is controlled by the module

bit 10 **MODE16:** Word/Byte Communication Select bit
1 = Communication is word-wide (16 bits)
0 = Communication is byte-wide (8 bits)

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
Slave mode:
SMP must be cleared when SPIx is used in Slave mode.

bit 8 **CKE:** SPIx Clock Edge Select bit[1]
1 = Serial output data changes on transition from active clock state to Idle clock state (see bit 6)
0 = Serial output data changes on transition from Idle clock state to active clock state (see bit 6)

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)[3]
1 = $\overline{SSx}$ pin used for Slave mode
0 = $\overline{SSx}$ pin not used by module; pin controlled by port function

bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

Note 1: The CKE bit is not used in the Framed SPI modes. Program this bit to ‘0’ for the Framed SPI modes (FRMEN = 1).
2: Do not set both primary and secondary prescalers to a value of 1:1.
3: This bit must be cleared when FRMEN = 1.

REGISTER 16-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 4-2	**SPRE<2:0>:** Secondary Prescale bits (Master mode)(2) 111 = Secondary prescale 1:1 110 = Secondary prescale 2:1 . . . 000 = Secondary prescale 8:1
bit 1-0	**PPRE<1:0>:** Primary Prescale bits (Master mode)(2) 11 = Primary prescale 1:1 10 = Primary prescale 4:1 01 = Primary prescale 16:1 00 = Primary prescale 64:1

Note 1: The CKE bit is not used in the Framed SPI modes. Program this bit to ‘0’ for the Framed SPI modes (FRMEN = 1).

2: Do not set both primary and secondary prescalers to a value of 1:1.

3: This bit must be cleared when FRMEN = 1.

REGISTER 16-3: SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	FRMPOL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	FRMDLY	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **FRMEN**: Framed SPIx Support bit
1 = Framed SPIx support enabled ($\overline{SSx}$ pin used as frame sync pulse input/output)
0 = Framed SPIx support disabled

bit 14 **SPIFSD**: Frame Sync Pulse Direction Control bit
1 = Frame sync pulse input (slave)
0 = Frame sync pulse output (master)

bit 13 **FRMPOL**: Frame Sync Pulse Polarity bit
1 = Frame sync pulse is active-high
0 = Frame sync pulse is active-low

bit 12-2 **Unimplemented:** Read as ‘0’

bit 1 **FRMDLY**: Frame Sync Pulse Edge Select bit
1 = Frame sync pulse coincides with first bit clock
0 = Frame sync pulse precedes first bit clock

bit 0 **Unimplemented:** This bit must not be set to ‘1’ by the user application

NOTES:

17.0 INTER-INTEGRATED CIRCUIT (I^2C™)

> **Note:** This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*, **Section 19. "Inter-Integrated Circuit (I^2C™)"** (DS70195), which is available on the Microchip web site (www.microchip.com).

The Inter-Integrated Circuit (I^2C) module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard with a 16-bit interface.

The I^2C module has a 2-pin interface:

- The SCLx pin is clock.
- The SDAx pin is data.

The I^2C module offers the following key features:

- I^2C interface supporting both Master and Slave modes of operation.
- I^2C Slave mode supports 7-bit and 10-bit addressing.
- I^2C Master mode supports 7-bit and 10-bit addressing.
- I^2C port allows bidirectional transfers between master and slaves.
- Serial clock synchronization for I^2C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control).
- I^2C supports multi-master operation, detects bus collision and arbitrates accordingly.

17.1 Operating Modes

The hardware fully implements all the master and slave functions of the I^2C Standard and Fast mode specifications, as well as 7-bit and 10-bit addressing.

The I^2C module can operate either as a slave or a master on an I^2C bus.

The following types of I^2C operation are supported:

- I^2C slave operation with 7-bit addressing
- I^2C slave operation with 10-bit addressing
- I^2C master operation with 7-bit or 10-bit addressing

For details about the communication sequence in each of these modes, refer to the "*dsPIC33F Family Reference Manual*". Please see the Microchip web site (www.microchip.com) for the latest *"dsPIC33F Family Reference Manual"* chapters.

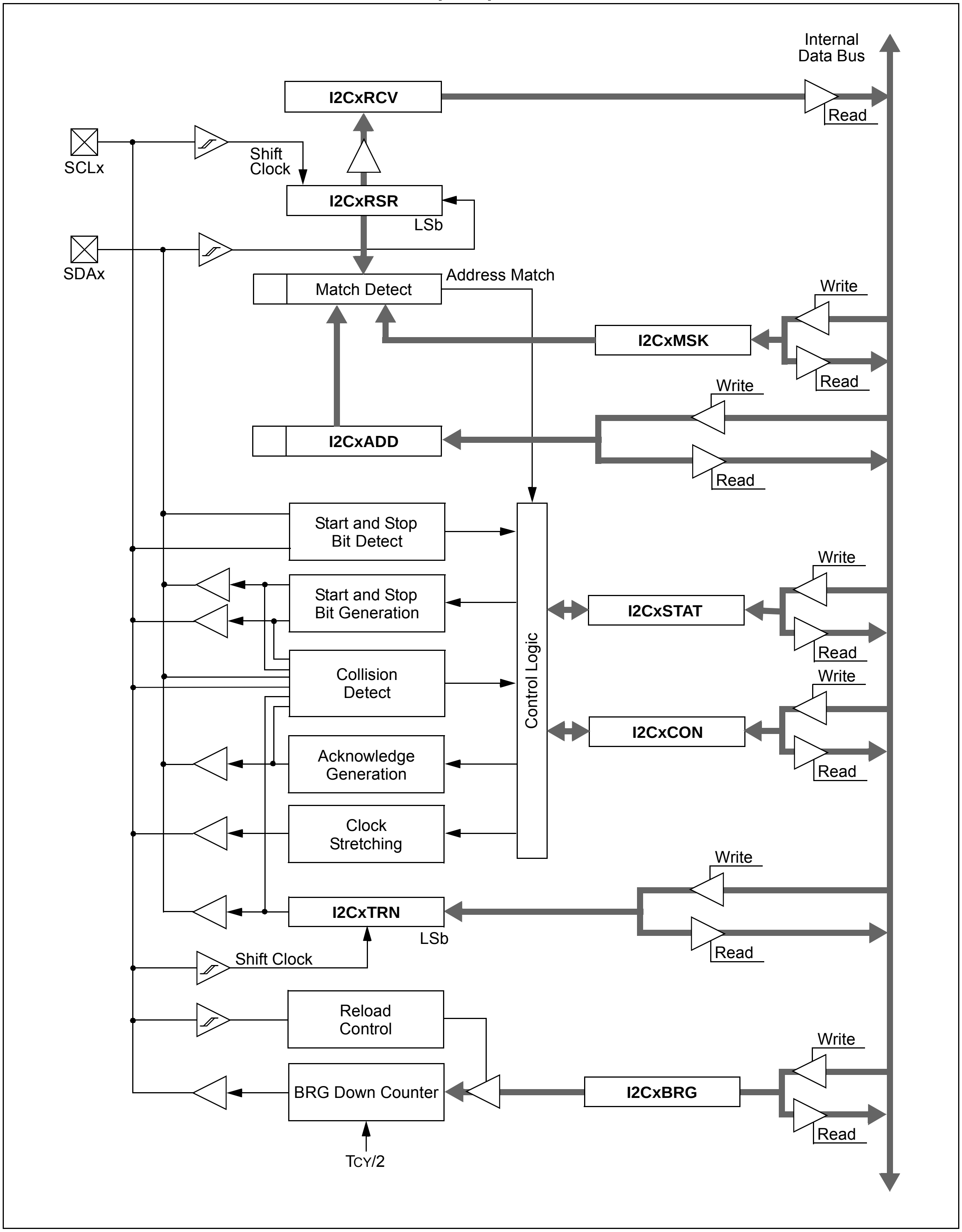
17.2 I^2C Registers

I2CxCON and I2CxSTAT are control and status registers, respectively. The I2CxCON register is readable and writable. The lower six bits of I2CxSTAT are read-only. The remaining bits of the I2CSTAT are read/write:

- I2CxRSR is the shift register used for shifting data internal to the module and the user application has no access to it.
- I2CxRCV is the receive buffer and the register to which data bytes are written, or from which data bytes are read.
- I2CxTRN is the transmit register to which bytes are written during a transmit operation.
- The I2CxADD register holds the slave address.
- A status bit, ADD10, indicates 10-Bit Address mode.
- The I2CxBRG acts as the Baud Rate Generator (BRG) reload value.

In receive operations, I2CxRSR and I2CxRCV together form a double-buffered receiver. When I2CxRSR receives a complete byte, it is transferred to I2CxRCV, and an interrupt pulse is generated.

FIGURE 17-1: I²C™ BLOCK DIAGRAM (x = 1)



REGISTER 17-1: I2CxCON: I2Cx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as ‘0’		
R = Readable bit	W = Writable bit	HS = Hardware Settable bit	HC = Hardware Clearable bit
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **I2CEN:** I2Cx Enable bit
1 = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins
0 = Disables the I2Cx module. All I^2C pins are controlled by port functions.

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **I2CSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters an Idle mode
0 = Continue module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I^2C slave)
1 = Release SCLx clock
0 = Hold SCLx clock low (clock stretch)
If STREN = 1:
Bit is R/W (i.e., software can write ‘0’ to initiate stretch and write ‘1’ to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.
If STREN = 0:
Bit is R/S (i.e., software can only write ‘1’ to release clock). Hardware clear at beginning of slave transmission.

bit 11 **IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit
1 = IPMI mode is enabled; all addresses acknowledged
0 = IPMI mode disabled

bit 10 **A10M:** 10-Bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control disabled
0 = Slew rate control enabled

bit 8 **SMEN:** SMbus Input Levels bit
1 = Enable I/O pin thresholds compliant with SMbus specification
0 = Disable SMbus input thresholds

bit 7 **GCEN:** General Call Enable bit (when operating as I^2C slave)
1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address disabled

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^2C slave)
Used in conjunction with SCLREL bit.
1 = Enable software or receive clock stretching
0 = Disable software or receive clock stretching

REGISTER 17-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 5	**ACKDT:** Acknowledge Data bit (when operating as I^2C master, applicable during master receive) Value that is transmitted when the software initiates an Acknowledge sequence. `1` = Send NACK during Acknowledge `0` = Send ACK during Acknowledge
bit 4	**ACKEN:** Acknowledge Sequence Enable bit (when operating as I^2C master, applicable during master receive) `1` = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit. Hardware clear at end of master Acknowledge sequence. `0` = Acknowledge sequence not in progress
bit 3	**RCEN:** Receive Enable bit (when operating as I^2C master) `1` = Enables Receive mode for I^2C. Hardware clear at end of eighth bit of master receive data byte. `0` = Receive sequence not in progress
bit 2	**PEN:** Stop Condition Enable bit (when operating as I^2C master) `1` = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence. `0` = Stop condition not in progress
bit 1	**RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master) `1` = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of master Repeated Start sequence. `0` = Repeated Start condition not in progress
bit 0	**SEN:** Start Condition Enable bit (when operating as I^2C master) `1` = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence. `0` = Start condition not in progress

REGISTER 17-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HSC	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7							bit 0

Legend:	U = Unimplemented bit, read as ‘0’		
R = Readable bit	W = Writable bit	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I^{2}C master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^{2}C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13-11 **Unimplemented:** Read as ‘0’

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I^{2}C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as I^{2}C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
Hardware clear at device address match. Hardware set by reception of slave byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

REGISTER 17-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 3	**S:** Start bit 1 = Indicates that a Start (or Repeated Start) bit has been detected last 0 = Start bit was not detected last Hardware set or clear when Start, Repeated Start or Stop detected.
bit 2	**R_W:** Read/Write Information bit (when operating as I^2C slave) 1 = Read – indicates data transfer is output from slave 0 = Write – indicates data transfer is input to slave Hardware set or clear after reception of I^2C device address byte.
bit 1	**RBF:** Receive Buffer Full Status bit 1 = Receive complete, I2CxRCV is full 0 = Receive not complete, I2CxRCV is empty Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.
bit 0	**TBF:** Transmit Buffer Full Status bit 1 = Transmit in progress, I2CxTRN is full 0 = Transmit complete, I2CxTRN is empty Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

REGISTER 17-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	AMSK<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **AMSK<9:0>:** Mask for Address bit x Select bits
1 = Enable masking for bit x of incoming message address; bit match not required in this position
0 = Disable masking for bit x; bit match required in this position

NOTES:

18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*, **Section 17. "UART"** (DS70188), which is available on the Microchip web site (www.microchip.com).

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 device families. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins and also includes an IrDA® encoder and decoder.

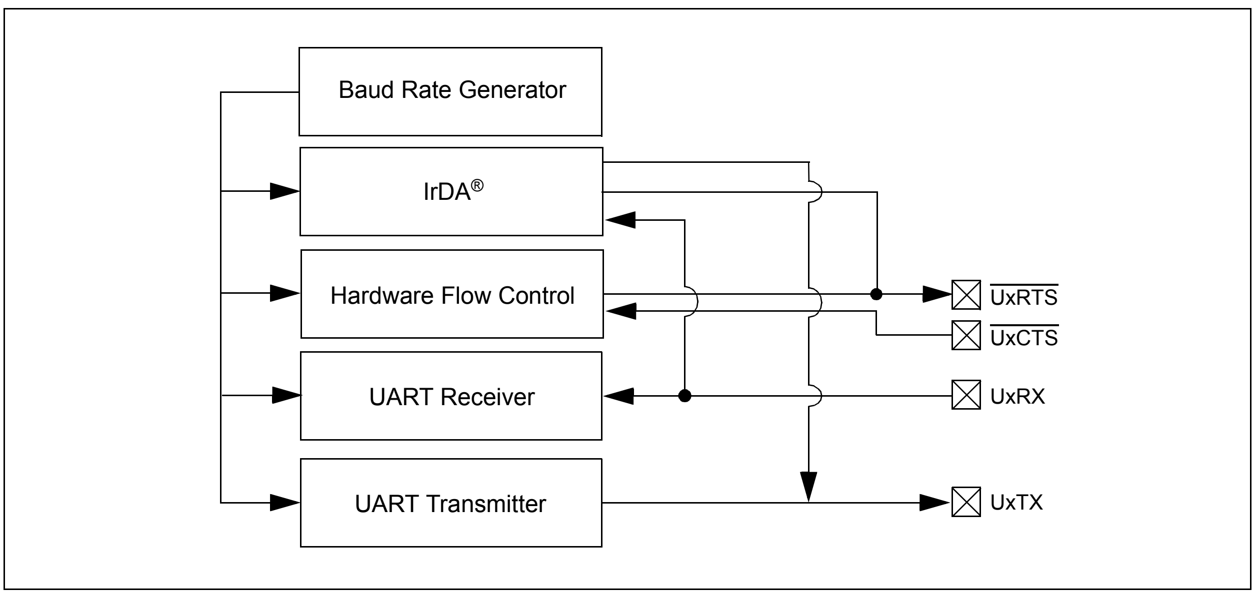
The primary features of the UART module are:

- Full-Duplex, 8-Bit or 9-Bit Data Transmission through the UxTX and UxRX pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 1 Mbps to 15 bps at 16x mode at 40 MIPS
- Baud Rates Ranging from 4 Mbps to 61 bps at 4x mode at 40 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = `1`)
- Transmit and Receive Interrupts
- A Separate Interrupt for all UART Error Conditions
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA® Support

A simplified block diagram of the UART module is shown in Figure 18-1. The UART module consists of these key hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

FIGURE 18-1: UART SIMPLIFIED BLOCK DIAGRAM



REGISTER 18-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN(1)	—	USIDL	IREN(2)	RTSMD	—	UEN<1:0>	
bit 15							bit 8

R/W-0 HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL
bit 7							bit 0

Legend:	HC = Hardware Clearable		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **UARTEN:** UARTx Enable bit(1)
- 1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
- 0 = UARTx is disabled; all UARTx pins are controlled by port latches; UARTx power consumption minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **USIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit(2)
- 1 = IrDA® encoder and decoder enabled
- 0 = IrDA® encoder and decoder disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits
- 11 = UxTX, UxRX and BCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin controlled by port latches
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin controlled by port latches
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/BCLK pins controlled by port latches

bit 7 **WAKE:** Wake-up on Start bit Detect During Sleep Mode Enable bit
- 1 = UARTx will continue to sample the UxRX pin; interrupt generated on falling edge; bit cleared in hardware on following rising edge
- 0 = No wake-up enabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Enable Loopback mode
- 0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
- 1 = Enable baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion
- 0 = Baud rate measurement disabled or completed

bit 4 **URXINV:** Receive Polarity Inversion bit
- 1 = UxRX Idle state is '0'
- 0 = UxRX Idle state is '1'

Note 1: Refer to **Section 17. "UART"** (DS70188) in the *"dsPIC33F Family Reference Manual"* for information on enabling the UART module for receive or transmit operation.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

REGISTER 18-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 3	**BRGH:** High Baud Rate Enable bit 1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode) 0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
bit 2-1	**PDSEL<1:0>:** Parity and Data Selection bits 11 = 9-bit data, no parity 10 = 8-bit data, odd parity 01 = 8-bit data, even parity 00 = 8-bit data, no parity
bit 0	**STSEL:** Stop Bit Selection bit 1 = Two Stop bits 0 = One Stop bit

Note 1: Refer to **Section 17. "UART"** (DS70188) in the *"dsPIC33F Family Reference Manual"* for information on enabling the UART module for receive or transmit operation.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

REGISTER 18-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN(1)	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15,13 **UTXISEL<1:0>:** Transmission Interrupt Mode Selection bits
- `11` = Reserved; do not use
- `10` = Interrupt when a character is transferred to the Transmit Shift register, and as a result, the transmit buffer becomes empty
- `01` = Interrupt when the last character is shifted out of the Transmit Shift register; all transmit operations are completed
- `00` = Interrupt when a character is transferred to the Transmit Shift register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** Transmit Polarity Inversion bit

If IREN = `0`:
- `1` = UxTX Idle state is ‘`0`’
- `0` = UxTX Idle state is ‘`1`’

If IREN = `1`:
- `1` = IrDA® encoded UxTX Idle state is ‘`1`’
- `0` = IrDA® encoded UxTX Idle state is ‘`0`’

bit 12 **Unimplemented:** Read as ‘`0`’

bit 11 **UTXBRK:** Transmit Break bit
- `1` = Send Sync Break on next transmission – Start bit, followed by twelve ‘`0`’ bits, followed by Stop bit; cleared by hardware upon completion
- `0` = Sync Break transmission disabled or completed

bit 10 **UTXEN:** Transmit Enable bit(1)
- `1` = Transmit enabled, UxTX pin controlled by UARTx
- `0` = Transmit disabled, any pending transmission is aborted and buffer is reset; UxTX pin controlled by port

bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)
- `1` = Transmit buffer is full
- `0` = Transmit buffer is not full; at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- `1` = Transmit Shift register is empty and transmit buffer is empty (the last transmission has completed)
- `0` = Transmit Shift register is not empty, a transmission is in progress or queued

bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bits
- `11` = Interrupt is set on UxRSR transfer making the receive buffer full (i.e., has 4 data characters)
- `10` = Interrupt is set on UxRSR transfer making the receive buffer 3/4 full (i.e., has 3 data characters)
- `0x` = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters

Note 1: Refer to **Section 17. “UART”** (DS70188) in the *“dsPIC33F Family Reference Manual”* for information on enabling the UART module for transmit operation.

REGISTER 18-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
- 1 = Address Detect mode enabled. If 9-bit mode is not selected, this does not take effect.
- 0 = Address Detect mode disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
- 1 = Receiver is Idle
- 0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (read-only)
- 1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
- 0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
- 1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
- 0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)
- 1 = Receive buffer has overflowed
- 0 = Receive buffer has not overflowed. Clearing a previously set OERR bit (1 → 0 transition) will reset the receiver buffer and the UxRSR to the empty state.

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
- 1 = Receive buffer has data, at least one more character can be read
- 0 = Receive buffer is empty

Note 1: Refer to **Section 17. “UART”** (DS70188) in the *“dsPIC33F Family Reference Manual”* for information on enabling the UART module for transmit operation.

NOTES:

19.0 HIGH-SPEED 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*, **Section 44. "High-Speed 10-Bit Analog-to-Digital Converter (ADC)"** (DS70321), which is available on the Microchip web site (www.microchip.com).

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices provide high-speed successive approximation analog to digital conversions to support applications such as AC/DC and DC/DC power converters.

19.1 Features Overview

The ADC module comprises the following features:

- 10-bit resolution
- Unipolar inputs
- Up to two Successive Approximation Registers (SARs)
- Up to 12 external input channels
- Up to two internal analog inputs
- Dedicated result register for each analog input
- ±1 LSB accuracy at 3.3V
- Single supply operation
- 4 Msps conversion rate at 3.3V (devices with two SARs)
- 2 Msps conversion rate at 3.3V (devices with one SAR)
- Low-power CMOS technology

19.2 Module Description

This ADC module is designed for applications that require low latency between the request for conversion and the resultant output data. Typical applications include:

- AC/DC power supplies
- DC/DC converters
- Power Factor Correction (PFC)

This ADC works with the high-speed PWM module in power control applications that require high-frequency control loops. This module can sample and convert two analog inputs in a 0.5 microsecond when two SARs are used. This small conversion delay reduces the "phase lag" between measurement and control system response.

Up to five inputs may be sampled at a time (four inputs from the dedicated sample and hold circuits and one from the shared sample and hold circuit). If multiple inputs request conversion, the ADC will convert them in a sequential manner, starting with the lowest order input.

This ADC design provides each pair of analog inputs (AN1,AN0), (AN3,AN2),..., the ability to specify its own trigger source out of a maximum of sixteen different trigger sources. This capability allows this ADC to sample and convert analog inputs that are associated with PWM generators operating on independent time bases.

The user application typically requires synchronization between analog data sampling and PWM output to the application circuit. The very high-speed operation of this ADC module allows "data on demand".

In addition, several hardware features have been added to the peripheral interface to improve real-time performance in a typical DSP based application.

- Result alignment options
- Automated sampling
- External conversion start control
- Two internal inputs to monitor 1.2V internal reference and EXTREF input signal

A block diagram of the ADC module is shown in Figure 19-6.

19.3 Module Functionality

The high-speed 10-bit ADC module is designed to support power conversion applications when used with the High-Speed PWM module. The ADC may have one or two SAR modules, depending on the device variant. If two SARs are present on a device, two conversions can be processed at a time, yielding 4 Msps conversion rate. If only one SAR is present on a device, only one conversion can be processed at a time, yielding 2 Msps conversion rate. The high-speed 10-bit ADC produces two 10-bit conversion results in a 0.5 microsecond.

The ADC module supports up to 12 external analog inputs and two internal analog inputs. To monitor reference voltage, two internal inputs, AN12 and AN13, are connected to the EXTREF and internal band gap voltages (1.2V), respectively.

The analog reference voltage is defined as the device supply voltage (AV_{DD}/AV_{SS}).

The ADC module uses the following control and status registers:

- ADCON: A/D Control Register
- ADSTAT: A/D Status Register
- ADBASE: A/D Base Register(1,2)
- ADPCFG: A/D Port Configuration Register
- ADCPC0: A/D Convert Pair Control Register 0
- ADCPC1: A/D Convert Pair Control Register 1
- ADCPC2: A/D Convert Pair Control Register 2(1)
- ADCPC3: A/D Convert Pair Control Register 3(1)

The ADCON register controls the operation of the ADC module. The ADSTAT register displays the status of the conversion processes. The ADPCFG registers configure the port pins as analog inputs or as digital I/O. The ADCPCx registers control the triggering of the ADC conversions. See Register 19-1 through Register 19-8 for detailed bit configurations.

Note:	A unique feature of the ADC module is its ability to sample inputs in an asynchronous manner. Individual sample and hold circuits can be triggered independently of each other.

FIGURE 19-1: ADC BLOCK DIAGRAM FOR dsPIC33FJ06GS101 DEVICES WITH ONE SAR

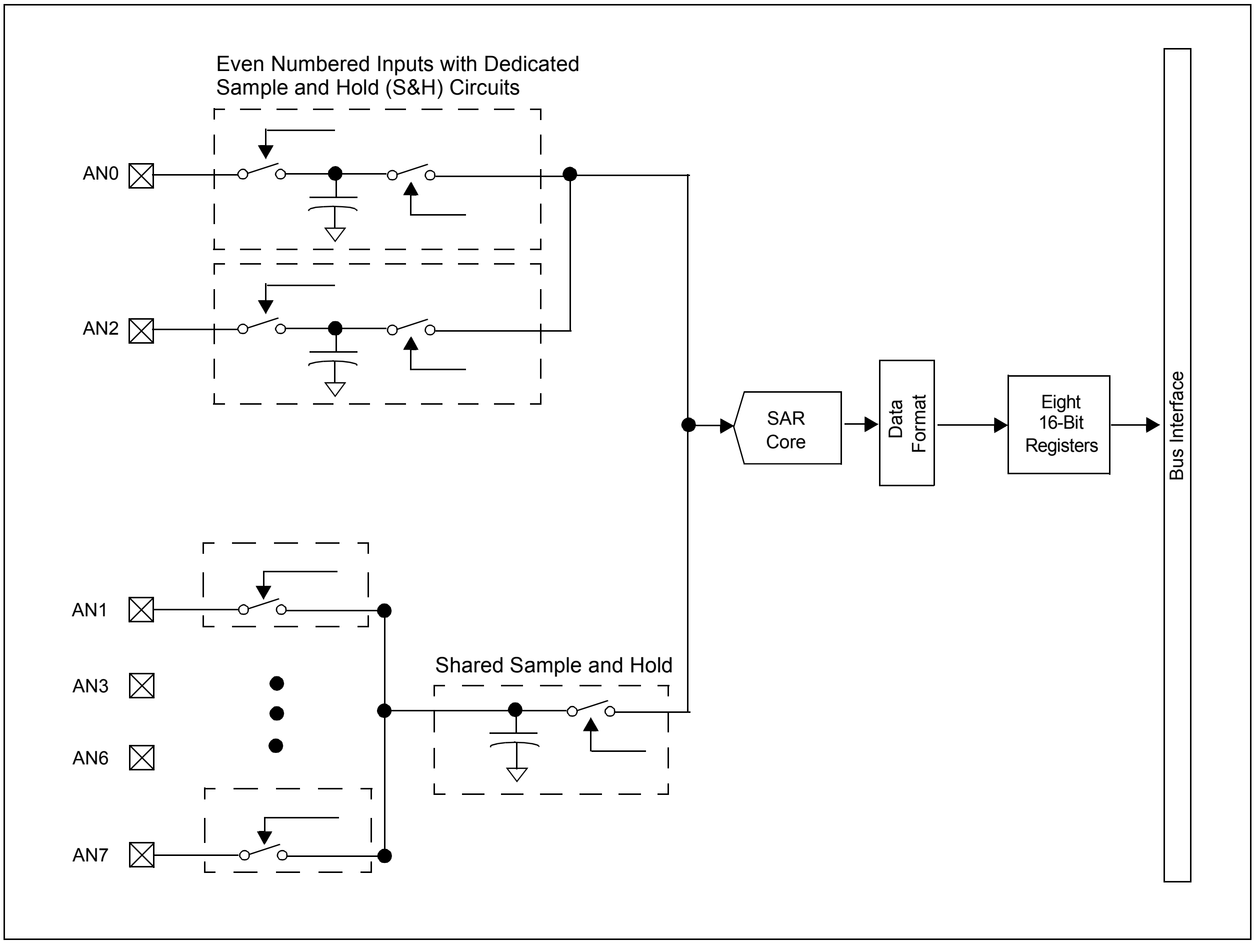
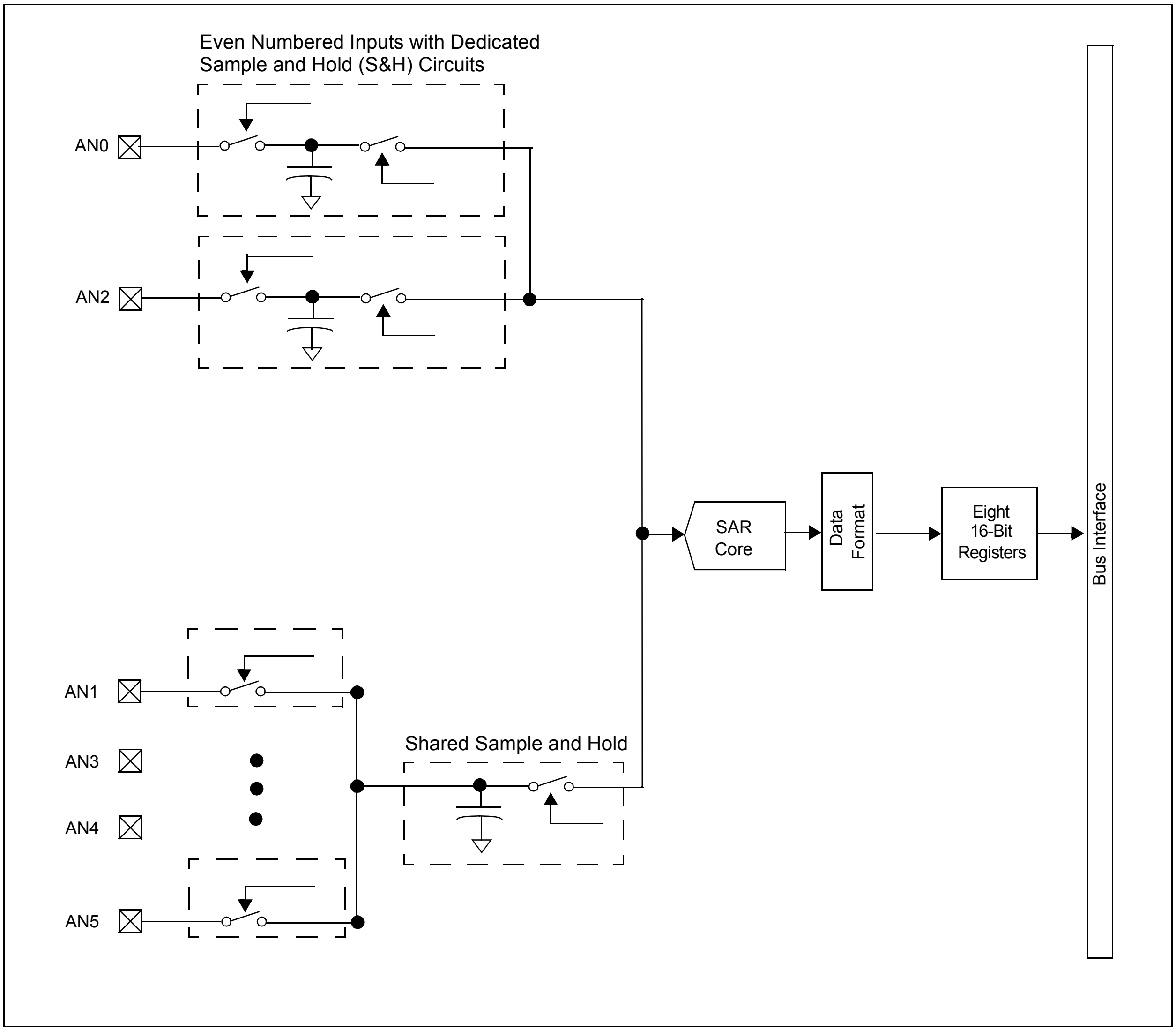
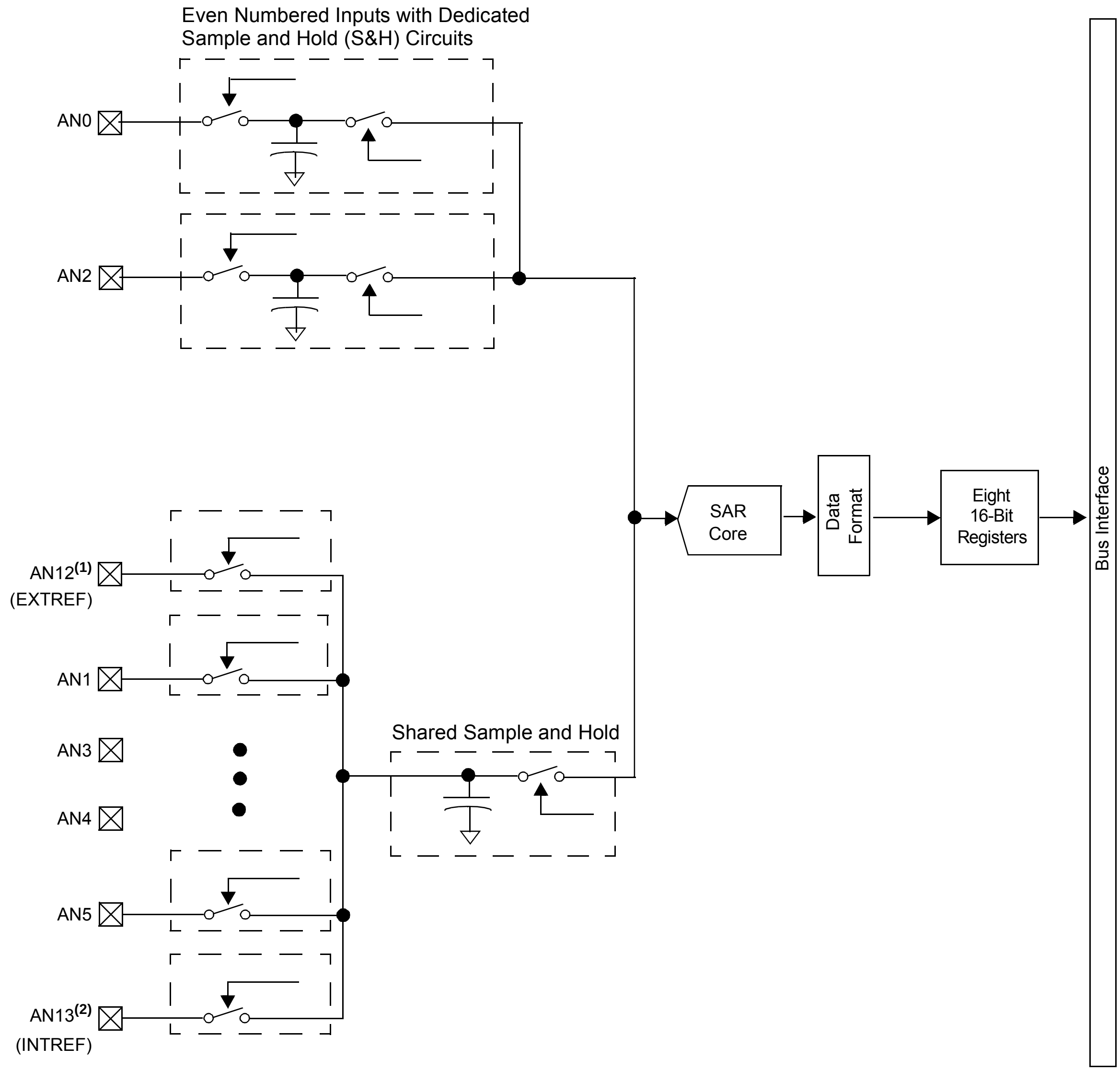


FIGURE 19-2: ADC BLOCK DIAGRAM FOR dsPIC33FJ06GS102 DEVICES WITH ONE SAR



 Preliminary

FIGURE 19-3: ADC BLOCK DIAGRAM FOR dsPIC33FJ06GS202 DEVICES WITH ONE SAR



Note 1: AN12 (EXTREF) is an internal analog input. To measure the voltage at AN12 (EXTREF), an analog comparator must be enabled and EXTREF must be selected as the comparator reference.

2: AN13 (INTREF) is an internal analog input and is not available on a pin.

FIGURE 19-4: ADC BLOCK DIAGRAM FOR dsPIC33FJ16GS402/404 DEVICES WITH ONE SAR

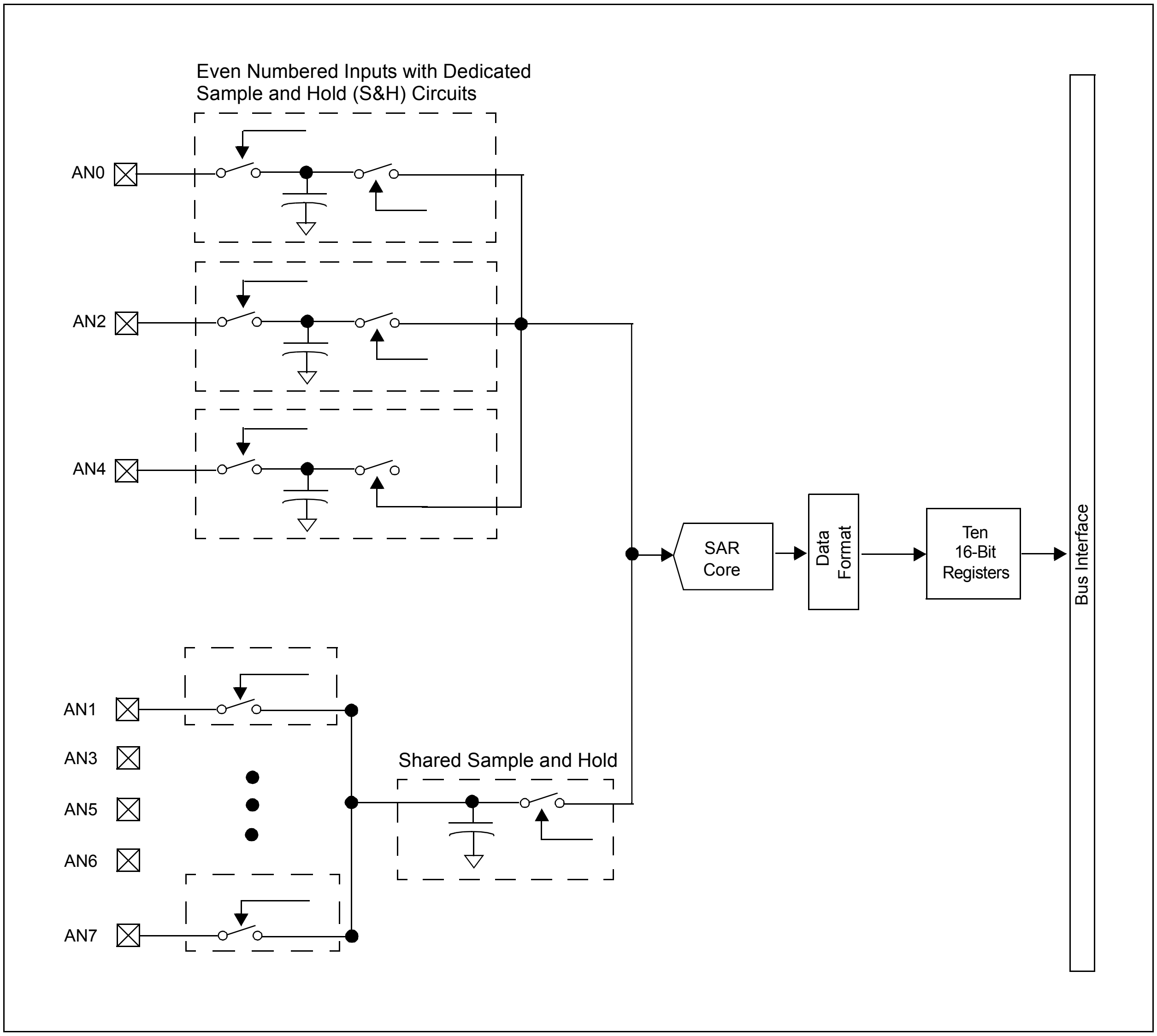
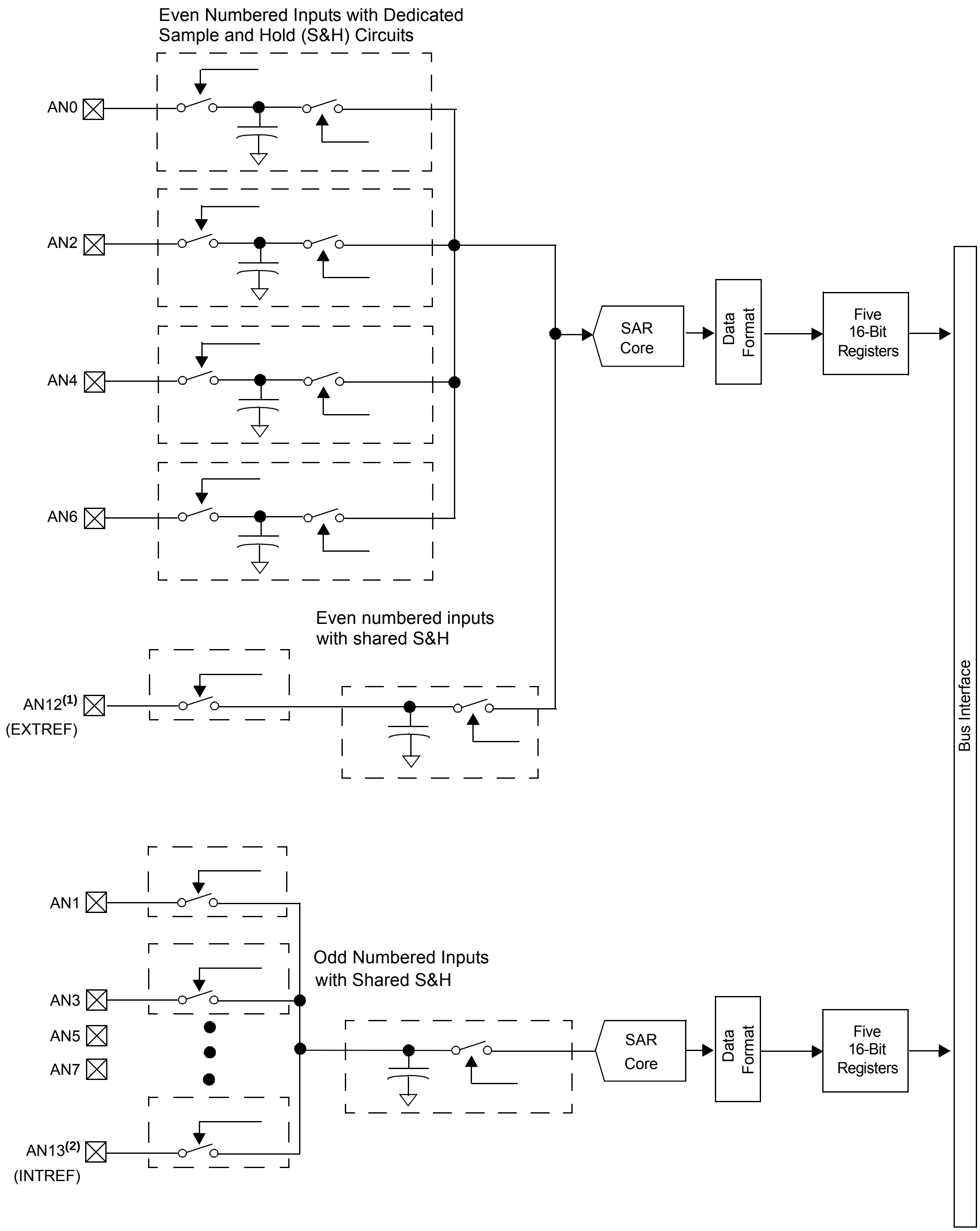


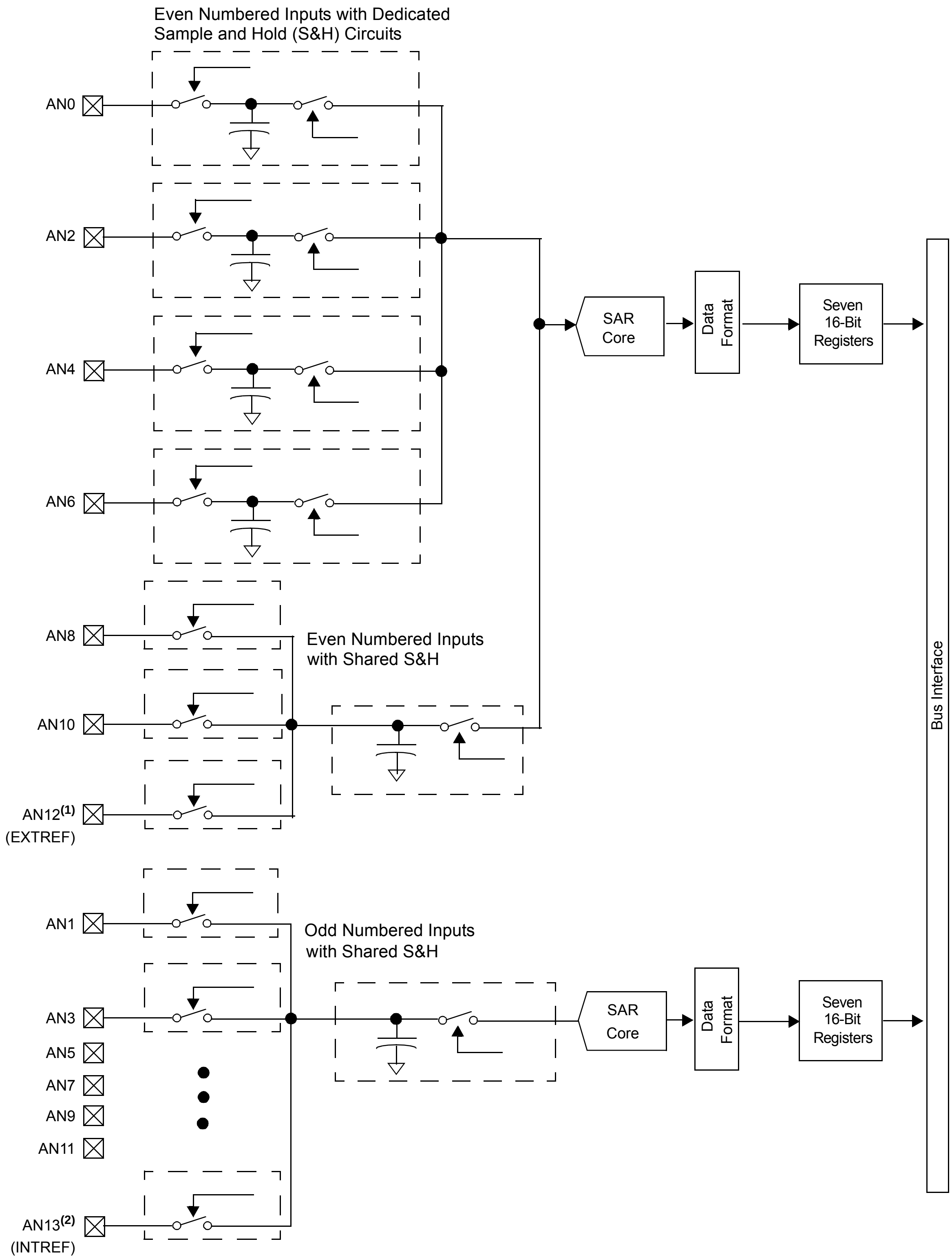
FIGURE 19-5: ADC BLOCK DIAGRAM FOR dsPIC33FJ16GS502 DEVICES WITH TWO SARS



Note 1: AN12 (EXTREF) is an internal analog input. To measure the voltage at AN12 (EXTREF), an analog comparator must be enabled and EXTREF must be selected as the comparator reference.

2: AN13 (INTREF) is an internal analog input and is not available on a pin.

FIGURE 19-6: ADC BLOCK DIAGRAM FOR dsPIC33FJ16GS504 DEVICES WITH TWO SARS



Note 1: AN12 (EXTREF) is an internal analog input. To measure the voltage at AN12 (EXTREF), an analog comparator must be enabled and EXTREF must be selected as the comparator reference.

2: AN13 (INTREF) is an internal analog input and is not available on a pin.

REGISTER 19-1: ADCON: A/D CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0
ADON	—	ADSIDL	SLOWCLK(1)	—	GSWTRG	—	FORM(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-1	R/W-1
EIE(1)	ORDER(1)	SEQSAMP(1)	ASYNCSAMP(1)	—	ADCS<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADON:** A/D Operating Mode bit
1 = A/D converter module is operating
0 = A/D converter is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **SLOWCLK:** Enable The Slow Clock Divider bit(1)
1 = ADC is clocked by the auxiliary PLL (ACLK)
0 = ADC is clock by the primary PLL (FVCO)

bit 11 **Unimplemented:** Read as '0'

bit 10 **GSWTRG:** Global Software Trigger bit
When this bit is set by the user, it will trigger conversions if selected by the TRGSRC<4:0> bits in the ADCPCx registers. This bit must be cleared by the user prior to initiating another global trigger (i.e., this bit is not auto-clearing).

bit 9 **Unimplemented:** Read as '0'

bit 8 **FORM:** Data Output Format bit(1)
1 = Fractional (DOUT = dddd dddd dd00 0000)
0 = Integer (DOUT = 0000 00dd dddd dddd)

bit 7 **EIE:** Early Interrupt Enable bit(1)
1 = Interrupt is generated after first conversion is completed
0 = Interrupt is generated after second conversion is completed

bit 6 **ORDER:** Conversion Order bit(1)
1 = Odd numbered analog input is converted first, followed by conversion of even numbered input
0 = Even numbered analog input is converted first, followed by conversion of odd numbered input

bit 5 **SEQSAMP:** Sequential Sample Enable bit(1)
1 = Shared Sample and Hold (S&H) circuit is sampled at the start of the second conversion if ORDER = 0. If ORDER = 1, then the shared S&H is sampled at the start of the first conversion.
0 = Shared S&H is sampled at the same time the dedicated S&H is sampled if the shared S&H is not currently busy with an existing conversion process. If the shared S&H is busy at the time the dedicated S&H is sampled, then the shared S&H will sample at the start of the new conversion cycle.

Note 1: This control bit can only be changed while ADC is disabled (ADON = 0), and only applies to single SAR devices.

REGISTER 19-1: ADCON: A/D CONTROL REGISTER (CONTINUED)

bit 4 **ASYNCSAMP:** Asynchronous Dedicated S&H Sampling Enable bit(1)

1 = The dedicated S&H is constantly sampling and then terminates sampling as soon as the trigger pulse is detected.

0 = The dedicated S&H starts sampling when the trigger event is detected and completes the sampling process in two ADC clock cycles.

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Divider Select bits(1)

111 = FADC/8
110 = FADC/7
101 = FADC/6
100 = FADC/5
011 = FADC/4 (default)
010 = FADC/3
001 = FADC/2
000 = FADC/1

Note 1: This control bit can only be changed while ADC is disabled (ADON = 0), and only applies to single SAR devices.

REGISTER 19-2: ADSTAT: A/D STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/C-0, HS	R/C-0, HS	R/C-0, HS	R/C-0, HS	R/C-0, HS	R/C-0, HS	R/C-0, HS
—	P6RDY(1)	P5RDY(2)	P4RDY(2)	P3RDY(3)	P2RDY(4)	P1RDY	P0RDY
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
C = Clearable bit	HS = Hardware Settable bit		

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **P6RDY:** Conversion Data for Pair 6 Ready bit(1)
Bit is set when data is ready in buffer, cleared when a '0' is written to this bit.

bit 5 **P5RDY:** Conversion Data for Pair 5 Ready bit(2)
Bit is set when data is ready in buffer, cleared when a '0' is written to this bit.

bit 4 **P4RDY:** Conversion Data for Pair 4 Ready bit(2)
Bit is set when data is ready in buffer, cleared when a '0' is written to this bit.

bit 3 **P3RDY:** Conversion Data for Pair 3 Ready bit(3)
Bit is set when data is ready in buffer, cleared when a '0' is written to this bit.

bit 2 **P2RDY:** Conversion Data for Pair 2 Ready bit(4)
Bit is set when data is ready in buffer, cleared when a '0' is written to this bit.

bit 1 **P1RDY:** Conversion Data for Pair 1 Ready bit
Bit is set when data is ready in buffer, cleared when a '0' is written to this bit.

bit 0 **P0RDY:** Conversion Data for Pair 0 Ready bit
Bit is set when data is ready in buffer, cleared when a '0' is written to this bit.

Note 1: This bit is available in the dsPIC33FJ16GS502, dsPIC33FJ16GS504 and dsPIC33FJ06GS202 devices only.

2: This bit is available in the dsPIC33FJ16GS504 devices only.

3: This bit is available in the dsPIC33FJ16GS402/404, dsPIC33FJ16GS502, dsPIC33FJ16GS504 and dsPIC33FJ06GS101 devices only.

4: This bit is available in the dsPIC33FJ16GS504 and dsPIC33FJ16GS502 devices only.

REGISTER 19-3: ADBASE: A/D BASE REGISTER[1,2]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADBASE<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
ADBASE<7:1>							—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1 **ADBASE<15:1>:** This register contains the base address of the user's ADC Interrupt Service Routine jump table. This register, when read, contains the sum of the ADBASE register contents and the encoded value of the PxRDY status bits.

The encoder logic provides the bit number of the highest priority PxRDY bits where P0RDY is the highest priority, and P6RDY is the lowest priority.

bit 0 **Unimplemented:** Read as '0'

Note 1: The encoding results are shifted left two bits so bits 1-0 of the result are always zero.

2: As an alternative to using the ADBASE Register, the ADCP0-6 ADC Pair Conversion Complete Interrupts can be used to invoke A to D conversion completion routines for individual ADC input pairs.

REGISTER 19-4: ADPCFG: A/D PORT CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	PCFG11	PCFG10	PCFG9	PCFG8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **PCFG<11:0>:** A/D Port Configuration Control bits[1,2,3,4]

1 = Port pin in Digital mode, port read input enabled, A/D input multiplexor connected to AVSS
0 = Port pin in Analog mode, port read input disabled, A/D samples pin voltage

Note: Not all PCFGx bits are available on all devices. See Figure 19-1 through Figure 19-6 for the available analog pins (PCFGx = ANx, where x = 0-11).

REGISTER 19-5: ADCPC0: A/D CONVERT PAIR CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN1	PEND1	SWTRG1	TRGSRC1<4:0>				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN0	PEND0	SWTRG0	TRGSRC0<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **IRQEN1:** Interrupt Request Enable 1 bit
1 = Enable IRQ generation when requested conversion of channels AN3 and AN2 is completed
0 = IRQ is not generated

bit 14 **PEND1:** Pending Conversion Status 1 bit
1 = Conversion of channels AN3 and AN2 is pending. Set when selected trigger is asserted
0 = Conversion is complete

bit 13 **SWTRG1:** Software Trigger 1 bit
1 = Start conversion of AN3 and AN2 (if selected in TRGSRC bits)(1)
This bit is automatically cleared by hardware when the PEND1 bit is set.
0 = Conversion is not started

bit 12-8 **TRGSRC1<4:0>:** Trigger 1 Source Selection bits
Selects trigger source for conversion of analog channels AN3 and AN2.
00000 = No conversion enabled
00001 = Individual software trigger selected
00010 = Global software trigger selected
00011 = PWM Special Event Trigger selected
00100 = PWM Generator 1 primary trigger selected
00101 = PWM Generator 2 primary trigger selected
00110 = PWM Generator 3 primary trigger selected
00111 = PWM Generator 4 primary trigger selected
01000 = Reserved
•
•
•
01100 = Timer1 period match
01101 = Reserved
01110 = PWM Generator 1 secondary trigger selected
01111 = PWM Generator 2 secondary trigger selected
10000 = PWM Generator 3 secondary trigger selected
10001 = PWM Generator 4 secondary trigger selected
10010 = Reserved
•
•
•
10110 = Reserved
10111 = PWM Generator 1 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11010 = PWM Generator 4 current-limit ADC trigger
11011 = Reserved
•
•
•
11111 = Timer2 period match

Note 1: If other conversions are in progress, then conversion will be performed when the conversion resources are available.

REGISTER 19-5: ADCPC0: A/D CONVERT PAIR CONTROL REGISTER 0 (CONTINUED)

bit 7	**IRQEN0:** Interrupt Request Enable 0 bit `1` = Enable IRQ generation when requested conversion of channels AN1 and AN0 is completed `0` = IRQ is not generated
bit 6	**PEND0:** Pending Conversion Status 0 bit `1` = Conversion of channels AN1 and AN0 is pending; set when selected trigger is asserted `0` = Conversion is complete
bit 5	**SWTRG0:** Software Trigger 0 bit `1` = Start conversion of AN1 and AN0 (if selected by TRGSRC bits)[(1)] This bit is automatically cleared by hardware when the PEND0 bit is set. `0` = Conversion is not started
bit 4-0	**TRGSRC0<4:0>:** Trigger 0 Source Selection bits Selects trigger source for conversion of analog channels AN1 and AN0. `00000` = No conversion enabled `00001` = Individual software trigger selected `00010` = Global software trigger selected `00011` = PWM Special Event Trigger selected `00100` = PWM Generator 1 primary trigger selected `00101` = PWM Generator 2 primary trigger selected `00110` = PWM Generator 3 primary trigger selected `00111` = PWM Generator 4 primary trigger selected `01000` = Reserved • • • `01100` = Timer1 period match `01101` = Reserved `01110` = PWM Generator 1 secondary trigger selected `01111` = PWM Generator 2 secondary trigger selected `10000` = PWM Generator 3 secondary trigger selected `10001` = PWM Generator 4 secondary trigger selected `10010` = Reserved • • • `10110` = Reserved `10111` = PWM Generator 1 current-limit ADC trigger `11000` = PWM Generator 2 current-limit ADC trigger `11001` = PWM Generator 3 current-limit ADC trigger `11010` = PWM Generator 4 current-limit ADC trigger `11011` = Reserved • • • `11111` = Timer2 period match

Note 1: If other conversions are in progress, then conversion will be performed when the conversion resources are available.

REGISTER 19-6: ADCPC1: A/D CONVERT PAIR CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN3[(1)]	PEND3[(1)]	SWTRG3[(1)]	TRGSRC3<4:0>[(1)]				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN2[(2)]	PEND2[(2)]	SWTRG2[(2)]	TRGSRC2<4:0>[(2)]				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **IRQEN3:** Interrupt Request Enable 3 bit[(1)]
1 = Enable IRQ generation when requested conversion of channels AN7 and AN6 is completed
0 = IRQ is not generated

bit 14 **PEND3:** Pending Conversion Status 3 bit[(1)]
1 = Conversion of channels AN7 and AN6 is pending. Set when selected trigger is asserted
0 = Conversion is complete

bit 13 **SWTRG3:** Software Trigger 3 bit[(1)]
1 = Start conversion of AN7 and AN6 (if selected in TRGSRC bits)[(3)]
This bit is automatically cleared by hardware when the PEND3 bit is set.
0 = Conversion is not started

Note 1: These bits are available in the dsPIC33FJ16GS402/404, dsPIC33FJ16GS504, dsPIC33FJ16GS502 and dsPIC33FJ06GS101 devices only.

2: These bits are available in the dsPIC33FJ16GS502, dsPIC33FJ16GS504, dsPIC33FJ06GS102, dsPIC33FJ06GS202 and dsPIC33FJ16GS402/404 devices only.

3: If other conversions are in progress, then conversion will be performed when the conversion resources are available.

REGISTER 19-6: ADCPC1: A/D CONVERT PAIR CONTROL REGISTER 1 (CONTINUED)

bit 12-8 **TRGSRC3<4:0>:** Trigger 3 Source Selection bits(1)

Selects trigger source for conversion of analog channels AN7 and AN6.
`00000` = No conversion enabled
`00001` = Individual software trigger selected
`00010` = Global software trigger selected
`00011` = PWM Special Event Trigger selected
`00100` = PWM Generator 1 primary trigger selected
`00101` = PWM Generator 2 primary trigger selected
`00110` = PWM Generator 3 primary trigger selected
`00111` = PWM Generator 4 primary trigger selected
`01000` = Reserved
•
•
•
`01100` = Timer1 period match
`01101` = Reserved
`01110` = PWM Generator 1 secondary trigger selected
`01111` = PWM Generator 2 secondary trigger selected
`10000` = PWM Generator 3 secondary trigger selected
`10001` = PWM Generator 4 secondary trigger selected
`10010` = Reserved
•
•
•
`10110` = Reserved
`10111` = PWM Generator 1 current-limit ADC trigger
`11000` = PWM Generator 2 current-limit ADC trigger
`11001` = PWM Generator 3 current-limit ADC trigger
`11010` = PWM Generator 4 current-limit ADC trigger
`11011` = Reserved
•
•
•
`11111` = Timer2 period match

bit 7 **IRQEN2:** Interrupt Request Enable 2 bit(2)

`1` = Enable IRQ generation when requested conversion of channels AN5 and AN4 is completed
`0` = IRQ is not generated

bit 6 **PEND2:** Pending Conversion Status 2 bit(2)

`1` = Conversion of channels AN5 and AN4 is pending; set when selected trigger is asserted.
`0` = Conversion is complete

bit 5 **SWTRG2:** Software Trigger 2 bit(2)

`1` = Start conversion of AN5 and AN4 (if selected by TRGSRC bits)(3)
This bit is automatically cleared by hardware when the PEND2 bit is set.
`0` = Conversion is not started

Note 1: These bits are available in the dsPIC33FJ16GS402/404, dsPIC33FJ16GS504, dsPIC33FJ16GS502 and dsPIC33FJ06GS101 devices only.

2: These bits are available in the dsPIC33FJ16GS502, dsPIC33FJ16GS504, dsPIC33FJ06GS102, dsPIC33FJ06GS202 and dsPIC33FJ16GS402/404 devices only.

3: If other conversions are in progress, then conversion will be performed when the conversion resources are available.

REGISTER 19-6: ADCPC1: A/D CONVERT PAIR CONTROL REGISTER 1 (CONTINUED)

bit 4-0 **TRGSRC2<4:0>:** Trigger 2 Source Selection bits

Selects trigger source for conversion of analog channels AN5 and AN4.

00000 = No conversion enabled
00001 = Individual software trigger selected
00010 = Global software trigger selected
00011 = PWM Special Event Trigger selected
00100 = PWM Generator 1 primary trigger selected
00101 = PWM Generator 2 primary trigger selected
00110 = PWM Generator 3 primary trigger selected
00111 = PWM Generator 4 primary trigger selected
01000 = Reserved
•
•
•
01100 = Timer1 period match
01101 = Reserved
01110 = PWM Generator 1 secondary trigger selected
01111 = PWM Generator 2 secondary trigger selected
10000 = PWM Generator 3 secondary trigger selected
10001 = PWM Generator 4 secondary trigger selected
10010 = Reserved
•
•
•
10110 = Reserved
10111 = PWM Generator 1 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11010 = PWM Generator 4 current-limit ADC trigger
11011 = Reserved
•
•
•
11111 = Timer2 period match

Note 1: These bits are available in the dsPIC33FJ16GS402/404, dsPIC33FJ16GS504, dsPIC33FJ16GS502 and dsPIC33FJ06GS101 devices only.

2: These bits are available in the dsPIC33FJ16GS502, dsPIC33FJ16GS504, dsPIC33FJ06GS102, dsPIC33FJ06GS202 and dsPIC33FJ16GS402/404 devices only.

3: If other conversions are in progress, then conversion will be performed when the conversion resources are available.

REGISTER 19-7: ADCPC2: A/D CONVERT PAIR CONTROL REGISTER 2(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN5	PEND5	SWTRG5	TRGSRC5<4:0>				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN4	PEND4	SWTRG4	TRGSRC4<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **IRQEN5:** Interrupt Request Enable 5 bit
`1` = Enable IRQ generation when requested conversion of channels AN11 and AN10 is completed
`0` = IRQ is not generated

bit 14 **PEND5:** Pending Conversion Status 5 bit
`1` = Conversion of channels AN11 and AN10 is pending; set when selected trigger is asserted
`0` = Conversion is complete

bit 13 **SWTRG5:** Software Trigger 5 bit
`1` = Start conversion of AN11 and AN10 (if selected in TRGSRC bits)(2)
This bit is automatically cleared by hardware when the PEND5 bit is set.
`0` = Conversion is not started

Note 1: This register is only implemented on the dsPIC33FJ16GS504 devices.

2: If other conversions are in progress, then conversion will be performed when the conversion resources are available.

REGISTER 19-7: ADCPC2: A/D CONVERT PAIR CONTROL REGISTER 2(1) (CONTINUED)

bit 12-8 **TRGSRC5<4:0>:** Trigger 5 Source Selection bits
Selects trigger source for conversion of analog channels AN11 and AN10.
00000 = No conversion enabled
00001 = Individual software trigger selected
00010 = Global software trigger selected
00011 = PWM Special Event Trigger selected
00100 = PWM Generator 1 primary trigger selected
00101 = PWM Generator 2 primary trigger selected
00110 = PWM Generator 3 primary trigger selected
00111 = PWM Generator 4 primary trigger selected
01000 = Reserved
•
•
•
01100 = Timer1 period match
01101 = Reserved
01110 = PWM Generator 1 secondary trigger selected
01111 = PWM Generator 2 secondary trigger selected
10000 = PWM Generator 3 secondary trigger selected
10001 = PWM Generator 4 secondary trigger selected
10010 = Reserved
•
•
•
10110 = Reserved
10111 = PWM Generator 1 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11010 = PWM Generator 4 current-limit ADC trigger
11011 = Reserved
•
•
•
11111 = Timer2 period match

bit 7 **IRQEN4:** Interrupt Request Enable 4 bit
1 = Enable IRQ generation when requested conversion of channels AN9 and AN8 is completed
0 = IRQ is not generated

bit 6 **PEND4:** Pending Conversion Status 4 bit
1 = Conversion of channels AN9 and AN8 is pending; set when selected trigger is asserted
0 = Conversion is complete

bit 5 **SWTRG4:** Software Trigger4 bit
1 = Start conversion of AN9 and AN8 (if selected by TRGSRC bits)(2)
This bit is automatically cleared by hardware when the PEND4 bit is set.
0 = Conversion is not started

Note 1: This register is only implemented on the dsPIC33FJ16GS504 devices.
2: If other conversions are in progress, then conversion will be performed when the conversion resources are available.

REGISTER 19-7: ADCPC2: A/D CONVERT PAIR CONTROL REGISTER 2(1) (CONTINUED)

bit 4-0 **TRGSRC4<4:0>:** Trigger 4 Source Selection bits

Selects trigger source for conversion of analog channels AN9 and AN8.

`00000` = No conversion enabled
`00001` = Individual software trigger selected
`00010` = Global software trigger selected
`00011` = PWM Special Event Trigger selected
`00100` = PWM Generator 1 primary trigger selected
`00101` = PWM Generator 2 primary trigger selected
`00110` = PWM Generator 3 primary trigger selected
`00111` = PWM Generator 4 primary trigger selected
`01000` = Reserved
•
•
•
`01100` = Timer1 period match
`01101` = Reserved
`01110` = PWM Generator 1 secondary trigger selected
`01111` = PWM Generator 2 secondary trigger selected
`10000` = PWM Generator 3 secondary trigger selected
`10001` = PWM Generator 4 secondary trigger selected
`10010` = Reserved
•
•
•
`10110` = Reserved
`10111` = PWM Generator 1 current-limit ADC trigger
`11000` = PWM Generator 2 current-limit ADC trigger
`11001` = PWM Generator 3 current-limit ADC trigger
`11010` = PWM Generator 4 current-limit ADC trigger
`11011` = Reserved
•
•
•
`11111` = Timer2 period match

Note 1: This register is only implemented on the dsPIC33FJ16GS504 devices.

2: If other conversions are in progress, then conversion will be performed when the conversion resources are available.

REGISTER 19-8: ADCPC3: A/D CONVERT PAIR CONTROL REGISTER 3(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN6	PEND6	SWTRG6	TRGSRC6<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **IRQEN6:** Interrupt Request Enable 6 bit
1 = Enable IRQ generation when requested conversion of channels AN13 and AN12 is completed
0 = IRQ is not generated

bit 6 **PEND6:** Pending Conversion Status 6 bit
1 = Conversion of channels AN13 and AN 12 is pending; set when selected trigger is asserted
0 = Conversion is complete

bit 5 **SWTRG6:** Software Trigger 6 bit
1 = Start conversion of AN13 (INTREF) and AN12 (EXTREF) (if selected by TRGSRC bits)(2)
This bit is automatically cleared by hardware when the PEND6 bit is set.
0 = Conversion is not started

Note 1: This register is only implemented on the dsPIC33FJ16GS502 and dsPIC33FJ16GS504 devices.

2: If other conversions are in progress, conversion will be performed when the conversion resources are available.

REGISTER 19-8: ADCPC3: A/D CONVERT PAIR CONTROL REGISTER 3[1] (CONTINUED)

bit 4-0	**TRGSRC6<4:0>:** Trigger 6 Source Selection bits Selects trigger source for conversion of analog channels AN13 and AN12. `00000` = No conversion enabled `00001` = Individual software trigger selected `00010` = Global software trigger selected `00011` = PWM Special Event Trigger selected `00100` = PWM Generator 1 primary trigger selected `00101` = PWM Generator 2 primary trigger selected `00110` = PWM Generator 3 primary trigger selected `00111` = PWM Generator 4 primary trigger selected `01000` = Reserved • • • `01100` = Timer1 period match `01101` = Reserved `01110` = PWM Generator 1 secondary trigger selected `01111` = PWM Generator 2 secondary trigger selected `10000` = PWM Generator 3 secondary trigger selected `10001` = PWM Generator 4 secondary trigger selected `10010` = Reserved • • • `10110` = Reserved `10111` = PWM Generator 1 current-limit ADC trigger `11000` = PWM Generator 2 current-limit ADC trigger `11001` = PWM Generator 3 current-limit ADC trigger `11010` = PWM Generator 4 current-limit ADC trigger `11011` = Reserved • • • `11111` = Timer2 period match

Note 1: This register is only implemented on the dsPIC33FJ16GS502 and dsPIC33FJ16GS504 devices.

2: If other conversions are in progress, conversion will be performed when the conversion resources are available.

20.0 HIGH-SPEED ANALOG COMPARATOR

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*, **Section 45. "High-Speed Analog Comparator"** (DS70296), which is available on the Microchip web site (www.microchip.com).

The dsPIC33F SMPS Comparator module monitors current and/or voltage transients that may be too fast for the CPU and ADC to capture.

20.1 Features Overview

The SMPS comparator module offers the following major features:

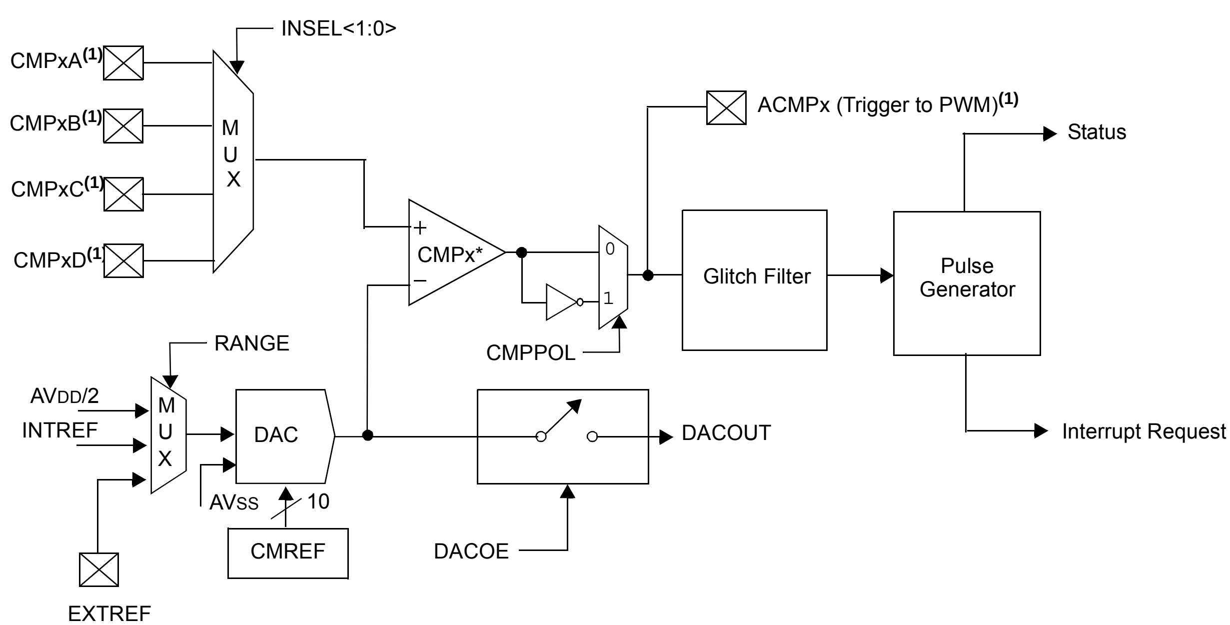
- 16 selectable comparator inputs
- Up to four analog comparators
- 10-bit DAC for each analog comparator
- Programmable output polarity
- Interrupt generation capability
- DACOUT pin to provide DAC output
- DAC has three ranges of operation:
  - $AV_{DD}/2$
  - Internal Reference 1.2V, 1%
  - External Reference < (AV_{DD} – 1.6V)
- ADC sample and convert trigger capability
- Disable capability reduces power consumption
- Functional support for PWM module:
  - PWM duty cycle control
  - PWM period control
  - PWM Fault detect

20.2 Module Description

Figure 20-1 shows a functional block diagram of one analog comparator from the SMPS comparator module. The analog comparator provides high-speed operation with a typical delay of 20 ns. The comparator has a typical offset voltage of ±5 mV. The negative input of the comparator is always connected to the DAC circuit. The positive input of the comparator is connected to an analog multiplexer that selects the desired source pin.

The analog comparator input pins are typically shared with pins used by the Analog-to-Digital Converter (ADC) module. Both the comparator and the ADC can use the same pins at the same time. This capability enables a user to measure an input voltage with the ADC and detect voltage transients with the comparator.

FIGURE 20-1: COMPARATOR MODULE BLOCK DIAGRAM



Note 1: x = 1, 2, 3, and 4.

20.3 Module Applications

This module provides a means for the SMPS dsPIC DSC devices to monitor voltage and currents in a power conversion application. The ability to detect transient conditions and stimulate the dsPIC DSC processor and/or peripherals, without requiring the processor and ADC to constantly monitor voltages or currents, frees the dsPIC DSC to perform other tasks.

The comparator module has a high-speed comparator and an associated 10-bit DAC that provides a programmable reference voltage to the inverting input of the comparator. The polarity of the comparator output is user-programmable. The output of the module can be used in the following modes:

- Generate an Interrupt
- Trigger an ADC Sample and Convert Process
- Truncate the PWM Signal (current limit)
- Truncate the PWM Period (current minimum)
- Disable the PWM Outputs (Fault latch)

The output of the comparator module may be used in multiple modes at the same time, such as: (1) generate an interrupt, (2) have the ADC take a sample and convert it, and (3) truncate the PWM output in response to a voltage being detected beyond its expected value.

The comparator module can also be used to wake-up the system from Sleep or Idle mode when the analog input voltage exceeds the programmed threshold voltage.

20.4 DAC

The range of the DAC is controlled via an analog multiplexer that selects either $AV_{DD}/2$, internal 1.2V, 1% reference, or an external reference source, EXTREF. The full range of the DAC ($AV_{DD}/2$) will typically be used when the chosen input source pin is shared with the ADC. The reduced range option (INTREF) will likely be used when monitoring current levels using a current sense resistor. Usually, the measured voltages in such applications are small (<1.25V); therefore the option of using a reduced reference range for the comparator extends the available DAC resolution in these applications. The use of an external reference enables the user to connect to a reference that better suits their application.

DACOUT, shown in Figure 20-1, can only be associated with a single comparator at a given time.

Note:	It should be ensured in software that multiple DACOE bits are not set. The output on the DACOUT pin will be indeterminate if multiple comparators enable the DAC output.

20.5 Interaction with I/O Buffers

If the comparator module is enabled and a pin has been selected as the source for the comparator, then the chosen I/O pad must disable the digital input buffer associated with the pad to prevent excessive currents in the digital buffer due to analog input voltages.

20.6 Digital Logic

The CMPCONx register (see Register 20-1) provides the control logic that configures the comparator module. The digital logic provides a glitch filter for the comparator output to mask transient signals in less than two instruction cycles. In Sleep or Idle mode, the glitch filter is bypassed to enable an asynchronous path from the comparator to the interrupt controller. This asynchronous path can be used to wake-up the processor from Sleep or Idle mode.

The comparator can be disabled while in Idle mode if the CMPSIDL bit is set. If a device has multiple comparators, if any CMPSIDL bit is set, then the entire group of comparators will be disabled while in Idle mode. This behavior reduces complexity in the design of the clock control logic for this module.

The digital logic also provides a one T_{CY} width pulse generator for triggering the ADC and generating interrupt requests.

The CMPDACx (see Register 20-2) register provides the digital input value to the reference DAC.

If the module is disabled, the DAC and comparator are disabled to reduce power consumption.

20.7 Comparator Input Range

The comparator has a limitation for the input Common Mode Range (CMR) of (AV_{DD} – 1.5V), typical. This means that both inputs should not exceed this range. As long as one of the inputs is within the Common Mode Range, the comparator output will be correct. However, any input exceeding the CMR limitation will cause the comparator input to be saturated.

If both inputs exceed the CMR, the comparator output will be indeterminate.

20.8 DAC Output Range

The DAC has a limitation for the maximum reference voltage input of (AV_{DD} – 1.6) volts. An external reference voltage input should not exceed this value or the reference DAC output will become indeterminate.

20.9 Comparator Registers

The comparator module is controlled by the following registers:

- CMPCONx: Comparator Control Register
- CMPDACx: Comparator DAC Control Register

REGISTER 20-1: CMPCONx: COMPARATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
CMPON	—	CMPSIDL	—	—	—	—	DACOE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
INSEL<1:0>		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CMPON:** Comparator Operating Mode bit
1 = Comparator module is enabled
0 = Comparator module is disabled (reduces power consumption)

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **CMPSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode.
0 = Continue module operation in Idle mode
If a device has multiple comparators, any CMPSIDL bit set to ‘1’ disables **ALL** comparators while in Idle mode.

bit 12-9 **Reserved:** Read as ‘0’

bit 8 **DACOE:** DAC Output Enable
1 = DAC analog voltage is output to DACOUT pin(1)
0 = DAC analog voltage is not connected to DACOUT pin

bit 7-6 **INSEL<1:0>:** Input Source Select for Comparator bits
00 = Select CMPxA input pin
01 = Select CMPxB input pin
10 = Select CMPxC input pin
11 = Select CMPxD input pin

bit 5 **EXTREF:** Enable External Reference bit
1 = External source provides reference to DAC (maximum DAC voltage determined by external voltage source)
0 = Internal reference sources provide reference to DAC (maximum DAC voltage determined by RANGE bit setting)

bit 4 **Reserved:** Read as ‘0’

bit 3 **CMPSTAT:** Current State of Comparator Output Including CMPPOL Selection bit

bit 2 **Reserved:** Read as ‘0’

bit 1 **CMPPOL:** Comparator Output Polarity Control bit
1 = Output is inverted
0 = Output is non-inverted

bit 0 **RANGE:** Selects DAC Output Voltage Range bit
1 = High Range: Max DAC Value = $AV_{DD}/2$, 1.65V at 3.3V AV_{DD}
0 = Low Range: Max DAC Value = INTREF, 1.2V, ±1%

Note 1: DACOUT can be associated only with a single comparator at any given time. The software must ensure that multiple comparators do not enable the DAC output by setting their respective DACOE bit.

REGISTER 20-2: CMPDACx: COMPARATOR DAC CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CMREF<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMREF<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **Reserved:** Read as ‘0’

bit 9-0 **CMREF<9:0>:** Comparator Reference Voltage Select bits

1111111111 = (CMREF * INTREF/1024) or (CMREF * (AV_{DD}/2)/1024) volts depending on RANGE bit or (CMREF * EXTREF/1024) if EXTREF is set

•

•

•

0000000000 = 0.0 volts

21.0 SPECIAL FEATURES

Note:	This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest *"dsPIC33F Family Reference Manual"* sections.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation
- Brown-out Reset (BOR)

21.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location 0xF80000.

The individual Configuration bit descriptions for the FBS, FGS, FOSCSEL, FOSC, FWDT, FPOR and FICD Configuration registers are shown in Table 21-2.

Note that address, 0xF80000, is beyond the user program memory space. It belongs to the configuration memory space (0x800000-0xFFFFFF), which can only be accessed using table reads and table writes.

The upper byte of all device Configuration registers should always be '1111 1111'. This makes them appear to be `NOP` instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

To prevent inadvertent configuration changes during code execution, all programmable Configuration bits are write-once. After a bit is initially programmed during a power cycle, it cannot be written to again. Changing a device configuration requires that power to the device be cycled.

The device Configuration register map is shown in Table 21-1.

TABLE 21-1: DEVICE CONFIGURATION REGISTER MAP

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF80000	FBS	—	—	—	—	BSS<2:0>			BWRP
0xF80002	RESERVED	Reserved(1)							
0xF80004	FGS	—	—	—	—	—	GSS<1:0>		GWRP
0xF80006	FOSCSEL	IESO	—	—	—		FNOSC<2:0>		
0xF80008	FOSC	FCKSM<1:0>		IOL1WAY	—	—	OSCIOFNC	POSCMD<1:0>	
0xF8000A	FWDT	FWDTEN	WINDIS	—	WDTPRE	WDTPOST<3:0>			
0xF8000C	FPOR	—	—	—	—	—	FPWRT<2:0>		
0xF8000E	FICD	Reserved(1)		JTAGEN	—	—	—	ICS<1:0>	
0xF80010	FUID0	User Unit ID Byte 0							
0xF80012	FUID1	User Unit ID Byte 1							

Note 1: When read, these bits will appear as '1'. When you write to these bits, set these bits to '1'.

TABLE 21-2: dsPIC33F CONFIGURATION BITS DESCRIPTION

Bit Field	Register	Description
BWRP	FBS	Boot Segment Program Flash Write Protection bit `1` = Boot segment can be written `0` = Boot segment is write-protected
BSS<2:0>	FBS	Boot Segment Program Flash Code Protection Size bits `X11` = No boot program Flash segment Boot space is 256 instruction words (except interrupt vectors) `110` = Standard security; boot program Flash segment ends at 0x0003FE `010` = High security; boot program Flash segment ends at 0x0003FE Boot space is 768 instruction words (except interrupt vectors) `101` = Standard security; boot program Flash segment ends at 0x0007FE `001` = High security; boot program Flash segment ends at 0x0007FE Boot space is 1792 instruction words (except interrupt vectors) `100` = Standard security; boot program Flash segment ends at 0x000FFE `000` = High security; boot program Flash segment ends at 0x000FFE
GSS<1:0>	FGS	General Segment Code-Protect bits `11` = User program memory is not code-protected `10` = Standard security `0x` = High security
GWRP	FGS	General Segment Write-Protect bit `1` = User program memory is not write-protected `0` = User program memory is write-protected
IESO	FOSCSEL	Two-speed Oscillator Start-up Enable bit `1` = Start-up device with FRC, then automatically switch to the user-selected oscillator source when ready `0` = Start-up device with user-selected oscillator source
FNOSC<2:0>	FOSCSEL	Initial Oscillator Source Selection bits `111` = Internal Fast RC (FRC) oscillator with postscaler `110` = Internal Fast RC (FRC) oscillator with divide-by-16 `101` = LPRC oscillator `100` = Secondary (LP) oscillator `011` = Primary (XT, HS, EC) oscillator with PLL `010` = Primary (XT, HS, EC) oscillator `001` = Internal Fast RC (FRC) oscillator with PLL `000` = FRC oscillator
FCKSM<1:0>	FOSC	Clock Switching Mode bits `1x` = Clock switching is disabled, Fail-Safe Clock Monitor is disabled `01` = Clock switching is enabled, Fail-Safe Clock Monitor is disabled `00` = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	FOSC	Peripheral Pin Select Configuration bit `1` = Allow only one reconfiguration `0` = Allow multiple reconfigurations
OSCIOFNC	FOSC	OSC2 Pin Function bit (except in XT and HS modes) `1` = OSC2 is clock output `0` = OSC2 is general purpose digital I/O pin
POSCMD<1:0>	FOSC	Primary Oscillator Mode Select bits `11` = Primary oscillator disabled `10` = HS Crystal Oscillator mode `01` = XT Crystal Oscillator mode `00` = EC (External Clock) mode

TABLE 21-2: dsPIC33F CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	Description
FWDTEN	FWDT	Watchdog Timer Enable bit 1 = Watchdog Timer always enabled (LPRC oscillator cannot be disabled; clearing the SWDTEN bit in the RCON register will have no effect) 0 = Watchdog Timer enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WINDIS	FWDT	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
WDTPRE	FWDT	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST<3:0>	FWDT	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1
FPWRT<2:0>	FPOR	Power-on Reset Timer Value Select bits 111 = PWRT = 128 ms 110 = PWRT = 64 ms 101 = PWRT = 32 ms 100 = PWRT = 16 ms 011 = PWRT = 8 ms 010 = PWRT = 4 ms 001 = PWRT = 2 ms 000 = PWRT = Disabled
JTAGEN	FICD	JTAG Enable bit 1 = JTAG is enabled 0 = JTAG is disabled
ICS<1:0>	FICD	ICD Communication Channel Select Enable bits 11 = Communicate on PGEC1 and PGED1 10 = Communicate on PGEC2 and PGED2 01 = Communicate on PGEC3 and PGED3 00 = Reserved, do not use.

21.2 On-Chip Voltage Regulator

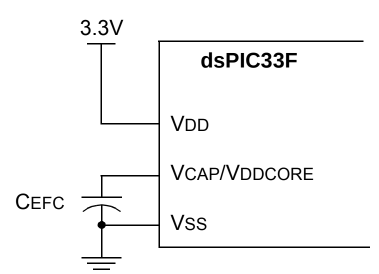
The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices power their core digital logic at a nominal 2.5V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families incorporate an on-chip regulator that allows the device to run its core logic from V_{DD}.

The regulator provides power to the core from the other V_{DD} pins. When the regulator is enabled, a low-ESR (less than 5 ohms) capacitor (such as tantalum or ceramic) must be connected to the V_{CAP}/V_{DDCORE} pin (Figure 21-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 24-13 located in **Section 24.1 “DC Characteristics”**.

Note:	It is important for the low-ESR capacitor to be placed as close as possible to the V_{CAP}/V_{DDCORE} pin.

On a POR, it takes approximately 20 μs for the on-chip voltage regulator to generate an output voltage. During this time, designated as $T_{STARTUP}$, code execution is disabled. $T_{STARTUP}$ is applied every time the device resumes operation after any power-down.

FIGURE 21-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR[1,2]



Note 1: These are typical operating voltages. Refer to Table 24-13 located in **Section 24.1 “DC Characteristics”** for the full operating ranges of V_{DD} and V_{CAP}/V_{DDCORE}.

2: It is important for the low-ESR capacitor to be placed as close as possible to the V_{CAP}/V_{DDCORE} pin.

21.3 BOR: Brown-Out Reset

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage V_{CAP}/V_{DDCORE}. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines, or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is ‘1’.

Concurrently, the PWRT time-out (T_{PWRT}) is applied before the internal Reset is released. If T_{PWRT} = 0 and a crystal oscillator is being used, then a nominal delay of T_{FSCM} = 100 is applied. The total delay in this case is T_{FSCM}.

The BOR Status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should V_{DD} fall below the BOR threshold voltage.

21.4 Watchdog Timer (WDT)

For dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

21.4.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler than can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a nominal WDT time-out period (T_{WDT}) of 1 ms in 5-bit mode, or 4 ms in 7-bit mode.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>) which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a `PWRSAV` instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a `CLRWDT` instruction during normal execution

Note:	The `CLRWDT` and `PWRSAV` instructions clear the prescaler and postscaler counts when executed.

21.4.2 SLEEP AND IDLE MODES

If the WDT is enabled, it will continue to run during Sleep or Idle modes. When the WDT time-out occurs, the device will wake the device and code execution will continue from where the `PWRSAV` instruction was executed. The corresponding SLEEP or IDLE bits (RCON<3:2>) will need to be cleared in software after the device wakes up.

21.4.3 ENABLING WDT

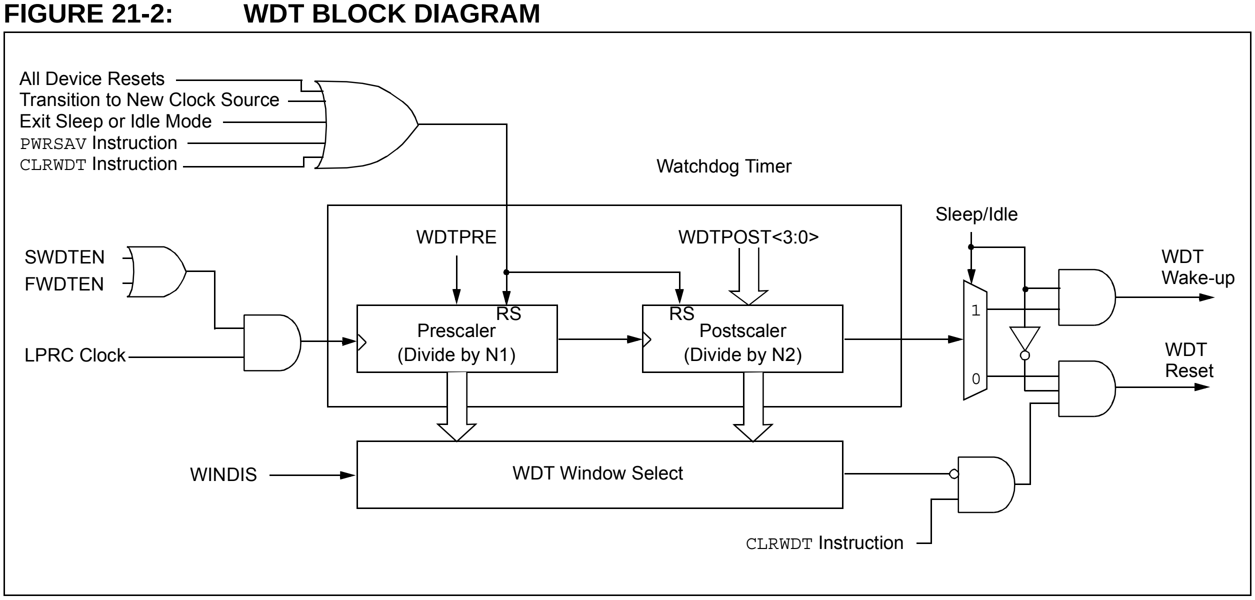
The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '`0`'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

Note:	If the WINDIS bit (FWDT<6>) is cleared, the `CLRWDT` instruction should be executed by the application software only during the last 1/4 of the WDT period. This `CLRWDT` window can be determined by using a timer. If a `CLRWDT` instruction is executed before this window, a WDT Reset occurs.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

FIGURE 21-2: WDT BLOCK DIAGRAM



21.5 JTAG Interface

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices implement a JTAG interface, which supports boundary scan device testing, as well as in-circuit programming. Detailed information on this interface will be provided in future revisions of the document.

21.6 In-Circuit Serial Programming

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 family digital signal controllers can be serially programmed while in the end application circuit. This is done with two lines for clock and data and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the digital signal controller just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

21.7 In-Circuit Debugger

When MPLAB® ICD 2 is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the EMUCx (Emulation/Debug Clock) and EMUDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to MCLR, V_{DD}, V_{SS}, and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

21.8 Code Protection and CodeGuard™ Security

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices offer the intermediate implementation of CodeGuard™ Security. CodeGuard Security enables multiple parties to securely share resources (memory, interrupts and peripherals) on a single chip. This feature helps protect individual Intellectual Property in collaborative system designs.

When coupled with software encryption libraries, CodeGuard™ Security can be used to securely update Flash even when multiple IPs reside on a single chip.

The code protection features are controlled by the Configuration registers: FBS and FGS.

Secure segment and RAM protection is not implemented in dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices.

Note:	Refer to *CodeGuard Security Reference Manual* (DS70180) for further information on usage, configuration and operation of CodeGuard Security.

TABLE 21-3: CODE FLASH SECURITY SEGMENT SIZES FOR 6-Kbyte DEVICES

Configuration Bits		
BSS<2:0> = x11 **0K**	VS = 256 IW GS = 1792 IW (unused)	000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh
BSS<2:0> = x10 **256**	VS = 256 IW BS = 256 IW GS = 1536 IW (unused)	000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh
BSS<2:0> = x01 **768**	VS = 256 IW BS = 768 IW GS = 1024 IW (unused)	000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh
BSS<2:0> = x00 **1792**	VS = 256 IW BS = 1792 IW (unused)	000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh

TABLE 21-4: CODE FLASH SECURITY SEGMENT SIZES FOR 16-Kbyte DEVICES

Configuration Bits		
BSS<2:0> = x11 **0K**	VS = 256 IW GS = 5376 IW	000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh
BSS<2:0> = x10 **256**	VS = 256 IW BS = 256 IW GS = 5120 IW	000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh
BSS<2:0> = x01 **768**	VS = 256 IW BS = 768 IW GS = 4608 IW	000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh
BSS<2:0> = x00 **1792**	VS = 256 IW BS = 1792 IW GS = 3584 IW	000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh

NOTES:

22.0 INSTRUCTION SET SUMMARY

> **Note:** This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *“dsPIC33F Family Reference Manual”*. Please see the Microchip web site (www.microchip.com) for the latest *“dsPIC33F Family Reference Manual”* sections.

The dsPIC33F instruction set is identical to that of the dsPIC30F.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- DSP operations
- Control operations

Table 22-1 shows the general symbols used in describing the instructions.

The dsPIC33F instruction set summary in Table 22-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register ‘Wb’ without any address modifier
- The second source operand, which is typically a register ‘Ws’ with or without an address modifier
- The destination of the result, which is typically a register ‘Wd’ with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value, ‘f’
- The destination, which could be either the file register, ‘f’, or the W0 register, which is denoted as ‘WREG’

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of ‘Ws’ or ‘f’)
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register ‘Wb’)

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by ‘k’)
- The W register or file register where the literal value is to be loaded (specified by ‘Wb’ or ‘f’)

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register ‘Wb’ without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register ‘Wd’ with or without an address modifier

The `MAC` class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write-back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register, ‘Wn’, or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the table read and table write instructions

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all table reads and writes and RETURN/RETFIE instructions, which are single-word instructions but take two or three cycles. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the *"dsPIC30F/33F Programmer's Reference Manual"* (DS70157).

TABLE 22-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator Write-Back Destination Address register ∈ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word-addressed instructions) ∈ {0...15}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x0000...0x1FFF}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {0...15}
lit5	5-bit unsigned literal ∈ {0...31}
lit8	8-bit unsigned literal ∈ {0...255}
lit10	10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {0...16384}
lit16	16-bit unsigned literal ∈ {0...65535}
lit23	23-bit unsigned literal ∈ {0...8388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512...511}
Slit16	16-bit signed literal ∈ {-32768...32767}
Slit6	6-bit signed literal ∈ {-16...16}
Wb	Base W register ∈ {W0..W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (Direct Addressing)

 Preliminary

TABLE 22-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm*Wm	Multiplicand and Multiplier Working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier Working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 Working registers ∈ {W0..W15}
Wnd	One of 16 Destination Working registers ∈ {W0...W15}
Wns	One of 16 Source Working registers ∈ {W0...W15}
WREG	W0 (Working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] }
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4...W7}
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4...W7}

TABLE 22-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
1	ADD	ADD	Acc	Add Accumulators	1	1	OA,OB,SA,SB
		ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD	f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD	Wso,#Slit4,Acc	16-Bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (2)	None
		BRA	GE,Expr	Branch if Greater Than or Equal	1	1 (2)	None
		BRA	GEU,Expr	Branch if Unsigned Greater Than or Equal	1	1 (2)	None
		BRA	GT,Expr	Branch if Greater Than	1	1 (2)	None
		BRA	GTU,Expr	Branch if Unsigned Greater Than	1	1 (2)	None
		BRA	LE,Expr	Branch if Less Than or Equal	1	1 (2)	None
		BRA	LEU,Expr	Branch if Unsigned Less Than or Equal	1	1 (2)	None
		BRA	LT,Expr	Branch if Less Than	1	1 (2)	None
		BRA	LTU,Expr	Branch if Unsigned Less Than	1	1 (2)	None
		BRA	N,Expr	Branch if Negative	1	1 (2)	None
		BRA	NC,Expr	Branch if Not Carry	1	1 (2)	None
		BRA	NN,Expr	Branch if Not Negative	1	1 (2)	None
		BRA	NOV,Expr	Branch if Not Overflow	1	1 (2)	None
		BRA	NZ,Expr	Branch if Not Zero	1	1 (2)	None
		BRA	OA,Expr	Branch if Accumulator A Overflow	1	1 (2)	None
		BRA	OB,Expr	Branch if Accumulator B Overflow	1	1 (2)	None
		BRA	OV,Expr	Branch if Overflow	1	1 (2)	None
		BRA	SA,Expr	Branch if Accumulator A Saturated	1	1 (2)	None
		BRA	SB,Expr	Branch if Accumulator B Saturated	1	1 (2)	None
		BRA	Expr	Branch Unconditionally	1	2	None
		BRA	Z,Expr	Branch if Zero	1	1 (2)	None
		BRA	Wn	Computed Branch	1	2	None
7	BSET	BSET	f,#bit4	Bit Set f	1	1	None
		BSET	Ws,#bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C	Ws,Wb	Write C bit to Ws<Wb>	1	1	None
		BSW.Z	Ws,Wb	Write Z bit to Ws<Wb>	1	1	None
9	BTG	BTG	f,#bit4	Bit Toggle f	1	1	None
		BTG	Ws,#bit4	Bit Toggle Ws	1	1	None

TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
10	BTSC	BTSC f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
		BTSC Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS f,#bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS Ws,#bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST f,#bit4	Bit Test f	1	1	Z
		BTST.C Ws,#bit4	Bit Test Ws to C	1	1	C
		BTST.Z Ws,#bit4	Bit Test Ws to Z	1	1	Z
		BTST.C Ws,Wb	Bit Test Ws<Wb> to C	1	1	C
		BTST.Z Ws,Wb	Bit Test Ws<Wb> to Z	1	1	Z
13	BTSTS	BTSTS f,#bit4	Bit Test then Set f	1	1	Z
		BTSTS.C Ws,#bit4	Bit Test Ws to C, then Set	1	1	C
		BTSTS.Z Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL lit23	Call Subroutine	2	2	None
		CALL Wn	Call Indirect Subroutine	1	2	None
15	CLR	CLR f	f = 0x0000	1	1	None
		CLR WREG	WREG = 0x0000	1	1	None
		CLR Ws	Ws = 0x0000	1	1	None
		CLR Acc,Wx,Wxd,Wy,Wyd,AWB	Clear Accumulator	1	1	OA,OB,SA,SB
16	CLRWDT	CLRWDT	Clear Watchdog Timer	1	1	WDTO,Sleep
17	COM	COM f	f = $\overline{f}$	1	1	N,Z
		COM f,WREG	WREG = $\overline{f}$	1	1	N,Z
		COM Ws,Wd	Wd = $\overline{Ws}$	1	1	N,Z
18	CP	CP f	Compare f with WREG	1	1	C,DC,N,OV,Z
		CP Wb,#lit5	Compare Wb with lit5	1	1	C,DC,N,OV,Z
		CP Wb,Ws	Compare Wb with Ws (Wb – Ws)	1	1	C,DC,N,OV,Z
19	CP0	CP0 f	Compare f with 0x0000	1	1	C,DC,N,OV,Z
		CP0 Ws	Compare Ws with 0x0000	1	1	C,DC,N,OV,Z
20	CPB	CPB f	Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z
		CPB Wb,#lit5	Compare Wb with lit5, with Borrow	1	1	C,DC,N,OV,Z
		CPB Wb,Ws	Compare Wb with Ws, with Borrow (Wb – Ws – $\overline{C}$)	1	1	C,DC,N,OV,Z
21	CPSEQ	CPSEQ Wb, Wn	Compare Wb with Wn, Skip if =	1	1 (2 or 3)	None
22	CPSGT	CPSGT Wb, Wn	Compare Wb with Wn, Skip if >	1	1 (2 or 3)	None
23	CPSLT	CPSLT Wb, Wn	Compare Wb with Wn, Skip if <	1	1 (2 or 3)	None
24	CPSNE	CPSNE Wb, Wn	Compare Wb with Wn, Skip if ≠	1	1 (2 or 3)	None
25	DAW	DAW Wn	Wn = Decimal Adjust Wn	1	1	C
26	DEC	DEC f	f = f – 1	1	1	C,DC,N,OV,Z
		DEC f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC Ws,Wd	Wd = Ws – 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2 f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2 f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2 Ws,Wd	Wd = Ws – 2	1	1	C,DC,N,OV,Z
28	DISI	DISI #lit14	Disable Interrupts for k Instruction Cycles	1	1	None

TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF	Wm,Wn	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO	#lit14,Expr	Do code to PC + Expr, lit14 + 1 times	2	2	None
		DO	Wn,Expr	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC	Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
34	EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL	Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	C
36	FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	C
37	FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	C
38	GOTO	GOTO	Expr	Go to Address	2	2	None
		GOTO	Wn	Go to Indirect	1	2	None
39	INC	INC	f	f = f + 1	1	1	C,DC,N,OV,Z
		INC	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2	f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2	f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2	Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR	f	f = f .IOR. WREG	1	1	N,Z
		IOR	f,WREG	WREG = f .IOR. WREG	1	1	N,Z
		IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC	Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
43	LNK	LNK	#lit14	Link Frame Pointer	1	1	None
44	LSR	LSR	f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd , AWB	Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
46	MOV	MOV	f,Wn	Move f to Wn	1	1	None
		MOV	f	Move f to f	1	1	N,Z
		MOV	f,WREG	Move f to WREG	1	1	N,Z
		MOV	#lit16,Wn	Move 16-Bit Literal to Wn	1	1	None
		MOV.b	#lit8,Wn	Move 8-Bit Literal to Wn	1	1	None
		MOV	Wn,f	Move Wn to f	1	1	None
		MOV	Wso,Wdo	Move Ws to Wd	1	1	None
		MOV	WREG,f	Move WREG to f	1	1	N,Z
		MOV.D	Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D	Ws,Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
47	MOVSAC	MOVSAC	Acc,Wx,Wxd,Wy,Wyd,AWB	Prefetch and Store Accumulator	1	1	None

TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
48	MPY	MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
49	MPY.N	MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	-(Multiply Wm by Wn) to Accumulator	1	1	None
50	MSC	MSC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd, AWB	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
51	MUL	MUL.SS Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.US Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None
52	NEG	NEG Acc	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG f	f = $\overline{f}$ + 1	1	1	C,DC,N,OV,Z
		NEG f,WREG	WREG = $\overline{f}$ + 1	1	1	C,DC,N,OV,Z
		NEG Ws,Wd	Wd = $\overline{Ws}$ + 1	1	1	C,DC,N,OV,Z
53	NOP	NOP	No Operation	1	1	None
		NOPR	No Operation	1	1	None
54	POP	POP f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		POP.S	Pop Shadow Registers	1	1	All
55	PUSH	PUSH f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S	Push Shadow Registers	1	1	None
56	PWRSAV	PWRSAV #lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep
57	RCALL	RCALL Expr	Relative Call	1	2	None
		RCALL Wn	Computed Call	1	2	None
58	REPEAT	REPEAT #lit14	Repeat Next Instruction lit14 + 1 times	1	1	None
		REPEAT Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
59	RESET	RESET	Software Device Reset	1	1	None
60	RETFIE	RETFIE	Return from interrupt	1	3 (2)	None
61	RETLW	RETLW #lit10,Wn	Return with Literal in Wn	1	3 (2)	None
62	RETURN	RETURN	Return from Subroutine	1	3 (2)	None
63	RLC	RLC f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
		RLC Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z
64	RLNC	RLNC f	f = Rotate Left (No Carry) f	1	1	N,Z
		RLNC f,WREG	WREG = Rotate Left (No Carry) f	1	1	N,Z
		RLNC Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z
65	RRC	RRC f	f = Rotate Right through Carry f	1	1	C,N,Z
		RRC f,WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z
		RRC Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z

TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
66	RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	f,WREG	WREG = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N,Z
67	SAC	SAC	Acc,#Slit4,Wdo	Store Accumulator	1	1	None
		SAC.R	Acc,#Slit4,Wdo	Store Rounded Accumulator	1	1	None
68	SE	SE	Ws,Wnd	Wnd = Sign-Extended Ws	1	1	C,N,Z
69	SETM	SETM	f	f = 0xFFFF	1	1	None
		SETM	WREG	WREG = 0xFFFF	1	1	None
		SETM	Ws	Ws = 0xFFFF	1	1	None
70	SFTAC	SFTAC	Acc,Wn	Arithmetic Shift Accumulator by (Wn)	1	1	OA,OB,OAB, SA,SB,SAB
		SFTAC	Acc,#Slit6	Arithmetic Shift Accumulator by Slit6	1	1	OA,OB,OAB, SA,SB,SAB
71	SL	SL	f	f = Left Shift f	1	1	C,N,OV,Z
		SL	f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL	Ws,Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
72	SUB	SUB	Acc	Subtract Accumulators	1	1	OA,OB,OAB, SA,SB,SAB
		SUB	f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB	f,WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB	#lit10,Wn	Wn = Wn – lit10	1	1	C,DC,N,OV,Z
		SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
73	SUBB	SUBB	f	f = f – WREG – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB	f,WREG	WREG = f – WREG – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB	#lit10,Wn	Wn = Wn – lit10 – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB	Wb,Ws,Wd	Wd = Wb – Ws – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB	Wb,#lit5,Wd	Wd = Wb – lit5 – ($\overline{C}$)	1	1	C,DC,N,OV,Z
74	SUBR	SUBR	f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	f,WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
75	SUBBR	SUBBR	f	f = WREG – f – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR	f,WREG	WREG = WREG – f – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR	Wb,Ws,Wd	Wd = Ws – Wb – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR	Wb,#lit5,Wd	Wd = lit5 – Wb – ($\overline{C}$)	1	1	C,DC,N,OV,Z
76	SWAP	SWAP.b	Wn	Wn = Nibble Swap Wn	1	1	None
		SWAP	Wn	Wn = Byte Swap Wn	1	1	None
77	TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	2	None
78	TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	2	None
79	TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
80	TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
81	ULNK	ULNK		Unlink Frame Pointer	1	1	None
82	XOR	XOR	f	f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
83	ZE	ZE	Ws,Wnd	Wnd = Zero-Extend Ws	1	1	C,Z,N

23.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

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  - MPLAB® IDE Software
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  - MPLAB C18 and MPLAB C30 C Compilers
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  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debugger
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  - PICkit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

23.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (assembly or C)
  - Mixed assembly and C
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

23.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

23.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

23.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of linking many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

23.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

23.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

23.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

23.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

23.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

23.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

23.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

23.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

23.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

24.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings(1)

Ambient temperature under bias .... -40°C to +125°C
Storage temperature .... -65°C to +150°C
Voltage on VDD with respect to VSS .... -0.3V to +4.0V
Voltage on any combined analog and digital pin and $\overline{\text{MCLR}}$, with respect to VSS .... -0.3V to (VDD + 0.3V)
Voltage on any digital-only pin with respect to VSS .... -0.3V to +5.6V
Voltage on VCAP/VDDCORE with respect to VSS .... 2.25V to 2.75V
Maximum current out of VSS pin .... 300 mA
Maximum current into VDD pin(2) .... 250 mA
Maximum output current sunk by any I/O pin(3) .... 4 mA
Maximum output current sourced by any I/O pin(3) .... 4 mA
Maximum current sunk by all ports .... 200 mA
Maximum current sourced by all ports(2) .... 200 mA
Maximum output current sunk by non-remappable PWM pins .... 16 mA
Maximum output current sourced by non-remappable PWM pins .... 16 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 24-2).

3: Exceptions are PWMxL, and PWMxH, which are able to sink/source 16 mA, and digital pins, which are able to sink/source 8 mA.

24.1 DC Characteristics

TABLE 24-1: OPERATING MIPS VS. VOLTAGE

Characteristic	V_{DD} Range (in Volts)	Temp Range (in °C)	Max MIPS
			dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04
	3.0-3.6V	-40°C to +85°C	40
	3.0-3.6V	-40°C to +125°C	40

TABLE 24-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+140	°C
Operating Ambient Temperature Range	T_A	-40	—	+125	°C
Power Dissipation: Internal chip power dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $I/O = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 24-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 44-Pin QFN	θ_{JA}	28	—	°C/W	1
Package Thermal Resistance, 44-Pin TFQP	θ_{JA}	39	—	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θ_{JA}	42	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θ_{JA}	47	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN-S	θ_{JA}	34	—	°C/W	1
Package Thermal Resistance, 18-Pin SOIC	θ_{JA}	57	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

TABLE 24-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Operating Voltage							
	Supply Voltage						
DC10	VDD		3.0	—	3.6	V	Industrial and extended
DC12	VDR	**RAM Data Retention Voltage(2)**	1.8	—	—	V	
DC16	VPOR	**VDD Start Voltage(4)** to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
DC17	SVDD	**VDD Rise Rate(3)** to Ensure Internal Power-on Reset Signal	0.03	—	—	V/ms	0-3.0V in 0.1s
DC18	VCORE	**VDD Core** Internal Regulator Voltage	2.25	—	2.75	V	Voltage is dependent on load, temperature and VDD

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.
2: This is the limit to which VDD may be lowered without losing RAM data.
3: These parameters are characterized but not tested in manufacturing.
4: VDD voltage must remain at VSS for a minimum of 200 μs to ensure POR.

TABLE 24-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Operating Current (IDD)(2)						
DC20d	55	70	mA	-40°C	3.3V	10 MIPS See **Note 2**
DC20a	55	70	mA	+25°C		
DC20b	55	70	mA	+85°C		
DC20c	55	70	mA	+125°C		
DC21d	68	85	mA	-40°C	3.3V	16 MIPS See **Note 2** and **Note 3**
DC21a	68	85	mA	+25°C		
DC21b	68	85	mA	+85°C		
DC21c	68	85	mA	+125°C		
DC22d	78	95	mA	-40°C	3.3V	20 MIPS See **Note 2** and **Note 3**
DC22a	78	95	mA	+25°C		
DC22b	78	95	mA	+85°C		
DC22c	78	95	mA	+125°C		
DC23d	88	110	mA	-40°C	3.3V	30 MIPS See **Note 2** and **Note 3**
DC23a	88	110	mA	+25°C		
DC23b	88	110	mA	+85°C		
DC23c	88	110	mA	+125°C		
DC24d	98	120	mA	-40°C	3.3V	40 MIPS See **Note 2**
DC24a	98	120	mA	+25°C		
DC24b	98	120	mA	+85°C		
DC24c	98	120	mA	+125°C		
DC25d	128	160	mA	-40°C	3.3V	40 MIPS See **Note 2**, except PWM is operating at maximum speed (PTCON2 = 0x0000)
DC25a	125	150	mA	+25°C		
DC25b	121	150	mA	+85°C		
DC25c	119	150	mA	+125°C		
DC26d	115	140	mA	-40°C	3.3V	40 MIPS See **Note 2**, except PWM is operating at 1/2 speed (PTCON2 = 0x0001)
DC26a	112	140	mA	+25°C		
DC26b	110	140	mA	+85°C		
DC26c	108	140	mA	+125°C		
DC27d	111	140	mA	-40°C	3.3V	40 MIPS See **Note 2**, except PWM is operating at 1/4 speed (PTCON2 = 0x0002)
DC27a	108	130	mA	+25°C		
DC27b	105	130	mA	+85°C		
DC27c	103	130	mA	+125°C		
DC28d	102	130	mA	-40°C	3.3V	40 MIPS See **Note 2**, except PWM is operating at 1/8 speed (PTCON2 = 0x0003)
DC28a	100	120	mA	+25°C		
DC28b	100	120	mA	+85°C		
DC28c	100	120	mA	+125°C		

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows: OSC1 driven with external square wave from rail to rail. All I/O pins are configured as inputs and pulled to VSS. $\overline{MCLR}$ = VDD, WDT and FSCM are disabled. CPU, SRAM, program memory and data memory are operational. No peripheral modules are operating (PMD bits are all set).

3: These parameters are characterized but not tested in manufacturing.

TABLE 24-6: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	Typical(1)	Max	Units	Conditions		
Idle Current (I_{IDLE}): Core Off Clock On Base Current(2)						
DC40d	80	100	mA	-40°C	3.3V	10 MIPS
DC40a	80	100	mA	+25°C		
DC40b	80	100	mA	+85°C		
DC40c	80	100	mA	+125°C		
DC41d	81	100	mA	-40°C	3.3V	16 MIPS(3)
DC41a	81	100	mA	+25°C		
DC41b	81	100	mA	+85°C		
DC41c	81	100	mA	+125°C		
DC42d	82	100	mA	-40°C	3.3V	20 MIPS(3)
DC42a	82	100	mA	+25°C		
DC42b	82	100	mA	+85°C		
DC42c	82	100	mA	+125°C		
DC43d	84	105	mA	-40°C	3.3V	30 MIPS(3)
DC43a	84	105	mA	+25°C		
DC43b	84	105	mA	+85°C		
DC43c	84	105	mA	+125°C		
DC44d	86	105	mA	-40°C	3.3V	40 MIPS
DC44a	86	105	mA	+25°C		
DC44b	86	105	mA	+85°C		
DC44c	86	105	mA	+125°C		

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: Base I_{IDLE} current is measured with core off, clock on and all modules turned off. Peripheral module Disable SFR registers are zeroed. All I/O pins are configured as inputs and pulled to V_{SS}.

3: These parameters are characterized but not tested in manufacturing.

TABLE 24-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical[1]**	**Max**	**Units**	**Conditions**		
Power-Down Current (IPD)[2,4]						
DC60d	304	500	μA	-40°C	3.3V	Base Power-Down Current
DC60a	317	500	μA	+25°C		
DC60b	321	500	μA	+85°C		
DC60c	800	950	μA	+125°C		
DC61d	40	50	μA	-40°C	3.3V	Watchdog Timer Current: ΔIWDT[3]
DC61a	40	50	μA	+25°C		
DC61b	40	50	μA	+85°C		
DC61c	80	90	μA	+125°C		

Note 1: Data in the Typical column is at 3.3V, +25°C unless otherwise stated.

2: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to VSS. WDT, etc., are all switched off, and VREGS (RCON<8>) = 1.

3: The Δ current is the additional current consumed when the WDT module is enabled. This current should be added to the base IPD current.

4: These currents are measured on the device containing the most memory in this family.

TABLE 24-8: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	**Typical[1]**	**Max**	**Doze Ratio**	**Units**	**Conditions**		
DC73a	86	105	1:2	mA	-40°C	3.3V	40 MIPS
DC73f	86	105	1:64	mA			
DC73g	86	105	1:128	mA			
DC70a	86	105	1:2	mA	+25°C	3.3V	40 MIPS
DC70f	86	105	1:64	mA			
DC70g	86	105	1:128	mA			
DC71a	86	105	1:2	mA	+85°C	3.3V	40 MIPS
DC71f	86	105	1:64	mA			
DC71g	86	105	1:128	mA			
DC72a	86	105	1:2	mA	+125°C	3.3V	40 MIPS
DC72f	86	105	1:64	mA			
DC72g	86	105	1:128	mA			

Note 1: Data in the Typical column is at 3.3V, +25°C unless otherwise stated.

TABLE 24-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
DI10		I/O Pins	VSS	—	0.2 VDD	V	
DI15		$\overline{MCLR}$	VSS	—	0.2 VDD	V	
DI16		I/O Pins with OSC1	VSS	—	0.2 VDD	V	
DI18		I/O Pins with SDAx, SCLx	VSS	—	0.3 VDD	V	SMbus disabled
DI19		I/O Pins with SDAx, SCLx	VSS	—	0.2 VDD	V	SMbus enabled
	VIH	**Input High Voltage**					
DI20		I/O Pins Not 5V Tolerant(4)	0.7 VDD	—	VDD	V	
DI21		I/O Pins 5V Tolerant(4)	0.7 VDD	—	5.5	V	
	ICNPU	**CNx Pull-up Current**					
DI30			—	250	—	μA	VDD = 3.3V, VPIN = VSS
	IIL	**Input Leakage Current(2,3,4)**					
DI50		I/O Pins with: 4 mA Source/Sink Capability	—	±2	—	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
		8 mA Source/Sink Capability	—	±4	—	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
		16 mA Source/Sink Capability	—	±8	—	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI55		$\overline{MCLR}$	—	—	±2	μA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	—	—	±2	μA	VSS ≤ VPIN ≤ VDD, XT and HS modes
	ISINK	**Sink Current** Pins: RA3, RA4, RB3, RB4, RB11-RB14	—	16	—	mA	
		Pins: RC3-RC8, RC11-RC13	—	8	—	mA	
		Pins: RA0-RA2, RB0, RB1, RB5-RB10, RB15, RC1, RC2, RC9, RC10	—	4	—	mA	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
3: Negative current is defined as current sourced by the pin.
4: See **"Pin Diagrams"** for the list of 5V tolerant I/O pins.

TABLE 24-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
DO10	V_{OL}	**Output Low Voltage**					
		I/O Ports:					
		4 mA Source/Sink Capability	—	0.4	—	V	I_{OL} = 4 mA, V_{DD} = 3.3V
		8 mA Source/Sink Capability	—	0.4	—	V	I_{OL} = 8 mA, V_{DD} = 3.3V
		16 mA Source/Sink Capability	—	0.4	—	V	I_{OL} = 16 mA, V_{DD} = 3.3V
DO16		OSC2/CLKO	—	0.4	—	V	I_{OL} = 2 mA, V_{DD} = 3.3V
DO20	V_{OH}	**Output High Voltage**					
		I/O Ports:					
		4 mA Source/Sink Capability	—	2.40	—	V	I_{OH} = -4 mA, V_{DD} = 3.3V
		8 mA Source/Sink Capability	—	2.40	—	V	I_{OH} = -8 mA, V_{DD} = 3.3V
		16 mA Source/Sink Capability	—	2.40	—	V	I_{OH} = -16 mA, V_{DD} = 3.3V
DO26		OSC2/CLKO	—	2.41	—	V	I_{OH} = -1.3 mA, V_{DD} = 3.3V
	I_{SOURCE}	**Source Current**					
		Pins: RA3, RA4, RB3, RB4, RB11-RB14	—	16	—	mA	
		Pins: RC3-RC8, RC11-RC13	—	8	—	mA	
		Pins: RA0-RA2, RB0, RB1, RB5-RB10, RB15, RC1, RC2, RC9, RC10	—	4	—	mA	

TABLE 24-11: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min(1)**	**Typ**	**Max**	**Units**	**Conditions**
BO10	V_{BOR}	BOR Event on V_{DD} Transition High-to-Low BOR Event is Tied to V_{DD} Core Voltage Decrease	2.55	—	2.79	V	

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

TABLE 24-12: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132B	VPEW	VDD for Self-Timed Write	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C
D135	IDDP	Supply Current during Programming	—	10	—	mA	
D136a	TRW	Row Write Time	1.32	—	1.74	ms	TRW = 11064 FRC cycles, TA = +85°C, See **Note 2**
D136b	TRW	Row Write Time	1.28	—	1.79	ms	TRW = 11064 FRC cycles, TA = +125°C, See **Note 2**
D137a	TPE	Page Erase Time	20.1	—	26.5	ms	TPE = 168517 FRC cycles, TA = +85°C, See **Note 2**
D137b	TPE	Page Erase Time	19.5	—	27.3	ms	TPE = 168517 FRC cycles, TA = +125°C, See **Note 2**
D138a	TWW	Word Write Cycle Time	42.3	—	55.9	µs	TWW = 355 FRC cycles, TA = +85°C, See **Note 2**
D138b	TWW	Word Write Cycle Time	41.1	—	57.6	µs	TWW = 355 FRC cycles, TA = +125°C, See **Note 2**

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

2: Other conditions: FRC = 7.37 MHz, TUN<5:0> = `b'011111` (for Min), TUN<5:0> = `b'100000` (for Max). This parameter depends on the FRC accuracy (see Table 24-20) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time see **Section 5.3 “Programming Operations”**.

TABLE 24-13: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	CEFC	External Filter Capacitor Value	4.7	10	—	µF	Capacitor must be low series resistance (< 5 ohms)

24.2 AC Characteristics and Timing Parameters

This section defines dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 AC characteristics and timing parameters.

TABLE 24-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended Operating voltage VDD range as described in **Section 24.0 "Electrical Characteristics"**.

FIGURE 24-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

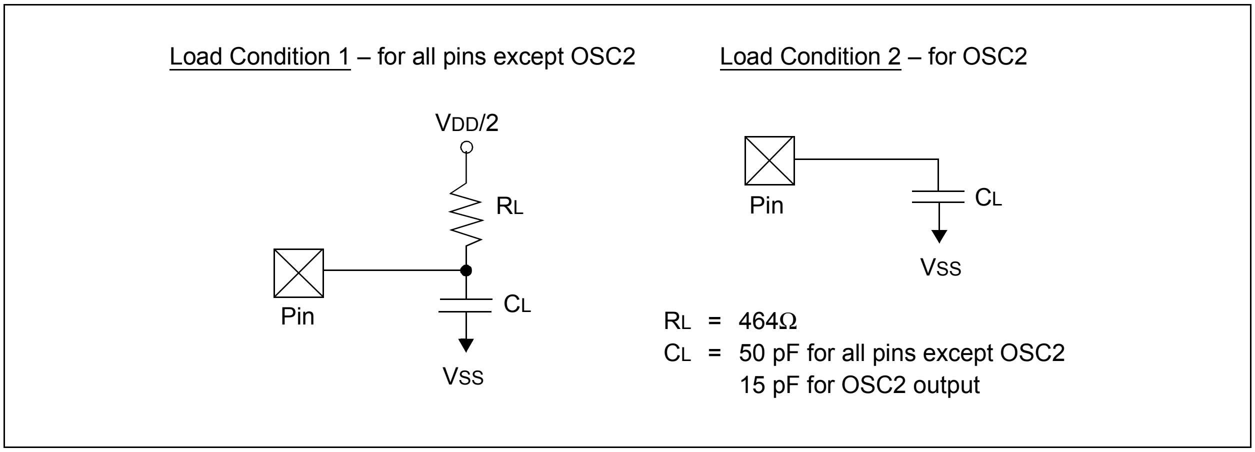


TABLE 24-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
DO50	COSCO	OSC2 Pin	—	—	15	pF	In XT and HS modes when external clock is used to drive OSC1
DO56	CIO	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^{2}C™ mode

FIGURE 24-2: EXTERNAL CLOCK TIMING

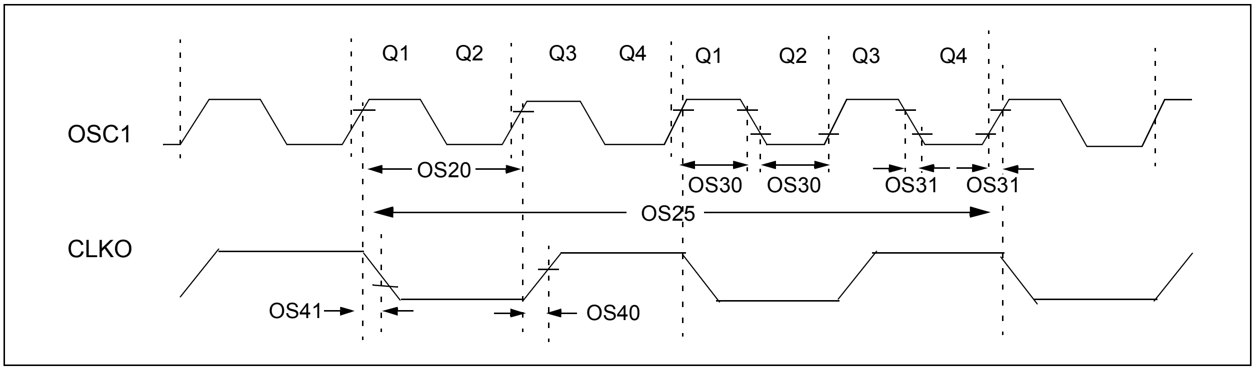


TABLE 24-16: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symb**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	40	MHz	EC
		Oscillator Crystal Frequency	3.5 10	— —	10 40	MHz MHz	XT HS
OS20	TOSC	TOSC = 1/FOSC	12.5	—	DC	ns	
OS25	TCY	Instruction Cycle Time(2)	25	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.375 x TOSC	—	0.625 x TOSC	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time(3)	—	5.2	—	ns	
OS41	TckF	CLKO Fall Time(3)	—	5.2	—	ns	
OS42	GM	External Oscillator Transconductance(4)	14	16	18	mA/V	VDD = 3.3V TA = +25ºC

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

2: Instruction cycle period (TCY) equals two times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

4: Data for this parameter is Preliminary. This parameter is characterized, but not tested in manufacturing.

TABLE 24-17: PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 3.0V TO 3.6V)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
OS50	F_{PLLI}	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8	MHz	ECPLL, XTPLL modes
OS51	F_{SYS}	On-Chip VCO System Frequency	100	—	200	MHz	
OS52	T_{LOCK}	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	mS	
OS53	D_{CLK}	CLKO Stability (Jitter)	-3	0.5	3	%	Measured over 100 ms period

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested in manufacturing.

TABLE 24-18: AUXILIARY PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 3.0V TO 3.6V)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	F_{HPOUT}	0n-Chip 16x PLL CCO Frequency	105	120	135	MHz	
	F_{HPIN}	On-Chip 16x PLL Phase Detector Input Frequency	6.56	7.5	8.44	MHz	
	T_{SU}	Frequency Generator Lock Time	—	—	10	µs	

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested in manufacturing.

TABLE 24-19: AC CHARACTERISTICS: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for industrial -40°C ≤ T_A ≤ +125°C for Extended					
Param No.	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
	Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1,2)						
F20	FRC	—	±2	—	%	-40°C ≤ T_A ≤ +85°C	V_{DD} = 3.0-3.6V
	FRC	—	±5	—	%	-40°C ≤ T_A ≤ +125°C	V_{DD} = 3.0-3.6V

Note 1: Frequency calibrated at +25°C and 3.3V. TUN bits can be used to compensate for temperature drift.

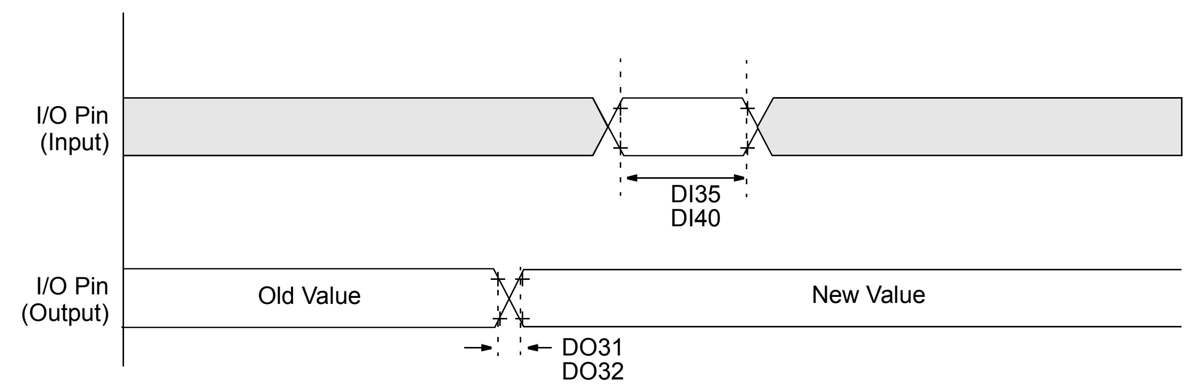
2: FRC is set to initial frequency of 7.37 MHz (±2%) at +25°C.

TABLE 24-20: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
	LPRC @ 32.768 kHz(1)						
F21	LPRC	-20	±6	+20	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
	LPRC	-70	—	+70	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: Change of LPRC frequency as VDD changes.

FIGURE 24-3: I/O TIMING CHARACTERISTICS



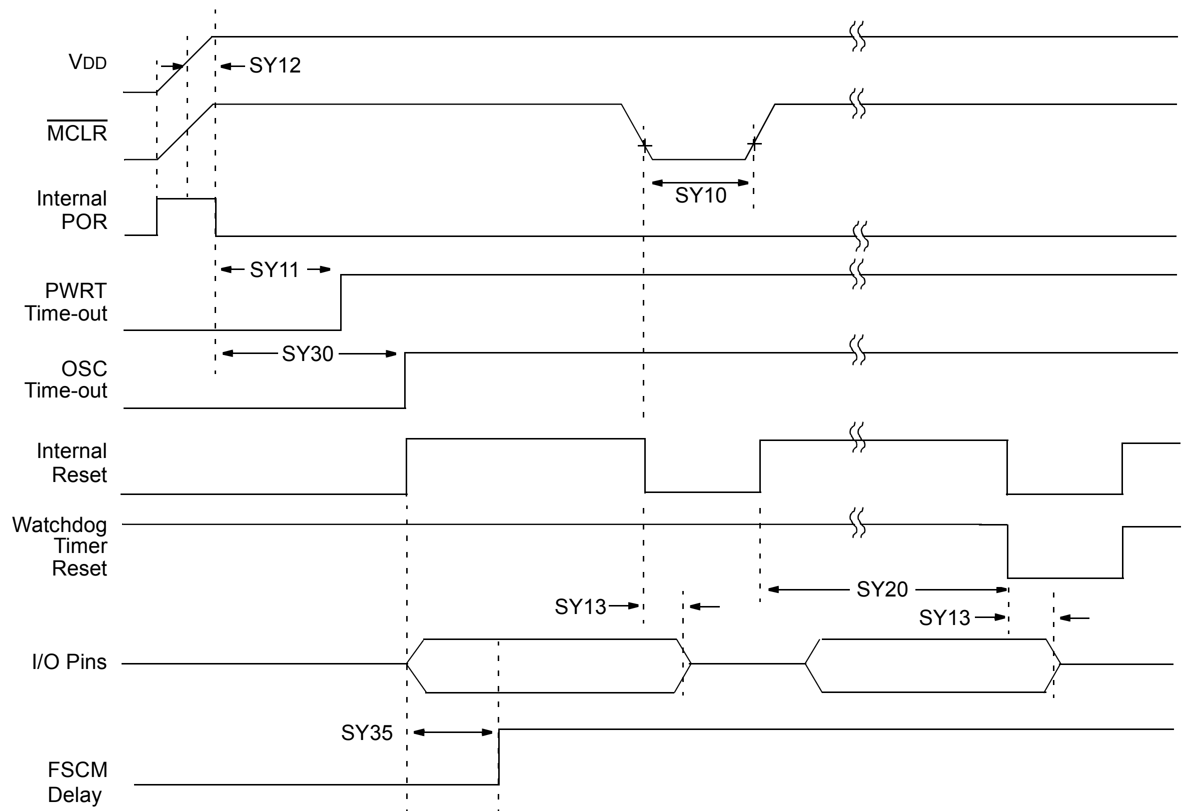
Note: Refer to Figure 24-1 for load conditions.

TABLE 24-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
DO31	TIOR	Port Output Rise Time	—	10	25	ns	Refer to Figure 24-1 for test conditions
DO32	TIOF	Port Output Fall Time	—	10	25	ns	Refer to Figure 24-1 for test conditions
DI35	TINP	INTx Pin High or Low Time (output)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TCY	

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

FIGURE 24-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING CHARACTERISTICS



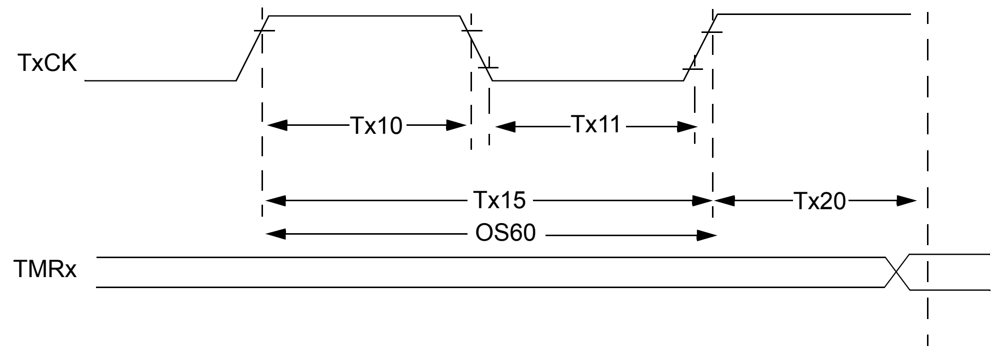
Note: Refer to Figure 24-1 for load conditions.

TABLE 24-22: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic[1]**	**Min**	**Typ[2]**	**Max**	**Units**	**Conditions**
SY10	TMCL	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	μs	-40°C to +85°C
SY11	TPWRT	Power-up Timer Period	—	2 4 8 16 32 64 128	—	ms	-40°C to +85°C User programmable
SY12	TPOR	Power-on Reset Delay	3	10	30	μs	-40°C to +85°C
SY13	TIOZ	I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	0.68	0.72	1.2	μs	
SY20	TWDT1	Watchdog Timer Time-out Period	—	—	—	ms	See **Section 21.4 "Watchdog Timer (WDT)"** and LPRC parameter F21 (Table 24-20).
SY30	TOST	Oscillator Start-up Time	—	1024 TOSC	—	—	TOSC = OSC1 period

Note 1: These parameters are characterized but not tested in manufacturing.
2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

FIGURE 24-5: TIMER1, 2 AND 3 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 24-1 for load conditions.

TABLE 24-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)

AC CHARACTERISTICS				**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
TA10	TTXH	TxCK High Time	Synchronous, no prescaler	0.5 TCY + 20	—	—	ns	Must also meet parameter TA15
			Synchronous, with prescaler	10	—	—	ns	
			Asynchronous	10	—	—	ns	
TA11	TTXL	TxCK Low Time	Synchronous, no prescaler	0.5 TCY + 20	—	—	ns	Must also meet parameter TA15
			Synchronous, with prescaler	10	—	—	ns	
			Asynchronous	10	—	—	ns	
TA15	TTXP	TxCK Input Period	Synchronous, no prescaler	TCY + 40	—	—	ns	
			Synchronous, with prescaler	Greater of: 20 ns or (TCY + 40)/N	—	—	—	N = prescale value (1, 8, 64, 256)
			Asynchronous	20	—	—	ns	
OS60	Ft1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>))		DC	—	50	kHz	
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.5 TCY		1.5 TCY	—	

Note 1: Timer1 is a Type A.

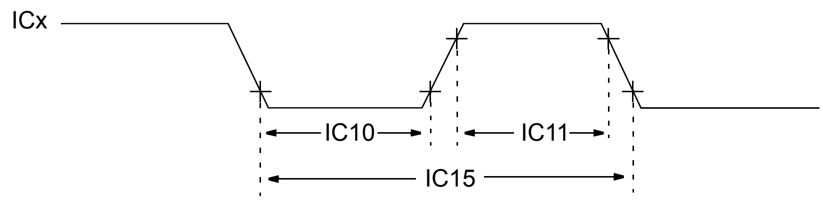
TABLE 24-24: TIMER2 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
TB10	TTXH	TxCK High Time	Synchronous, no prescaler	0.5 TCY + 20	—	—	ns	Must also meet parameter TB15
			Synchronous, with prescaler	10	—	—	ns	
TB11	TTXL	TxCK Low Time	Synchronous, no prescaler	0.5 TCY + 20	—	—	ns	Must also meet parameter TB15
			Synchronous, with prescaler	10	—	—	ns	
TB15	TTXP	TxCK Input Period	Synchronous, no prescaler	TCY + 40	—	—	ns	N = prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	Greater of: 20 ns or (TCY + 40)/N				
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.5 TCY	—	1.5 TCY	—	

TABLE 24-25: TIMER3 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
TC10	TTXH	TxCK High Time	Synchronous	0.5 TCY + 20	—	—	ns	Must also meet parameter TC15
TC11	TTXL	TxCK Low Time	Synchronous	0.5 TCY + 20	—	—	ns	Must also meet parameter TC15
TC15	TTXP	TxCK Input Period	Synchronous, no prescaler	TCY + 40	—	—	ns	N = prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	Greater of: 20 ns or (TCY + 40)/N				
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.5 TCY	—	1.5 TCY	—	

FIGURE 24-6: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS



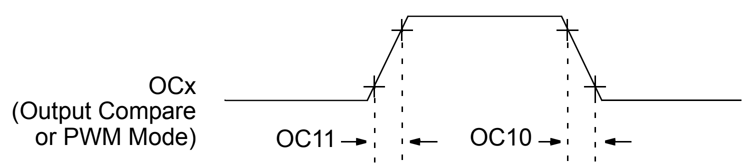
Note: Refer to Figure 24-1 for load conditions.

TABLE 24-26: INPUT CAPTURE TIMING REQUIREMENTS

AC CHARACTERISTICS				**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic(1)**		**Min**	**Max**	**Units**	**Conditions**
IC10	TccL	ICx Input Low Time	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
IC11	TccH	ICx Input High Time	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
IC15	TccP	ICx Input Period		(TCY + 40)/N	—	ns	N = prescale value (1, 4, 16)

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 24-7: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 24-1 for load conditions.

TABLE 24-27: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter D032
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter D031

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 24-8: OC/PWM MODULE TIMING CHARACTERISTICS

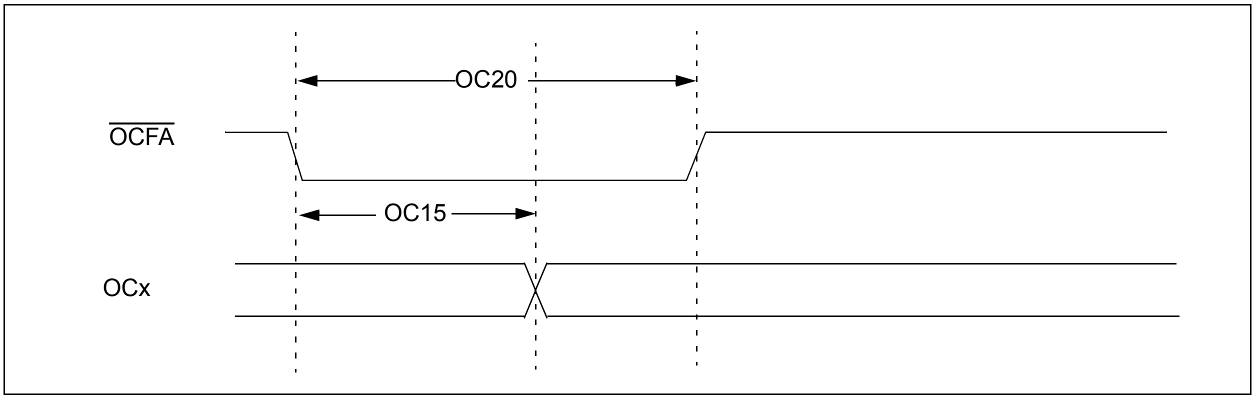


TABLE 24-28: SIMPLE OC/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic(1)	Min	Typ	Max	Units	Conditions
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 24-9: HIGH-SPEED PWM MODULE FAULT TIMING CHARACTERISTICS

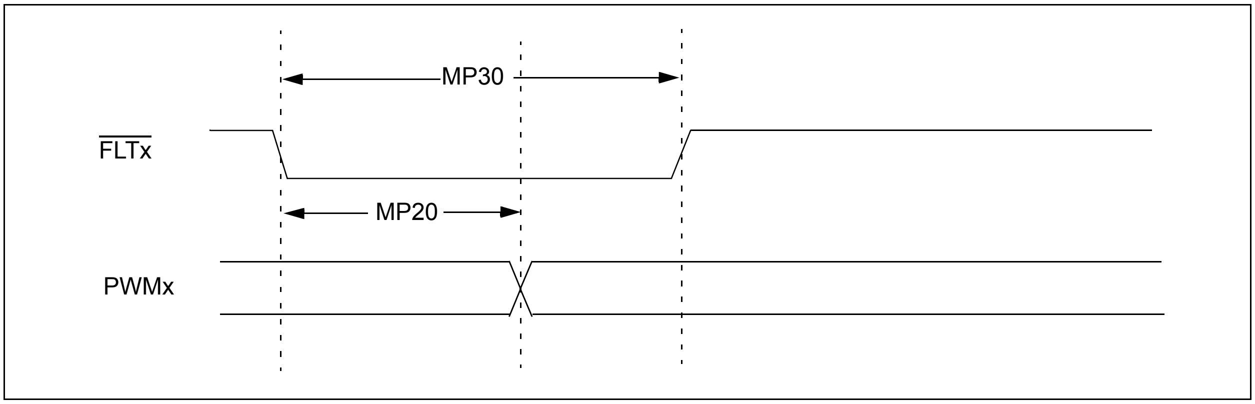
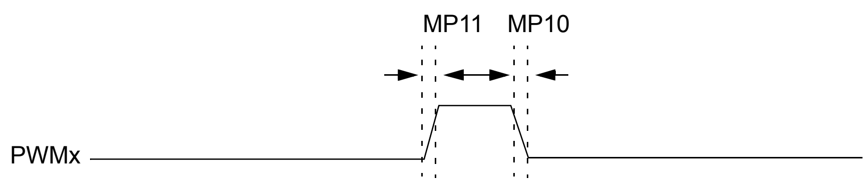


FIGURE 24-10: HIGH-SPEED PWM MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 24-1 for load conditions.

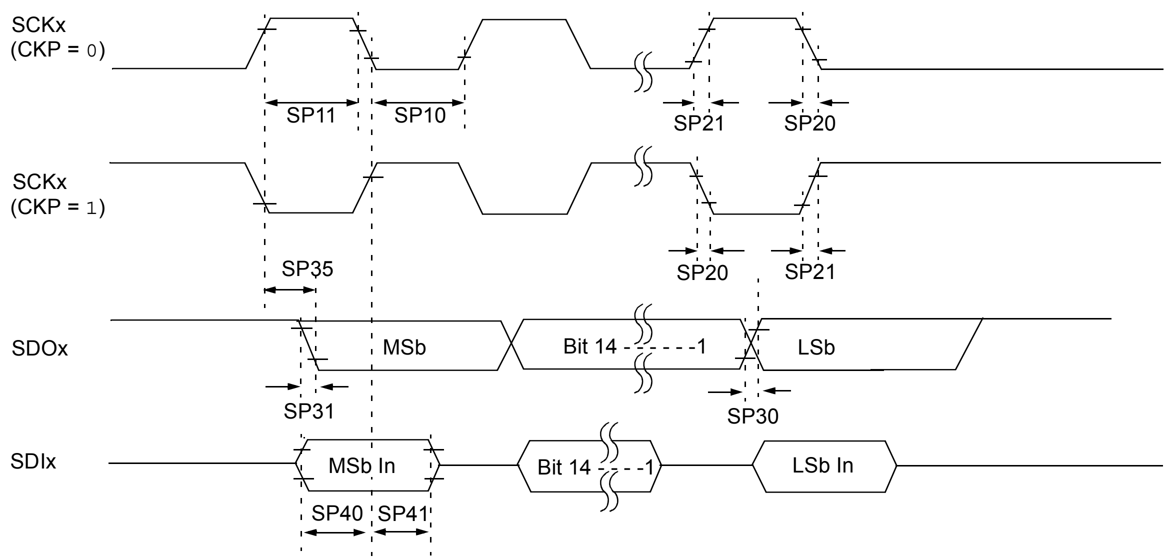
TABLE 24-29: HIGH-SPEED PWM MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
MP10	TFPWM	PWM Output Fall Time	—	2.5	—	ns	See parameter D032
MP11	TRPWM	PWM Output Rise Time	—	2.5	—	ns	See parameter D031
MP20	TFD	Fault Input ↓ to PWM I/O Change	—	—	15	ns	
MP30	TFH	Minimum Pulse Width	—	8	—	ns	
	TPDLY	Tap Delay	—	1.04	—	ns	ACLK = 120 MHz
	ACLK	PWM Input Clock	—	—	120	MHz	

Note 1: These parameters are characterized but not tested in manufacturing.

 Preliminary

FIGURE 24-11: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



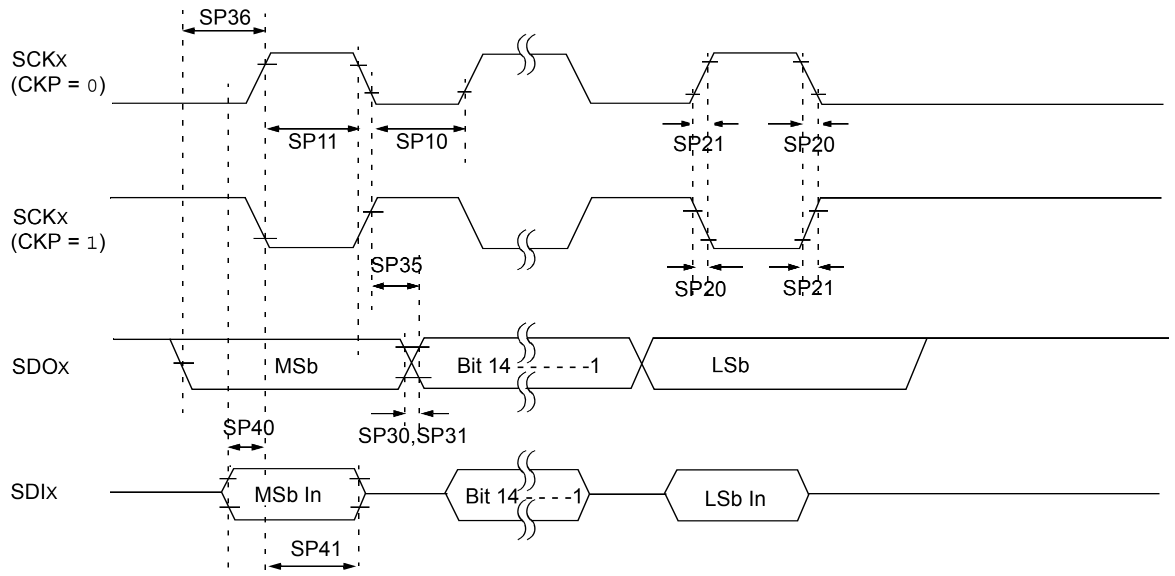
Note: Refer to Figure 24-1 for load conditions.

TABLE 24-30: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time	TCY/2	—	—	ns	See **Note 3**
SP11	TscH	SCKx Output High Time	TCY/2	—	—	ns	See **Note 3**
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See parameter D032 and **Note 4**
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See parameter D031 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter D032 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter D031 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	23	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.
2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
3: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.
4: Assumes 50 pF load on all SPIx pins.

FIGURE 24-12: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



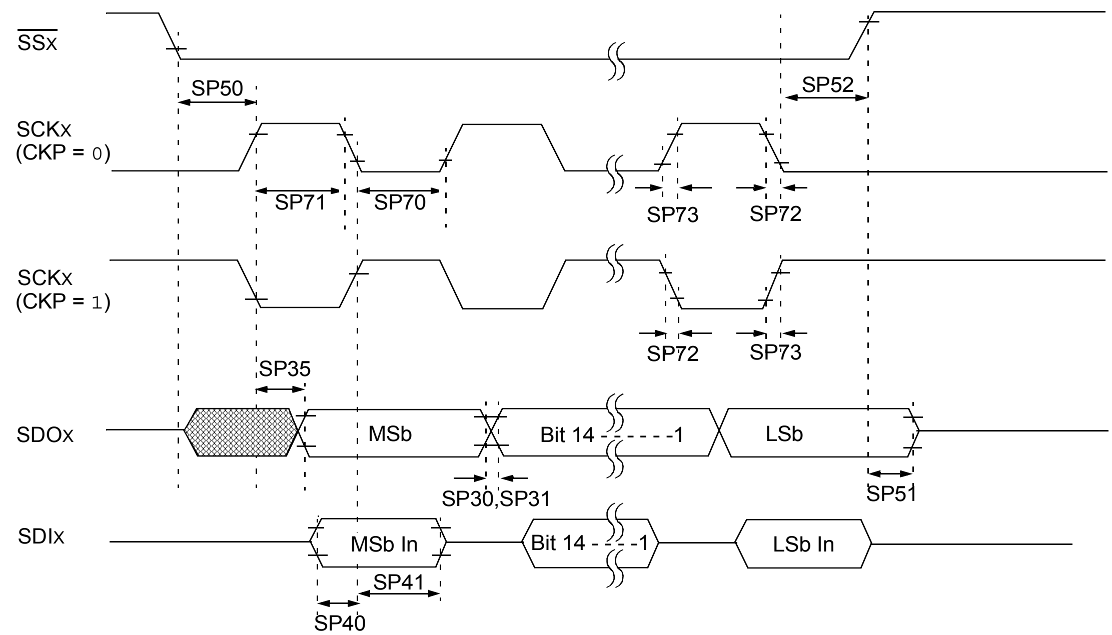
Note: Refer to Figure 24-1 for load conditions.

TABLE 24-31: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic(1)	Min	Typ(2)	Max	Units	Conditions
SP10	TscL	SCKx Output Low Time	TCY/2	—	—	ns	See **Note 3**
SP11	TscH	SCKx Output High Time	TCY/2	—	—	ns	See **Note 3**
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See parameter D032 and **Note 4**
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See parameter D031 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter D032 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter D031 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	23	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.
2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
3: The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.
4: Assumes 50 pF load on all SPIx pins.

FIGURE 24-13: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS



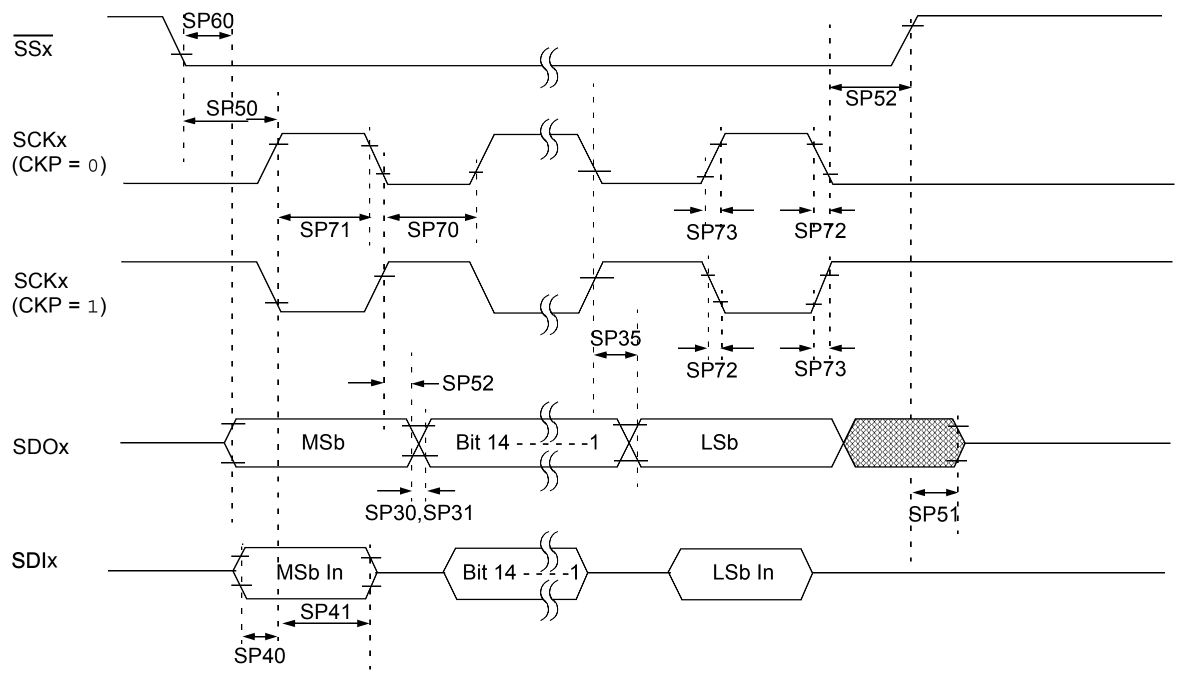
Note: Refer to Figure 24-1 for load conditions.

TABLE 24-32: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic[1]**	**Min**	**Typ[2]**	**Max**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time	30	—	—	ns	
SP71	TscH	SCKx Input High Time	30	—	—	ns	
SP72	TscF	SCKx Input Fall Time	—	10	25	ns	See **Note 3**
SP73	TscR	SCKx Input Rise Time	—	10	25	ns	See **Note 3**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter D032 and **Note 3**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter D031 and **Note 3**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{\text{SSx}}$ ↓ to SCKx ↑ or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{\text{SSx}}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	See **Note 3**
SP52	TscH2ssH TscL2ssH	$\overline{\text{SSx}}$ after SCKx Edge	1.5 TCY +40	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.
2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
3: Assumes 50 pF load on all SPIx pins.

FIGURE 24-14: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 24-1 for load conditions.

TABLE 24-33: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]	Min	Typ[2]	Max	Units	Conditions
SP70	TscL	SCKx Input Low Time	30	—	—	ns	
SP71	TscH	SCKx Input High Time	30	—	—	ns	
SP72	TscF	SCKx Input Fall Time	—	10	25	ns	See **Note 3**
SP73	TscR	SCKx Input Rise Time	—	10	25	ns	See **Note 3**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter D032 and **Note 3**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter D031 and **Note 3**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	1.5 TCY + 40	—	—	ns	
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	50	ns	

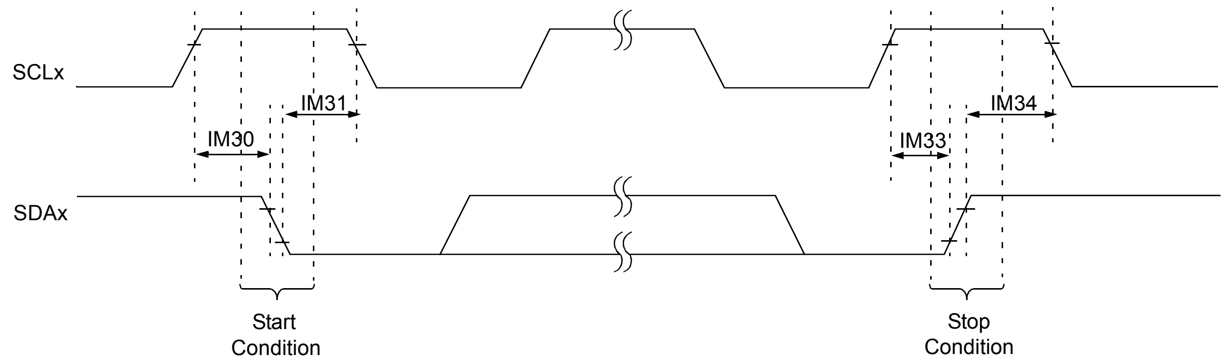
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.

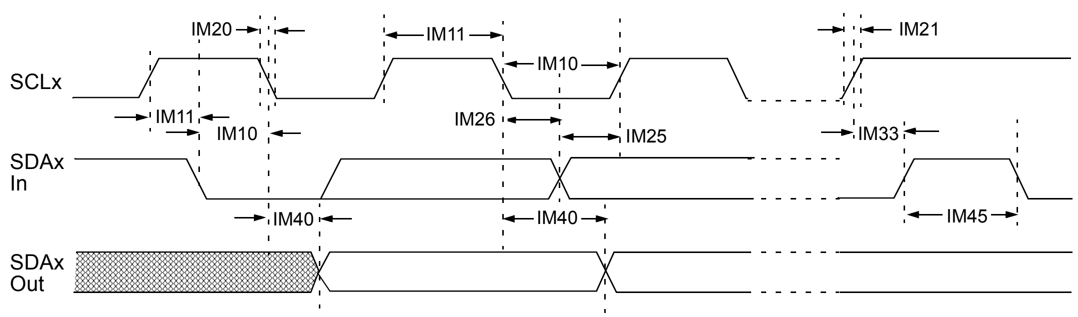
4: Assumes 50 pF load on all SPIx pins.

FIGURE 24-15: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 24-1 for load conditions.

FIGURE 24-16: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 24-1 for load conditions.

TABLE 24-34: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic**		**Min(1)**	**Max**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM11	THI:SCL	Clock High Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 pF to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 pF to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(2)	40	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(2)	0.2	—	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	After this period the first clock pulse is generated
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TCY/2 (BRG + 1)	—	µs	
			400 kHz mode	TCY/2 (BRG + 1)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TCY/2 (BRG + 1)	—	ns	
			400 kHz mode	TCY/2 (BRG + 1)	—	ns	
			1 MHz mode(2)	TCY/2 (BRG + 1)	—	ns	
IM40	TAA:SCL	Output Valid From Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode(2)	—	400	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(2)	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	400	pF	

Note 1: BRG is the value of the I²C™ Baud Rate Generator. Refer to **Section 19. "Inter-Integrated Circuit (I²C™)"** (DS70195) in the "*dsPIC33F Family Reference Manual*" available from the Microchip web site.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

FIGURE 24-17: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

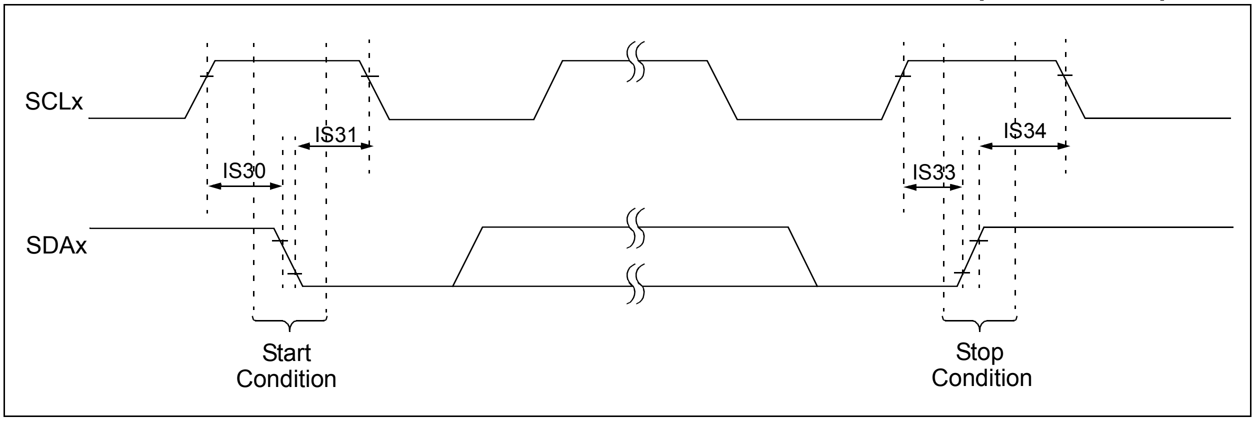


FIGURE 24-18: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

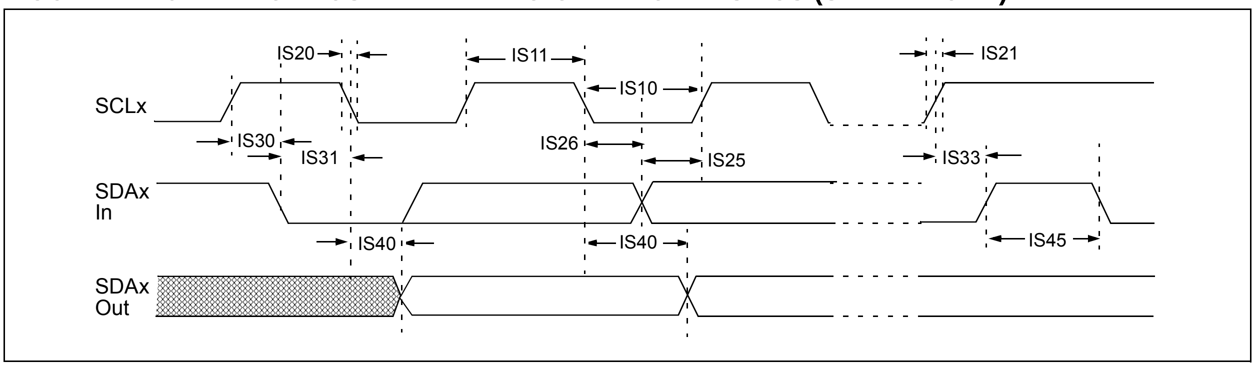


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TABLE 24-35: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param.	**Symbol**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a minimum of 10 MHz
			1 MHz mode(1)	0.5	—	μs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			1 MHz mode(1)	0.5	—	μs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 pF to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 pF to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(1)	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	
			400 kHz mode	0	0.9	μs	
			1 MHz mode(1)	0	0.3	μs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	μs	
			1 MHz mode(1)	0.25	—	μs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	μs	
			1 MHz mode(1)	0.25	—	μs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
			1 MHz mode(1)	0.6	—	μs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1 MHz mode(1)	250		ns	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode(1)	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode(1)	0.5	—	μs	
IS50	CB	Bus Capacitive Loading		—	400	pF	

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

TABLE 24-36: 10-BIT HIGH-SPEED A/D MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V and 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	—	—	—	—	See the VDD specification (DC10) in Table 24-4
AD02	AVSS	Module VSS Supply	—	—	—	—	AVSS is connected to VSS
Analog Input							
AD10	VINH-VINL	Full-Scale Input Span	VSS		VDD	V	
AD11	VIN	Absolute Input Voltage	AVSS		AVDD	V	
AD12	IAD	Operating Current	—	8	—	mA	
AD13	—	Leakage Current	—	±0.6	—	μA	VINL = AVSS = 0V, AVDD = 3.3V Source Impedance = 100Ω
AD17	RIN	Recommended Impedance Of Analog Voltage Source	—		100	Ω	
DC Accuracy							
AD20	Nr	Resolution	10 data bits			bits	
AD21A	INL	Integral Nonlinearity	—	±0.5	<±2	LSb	See Note 2
AD22A	DNL	Differential Nonlinearity	—	±0.5	<±1	LSb	See Note 2
AD23A	GERR	Gain Error	—	±0.75	<±3.0	LSb	See Note 2
AD24A	EOFF	Offset Error	—	±2.0	<±5.0	LSb	See Note 2
AD25	—	Monotonicity(1)	—	—	—	—	Guaranteed
Dynamic Performance							
AD30	THD	Total Harmonic Distortion	—	-73	—	dB	
AD31	SINAD	Signal to Noise and Distortion	—	58	—	dB	
AD32	SFDR	Spurious Free Dynamic Range	—	-73	—	dB	
AD33	FNYQ	Input Signal Bandwidth	—	—	0.5	MHz	
AD34	ENOB	Effective Number of Bits	—	9.4	—	bits	

Note 1: The A/D conversion result never decreases with an increase in the input voltage, and has no missing codes.

2: This parameter is characterized under the following conditions: AV_{DD} = 3.3V, 2.0 MSPS for dedicated S/H, 1.5 MSPS for shared S/H. This parameter is not tested in manufacturing.

TABLE 24-37: 10-BIT HIGH-SPEED A/D MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ(1)	Max.	Units	Conditions
Clock Parameters							
AD50b	TAD	ADC Clock Period	35.8	—	—	ns	
Conversion Rate							
AD55b	tCONV	Conversion Time	—	14 TAD	—	—	
AD56b	FCNV	Throughput Rate					
		Devices with Single SAR	—	—	2.0	Msps	
		Devices with Dual SARs	—	—	4.0	Msps	
Timing Parameters							
AD63b	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On(1)	1.0	—	10	µs	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 24-19: A/D CONVERSION TIMING PER INPUT

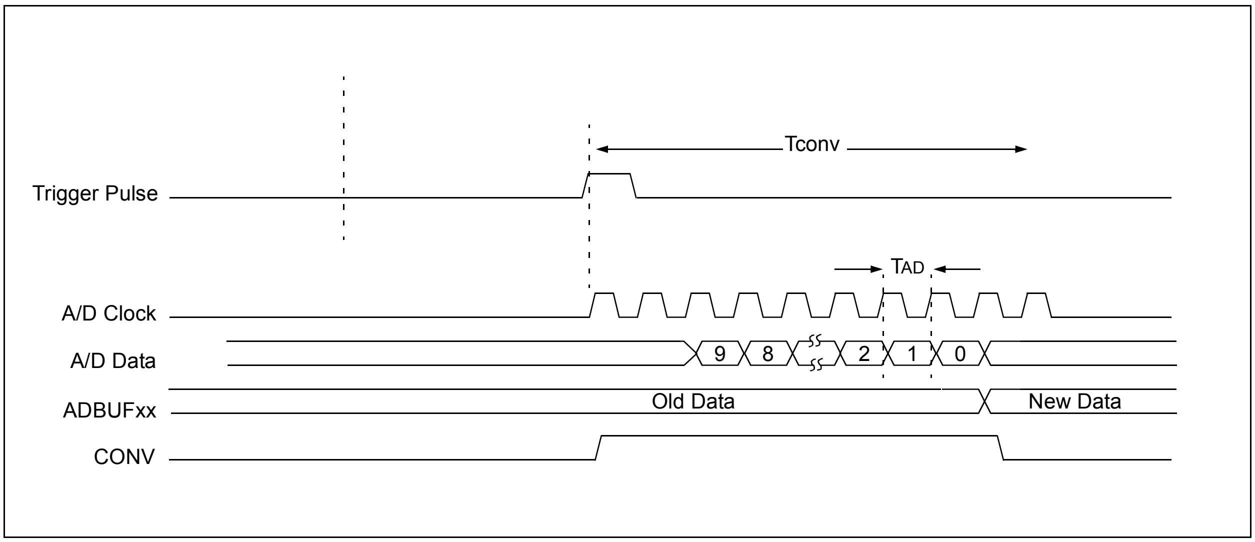


TABLE 24-38: COMPARATOR AC AND DC SPECIFICATIONS

			Standard Operating Conditions (unless otherwise stated) Operating temperature: -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	V_{IOFF}	Input Offset Voltage		±5	±15	mV	
	V_{ICM}	Input Common Mode Voltage Range(1)	0	—	AV_{DD} – 1.5	V	
	V_{GAIN}	Open Loop Gain(1)	90	—	—	db	
	CMRR	Common Mode Rejection Ratio(1)	70	—	—	db	
	T_{RESP}	Large Signal Response		20	30	ns	V+ input step of 100 mv while V- input held at AV_{DD}/2. Delay measured from analog input pin to PWM output pin.

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

TABLE 24-39: DAC DC SPECIFICATIONS

			Standard Operating Conditions (unless otherwise stated) Operating temperature: -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	CV_{RSRC}	External Reference Voltage(1)	0		AV_{DD} – 1.6	V	
	CV_{RES}	Resolution		10		Bits	
		Transfer Function Accuracy					AV_{DD} = 3.3V, DAC_{REF} = (AV_{DD}/2)V
	INL	Integral Nonlinearity Error	—	±1.0	—	LSB	
	DNL	Differential Nonlinearity Error	—	±0.8	—	LSB	
	EOFF	Offset Error	—	±2.0	—	LSB	
	EG	Gain Error	—	±2.0	—	LSB	

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

TABLE 24-40: DAC AC SPECIFICATIONS

			Standard Operating Conditions (unless otherwise stated) Operating temperature: -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	T_{SET}	Settling Time(1)			650	nsec	Measured when range = 1 (high range), and CMREF<9:0> transitions from 0x1FF to 0x300.

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

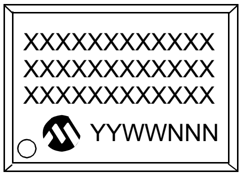
TABLE 24-41: DAC OUTPUT BUFFER DC SPECIFICATIONS

			Standard Operating Conditions (unless otherwise stated) Operating temperature: -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	RLOAD	Resistive Output Load Impedance	3K	—	—	Ω	
	CLOAD	Output Load Capacitance	—	20	35	pF	
	IOUT	Output Current Drive Strength	200	300	400	μA	Sink and source
	VRANGE	Full Output Drive Strength Voltage Range	AVSS + 250 mV	—	AVDD – 900 mV	V	
	VLRANGE	Output Drive Voltage Range at Reduced Current Drive of 50 μA	AVSS + 50 mV	—	AVDD – 500 mV	V	
	IDD	Current Consumed when Module is Enabled, High-Power Mode	—	—	1.3 x IOUT	μA	Module will always consume this current even if no load is connected to the output
	RIN	Input Impedance	10^9	—	—	Ω	
	ROUTON	Output Impedance when Module is Enabled	—	—	10	Ω	Closed loop output resistance
	ROUT-OFF	Output Impedance when Module is Disabled	10^7	—	—	Ω	`buf_enable = 0`

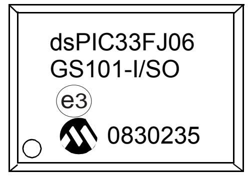
NOTES:

25.0 PACKAGING INFORMATION

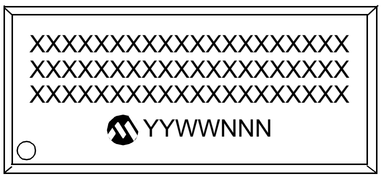
18-Lead SOIC (.300")



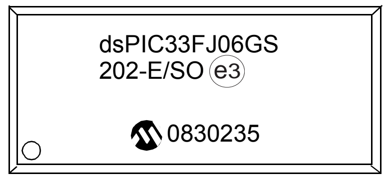
Example



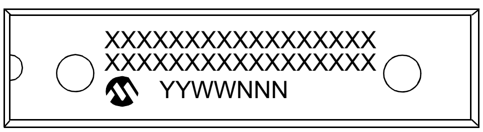
28-Lead SOIC



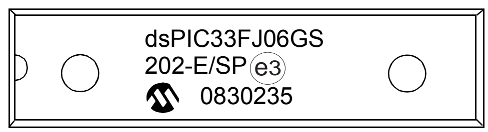
Example



28-Lead SPDIP



Example

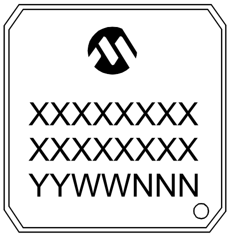


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.

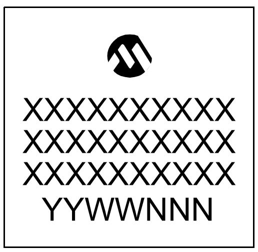
25.1 Package Marking Information (Continued)

28-Lead QFN-S



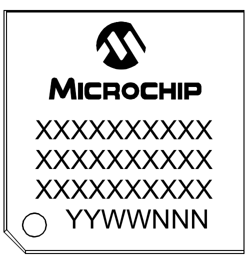
Example

44-Lead QFN

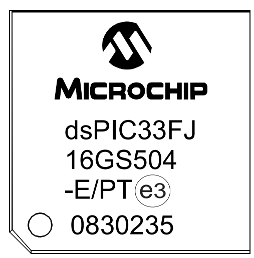


Example

44-Lead TQFP



Example

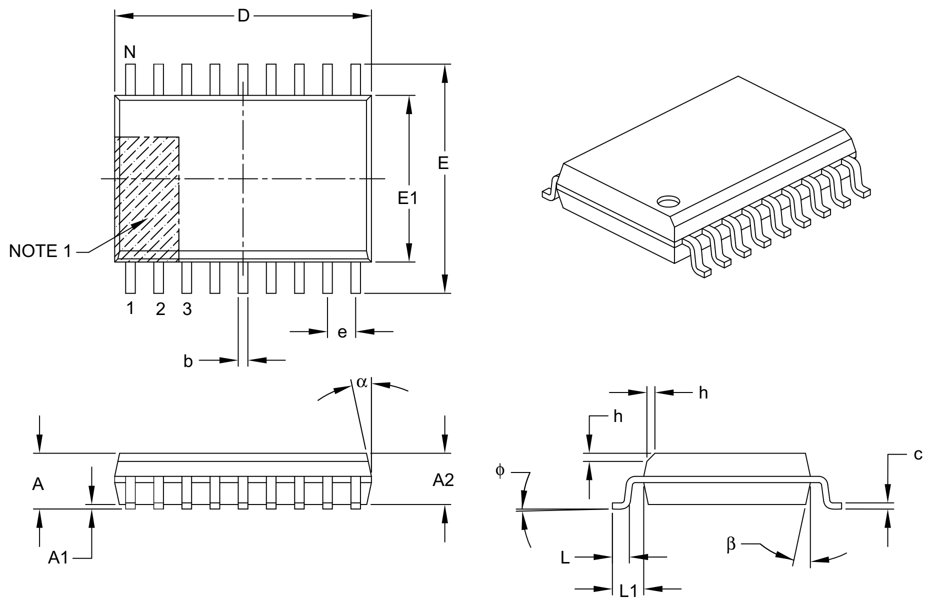


Preliminary

25.2 Package Details

18-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	18		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	11.55 BSC		
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1	1.40 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.20	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

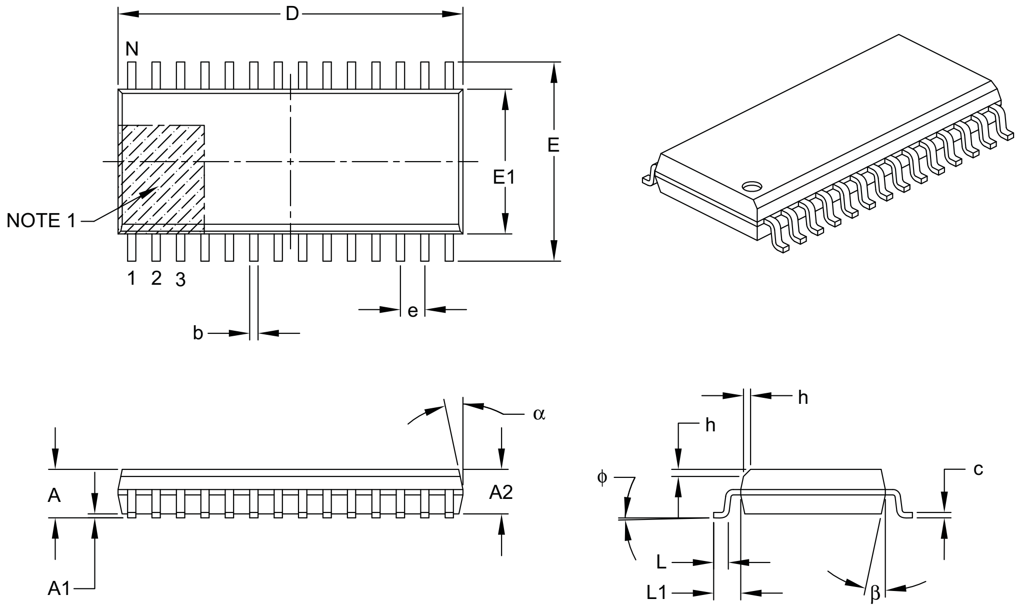
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-051B

28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1	1.40 REF		
Foot Angle Top	φ	0°	–	8°
Lead Thickness	c	0.18	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

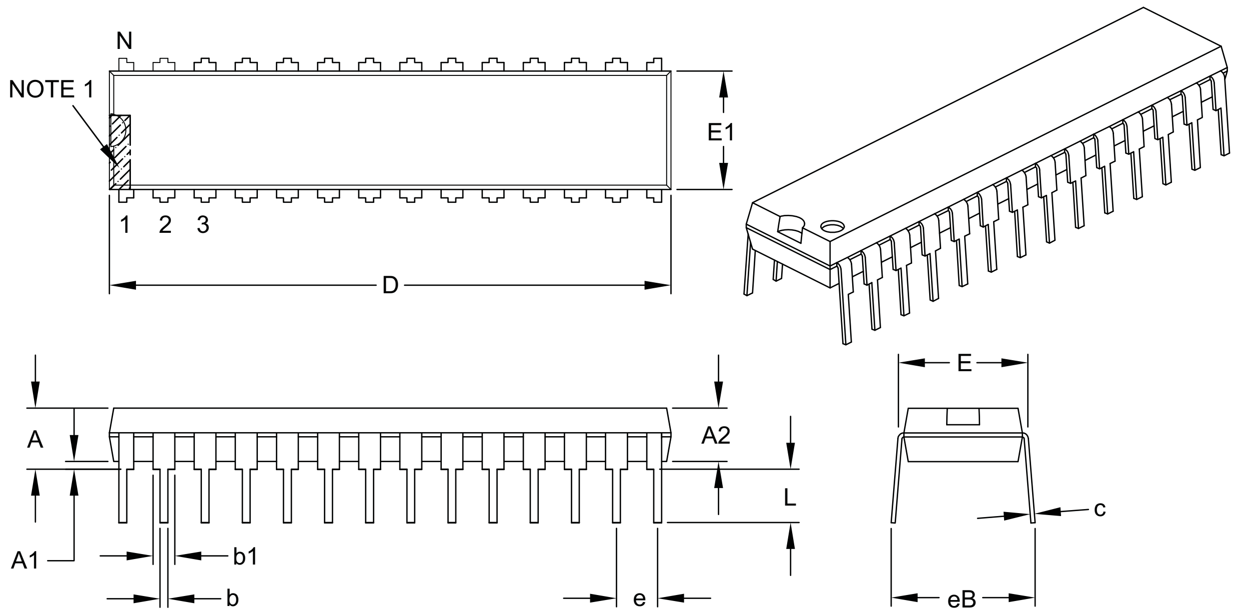
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

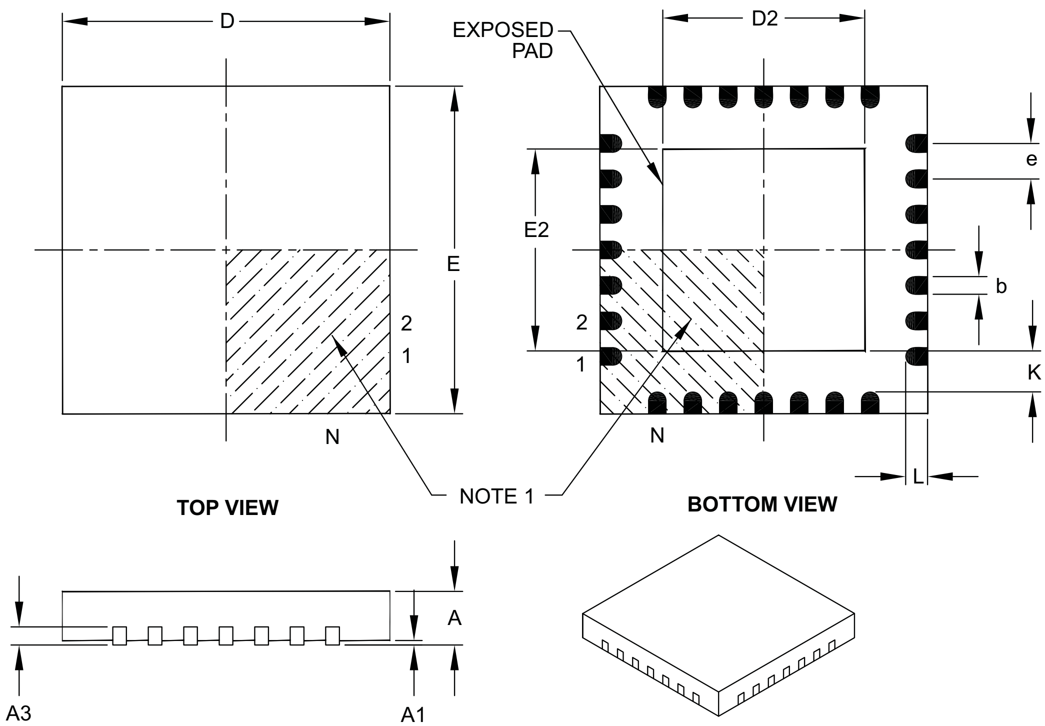
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.70
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.70
Contact Width	b	0.23	0.38	0.43
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

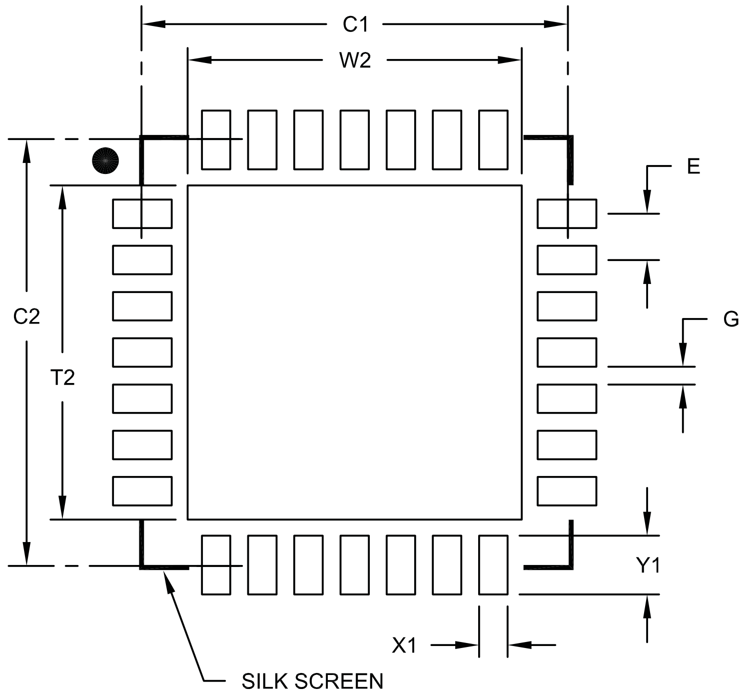
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124B

 Preliminary

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

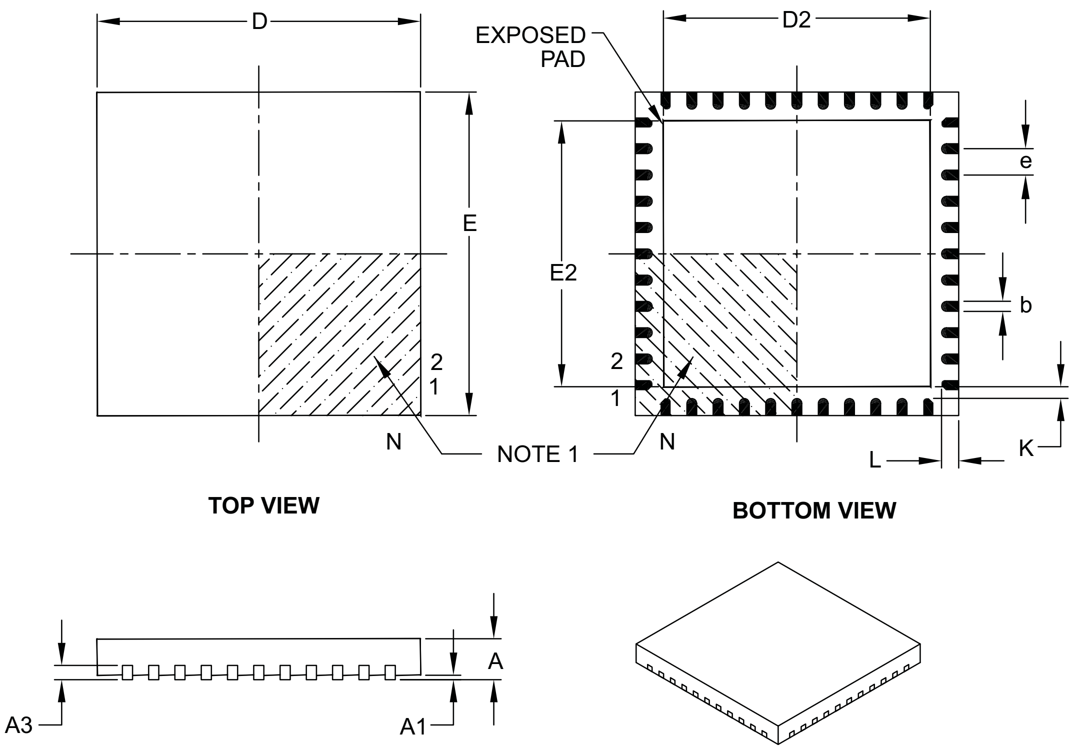
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



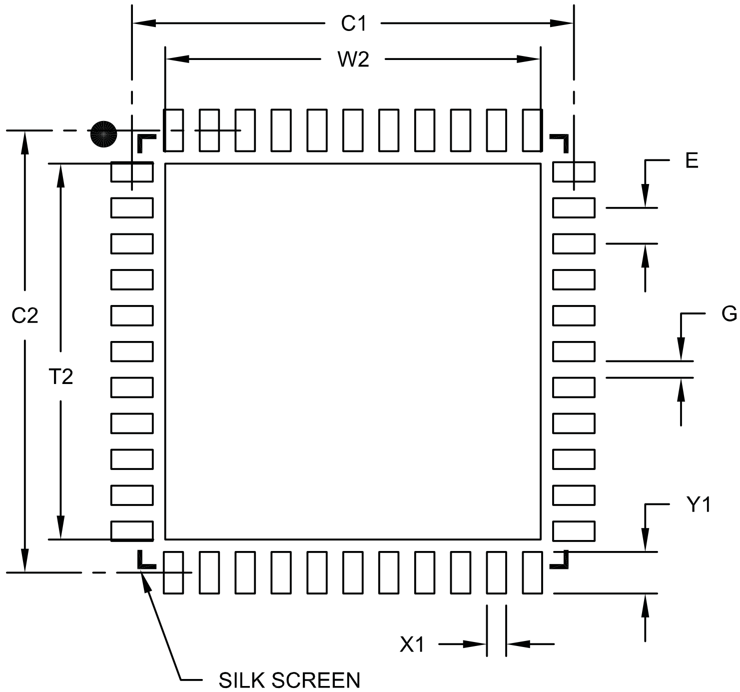
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			6.80
Optional Center Pad Length	T2			6.80
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.80
Distance Between Pads	G	0.25		

Notes:

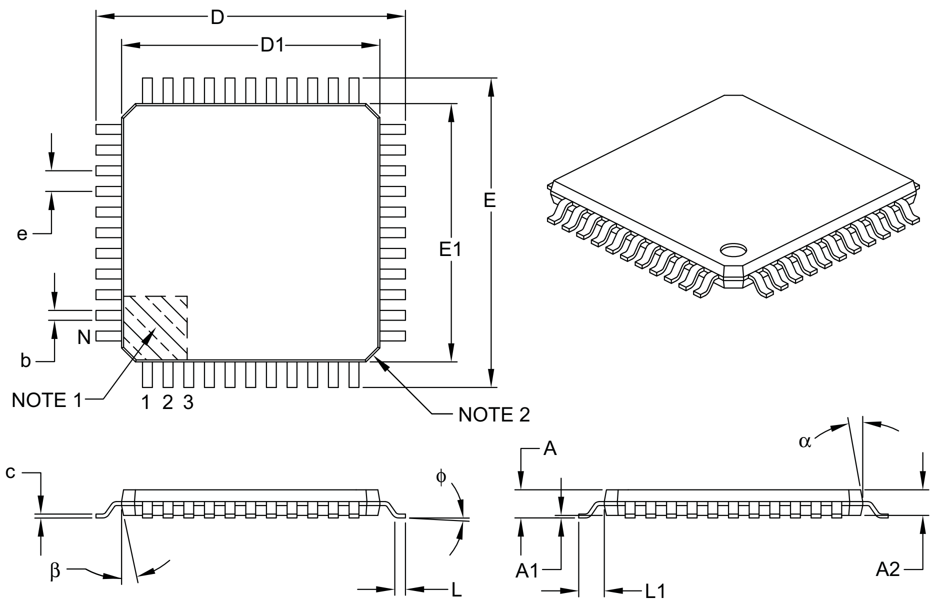
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	44		
Lead Pitch	e	0.80 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

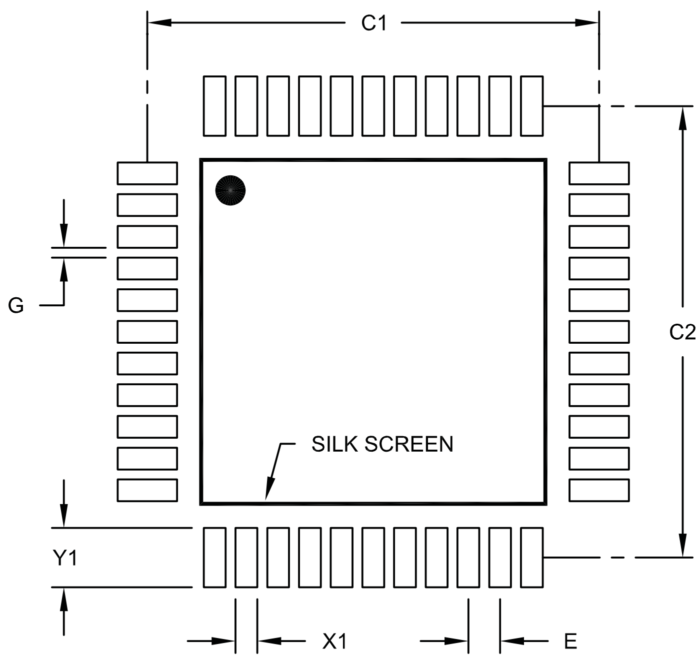
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (January 2008)

This is the initial revision of this document.

Revision B (June 2008)

This revision includes minor typographical and formatting changes throughout the data sheet text. In addition, redundant information was removed that is now available in the respective chapters of the *dsPIC33F Family Reference Manual*, which can be obtained from the Microchip website (www.microchip.com).

The major changes are referenced by their respective section in the following table.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
“High-Performance, 16-Bit Digital Signal Controllers”	Moved location of Note 1 (RP# pin) references (see **“Pin Diagrams”**).
Section 3.0 “Memory Organization”	Updated CPU Core Register map SFR reset value for CORCON (see Table 3-1). Removed Interrupt Controller Register Map SFR IPC29 and updated reset values for IPC0, IPC1, IPC14, IPC16, IPC23, IPC24, IPC27, and IPC28 (see Table 3-5). Removed Interrupt Controller Register Map SFR IPC24 and IPC29 and updated reset values for IPC0, IPC1, IPC2, IPC14, IPC16, IPC23, IPC27, and IPC28 (see Table 3-6). Removed Interrupt Controller Register Map SFR IPC24 and updated reset values for IPC1, IPC2, IPC4, IPC14, IPC16, IPC23, IPC24, IPC27, and IPC28 (see Table 3-7). Updated Interrupt Controller Register Map SFR reset values for IPC1, IPC14, IPC16, IPC23, IPC24, IPC27, and IPC28 (see Table 3-8). Updated Interrupt Controller Register Map SFR reset values for IPC1, IPC14, IPC16, IPC23, IPC24, IPC25, IPC26, IPC27, IPC28, and IPC29 (see Table 3-9). Updated Interrupt Controller Register Map SFR reset values for IPC1, IPC4, IPC14, IPC16, IPC23, IPC24, IPC25, IPC26, IPC27, IPC28, and IPC29 (see Table 3-10). Added SFR definitions for RPOR16 and RPOR17 (see Table 3-34, Table 3-35, and Table 3-36). Updated bit definitions for PORTA, PORTB, and PORTC SFRs (ODCA, ODCB, and ODCC) (see Table 3-37, Table 3-38, Table 3-39, and Table 3-40). Updated bit definitions and reset value for System Control Register map SFR CLKDIV (see Table 3-41). Added device-specific information to title of PMD Register Map (see Table 3-47). Added device-specific PMD Register Maps (see Table 3-46, Table 3-45, and Table 3-43).

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 7.0 "Oscillator Configuration"	Removed the first sentence of the third clock source item (External Clock) in **Section 7.1.1 "System Clock sources"** Updated the default bit values for DOZE and FRCDIV in the Clock Divisor Register (see Register 7-2).
Section 8.0 "Power-Saving Features"	Added the following six registers: • **"PMD1: Peripheral Module Disable Control Register 1"** • **"PMD2: Peripheral Module Disable Control Register 2"** • **"PMD3: Peripheral Module Disable Control Register 3"** • **"PMD4: Peripheral Module Disable Control Register 4"** • **"PMD6: Peripheral Module Disable Control Register 6"** • **"PMD7: Peripheral Module Disable Control Register 7"**
Section 9.0 "I/O Ports"	Added paragraph and Table 9-1 to **Section 9.1.1 "Open-Drain Configuration"**, which provides details on I/O pins and their functionality. Removed 9.1.2 "5V Tolerance". Updated MUX range and removed virtual pin details in Figure 9-2. Updated PWM Input Name descriptions in Table 9-1. Added **Section 9.4.2.3 "Virtual Pins"**. Updated bit values in all Peripheral Pin Select Input Registers (see Register 9-1 through Register 9-14). Updated bit name information for Peripheral Pin Select Output Registers RPOR16 and RPOR17 (see Register 9-30 and Register 9-31). Added the following two registers: • **"RPOR16: Peripheral Pin Select Output Register 16"** • **"RPOR17: Peripheral Pin Select Output Register 17"** Removed the following sections: • 9.4.2 "Available Peripherals" • 9.4.3.2 "Virtual Input Pins" • 9.4.3.4 "Peripheral Mapping" • 9.4.5 "Considerations for Peripheral Pin Selection" (and all subsections)
Section 14.0 "High-Speed PWM"	Added Note 1 (remappable pin reference) to Figure 14-1. Added Note 2 (Duty Cycle resolution) to PWM Master Duty Cycle Register (Register 14-5), PWM Generator Duty Cycle Register (Register 14-7), and PWM Secondary Duty Cycle Register (Register 14-8). Added Note 2 and Note 3 and updated bit information for CLSRC and FLTSRC in the PWM Fault Current-Limit Control Register (Register 14-15).
Section 15.0 "Serial Peripheral Interface (SPI)"	Removed the following sections, which are now available in the related section of the dsPIC33F Family Reference Manual: • 15.1 "Interrupts" • 15.2 "Receive Operations" • 15.3 "Transmit Operations" • 15.4 "SPI Setup" (retained Figure 15-1: SPI Module Block Diagram)

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 16.0 "Inter-Integrated Circuit (I^2C™)"	Removed the following sections, which are now available in the related section of the dsPIC33F Family Reference Manual: • 16.3 "I^2C Interrupts" • 16.4 "Baud Rate Generator" (retained Figure 16-1: I^2C Block Diagram) • 16.5 "I^2C Module Addresses • 16.6 "Slave Address Masking" • 16.7 "IPMI Support" • 16.8 "General Call Address Support" • 16.9 "Automatic Clock Stretch" • 16.10 "Software Controlled Clock Stretching (STREN = `1`)" • 16.11 "Slope Control" • 16.12 "Clock Arbitration" • 16.13 "Multi-Master Communication, Bus Collision, and Bus Arbitration
Section 17.0 "Universal Asynchronous Receiver Transmitter (UART)"	Removed the following sections, which are now available in the related section of the dsPIC33F Family Reference Manual: • 17.1 "UART Baud Rate Generator" • 17.2 "Transmitting in 8-bit Data Mode • 17.3 "Transmitting in 9-bit Data Mode • 17.4 "Break and Sync Transmit Sequence" • 17.5 "Receiving in 8-bit or 9-bit Data Mode" • 17.6 "Flow Control Using $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins" • 17.7 "Infrared Support" Removed IrDA references and Note 1, and updated the bit and bit value descriptions for UTXINV (UxSTA<14>) in the UARTx Status and Control Register (see Register 17-2).
Section 18.0 "High-Speed 10-bit Analog-to-Digital Converter (ADC)"	Updated bit value information for A/D Control Register (see Register 18-1). Updated TRGSRC6 bit value for Timer1 period match in the A/D Convert Pair Control Register 3 (see Register 18-8).

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 23.0 “Electrical Characteristics”	Updated Typ values for Thermal Packaging Characteristics (Table 23-3). Removed Typ value for DC Temperature and Voltage Specifications parameter DC12 (Table 23-4). Updated all Typ values and conditions for DC Characteristics: Operating Current (I_{DD}), updated last sentence in Note 2 (Table 23-5). Updated all Typ values for DC Characteristics: Idle Current (I_{IDLE}) (see Table 23-6). Updated all Typ values for DC Characteristics: Power Down Current (I_{PD}) (see Table 23-7). Updated all Typ values for DC Characteristics: Doze Current (I_{DOZE}) (see Table 23-8). Added Note 4 (reference to new table containing digital-only and analog pin information, as well as Current Sink/Source capabilities) in the I/O Pin Input Specifications (Table 23-9). Updated Max value for BOR electrical characteristics parameter BO10 (see Table 23-11). Swapped Min and Typ values for Program Memory parameters D136 and D137 (Table 23-12). Updated Typ values for Internal RC Accuracy parameter F20 and added Extended temperature range to table heading (see Table 23-19). Removed all values for Reset, Watchdog Timer, Oscillator Start-up Timer, and Power-up Timer parameter SY20 and updated conditions, which now refers to **Section 20.4 “Watchdog Timer (WDT)”** and LPRC parameter F21 (see Table 23-22). Added specifications to High-Speed PWM Module Timing Requirements for Tap Delay (Table 23-29). Updated Min and Max values for 10-bit High-Speed A/D Module parameters AD01 and AD11 (see Table 23-36). Updated Max value and unit of measure for DAC AC Specification (see Table 23-40).

Revision C and D (March 2009)

This revision includes minor typographical and formatting changes throughout the data sheet text.

Global changes include:

- Changed all instances of OSCI to OSC1 and OSCO to OSC2
- Changed all instances of PGCx/EMUCx and PGDx/EMUDx (where x = 1, 2, or 3) to PGECx and PGEDx
- Changed all instances of VDDCORE and VDDCORE/VCAP to VCAP/VDDCORE

Other major changes are referenced by their respective section in the following table.

TABLE A-2: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-Bit Digital Signal Controllers"	Added **"Application Examples"** to list of features Updated all pin diagrams to denote the pin voltage tolerance (see **"Pin Diagrams"**). Added Note 2 to the 28-Pin QFN-S and 44-Pin QFN pin diagrams, which references pin connections to VSS.
Section 1.0 "Device Overview"	Added ACMP1-ACMP4 pin names and Peripheral Pin Select capability column to Pinout I/O Descriptions (see Table 1-1).
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers"	Added new section to the data sheet that provides guidelines on getting started with 16-bit Digital Signal Controllers.
Section 3.0 "CPU"	Updated CPU Core Block Diagram with a connection from the DSP Engine to the Y Data Bus (see Figure 3-1). Vertically extended the X and Y Data Bus lines in the DSP Engine Block Diagram (see Figure 3-3).
Section 4.0 "Memory Organization"	Updated Reset value for ADCON in Table 4-25. Removed reference to dsPIC33FJ06GS102 devices in the PMD Register Map and updated bit definitions for PMD1 and PMD6, and removed PMD7 (see Table 4-43). Added a new PMD Register Map, which references dsPIC33FJ06GS102 devices (see Table 4-44). Updated RAM stack address and SPLIM values in the third paragraph of **Section 4.2.6 "Software Stack"** Removed **Section 4.2.7 "Data Ram Protection Feature"**.
Section 5.0 "Flash Program Memory"	Updated **Section 5.3 "Programming Operations"** with programming time formula.

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 8.0 “Oscillator Configuration”	Added Note 2 to the Oscillator System Diagram (see Figure 8-1). Added a paragraph regarding FRC accuracy at the end of **Section 8.1.1 “System Clock Sources”**. Added Note 1 and Note 2 to the OSCON register (see Register). Added Note 1 to the OSCTUN register (see Register 8-4). Added Note 3 to **Section 8.4.2 “Oscillator Switching Sequence”**.
Section 10.0 “I/O Ports”	Removed Table 9-1 and added reference to pin diagrams for I/O pin availability and functionality. Added paragraph on ADPCFG register default values to **Section 10.2 “Configuring Analog Port Pins”**. Added Note box regarding PPS functionality with input mapping to **Section 10.4.2.1 “Input Mapping”**.
Section 15.0 “High-Speed PWM”	Updated Note 2 in the PTCON register (see Register 15-1). Added Note 4 to the PWMCONx register (see Register 15-6). Updated Notes for the PHASEx and SPHASEx registers (see Register 15-9 and Register 15-10, respectively).
Section 16.0 “Serial Peripheral Interface (SPI)”	Added Note 2 and Note 3 to the SPIxCON1 register (see Register 16-2).
Section 18.0 “Universal Asynchronous Receiver Transmitter (UART)”	Updated the Notes in the UxMode register (see Register 18-1). Updated the UTXINV bit settings in the UxSTA register and added Note 1 (see Register 18-2).
Section 19.0 “High-Speed 10-bit Analog-to-Digital Converter (ADC)”	Updated the SLOWCLK and ADCS<2:0> bit settings and updated Note 1in the ADCON register (see Register 19-1). Removed all notes in the ADPCFG register and replaced them with a single note (see Register 19-4). Updated the SWTRGx bit settings in the ADCPCx registers (see Register 19-5, Register 19-6, Register 19-7, and Register 19-8).

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 24.0 "Electrical Characteristics"	Updated Typical values for Thermal Packaging Characteristics (see Table 24-3). Updated Min and Max values for parameter DC12 (RAM Data Retention Voltage) and added Note 4 (see Table 24-4). Updated Characteristics for I/O Pin Input Specifications (see Table 24-9). Added ISOURCE to I/O Pin Output Specifications (see Table 24-10). Updated Program Memory values for parameters 136, 137, and 138 (renamed to 136a, 137a, and 138a), added parameters 136b, 137b, and 138b, and added Note 2 (see Table 24-12). Added parameter OS42 (GM) to the External Clock Timing Requirements (see Table 24-16). Updated Conditions for symbol TPDLY (Tap Delay) and added symbol ACLK (PWM Input Clock) to the High-Speed PWM Module Timing Requirements (see Table 24-29). Updated parameters AD01 and AD02 in the 10-bit High-Speed A/D Module Specifications (see Table 24-36). Updated parameters AD50b, AD55b, and AD56b, and removed parameters AD57b and AD60b from the 10-bit High-Speed A/D Module Timing Requirements (see Table 24-37).

NOTES:

INDEX

Numerics

H

I

J

M

O

P

R

 Preliminary

S

T

U

V

W

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dsPIC 33 FJ 06 GS1 02 T E / SP - XXX

- **Microchip Trademark** — dsPIC
- **Architecture** — 33
- **Flash Memory Family** — FJ
- **Program Memory Size (KB)** — 06
- **Product Group** — GS1
- **Pin Count** — 02
- **Tape and Reel Flag (if applicable)** — T
- **Temperature Range** — E
- **Package** — SP
- **Pattern** — XXX

Architecture:	33	=	16-bit Digital Signal Controller
Flash Memory Family:	FJ	=	Flash program memory, 3.3V
Product Group:	GS1	=	Switch Mode Power Supply (SMPS) family
	GS2	=	Switch Mode Power Supply (SMPS) family
	GS4	=	Switch Mode Power Supply (SMPS) family
	GS5	=	Switch Mode Power Supply (SMPS) family
Pin Count:	01	=	18-pin
	02	=	28-pin
	04	=	44-pin
Temperature Range:	I	=	-40°C to+85°C (Industrial)
	E	=	-40°C to+125°C (Extended)
Package:	SO	=	Plastic Small Outline - Wide - 7.50 mm body (SOIC)
	SP	=	Skinny Plastic Dual In-Line - 300 mil body (SPDIP)
	ML	=	Plastic Quad Flat, No Lead Package - 8x8 mm body (QFN)
	MM	=	Plastic Quad Flat, No Lead Package - 6x6x0.9 mm body (QFN-S)
	PT	=	Plastic Thin Quad Flatpack - 10x10x1 mm body (TQFP)

Examples:

a) dsPIC33FJ06GS102-E/SP:
SMPS dsPIC33, 6-Kbyte program memory, 28-pin, Extended temp.,SPDIP package.

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