BATRON

Specification

BT45231

BTHQ240064AVB1-EMN-06-LEDWHITE-COG

Doc. No.: COG-BT240064-34

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A	2010.12.02	First Release.	ZHU YANG NA	JIN YOU PING

CONTENTS

Specification
of
LCD Module Type
Model No.: COG-BT240064-34

1. General Description

- 240 x 64 Dots STN , Negative ,blue , Transmissive Dot Matrix LCD Module.
- Viewing angle: 6 o'clock.
- Driving scheme: 1/65 duty, 1/7 bias.
- 'SITRONIX' ST7565P (COG) 2PCS Dot Matrix LCD Drivers or equivalent.
- Logic voltage: 3V.
- FPC connection.
- White LED05 backlight.
- "RoHS" compliance.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	120.0(W) x 194.82(H) x 5.5(D) (Included FPC) (Excluded housing & cable of backlight)	mm
Viewing area	102.4(W) x 30.22(H)	mm
Active area	98.38(W) x 26.22(H)	mm
Display format	240 x 64 Dots	dots
Dot size	0.39(W) x 0.39(H)	mm
Dot spacing	0.02(W) x 0.02(H)	mm
Dot pitch	0.41(W) x 0.41(H)	mm
Weight	Approx: 42	gram

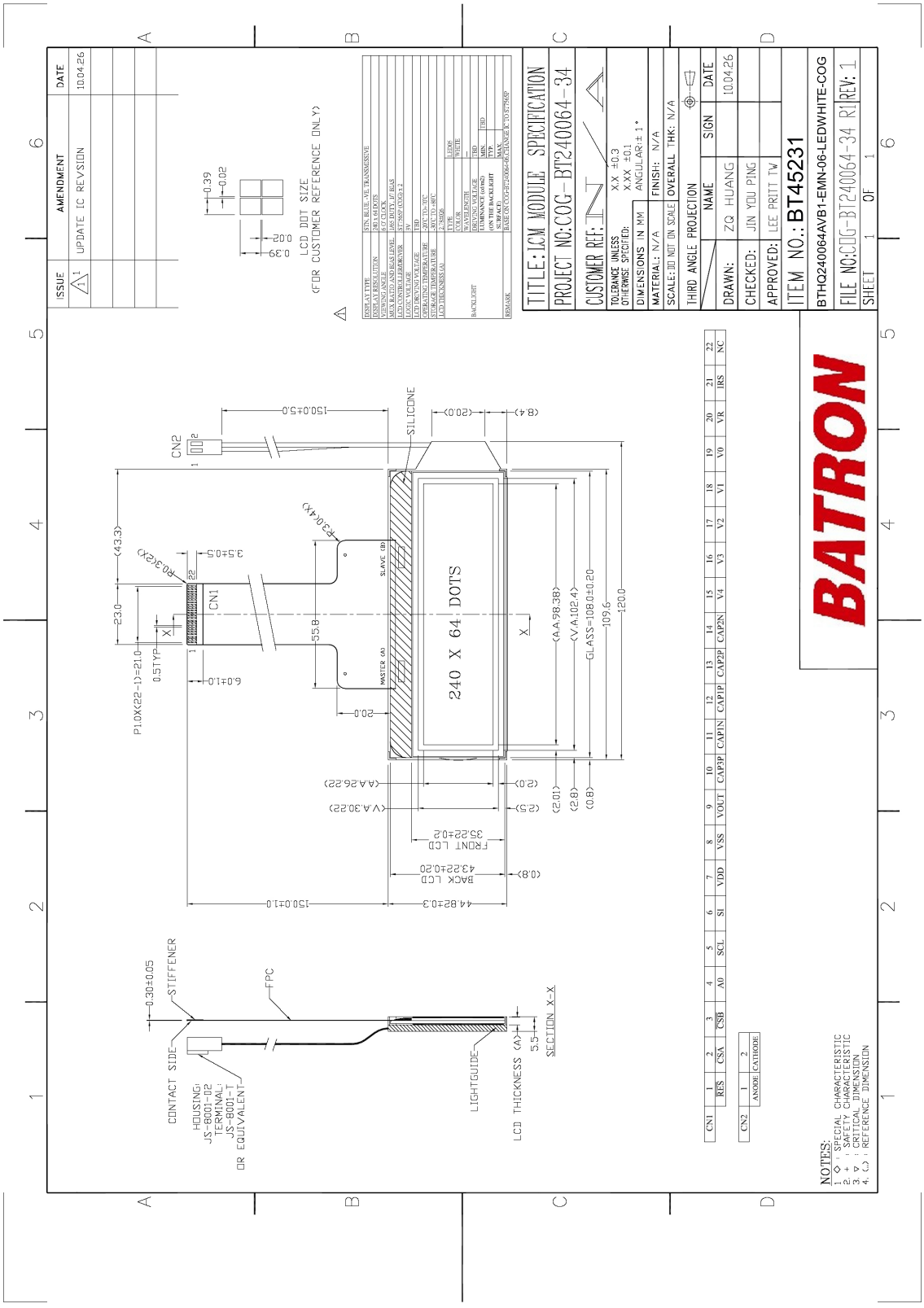


Figure 1: Module Specification

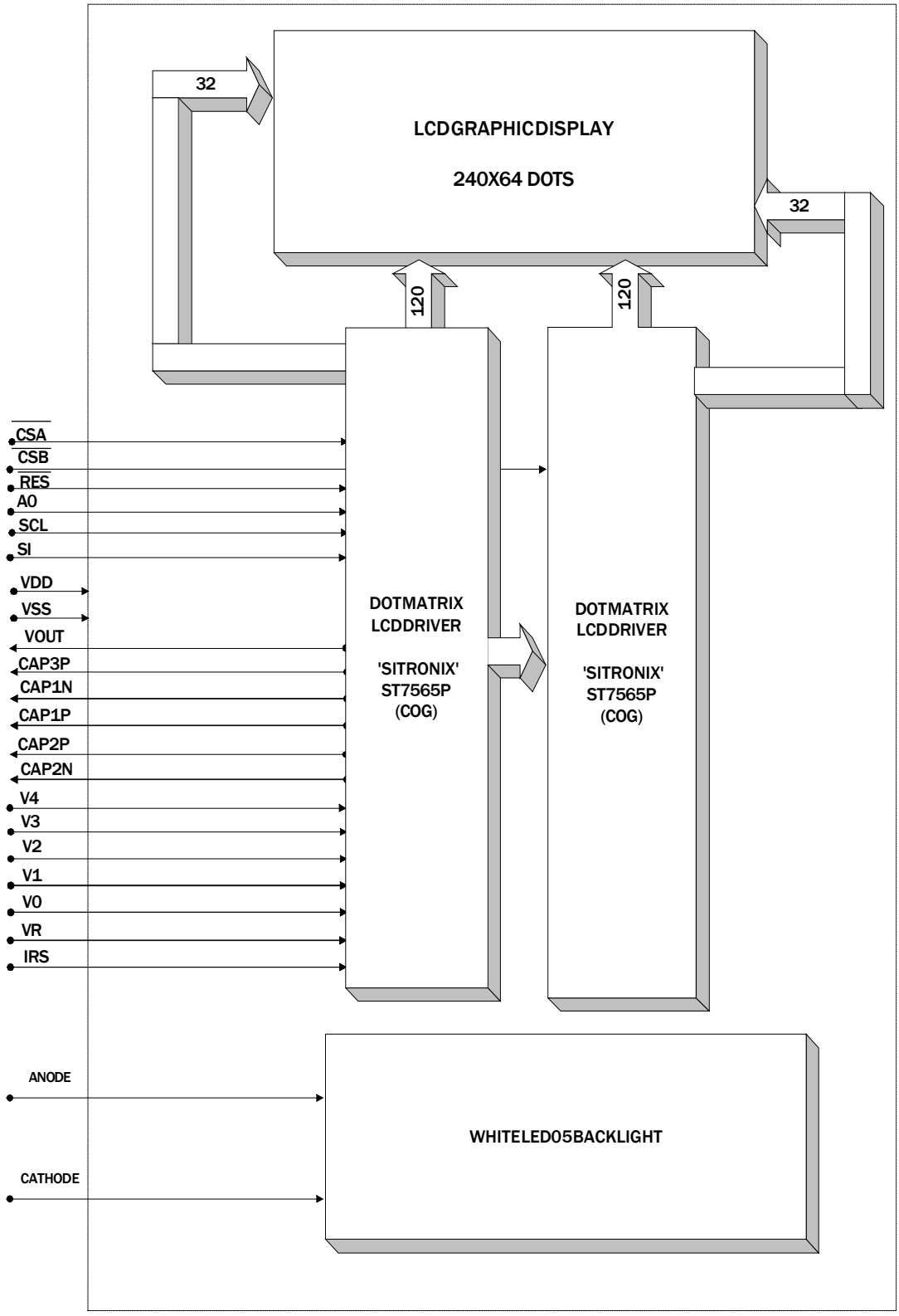


Figure 2: Block Diagram

3. Interface signals

Table 2(a): Pin Assignment of CN1

Pin No.	Symbol	Description
1	$\overline{RES}$	When /RES is set to "L", the register settings are initialized (cleared). The reset operation is performed by the /RES signal level.
2	$\overline{CSA}$	This is the chip select signal for Master driver. When$\overline{CSA}$ = LOW then the chip select becomes active, and data/command I/O is enabled.
3	$\overline{CSB}$	This is the chip select signal for Slave driver. When$\overline{CSB}$ = LOW then the chip select becomes active, and data/command I/O is enabled.
4	A0	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.
5	SCL	Serial clock input terminal.
6	SI	Serial data input terminal.
7	VDD	Power supply.
8	VSS	Ground.
9	VOUT	DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD.
10	CAP3P	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
11	CAP1N	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.
12	CAP1P	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
13	CAP2P	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
14	CAP2N	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.
15	V4	This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on Vss, and must maintain the relative magnitudes shown below. V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧Vss When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD biasset command. 1/65 DUTY: V1 8/9*V0,6/7*V0; V2 7/9*V0,5/7*V0; V3 2/9*V0,2/7*V0; V4 1/9*V0,1/7*V0 1/49 DUTY: V1 7/8*V0,5/6*V0; V2 6/8*V0,4/6*V0; V3 2/8*V0,2/6*V0; V4 1/8*V0,1/6*V0 1/33 DUTY: V1 5/6*V0,4/5*V0; V2 4/6*V0,3/5*V0; V3 2/6*V0,2/5*V0; V4 1/6*V0,1/5*V0 1/55 DUTY: V1 7/8*V0,5/6*V0; V2 6/8*V0,4/6*V0; V3 2/8*V0,2/6*V0; V4 1/8*V0,1/6*V0 1/53 DUTY: V1 7/8*V0,5/6*V0; V2 6/8*V0,4/6*V0; V3 2/8*V0,2/6*V0; V4 1/8*V0,1/6*V0
16	V3	
17	V2	
18	V1	
19	V0	

Table 2(b): Pin Assignment of CN1

Pin No.	Symbol	Description
20	VR	Output voltage regulator terminal. Provides the voltage between VSS and V0 through a resistive voltage divider. IRS = “L” : the V0 voltage regulator internal resistors are not used. IRS = “H” : the V0 voltage regulator internal resistors are used.
21	IRS	This terminal selects the resistors for the V0 voltage level adjustment. IRS = “H”: Use the internal resistors IRS = “L”: Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.
22	NC	No connection.

Table 2(c): Pin Assignment of CN2

Pin No.	Symbol	Description
1	ANODE	Anode of backlight.
2	CATHODE	Cathode of backlight.

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings- for IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD	-0.3	+3.6	V
Power Supply voltage (VSS2)(VDD standard)	VDD2	-0.3	+3.6	V
Power Supply voltage (V5,VOUT)(VDD standard)	V0, VOUT	-0.3	+14.5	V
Power Supply voltage (V1,V2,V3,V4)(VDD standard)	V1,V2,V3, V4	-0.3	V0+0.3	V
Input voltage	Vin	-0.3	VDD+0.3	V

Note: 1. The VDD2, V0 to V4 and VOUT are relative to the VSS = 0V reference.

2. Insure that the voltage levels of V1, V2, V3, and V4 are always such that VOUT ≧ V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4.

3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

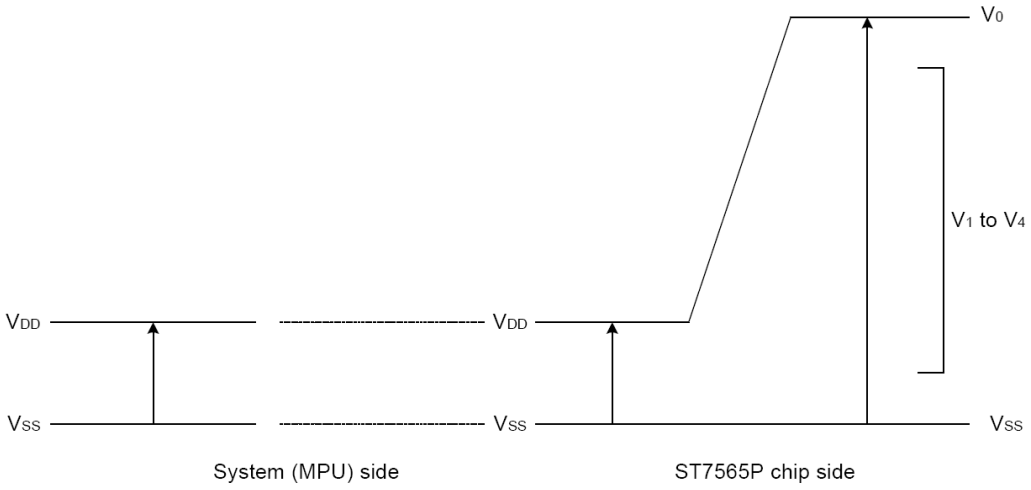


Figure 4

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg) (Note1)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity (Note1)	90% max. RH for Ta ≤ 40°C <50%RH for 40°C <Ta<= Maximum operating temperature				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

Note1: Product cannot sustain at extreme storage conditions for a long time.

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = +25 °C, VDD = +3.0±5%, VSS = 0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		2.85	3.0	3.15	V
Supply voltage (LCD) (built-in)	VLCD =V0- VSS	Ta = -20°C, VDD = +3.0V, Note 1	-	8.3	-	V
		Ta = 25 °C, VDD = +3.0V, Note 1	7.8	8.0	8.2	V
		Ta = +70 °C, VDD = +3.0V, Note 1	-	7.7	-	V
Low-level input signal voltage	V_{ILC}	Note 2	VSS	-	0.2xVDD	V
High-level input signal voltage	V_{IHC}	Note 2	0.8xVDD	-	VDD	V
Supply Current (Logic & LCD)	IDD	VDD = +3.0V,Note 1, Character mode	-	0.5	0.8	mA
		VDD = +3.0V,Note 1, Checker board mode	-	0.9	1.4	mA
Supply current of white LED05 backlight	If	Forward current =30 mA	3.8	4.0	4.2	V
Luminance (on the backlight surface) of backlight		Number of dies =1x2=2	-	360	-	cd/m^2

5.2 Timing Specifications

Reset Timing

At Ta = -20°C to +70 °C, VDD = +3.0V±5%, VSS = 0V.

Table 6

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time	/RES	t_R		—	—	2.0	µs
Reset "L" pulse width		t_{RW}		2.0	—	—	µs

Note: All timing is specified with 20% and 80% of VDD as the standard.

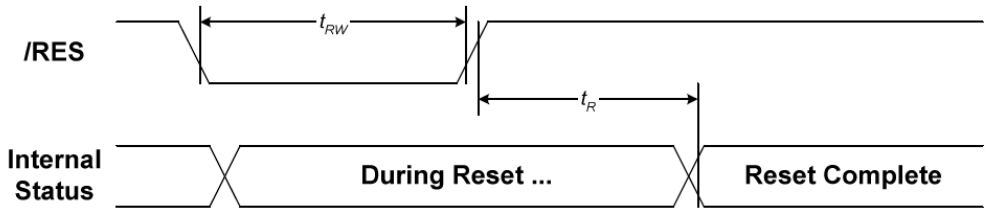


Figure 5: Reset Timing

The serial interface

At Ta = -20°C to +70 °C, VDD = +3.0V±5%, VSS = 0V.

Table 7

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		100	—	ns
SCL "H" pulse width		t_{SHW}		50	—	
SCL "L" pulse width		t_{SLW}		50	—	
Address setup time	A0	t_{SAS}		30	—	
Address hold time		t_{SAH}		20	—	
Data setup time	SI	t_{SDS}		30	—	
Data hold time		t_{SDH}		20	—	
CS-SCL time	CS	t_{CSS}		30	—	
CS-SCL time		t_{CSH}		60	—	

Note 1: The input signal rise and fall (tr, tf) are specified at 15ns or less.

Note 2: All timing is specified using 20% and 80% of VDD as the standard.

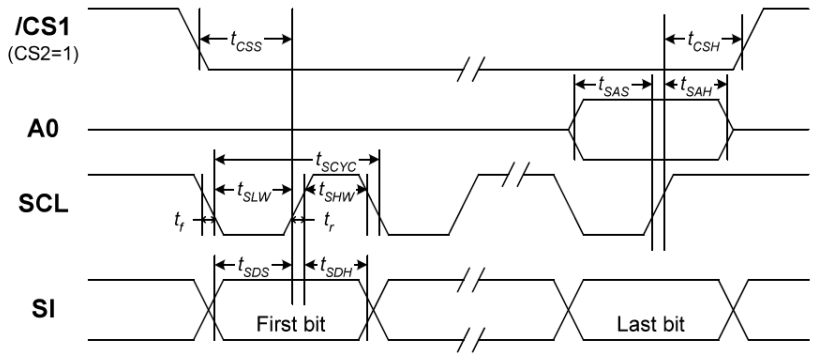


Figure 6: The timing diagram of serial interface

5.3 Command Table

Table 8

Command	Command Code										Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0 0	1 1	0 0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) Vo voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0 Electronic volume value	0	0	0	0	1	Set the Vo output voltage electronic volume register
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

5.3.1 Initial code setting (for reference only)

Table 9

Description	Setting data
SET SOFTEWARE RESET	0XE2
SET DISPLAY ON	0XAF
SET BAIS	0XA3
SET ADC	0XA1
SET SHL	0XC0
SET START LINE ADDRESS	0X40
SET PAGE ADDRESS	0XB0
SET CLUMN ADDRESS HIGH	0X10
SET CLUMN ADDRESS LOWER	0X00
SET DISPLAY MODE NORMAL	0XA6
INTERNAL RESISTOR RATIO	0X24
SET CONTRAST ON	0X81
SET CONTRAST	0X28
BOOSTER RATIO SET	0XF8
SELECT BOOSTER RATIO	0X00
SET POWERR ON	0X2F

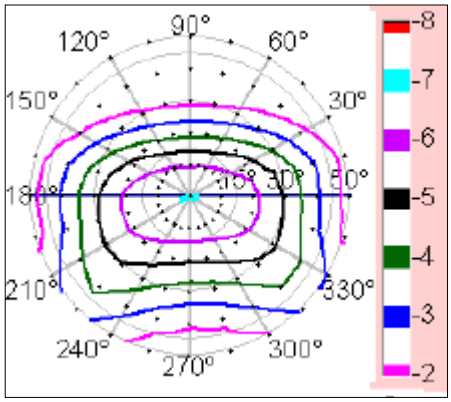
7. Electro-Optical Characteristics

Table 10

Item	Symbol	Temp. °C	Value			Unit	Condition	
			Min.	Typ.	Max.			
Driving voltage	Vop	+25	-	8.12	-	V	Vop= optimum voltage	
Response time	Ton	+25	-	148	200	msec	Vop= Optimum voltage θ = 0°, ϕ = 0°	
	Toff		-	116	160			
Optimum viewing area Cr ≥ TBD	θ1(6 o'clock)	+25	25	33	-	DEG	ϕ = 0°	Vop= Optimum voltage (Remark 1)
	θ2(12 o'clock)		20	25	-			
	ϕ1(3 o'clock)		35	40	-		θ = 0°	
	ϕ2(9 o'clock)		35	40	-			
Contrast ratio	Cr	+25	-	7	-	DEG	Vop = Optimum voltage θ = 0°, ϕ = 0°	
Transmittance		+25	-	28%	-	-	Vop = Optimum voltage	

Remark 1: Due to hardware limitation, the maximum measurable angle is 70 ^{O}.

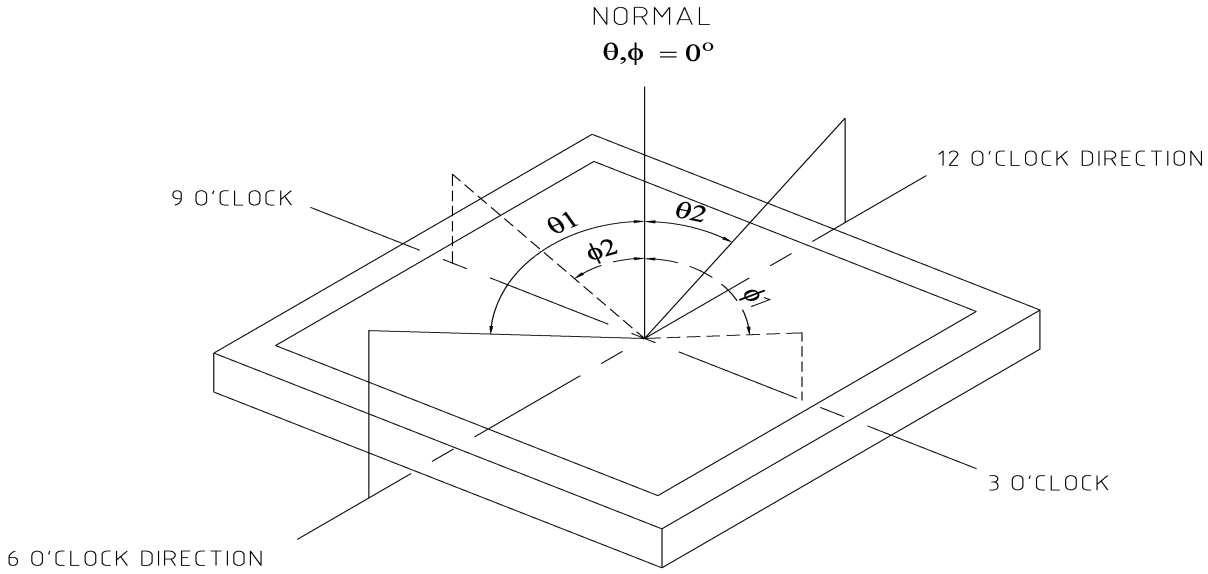
ISO plot:



AS +25°C

7.1 **Optical** Characteristics Definition

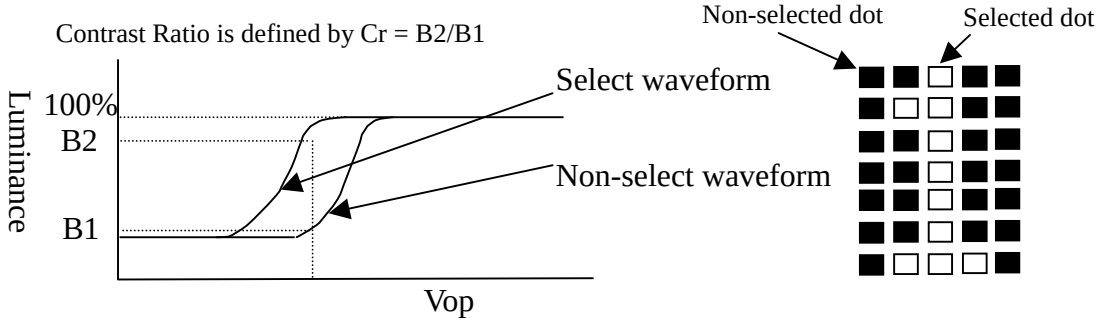
a.) Viewing Angle



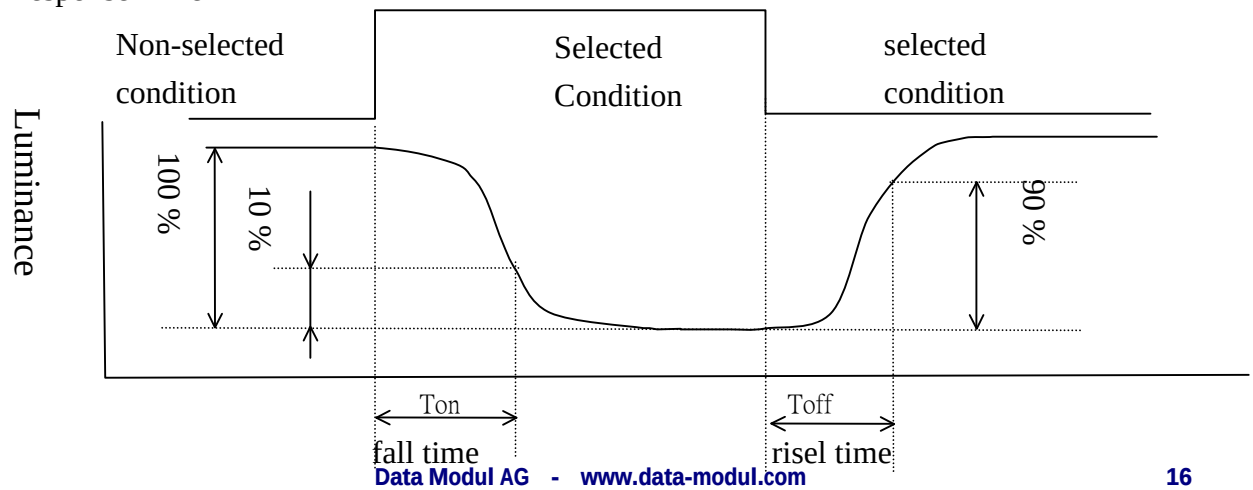
b.) Contrast Ratio

B1 = segments luminance in case of non-selected waveform

B2 = segments luminance in case of selected waveform



c.) Response Time



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