LD6806 series

Ultra low-dropout regulator, low noise, 200 mA

Rev. 2 — 24 August 2011 Product data sheet

1. Product profile

1.1 General description

The LD6806 series is a small size Low-DropOut regulator (LDO) family with a maximum voltage drop of 60 mV at 200 mA current rating.

The device is available in two different packages, one 0.4 mm pitch CSP and one leadless plastic package SOT886.

The operating voltage ranges from 2.3 V to 5.5 V and the output voltage ranges from 1.2 V to 3.6 V.

LD6806xxxH devices show a high-ohmic state at the output pin. All devices use the same regulator design and are manufactured in monolithic silicon technology.

These features make the LD6806 series ideal for use in applications requiring component miniaturization, such as mobile phone handsets, cordless telephones and personal digital devices.

1.2 Features and benefits

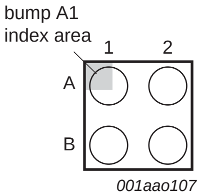
- Pb-free, RoHS compliant and free of Halogen and Antimony (dark green compliant)
- Input voltage range 2.3 V to 5.5 V
- Output voltage range 1.2 V to 3.6 V
- $V_{do} \leq$ 60 mV at 200 mA output rating
- Low quiescent current in shut down mode ($\leq$ 1.0 μA)
- 30 μV RMS output noise voltage (typical value) at 10 Hz to 100 kHz
- Turn-on time just 200 μs
- 55 dB Power Supply Rejection Ratio (PSRR) at 1 kHz
- LD6806xxxH: high-ohmic (3-state) output state when disabled
- Integrated ESD protection of 10 kV Human Body Model
- WLCSP with 0.4 mm pitch and package size of 0.76 mm × 0.76 mm × 0.47 mm
- SOT886 leadless package 1.0 mm × 1.45 mm × 0.5 mm

1.3 Applications

- Analog and digital interfaces requiring lower than standard supply voltage in mobile appliances such as mobile phones, media players etc.

2. Pinning information

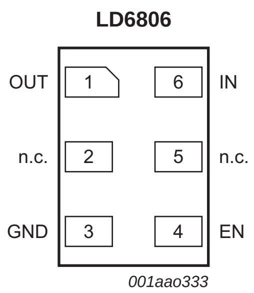
2.1 Pinning



transparent top view,
solder balls facing down

WLCSP4 package

Fig 1. Pin configuration for LD6806CX4/xxx



Transparent top view

SOT886 package

Fig 2. Pin configuration for LD6806F/xxx

2.2 Pin description

Table 1. Pin description LD6806CX4/xxx

Symbol	Pin	Description
GND	A1	supply ground
EN	A2	device enable input; active HIGH
OUT	B1	regulator output voltage
IN	B2	supply voltage input

Table 2. Pin description LD6806F/xxx

Symbol	Pin	Description
OUT	1	regulator output voltage
n.c.	2	not connected
GND	3	supply ground
EN	4	device enable input; active HIGH
n.c.	5	not connected
IN	6	supply voltage input

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
LD6806CX4/xxH	WLCSP4	wafer level chip-size package; 4 bumps (2 × 2)[1]	-
LD6806F/xxH	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886

[1] Size 0.76 mm × 0.76 mm.

3.1 Ordering options

Table 4. Type number and nominal output voltage

Type number	Nominal output voltage	Type number	Nominal output voltage
LD6806[CX4, F]/12H	1.2 V	LD6806[CX4, F]/23H	2.3 V
LD6806[CX4, F]/13H	1.3 V	LD6806[CX4, F]/25H	2.5 V
LD6806[CX4, F]/14H	1.4 V	LD6806[CX4, F]/28H	2.8 V
LD6806[CX4, F]/16H	1.6 V	LD6806[CX4, F]/29H	2.9 V
LD6806[CX4, F]/18H	1.8 V	LD6806[CX4, F]/30H	3.0 V
LD6806[CX4, F]/20H	2.0 V	LD6806[CX4, F]/33H	3.3 V
LD6806[CX4, F]/22H	2.2 V	LD6806[CX4, F]/36H	3.6 V

Further information on output voltage is available on request; see Section 21 "Contact information".

4. Block diagram

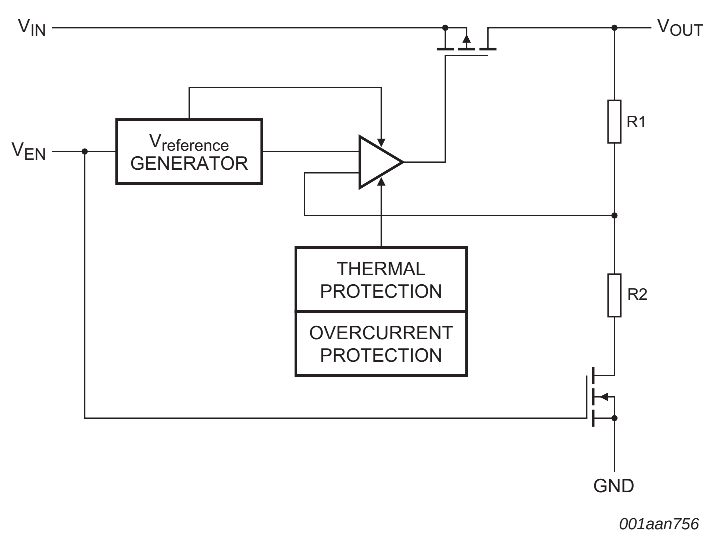


Fig 3. Block diagram of LD6806x/xxH

5. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{IN}	voltage on pin IN	4 ms transient		–0.5	+6.0	V
P_{tot}	total power dissipation	LD6806CX4/xxx	[1]	-	800	mW
		LD6806F/xxx	[1]	-	450	mW
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–40	+125	°C
T_{amb}	ambient temperature			–40	+85	°C
V_{ESD}	electrostatic discharge voltage	human body model level 6	[2]		±10	kV
		machine model class 3	[3]	-	±400	V

[1] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed in conjunction with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a two layer PCB.

[2] According to IEC 61340-3-1.

[3] According to JESD22-A115C.

6. Recommended operating conditions

Table 6. Operating conditions
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
T_{amb}	ambient temperature			–40	+85	°C
T_j	junction temperature			-	+125	°C
Pin IN						
V_{IN}	voltage on pin IN			2.3	5.5	V
Pin EN						
V_{EN}	voltage on pin EN			0	V_{IN}	V
Pin OUT						
$C_{L(ext)}$	external load capacitance		[1]	1.0	-	µF

[1] See Section 10.1 “Output capacitor values”.

7. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	LD6806CX4/xxx	[1][2]	130	K/W
		LD6806F/xxx	[1][2]	220	K/W

[1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area directly below the LDO. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Avoid the use of solder-stop varnish under the chip.

[2] Use the measurement data given for a rough estimation of the $R_{th(j-a)}$ in your application. The actual $R_{th(j-a)}$ value may vary in applications using different layer stacks and layouts.

8. Characteristics

Table 8. Electrical characteristics

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔV_O	output voltage variation	V_{OUT} < 1.8 V; I_{OUT} = 1 mA					
		T_{amb} = +25 °C		−3	-	+3	%
		−30 °C ≤ T_{amb} ≤ +85 °C		−4	-	+4	%
		V_{OUT} ≥ 1.8 V; I_{OUT} = 1 mA					
		T_{amb} = +25 °C		−2	-	+2	%
		−30 °C ≤ T_{amb} ≤ +85 °C		−3	-	+3	%
Line regulation error							
$\Delta V_O/(V_O x \Delta V_I)$	relative output voltage variation with input voltage	V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V		−0.1	-	+0.1	%/V
Load regulation error							
$\Delta V_O/(V_O x \Delta I_O)$	relative output voltage variation with output current	1 mA ≤ I_{OUT} ≤ 200 mA			0.0025	0.01	%/mA
V_{do}	dropout voltage	I_{OUT} = 200 mA; V_{IN} < $V_{O(nom)}$	[1]	-	60	100	mV
V_{IL}	LOW-level input voltage	pin EN		0	-	0.4	V
V_{IH}	HIGH-level input voltage	pin EN		1.4	-	5.5	V
I_{OUT}	current on pin OUT			-	-	200	mA
I_{OM}	peak output current	V_{IN} = ($V_{O(nom)}$ + 0.5 V) to 5.5 V	[1]				
		$V_{O(nom)}$ > 1.8 V; V_{OUT} = 0.95 × $V_{O(nom)}$		300	-	-	mA
		$V_{O(nom)}$ < 1.8 V; V_{OUT} = 0.9 × $V_{O(nom)}$		300	-	-	mA
I_{sc}	short-circuit current	pin OUT		-	600	-	mA
I_q	quiescent current	V_{EN} = 1.4 V; I_{OUT} = 0 mA		-	70	100	μA
		V_{EN} = 1.4 V; 1 mA ≤ I_{OUT} ≤ 200 mA		-	155	250	μA
		V_{EN} ≤ 0.4 V		-	-	1.0	μA
T_{sd}	shutdown temperature			-	160	-	°C
$T_{sd(hys)}$	shutdown temperature hysteresis		[2]	-	20	-	°K
PSRR	power supply rejection ratio	V_{IN} = $V_{O(nom)}$ + 0.2 V; I_{OUT} = 50 mA; f_{ripple} = 1 kHz	[1]	-	−55	-	dB
$V_{n(o)(RMS)}$	RMS output noise voltage	bandwidth = 10 Hz to 100 kHz; $C_{L(ext)}$ = 1 μF		-	30	-	μV
$t_{startup(reg)}$	regulator start-up time	V_{IN} = 5.5 V; V_{OUT} = 0.95 × $V_{O(nom)}$; I_{OUT} = 200 mA; $C_{L(ext)}$ = 1 μF	[1]	-	-	200	μs

[1] $V_{O(nom)}$ = nominal output voltage (device specific).

[2] The junction temperature must decrease by $T_{sd(hys)}$ to enable the device after T_{sd} was reached and the device was disabled.

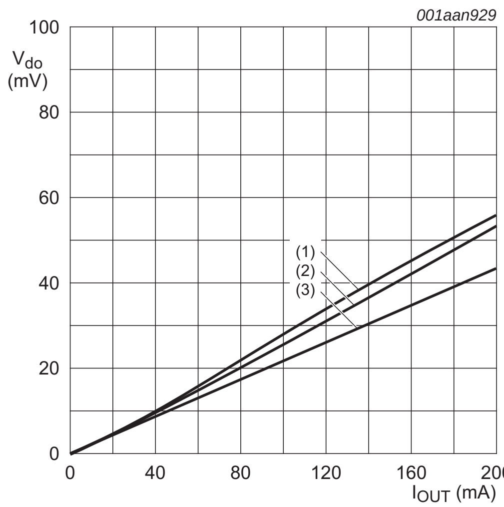
9. Dynamic behavior

All results described in Section 9 are based on measurements of types LD6806CX4xxx and LD6806Fxxx from the LD6806 product series.

9.1 Dropout

The dropout voltage is defined as the smallest input to output voltage difference at a specified load current when the regulator operates within its linear region with the pass transistor functioning simply as a resistor. This means that the input voltage is below the nominal output voltage value.

A small dropout voltage guarantees lower power consumption and maximizes efficiency.

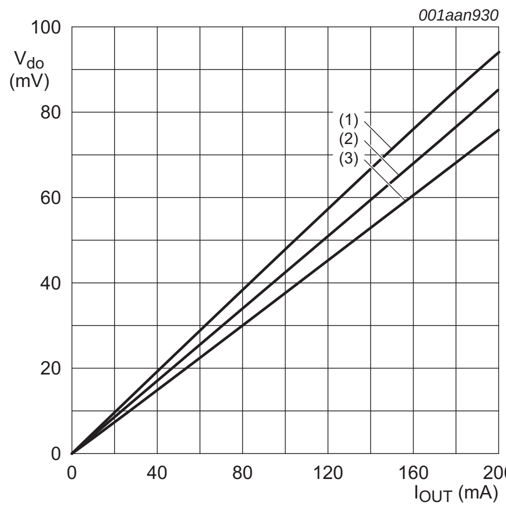


(1) +85 °C

(2) +25 °C

(3) −40 °C

Fig 4. Dropout as a function of temperature for LD6806CX4/25H

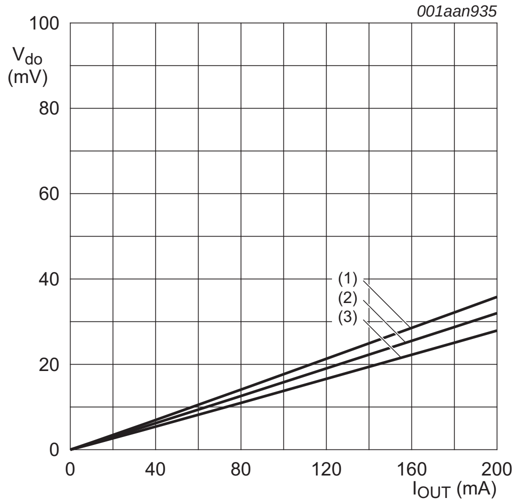


(1) +85 °C

(2) +25 °C

(3) −40 °C

Fig 5. Dropout as a function of temperature for LD6806F/25H

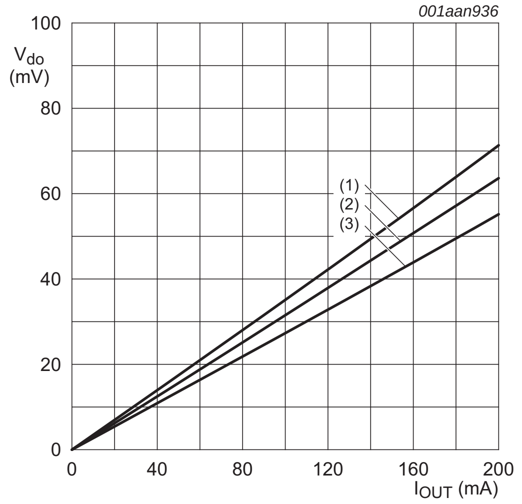


(1) +85 °C

(2) +25 °C

(3) −40 °C

Fig 6. Dropout as a function of temperature for LD6806CX4/36H



(1) +85 °C

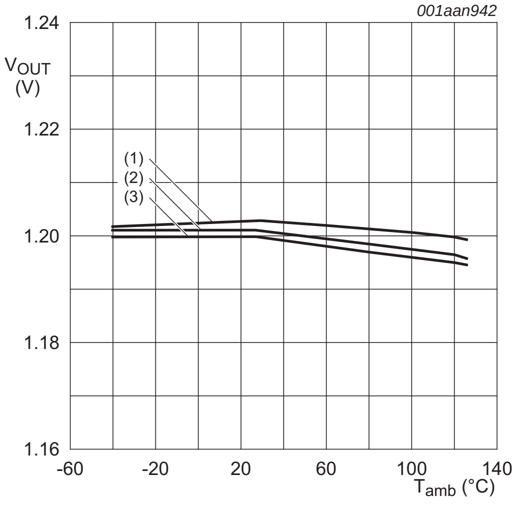
(2) +25 °C

(3) −40 °C

Fig 7. Dropout as a function of temperature for LD6806F/36H

9.2 Working voltage tolerance

The guaranteed output voltages are specified in Table 8.

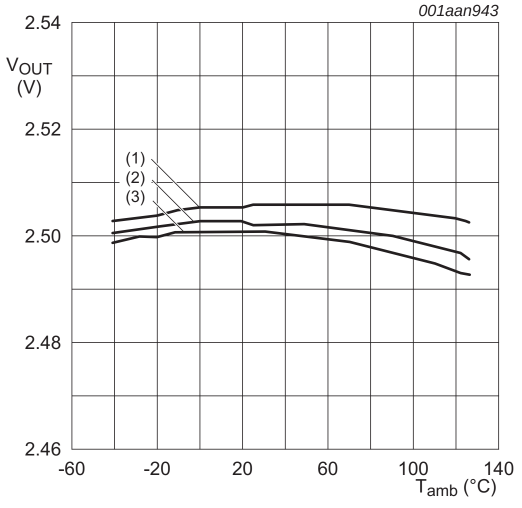


(1) I_{OUT} = 1 mA

(2) I_{OUT} = 100 mA

(3) I_{OUT} = 200 mA

Fig 8. Working voltage tolerance for LD6806CX4/12H



(1) I_{OUT} = 1 mA

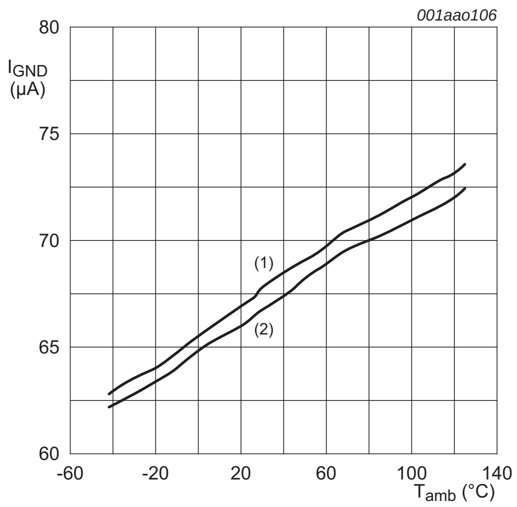
(2) I_{OUT} = 100 mA

(3) I_{OUT} = 200 mA

Fig 9. Working voltage tolerance for LD6806CX4/25H

9.3 Quiescent current

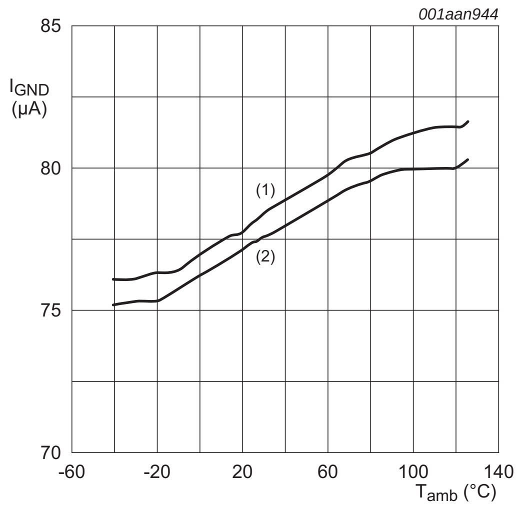
Quiescent or ground current is the difference between the input and the output current of the regulator.



(1) I_{OUT} = 10 mA

(2) I_{OUT} = 0 mA

Fig 10. Quiescent current for LD6806CX4/12H



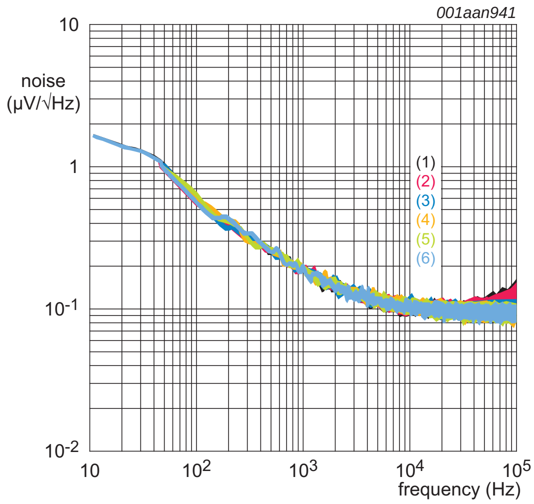
(1) I_{OUT} = 10 mA

(2) I_{OUT} = 0 mA

Fig 11. Quiescent current for LD6806CX4/25H

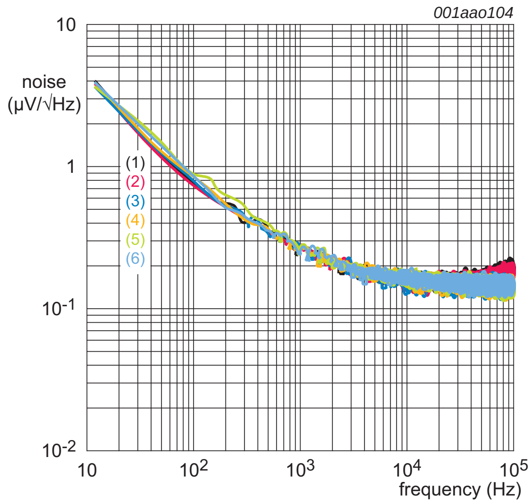
9.4 Noise

Output noise voltage of an LDO circuit is given as noise density or RMS output noise voltage over a defined range of frequencies (10 Hz to 100 kHz). Permanent conditions are a constant output current and a ripple-free input voltage. The output noise voltage is generated by the LDO regulator.



(1) 0 mA
(2) 1 mA
(3) 50 mA
(4) 100 mA
(5) 150 mA
(6) 200 mA

Fig 12. Noise density for LD6806CX4/25H



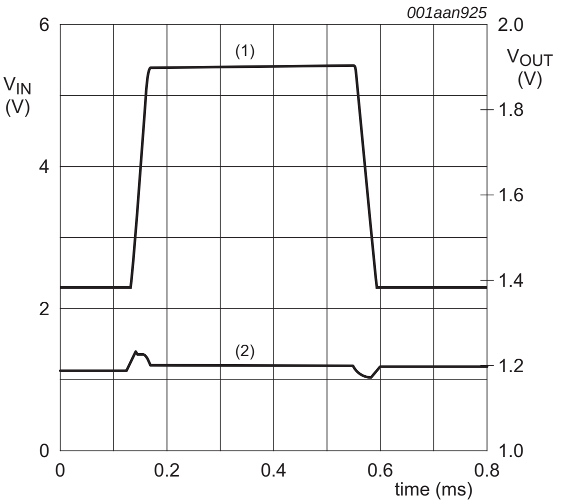
(1) 0 mA
(2) 1 mA
(3) 50 mA
(4) 100 mA
(5) 150 mA
(6) 200 mA

Fig 13. Noise density for LD6806CX4/36H

9.5 Line regulation

Line regulation response is the capability of the circuit to maintain the nominal output voltage while varying the input voltage.

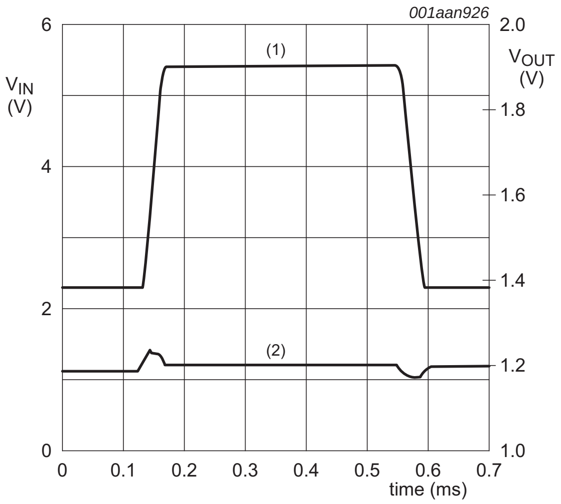
$$Regulation[\%/V] = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{100}{V_{OUT}}$$



(1) V_{IN}

(2) V_{OUT}

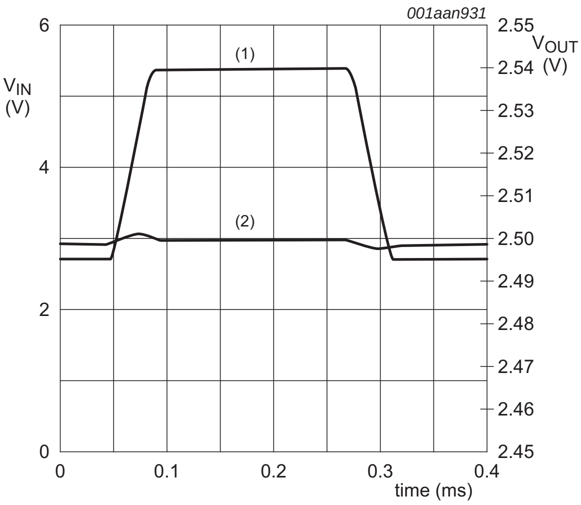
Fig 14. Line regulation for LD6806CX4/12H



(1) V_{IN}

(2) V_{OUT}

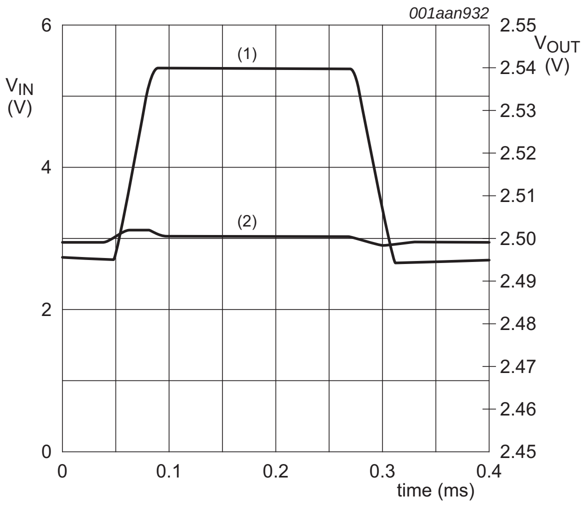
Fig 15. Line regulation for LD6806F/12H



(1) V_{IN}

(2) V_{OUT}

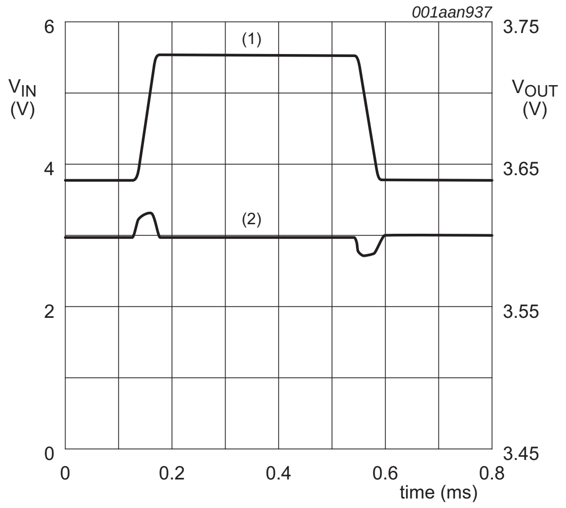
Fig 16. Line regulation for LD6806CX4/25H



(1) V_{IN}

(2) V_{OUT}

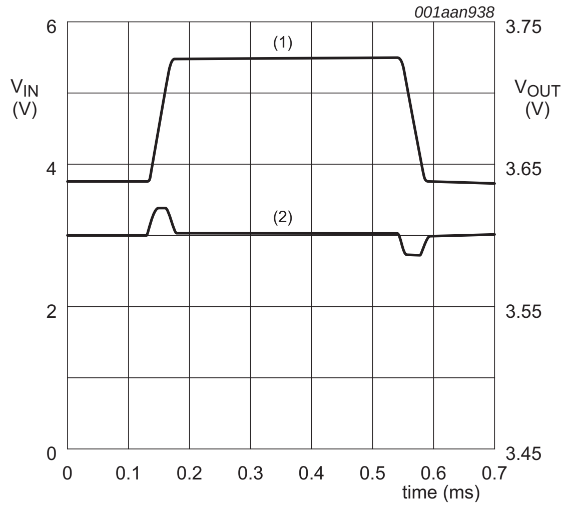
Fig 17. Line regulation for LD6806F/25H



(1) V_{IN}

(2) V_{OUT}

Fig 18. Line regulation for LD6806CX4/36H



(1) V_{IN}

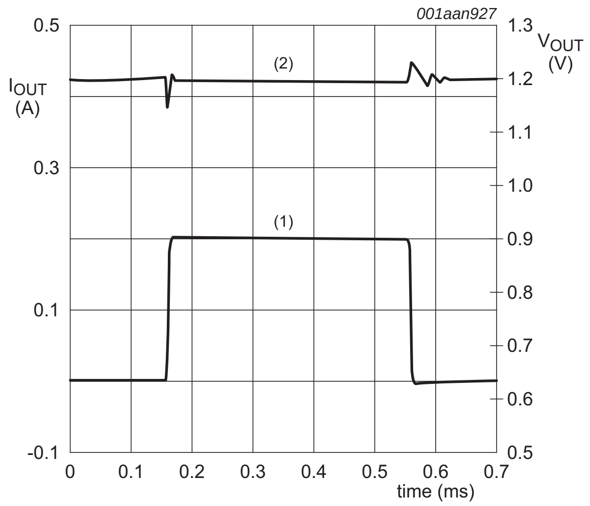
(2) V_{OUT}

Fig 19. Line regulation for LD6806F/36H

9.6 Load regulation

Load regulation is the capability of the circuit to maintain the nominal output voltage while varying the output load current.

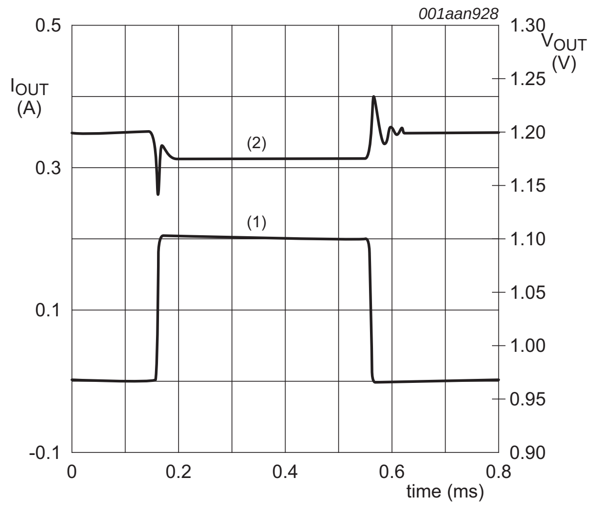
$$Load\ regulation[\%/mA] = \frac{\frac{\Delta V_{OUT}}{V_{O(nom)}} \times 100}{I_{OUT(max)}}$$



(1) I_{OUT}

(2) V_{OUT}

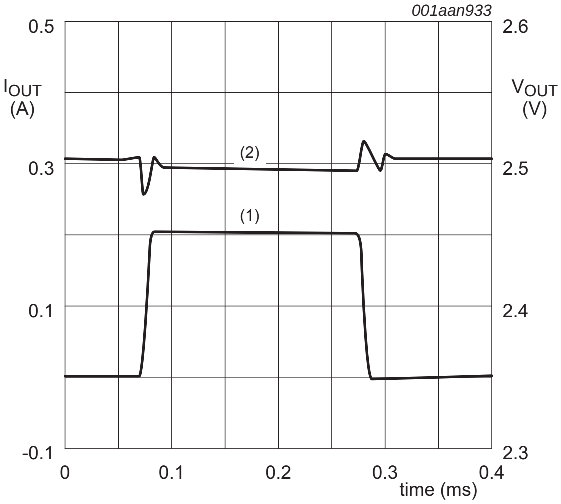
Fig 20. Load regulation for LD6806CX4/12H



(1) I_{OUT}

(2) V_{OUT}

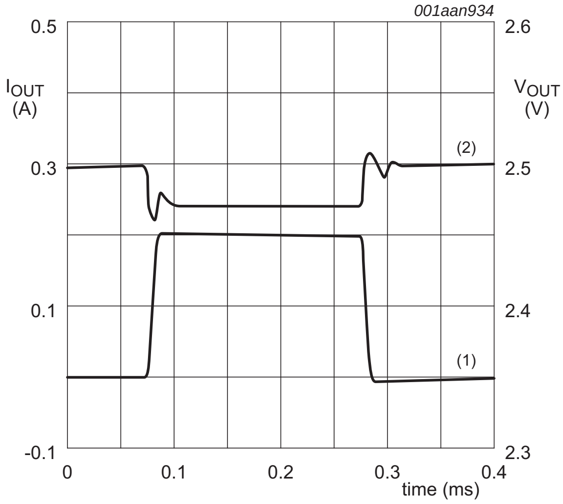
Fig 21. Load regulation for LD6806F/12H



(1) I_{OUT}

(2) V_{OUT}

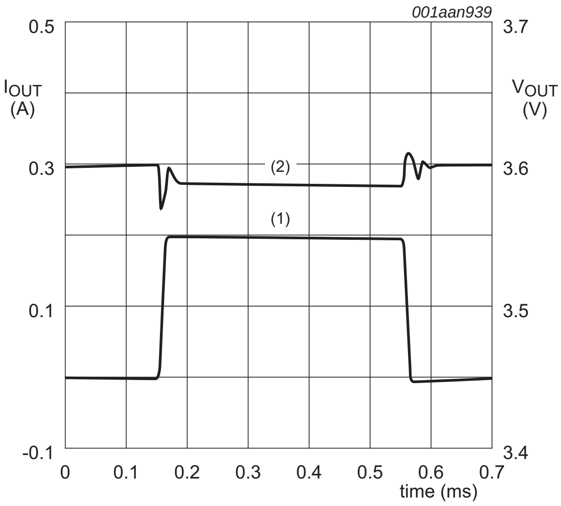
Fig 22. Load regulation for LD6806CX4/25H



(1) I_{OUT}

(2) V_{OUT}

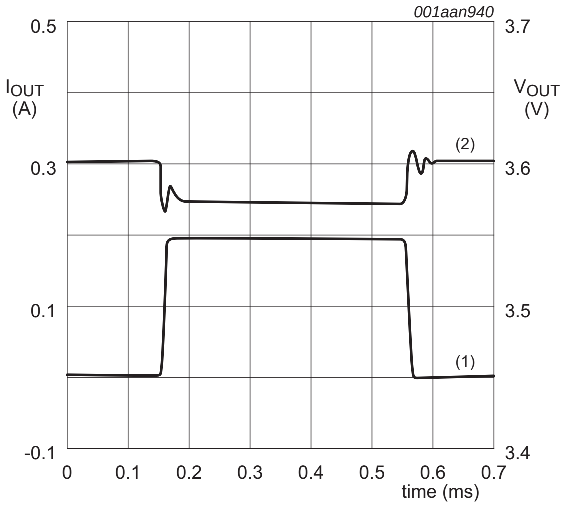
Fig 23. Load regulation for LD6806F/25H



(1) I_{OUT}

(2) V_{OUT}

Fig 24. Load regulation for LD6806CX4/36H



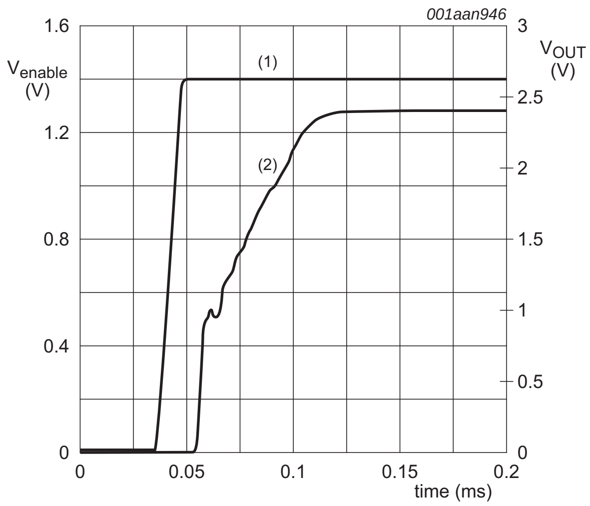
(1) I_{OUT}

(2) V_{OUT}

Fig 25. Load regulation for LD6806F/36H

9.7 Start-up

Start-up time defines the time needed for the LDO to achieve 95 % of its typical output voltage level after activation via the enable pin.



(1) V_{EN}

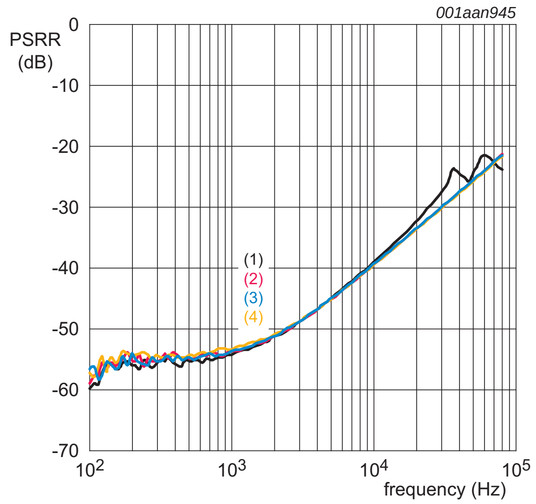
(2) V_{OUT}

Fig 26. Start-up for LD6806CX4/23H

9.8 Power Supply Rejection Ratio (PSRR)

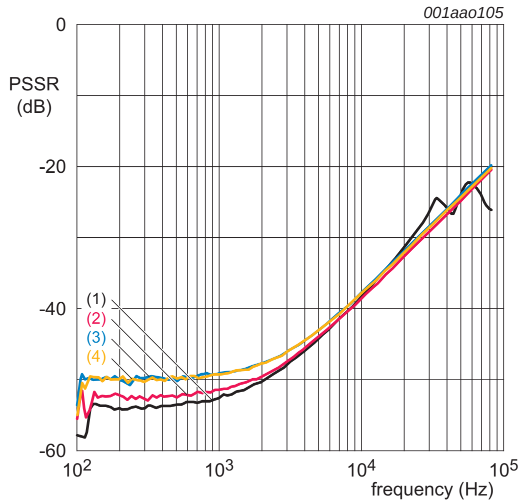
PSRR stands for the capability of the regulator to suppress unwanted signals on the input voltage like noise or ripples.

$$PSRR[dB] = 20log\frac{V_{out(ripple)}}{V_{in(ripple)}} \text{ for all frequencies}$$



(1) 1 mA
(2) 50 mA
(3) 100 mA
(4) 200 mA

Fig 27. PSRR for LD6806CX4/25H

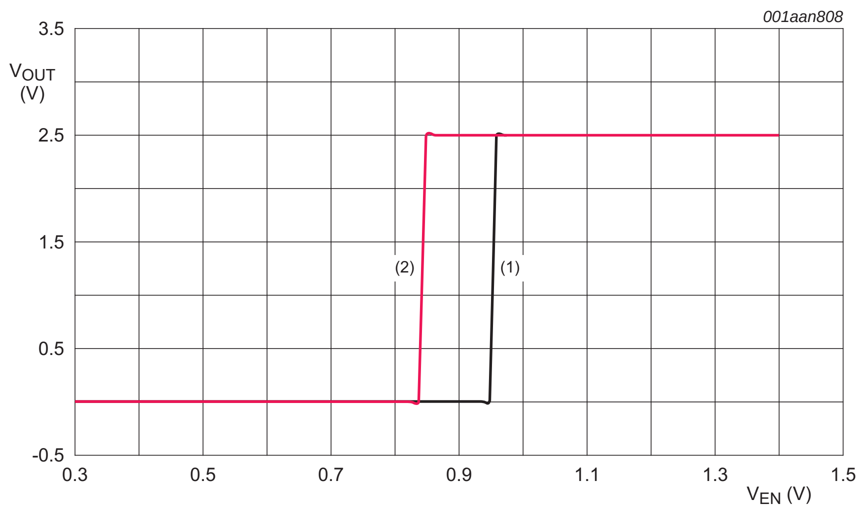


(1) 1 mA
(2) 50 mA
(3) 100 mA
(4) 200 mA

Fig 28. PSRR for LD6806CX4/36H

9.9 Enable threshold voltage

An active HIGH signal enables the LDO when the signal exceeds the minimum input HIGH voltage threshold. The device is in Off state as long the signal is below the maximum LOW threshold. The input voltage threshold is independent from the LDO supply voltage.



(1) LOW to HIGH

(2) HIGH to LOW

Fig 29. Enable threshold voltage

10. Application information

10.1 Output capacitor values

The LD6806 series requires external capacitors at the output to guarantee a stable regulator behavior. These capacitors should not under-run the specified minimum Equivalent Series Resistance (ESR).

The absolute value of the total capacitance attached to the output pin OUT influences the shutdown time ($t_{shutdown}$) of the LD6806 series.

Table 9. External load capacitor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{L(ext)}$	external load capacitance	[1]	-	1.0	-	μF
ESR	equivalent series resistance		5	-	500	mΩ

[1] The minimum value of capacitance for stability and correct operation is 0.7 μF. The capacitor tolerance should be ±30 % or better over the temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. The recommended capacitor type is X7R to meet the full device temperature specification of –40 °C to +125 °C.

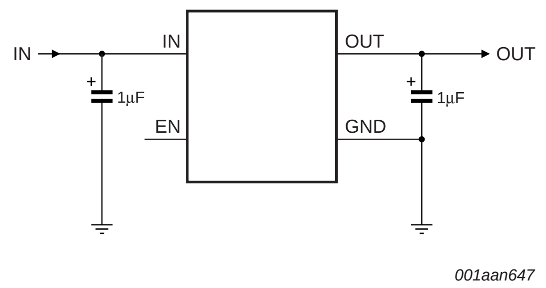


Fig 30. Application diagram

11. Test information

11.1 Quality information

This product has been qualified in accordance with *NX2-00001 NXP Semiconductors Quality and Reliability Specification* and is suitable for use in consumer applications.

12. Package outline

WLCSP4: wafer level chip-size package; 4 bumps (2 x 2)

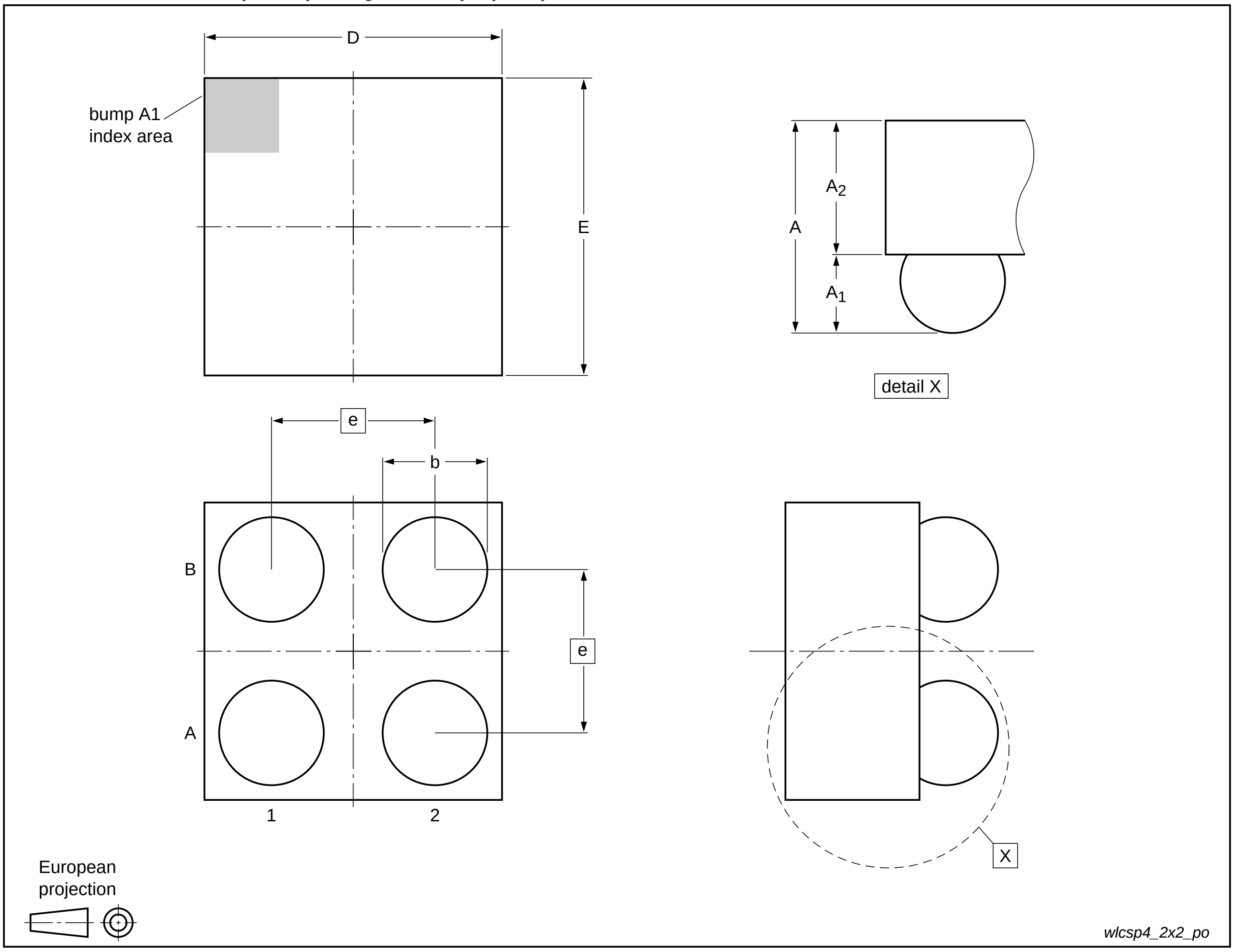
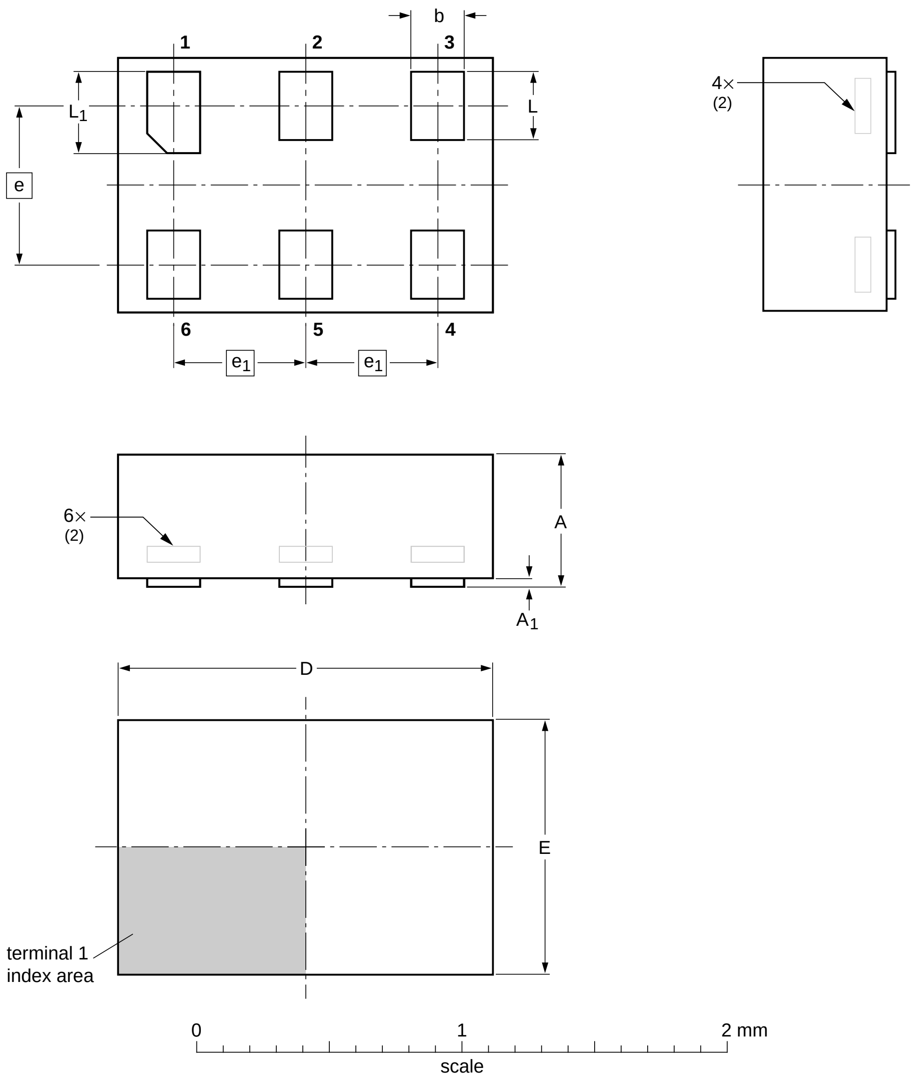


Fig 31. Package outline WLCSP4

Table 10. Dimensions of LD6806CX4/xxx for package outline WLCSP4; see Figure 31

Symbol	Min	Typ	Max	Unit
A	0.44	0.47	0.50	mm
A_1	0.18	0.20	0.22	mm
A_2	0.26	0.27	0.28	mm
b	0.21	0.26	0.31	mm
D	0.71	0.76	0.81	mm
E	0.71	0.76	0.81	mm
e	-	0.4	-	mm

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm **SOT886**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-15~~ 04-07-22

Fig 32. Package outline SOT886 (XSON6)

13. Soldering

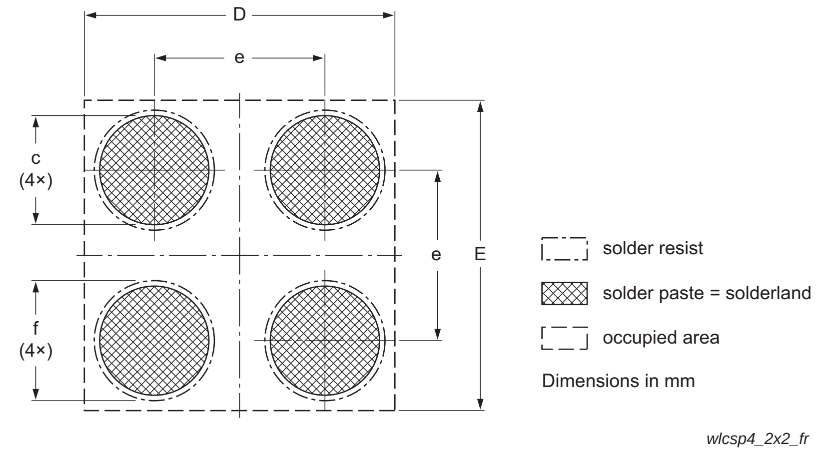


Fig 33. Soldering footprint WLCSP4

Table 11. Dimensions of soldering footprint WLCSP4; see Figure 33

Symbol	Min	Typ	Max	Unit
c	-	0.25	-	mm
D	0.71	0.76	0.81	mm
E	0.71	0.76	0.81	mm
e	-	0.4	-	mm
f	-	0.325	-	mm

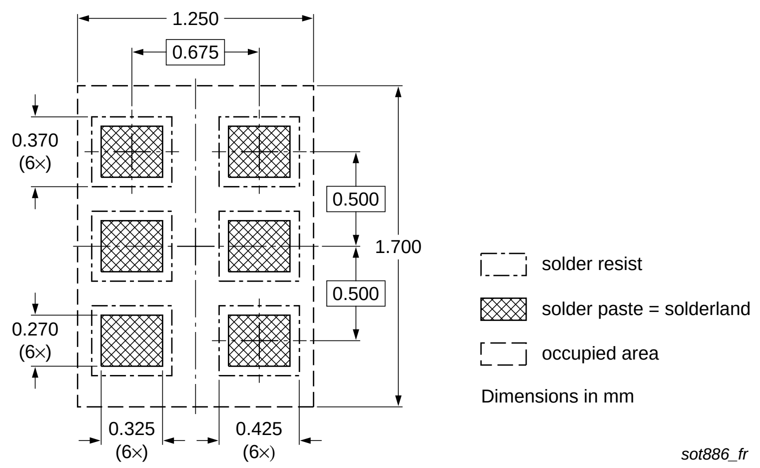


Fig 34. Soldering footprint SOT886 (XSON6)

14. Soldering of WLCSP packages

14.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

14.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

14.3 Reflow soldering

Key characteristics in reflow soldering are:

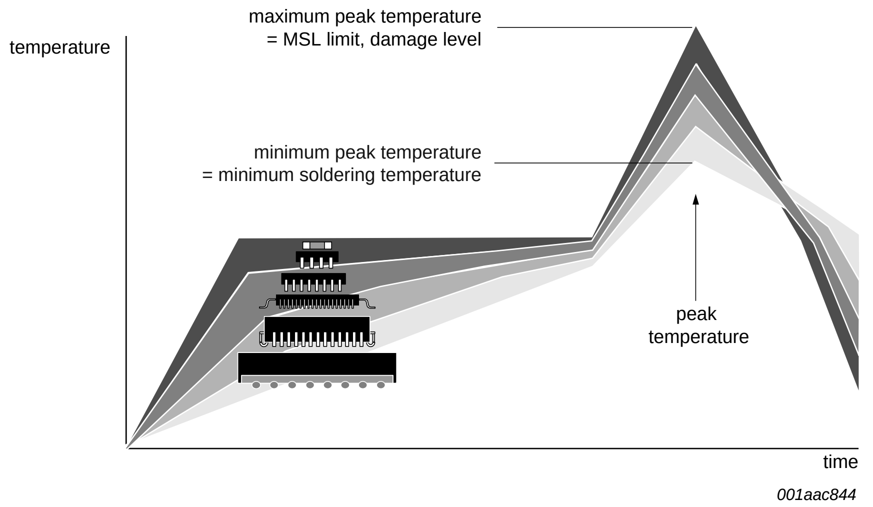
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 35) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12.

Table 12. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 35.



MSL: Moisture Sensitivity Level

Fig 35. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

14.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

14.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

14.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 “Surface mount reflow soldering description”*.

14.3.4 Cleaning

Cleaning can be done after reflow soldering.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation

- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 36) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and 14

Table 13. SnPb eutectic process (from J-STD-020C)

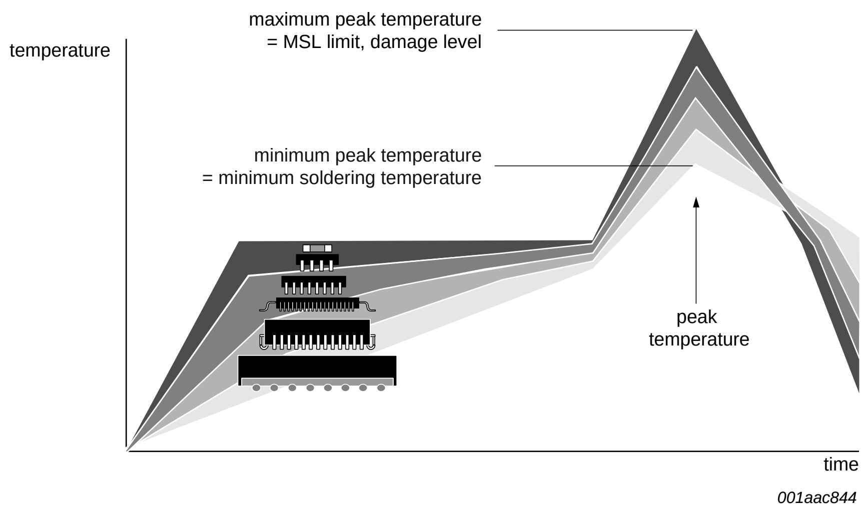
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 14. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 36.



MSL: Moisture Sensitivity Level

Fig 36. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Mounting

16.1 PCB design guidelines

It is recommended, for optimum performance, to use a Non-Solder Mask Defined (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. Refer to Table 15 for the recommended PCB design parameters.

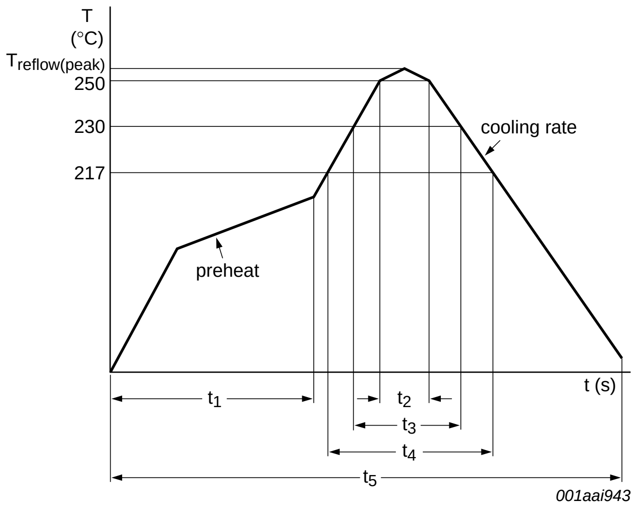
Table 15. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	250 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	325 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi or OSP
PCB material	FR4

16.2 PCB assembly guidelines for Pb-free soldering

Table 16. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	250 µm
Solder screen thickness	100 µm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %); Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 37



The device is capable of withstanding at least three reflows at this profile.

Fig 37. Pb-free solder reflow profile

Table 17. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		preheat	2.5	-	4.0	°C/s

17. Abbreviations

Table 18. Abbreviations

Acronym	Description
CSP	Chip-Size Package
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
HBM	Human Body Model
LDO	Low DropOut
MM	Machine Model
NSMD	Non-Solder Mask Design
OSP	Organic Solderability Preservation
PCB	Printed-Circuit Board
PSRR	Power Supply Rejection Ratio
PSU	Power Supply Unit
QRS	Quality and Reliability Specification
RMS	Root Mean Square
WLCSP	Wafer Level Chip-Size Package

18. References

[1] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[2] **IEC 61340-3-1 —** Methods for simulation of electrostatic effects - Human body model (HBM) electrostatic discharge test waveforms

[3] **JESD22-A115C —** Electrostatic discharge (ESD) Sensitivity Testing Machine Model (MM)

[4] **NX2-00001 —** NXP Semiconductors Quality and Reliability Specification

[5] **AN10439 —** Wafer Level Chip Size Package

[6] **AN10365 —** Surface mount reflow soldering description

19. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LD6806_SER v.2.1	20110824	Product data sheet	-	LD6806_SER v.1
Modifications:	• Document changed for World Wide Web			
LD6806_SER v.2	20110719	Product data sheet	-	LD6806_SER v.1
Modifications:	• Descriptive title updated • Table 4: title changed • Table 8: three parameters updated • Table 2: pin number updated • Section 9.4 and Section 9.8 drawings updated • Section 16: values updated • Minor text changes			
LD6806_SER v.1	20110516	Preliminary data sheet	-	-

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20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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22. Tables

23. Figures

continued >>

24. Contents

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