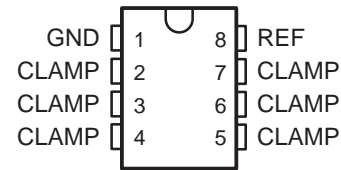


- Protects Against Latch-Up
- 25-mA Current Sink in Active State
- Less Than 1-mW Dissipation in Standby Condition
- Ideal for Applications in Environments Where Large Transient Spikes Occur
- Stable Operation for All Values of Capacitive Load
- No Output Overshoot

**D OR P PACKAGE
(TOP VIEW)**



description

The TL7726 consists of six identical clamping circuits that monitor an input voltage with respect to a reference value, REF. For an input voltage (V_I) in the range of GND to $< REF$, the clamping circuits present a very high impedance to ground, drawing current of less than 10 μA . The clamping circuits are active for $V_I < GND$ or $V_I > REF$ when they have a very low impedance and can sink up to 25 mA.

These characteristics make the TL7726 ideal as protection devices for CMOS semiconductor devices in environments where there are large positive or negative transients to protect analog-to-digital converters in automotive or industrial systems. The use of clamping circuits provides a safeguard against potential latch-up.

The TL7726C is characterized for operation over the temperature range of 0°C to 70°C. The TL7726I is characterized for operation over the temperature range of -40°C to 85°C. The TL7726Q is characterized for operation over the temperature range of -40°C to 125°C.

AVAILABLE OPTIONS

T_A	SOIC (D)	PLASTIC DIP (P)
0°C to 70°C	TL7726CD	TL7726CP
-40°C to 85°C	TL7726ID	TL7726IP
-40°C to 125°C	TL7726QD	TL7726QP

The D package is available taped and reeled. Add the suffix R to the device type (i.e., TL7726CDR).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PARAMETER MEASUREMENT INFORMATION

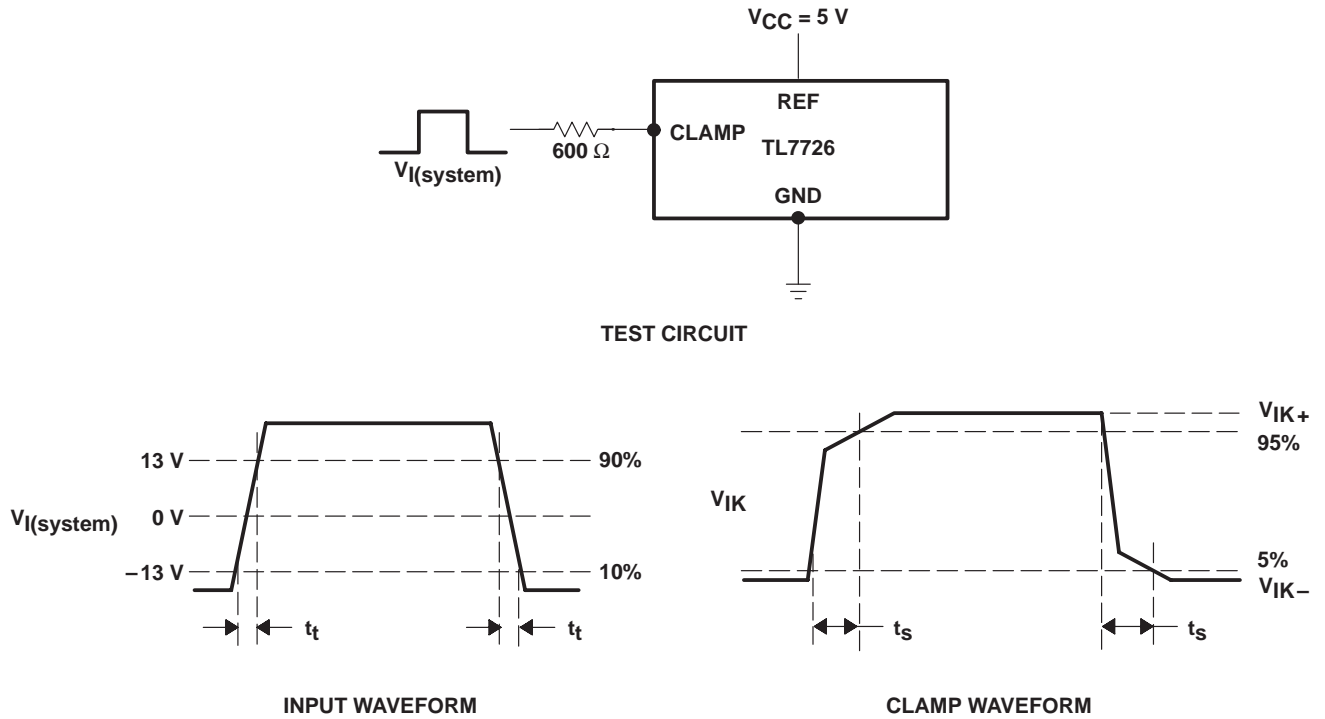


Figure 1. Switching Characteristics

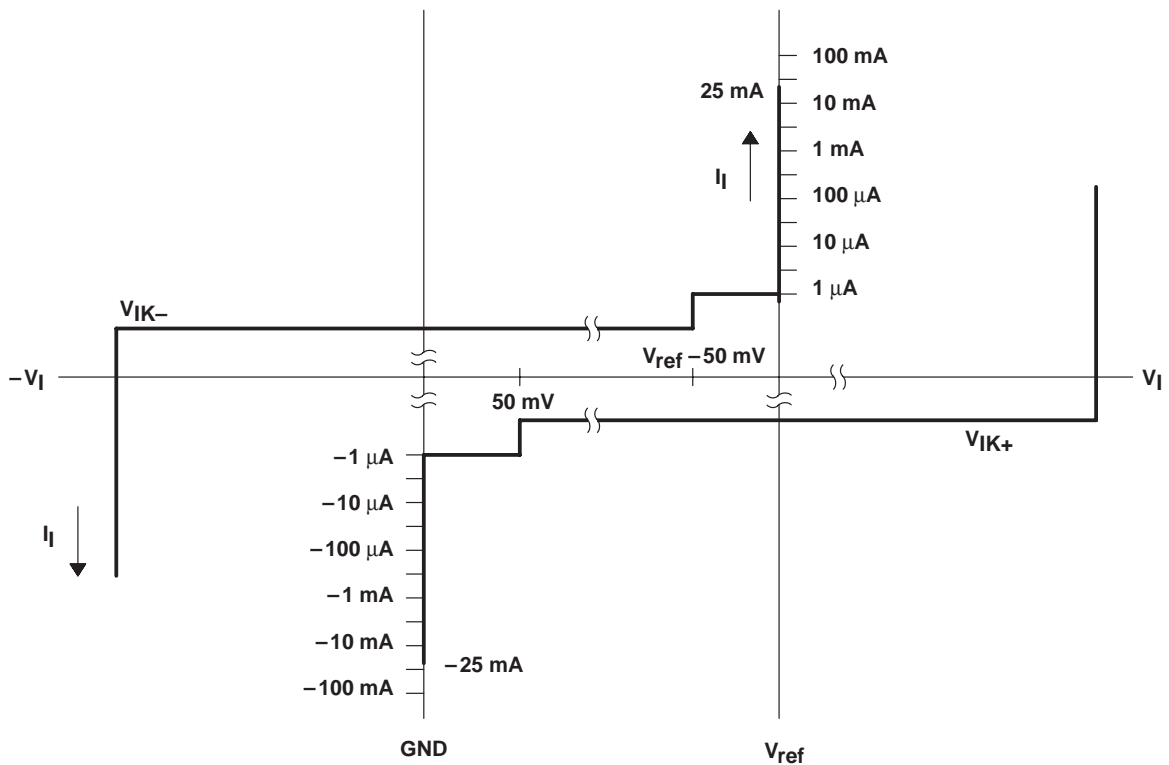
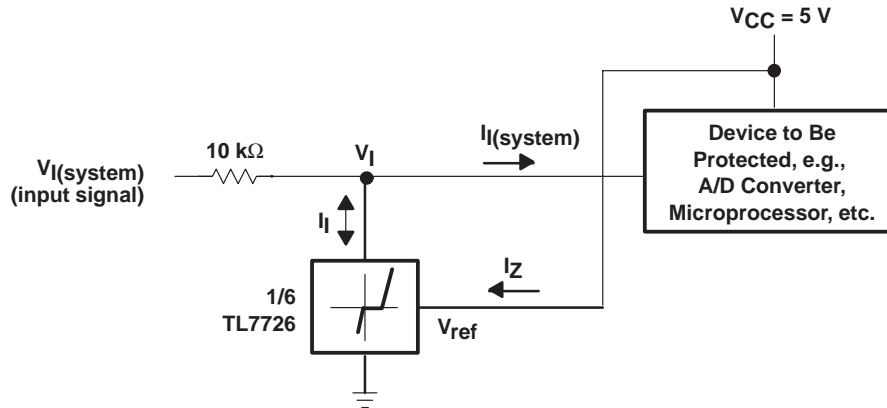


Figure 2. Tolerance Band for Clamping Circuit

TL7726 HEX CLAMPING CIRCUITS

SLAS078C – SEPTEMBER 1993 – REVISED JULY 1999

APPLICATION INFORMATION



Example: If $I_I \gg I_{(\text{system})}$, i.e., $V_{I(\text{system})} > V_{\text{ref}} + 200\text{ mV}$
where:

$I_{(\text{system})}$ = Input current to the device being protected

$V_{I(\text{system})}$ = Input voltage to the device being protected
then the maximum input voltage

$$\begin{aligned} V_{I(\text{system})\text{max}} &= V_{\text{ref}} + I_{I\text{max}}(10\text{ k}\Omega) \\ &= 5\text{ V} + 25\text{ mA}(10\text{ k}\Omega) \\ &= 5\text{ V} + 250\text{ V} \\ &= 255\text{ V} \end{aligned}$$

Figure 3. Typical Application

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL7726CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL7726ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL7726IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL7726QD	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM
TL7726QDR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
TL7726QP	ACTIVE	PDIP	P	8	50	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



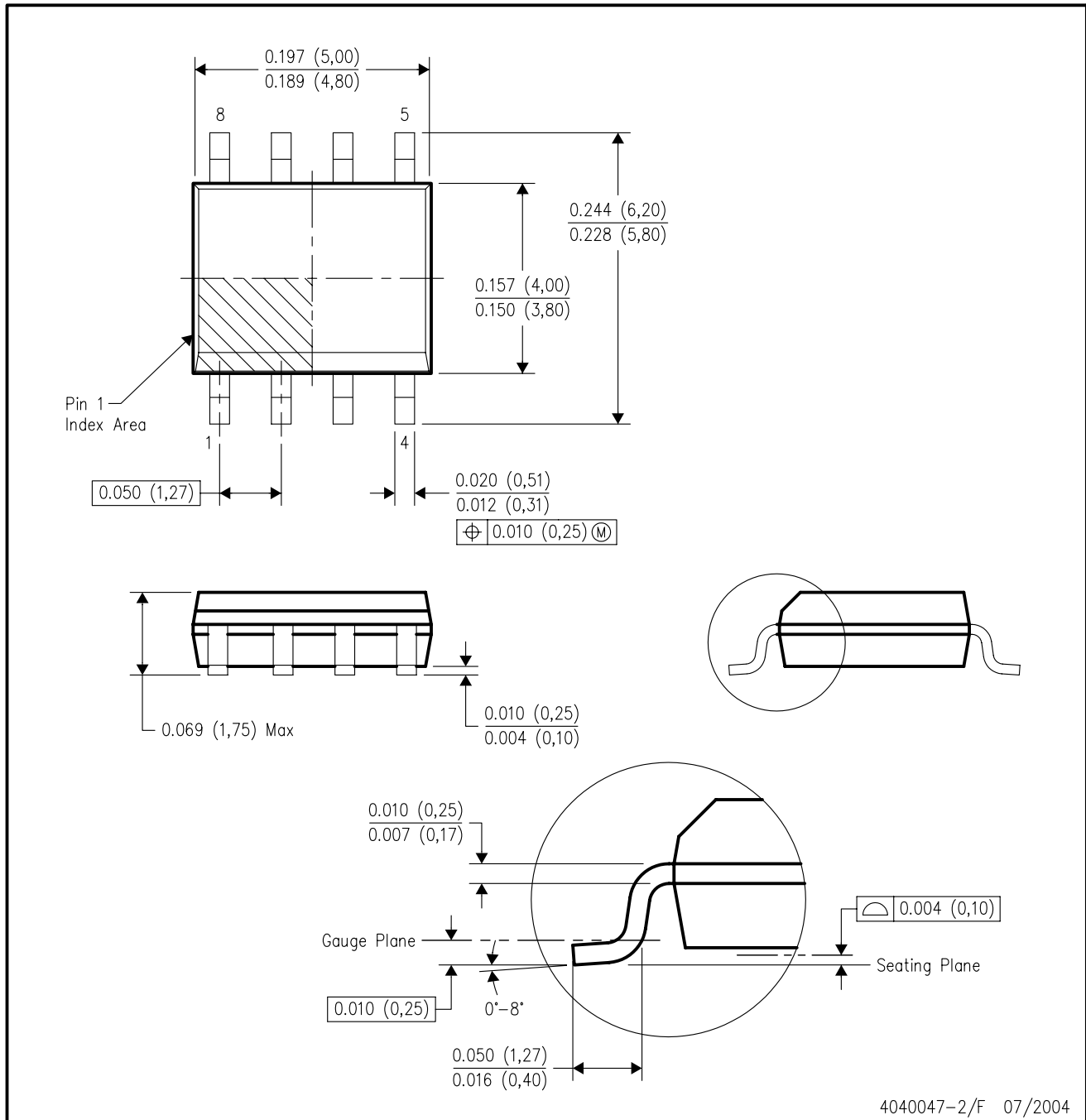
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AA.

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