EL2082C
Current-Mode Multiplier

Features

- Flexible inputs and outputs, all ground referred
- 150 MHz large and small-signal bandwidth
- 46 dB of calibrated gain control range
- 70 dB isolation in disable mode @ 10 MHz
- 0.15% diff gain and 0.05° diff phase performance at NTSC using application circuit
- Operates on ±5V to ±15V power supplies
- Outputs may be paralleled to function as a multiplexer

Applications

- Level adjust for video signals
- Video faders and mixers
- Signal routing multiplexers
- Variable active filters
- Video monitor contrast control
- AGC
- Receiver IF gain control
- Modulation/demodulation
- General "cold" front-panel control of AC signals

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2082CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2082CS	0°C to +75°C	8-Pin SO	MDP0027

General Description

The EL2082 is a general purpose variable gain control building block, built using an advanced proprietary complementary bipolar process. It is a two-quandrant multiplier, so that zero or negative control voltages do not allow signal feedthrough and very high attenuation is possible. The EL2082 works in current mode rather than voltage mode, so that the input impedance is low and the output impedance is high. This allows very wide bandwidth for both large and small signals.

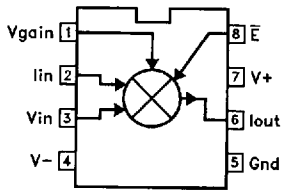
The I_{IN} pin replicates the voltage present on the V_{IN} pin; therefore, the V_{IN} pin can be used to reject common-mode noise and establish an input ground reference. The gain control input is calibrated to 1 mA/mA signal gain for 1V of control voltage. The disable pin ($\overline{E}$) is TTL-compatible, and the output current can comply with a wide range of output voltages.

Because current signals rather than voltages are employed, multiple inputs can be summed and many outputs wire-or'ed or mixed.

The EL2082 operates from a wide range of supplies and is available in standard 8-pin plastic DIP or 8-lead SO.

Connection Diagram

8-Pin DIP/SO



Top View

EL2082C
Current-Mode Multiplier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V_S^+ and V_S^-	+33V	P_D	Maximum Power Dissipation	See Curves
V_{IN}, I_{OUT}	Voltage	$\pm V_S$	T_A	Operating Temperature Range	0°C to +75°C
V_E, V_{GAIN}	Input Voltage	−1 to +7V	T_J	Operating Junction Temperature	150°C
I_{IN}	Input Current	±5 mA	T_{ST}	Storage Temperature	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

(V_S = ±15V, V_G = 1V, V_E = 0.8V, V_{OUT} = 0, V_{IN} = 0, I_{IN} = 0)

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{IO}	Input Offset Voltage	Full	−20		20	II	mV
I_{OO}	Output Offset Current	Full	−100		100	II	µA
R_{INI}	I_{IN} Input Impedance; I_{IN} = 0, 0.35 mA	Full	75	95	115	II	Ω
V_{CMRR}	Voltage Common-Mode Rejection Ratio V_{IN} = −10V, +10V	Full	45	55		II	dB
I_{CMRR}	Offset Current Common-Mode Rejection Ratio, V_{IN} = −10V, +10V	Full		0.5	5	II	µA/V
V_{PSRR}	Offset Voltage Power Supply Rejection Ratio, V_S = ±5V to ±15V	Full	60	80		II	dB
I_{PSRR}	Offset Current Power Supply Rejection Ratio, V_S = ±5V to ±15V	Full		1	10	II	µA/V
I_{BVIN}	V_{IN} Bias Current	Full	−10		10	II	µA
R_{INV}	V_{IN} Input Impedance; V_{IN} = −10V, +10V	Full	0.5	1.0		II	MΩ
Nlini	Signal Nonlinearity; I_{IN} = −0.7 mA, −0.35 mA, 0 mA, +0.35 mA, +0.7 mA	Full		0.10	0.4	II	%
R_{OUT}	Output Impedance V_{OUT} = −10V, +10V	Full	0.25	0.5		II	MΩ

DC Electrical Characteristics — Contd.

(V_S = ±15V, V_G = 1V, V_E = 0.8V, V_{OUT} = 0, V_{IN} = 0, I_{IN} = 0)

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OUT}	Output Swing; V_{GAIN} = 2V, I_{IN} ±2 mA, R_L = 4.0K	Full	−11		+11	II	V
V_{IOG}	V_{OS}, Gain Control, Extrapolated from V_{GAIN} = 0.1V, 1V	Full	−15		15	II	mV
A_I	Current Gain, I_{IN} ±350 µA	Full	0.9	1.0	1.1	II	mA/mA
Nling	Nonlinearity of Gain Control, V_{GAIN} = 0.1V, 0.5V, 1V	Full		2	5	II	%
I_{SO}	Input Isolation with V_{GAIN} = −0.1V	Full	−80	−96		II	dB
V_{INH}	$\overline{E}$ Logic High Level	Full	2.0			II	V
V_{INL}	$\overline{E}$ Logic Low Level	Full			0.8	II	V
I_{LH}	Input Current of $\overline{E}$, V_E = 5V	Full	−50		50	II	µA
I_{LL}	Input Current of $\overline{E}$, V_E = 0	Full	−50		50	II	µA
I_{ODIS}	I_{OUT}, Disabled $\overline{E}$ = 2.0V	Full			±10	II	µA
I_S	Supply Current	Full		13	16	II	mA

AC Electrical Characteristics

(R_L = 25Ω, C_L = 4 pF, C_{IIN} = 2 pF, T_A = 25°C, V_G = 1V, V_S = ±15V)

Parameter	Description	Min	Typ	Max	Test Level	Units
BW1	Current Mode Bandwidth −3 dB		150		V	MHz
BW2	±0.1 dB		30		V	MHz
BWp	Power, I_{IN} = 1 mA p-p		150		V	MHz
BWg	Gain Control Bandwidth		20		V	MHz
SRG	Gain Control Slew Rate V_G from 0.2V to 2V		12		V	(mA/mA)/µs
T_{REC}	Recovery Time from V_G < 0		250		V	ns
T_{EN}	Enable Time from $\overline{E}$ Pin		200		V	ns
T_{DIS}	Disable Time from $\overline{E}$ Pin		30		V	ns
D_G	Differential Gain, NTSC with I_{IN} = −0.35 mA to +0.35 mA		0.25		V	%
D_P	Differential Phase, NTSC with I_{IN} = −0.35 mA to +0.35 mA		0.05		V	Degree

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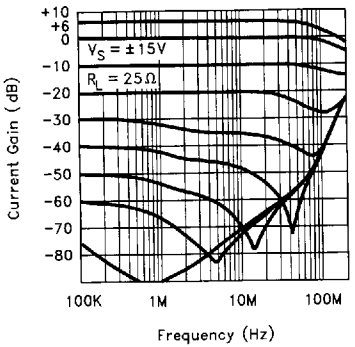
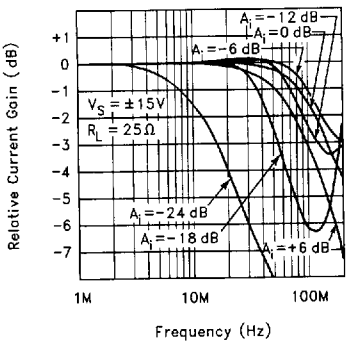
Typical Performance Curves

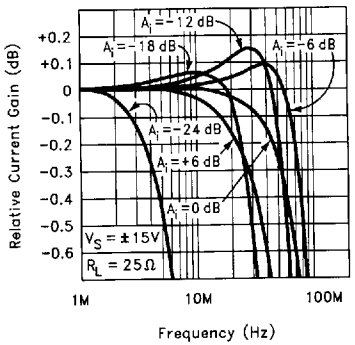
Current Gain vs Frequency for Different Gains



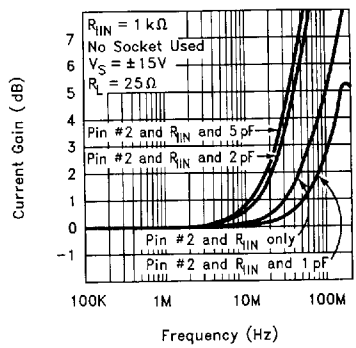
Current Gain vs Frequency



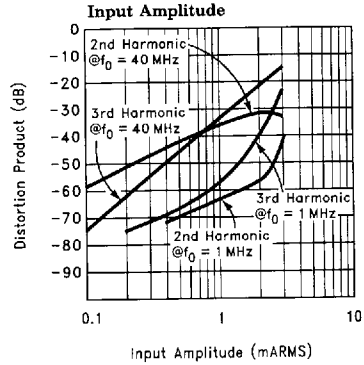
Current Gain Flatness



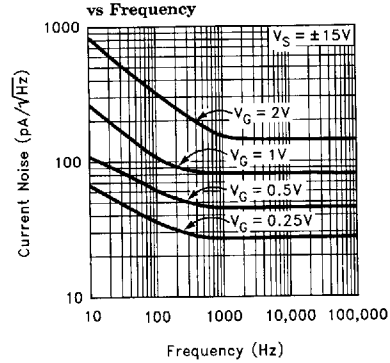
Frequency Response in Voltage Input Mode



Harmonic Distortion vs Input Amplitude



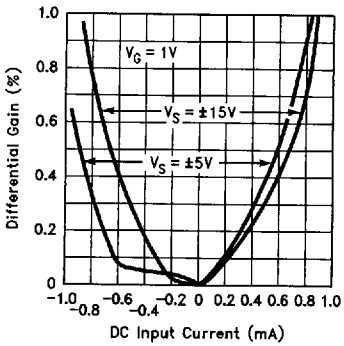
Output Current Noise vs Frequency



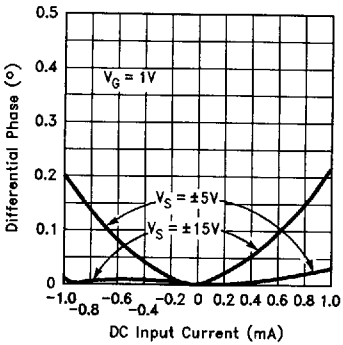
2082-2

Typical Performance Curves — Contd.

Differential Gain Error vs DC Offset Current

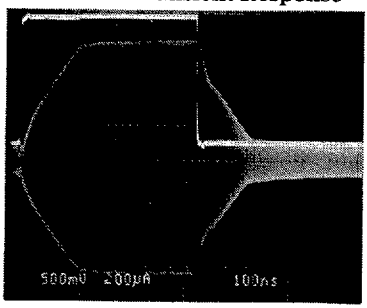


Differential Phase Error vs DC Offset Current



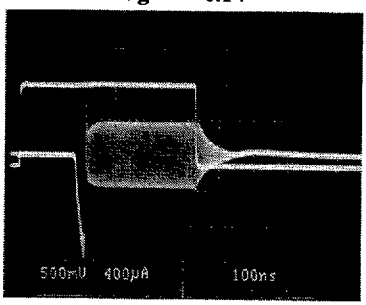
2082-3

Gain Pin Transient Response



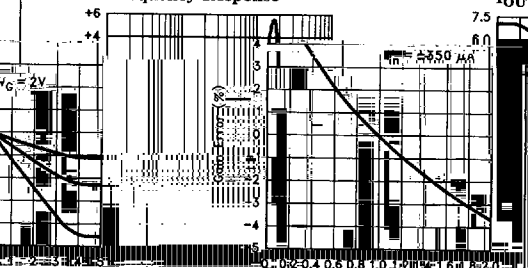
2082-4

Gain Control Recovery From Vg = −0.1V



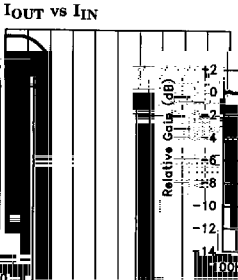
2082-5

Gain Control Pin Frequency Response

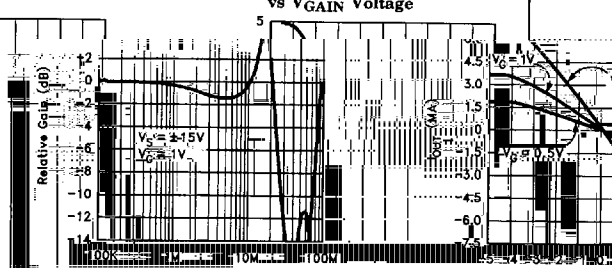


2082-6

I_{OUT} vs I_{IN}



Normalized Gain Error vs V_{GAIN} Voltage



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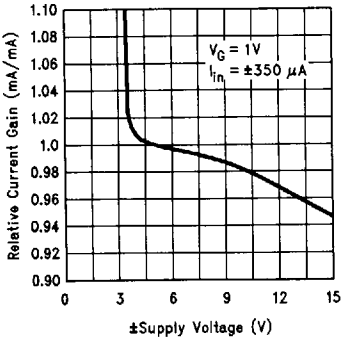
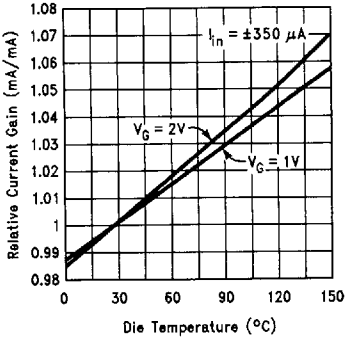
Typical Performance Curves — Contd.

Current Gain vs Supply Voltage

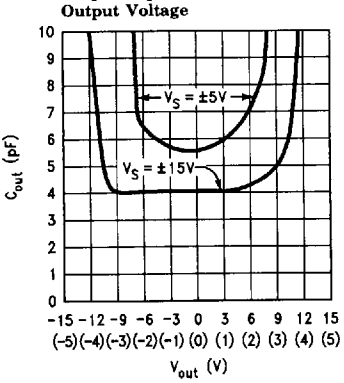


Current Gain vs Temperature



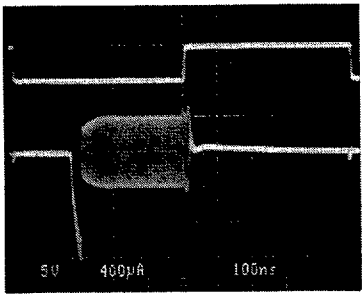
2082-7

Output Capacitance vs Output Voltage



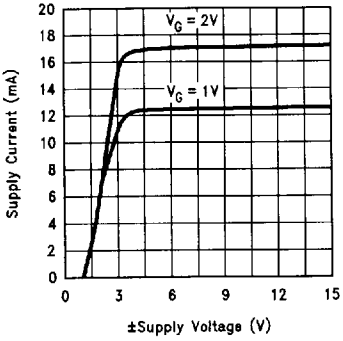
2082-8

Enable Pin Response

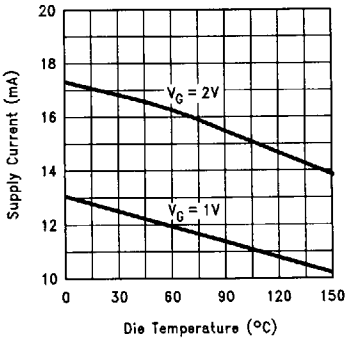


2082-9

Supply Current vs Supply Voltage



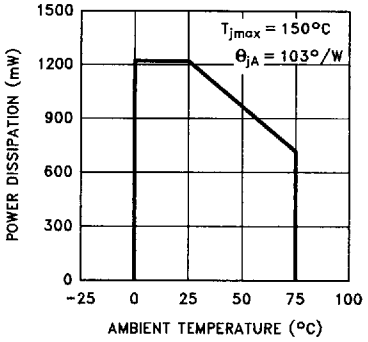
Supply Current vs Die Temperature



2082-10

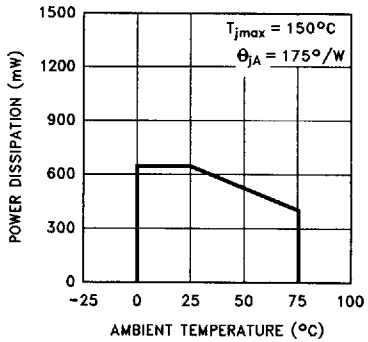
Typical Performance Curves — Contd.

8-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



2082-11

8-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



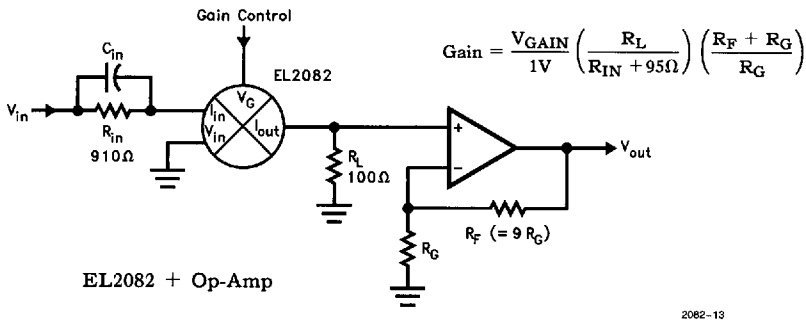
2082-12

Applications Information

The EL2082 is best thought of as a current-conveyor with variable current gain. A current input to the I_{IN} pin will be replicated as a current driven out the I_{OUT} pin, with a gain controlled by V_{GAIN}. Thus, an input of 1 mA will produce an output current of 1 mA for V_{GAIN} = 1V. An input of 1 mA will produce an output of 2 mA for V_{GAIN} = 2V. The useable V_{GAIN} range is zero to +2V. A negative level on V_{GAIN}, even only −20 mV, will yield very high signal attenuation.

The EL2082 in Conjunction with Op-Amps

This resistor-load circuit shows a simple method of converting voltage signals to currents and vice versa:



2082-13

R_{IN} would typically be 1 kΩ for video level inputs, or 10 kΩ for ±10V instrumentation signals. The higher the value of R_{IN} (the lower the input current), the lower the distortion levels of the EL2082 will be. An approximate expression of the nonlinearity of the EL2082 is:

$$\text{Nonlinearity (\%)} = 0.3 * I_{IN}\,(\text{mA})^2$$

Optimum input current level is a tradeoff between distortion and signal-to-noise-ratio. The distortion and input range do not change appreciably with V_{GAIN} levels; distortion is set by input currents alone.

EL2082C
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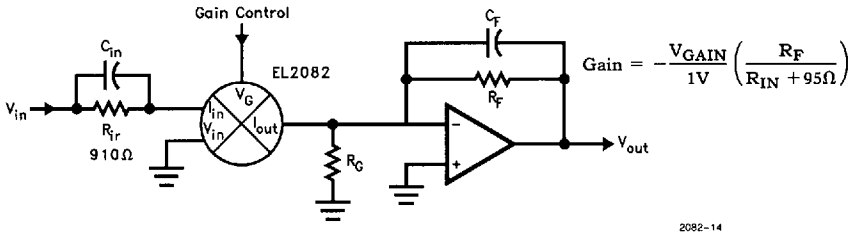
Applications Information — Contd.

The output current could be terminated with a 1 kΩ load resistor to achieve a nominal voltage gain of 1 at the EL2082, but the I_{OUT}, load, and stray capacitances would limit bandwidth greatly. The lowest practical total capacitance at I_{OUT} is about 12 pF, and this gives a 13 MHz bandwidth with a 1 kΩ load. In the above example a 100Ω load is used for an upper limit of 130 MHz. The operational amplifier gives a gain of +10 to bring the overall gain to unity. Wider bandwidth yet can be had by installing C_{IN}. This is a very small capacitor, typically 1 pf–2 pF, and it bolsters the gain above 100 MHz. Here is a table of results for this circuit used with various amplifiers:

Operational Amplifier	Power Supplies	Rf	Rg	C_{IN}	−3 dB Bandwidth	0.1 dB Bandwidth	Peaking
EL2020	±5V	620	68	—	34 MHz	5.6 MHz	0
EL2020	±15V	620	68	—	40 MHz	7.4 MHz	0
EL2130	±5V	620	68	—	73 MHz	11 MHz	1.0 dB
EL2030	±15V	620	68	—	93 MHz	12 MHz	1.3 dB
EL2090	±15V	240	27	—	60 MHz	10 MHz	0.5 dB
EL2120	±5V	220	24	—	57 MHz	10 MHz	0.4 dB
EL2120	±15V	220	24	—	65 MHz	11 MHz	0.3 dB
EL2070	±5V	200	22	2 pF	150 MHz	30 MHz	0.4 dB
EL2071	±5V	1.5K	240	2 pF	200 MHz	30 MHz	0
EL2075	±5V	620	68	2 pF	270 MHz	30 MHz	1.5 dB

Maximum bandwidth is maintained over a gain range of +6 to −16 dB; bandwidth drops at lower gains. If wider gain range with full bandwidth is required, two or more EL2082's can be cascaded with the I_{OUT} of one directly driving the I_{IN} of the next.

The EL2082 can also be used with an I ⟶ V operational circuit:



Inverting
EL2082 + Op-Amp

The circuit above gives a negative gain. The main concern of this connection involves the total I_{OUT} and stray capacitances at the amplifier's input. When using traditional op-amps, the pole caused by these capacitances can make the amplifier less stable and even cause oscillations in amplifiers whose gain-bandwidth is greater than 5 MHz. A typical cure is to add a capacitor Cf in the 2 pF–10 pF range. This will reduce overall bandwidth, so a capacitor C_{IN} can be added to regain frequency response. The ratio Cf/C_{IN} is made equal to R_{IN}/R_f.

Applications Information — Contd.

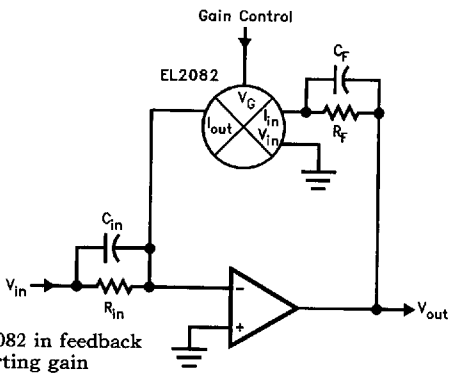
Current-feedback amplifiers eliminate this difficulty. Because their -input is a very low impedance, capacitance at the summing point of an inverting operational circuit is far less troublesome. Here is a table of results of various current-feedback circuits used in the inverting circuit:

Operational Amplifier	Power Supplies	Rf	R_{IN}	Rg	−3 dB Bandwidth	0.1 dB Bandwidth	Peaking
EL2020	±5V	1k	910	—	29 MHz	4.3 MHz	0
EL2020	±15V	1k	910	—	34 MHz	5.3 MHz	0
EL2130	±5V	1k	910	—	61 MHz	9.7 MHz	0
EL2030	±15V	1k	910	—	82 MHz	12.3 MHz	0
EL2171	±5V	2k	1.8k	1k	114 MHz	11 MHz	1.2 dB

with the EL2171 the EL2082 had ±15V supplies and the EL2171 required a 150Ω output load.

The EL2120 and EL2090 are suitable in this circuit but they are compensated for 300Ω feedback resistors. R_{IN} would have to be reduced greatly to obtain unity gain and the increased signal currents would cause the EL2082 to display much increased distortion. They could be used if the input resistor were maintained at 910Ω and Rf reduced for a $-\frac{1}{3}$ gain, or if Rf = 1k and an overall bandwidth of 25 MHz were acceptable.

The EL2082 can also be used within an op-amp's feedback loop:



EL2082 in feedback inverting gain

$$\text{Gain} = -\frac{1V}{V_{GAIN}}\left(\frac{R_F + 95\Omega}{R_{IN}}\right)$$

2082-15

With voltage-mode op-amps, the same concern about capacitance at the summing node exists, so Cf and C_{IN} should be used. As before, current-feedback amplifiers tend to solve the problem. However, in this circuit the inherent phase lag of the EL2082 detracts from the phase margin of the op-amp, and some overall bandwidth reduction may result. The EL2082 appears as a 3.0 ns delay, well past 100 MHz. Thus, for a 20 MHz loop bandwidth the EL2082 will subtract 20 MHz × 3.0 ns × 360 degrees = 216 degrees. The loop path should have at least 55 degrees of phase margin for low ringing in this connection. Loop bandwidth is always reduced by the ratio $R_{IN}/(R_{IN} + Rf)$ with voltage mode op-amps.

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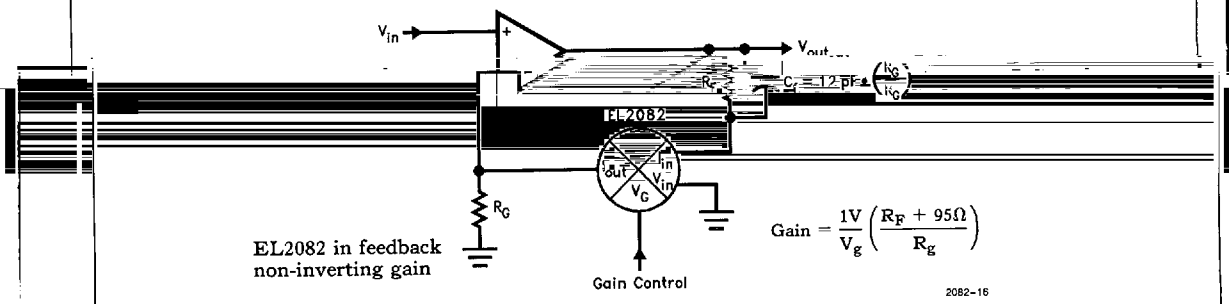
Applications Information — Contd.

Current-feedback op-amps again solve the summing-junction capacitance problem in this connection. The loop bandwidth here becomes a matter of transimpedance over frequency and its phase characteristics. Unfortunately, this is generally poorly documented in amplifier data sheets. A rule of thumb is that the transimpedance falls to the value of the recommended feedback resistor at a frequency of $F_{-3\ dB}/4$ to $F_{-3\ dB}/2$, where $F_{-3\ dB}$ is the unity-gain closed-loop bandwidth of the amplifier. The phase margin of the op-amp is usually close to 90 degrees at this frequency.

In general, Rf is initially the recommended value for the particular amplifier and is then empirically adjusted for amplifier stability at maximum V_{GAIN}, then R_{IN} is set for the overall circuit gain required. Sometimes a very small Cf can be used to improve loop stability, but it often must be in series with another resistor of value around Rf/2.

A virtue of placing the EL2082 in feedback is that the input-referred noise will drop as gain increases. This is ideal for level controls that are used to set the output to a constant level for a variety of inputs as well as AGC loops. Furthermore, the EL2082 has a relatively constant input signal amplitude for a variety of input levels, and its distortion will be relatively constant and controllable by setting Rf. Note that placing the EL2082 in the feedback path causes the circuit bandwidth to vary inversely with gain.

The next circuit shows use of the EL2082 in the feedback path of a non-inverting op-amp:

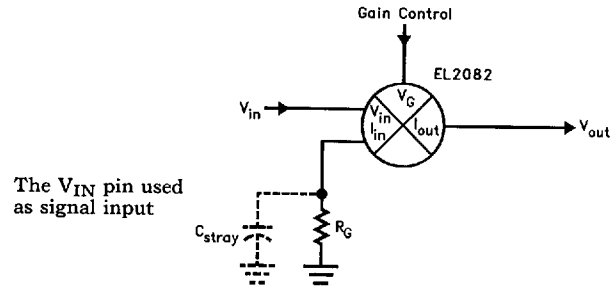


This example has the same virtues with regards to noise and distortion as the preceding circuit; and its bandwidth shrinks with increasing gain as well. The typical 12 pF sum of EL2082 output capacitance in parallel with stray capacitance necessitates the inclusion of Cf to prevent a feedback pole. Because of this 12 pF capacitance at the op-amp -input, current-feedback op-amps will generally not be useable. As before, the loop bandwidth and phase margin must accommodate the extra phase lag of the EL2082.

Applications Information — Contd.

Using the V_{IN} Pin

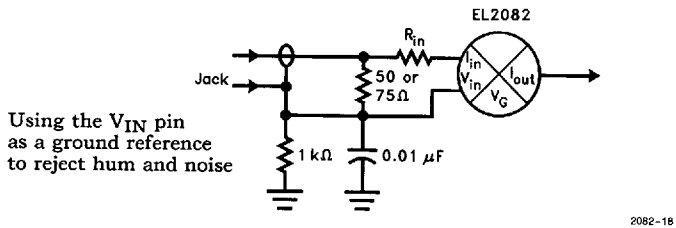
The V_{IN} pin can be used instead of the I_{IN} pin so:



$$Gm = \frac{I_{OUT}}{V_{IN}} = \frac{-Vg}{1v}\left(\frac{1}{R_g + 95\Omega}\right)$$

This connection is useful when a high input impedance is required. There are a few caveats when using the V_{IN} pin. The first is that V_{IN} has a 250 V/μs slew rate limitation. The second is that the inevitable C_{STRAY} across Rg causes a gain zero and gain INCREASES above the $1/(2\pi\ C_{STRAY}\ Rg)$ frequency and can peak as much as 20 dB with large C_{STRAY}. A graph of gain vs. frequency for several C_{STRAYS} is included in the typical performance curves. In general, if wide bandwidth and frequency flatness is desired, the I_{IN} pin should be used.

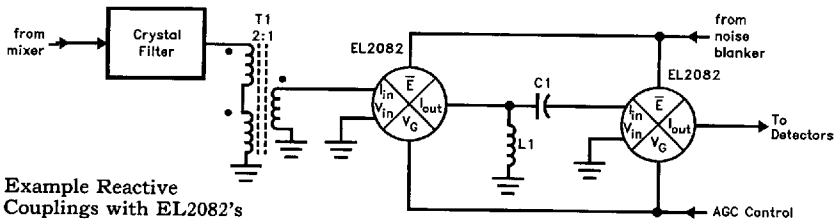
The V_{IN} pin does make an excellent ground reference pin, for instance when low-frequency noise is to be rejected. The next schematic shows the EL2082 V_{IN} pin rejecting possible 60 Hz hum induced on an RF input cable:



This example shows V_{IN} rejecting low-frequency field-induced noise but not adding peaking since the 0.01 μF bypass capacitor shunts high-frequency signals to local ground.

Reactive Couplings with the EL2082

The following sketch is an excerpt of a receiver IF amplifier showing methods of connecting the EL2082 to reactive networks:



EL2082C
Current-Mode Multiplier

Applications Information — Contd.

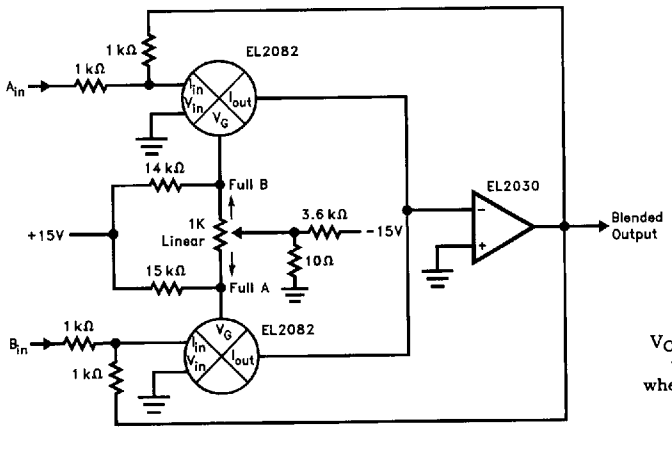
The I_{IN} pin of the EL2082 looks like 95Ω well past 100 MHz, and the output looks like a simple current-source in parallel with about 5 pF. There is no particular problem with any resistance or reactance connected to I_{IN} or I_{OUT}. The mixer output is generally sent to a crystal filter, which required a few hundred ohm terminating impedance. The impedance of the I_{IN} pin of the first EL2082 is transformed to about 400Ω by the 2:1 transformer T1. The two EL2082's are used as variable-gain IF amplifiers, with small gains offered by each. The output of the first EL2082 is coupled to the second by the resonant matching network L1–C1. For a Q of 5, Xc1 = x11 = 5 × 95Ω, approximately. The impedance seen at the first EL2082's I_{OUT} will be about $Q^2 \times 95\Omega$, or 2.5k, and by impedance transformation alone the first gain cell delivers 28 dB of gain at Vg = 1V. More gain cells can be used for a wider range of (calibrated) AGC compliance.

The $\overline{E}$ input can be used as a high-speed noise blanker gate.

Linearized Fader/Gain Control

The following circuit is an example of placing two EL2082's in the feedback network of an op-amp to significantly reduce their distortions:

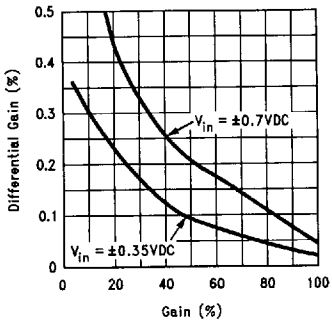
Linearized Gain Control/Fader



$V_{OUT} = K \bullet V_A + (1-K) \bullet V_B$
where $0 \leq K \leq 1$

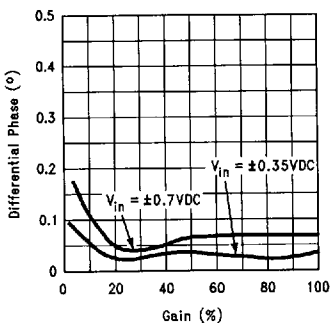
2062-20

Dual EL2082 Fader with EL2030 NTSC Differential Gain Error



2062-21

Dual EL2082 Fader with EL2030 NTSC Differential Phase Error



2062-22

Applications Information — Contd.

The circuit sums two inputs A and B, such that the sum of their respective path gains is unity, as controlled by the potentiometer. When the potentiometer's wiper is fully down, the slightly negative voltage at the Vg of the B-side EL2082 cuts off the B signal to better than 70 dB attenuation at 3.58 MHz. The A-side EL2082 is at unity gain, so the only (error) signal presented to the op-amp's -input is the same (error) signal at the I_{IN} of the A-side EL2082. The circuit thus outputs $-A_{IN}$. Since the error signal required by the op-amp is very small, even at video frequencies, the current through the A-side EL2082 is small and distortion is minimized.

At 50% potentiometer setting, equal error output signals flow from the EL2082's, since the op-amp still requires little net -input current. The EL2082's essentially buck each other to establish an output, and 50% gain occurs for both the A and B inputs. The EL2082's now contribute distortion, but less than in previous connections. The op-amp sees a constant 1k feedback resistor regardless of potentiometer setting, so frequency response is stable for all gain settings.

A single-input gain control is implemented by simply grounding B_{IN}.

Distortion can be improved by increasing the input resistors to lower signal currents. This will lower the overall gain accordingly, but will not affect bandwidth, which is dependent upon the feedback resistors. Reducing the signal input amplitude is an analogous tactic, but the [illegible] with [illegible] noise

3

cuitry, such as the
e −0.7V to +0.7V
−0.35V to +0.35V

for 300Ω feedback

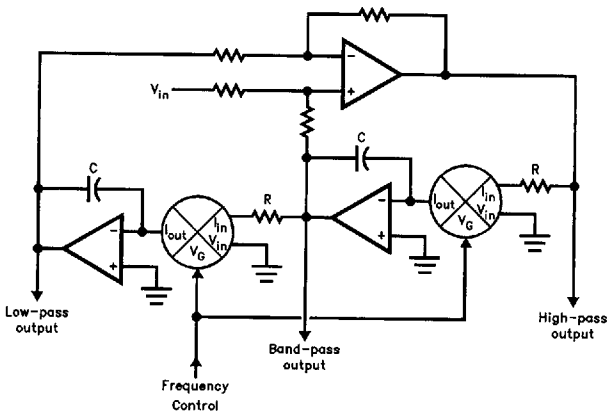
Another strategy to reduce distortion in video systems is to use DC restoration cir EL2090 ahead of the fader inputs to reduce the range of signals to be dealt with; th possible range of inputs (due to capacitor coupling) would be changed to a stabilized span.

The EL2020, EL2030, and EL2120 (at reduced bandwidth since it is compensated resistors) all give the same video performance at NTSC operation.

Variable Filters

This circuit is the familiar state-variable configuration, similar to the bi-quad:

Voltage Tuneable Bi-Quad Filter



$$F_0 = \frac{Vg}{1V}\left(\frac{1}{2\pi\,(R + 95\Omega)C}\right)$$

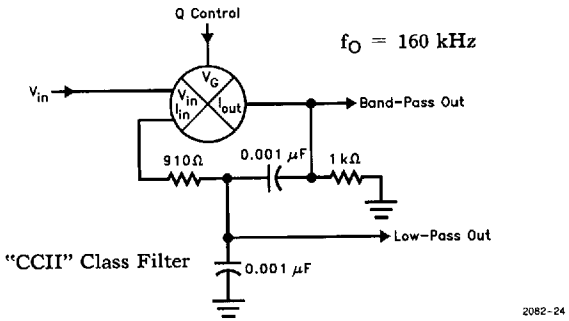
2082

EL2082C
Current-Mode Multiplier

Applications Information — Contd.

Frequency-setting resistors R are each effectively adjusted in value by an EL2082 to effect voltage-variable tuning. Two gain controls yields a linear frequency adjustment; using one gives a square-root-of-control voltage tuning. The EL2082's could be placed in series with the integrator capacitors instead to yield a tuning proportional to 1/Vg.

The next circuit is one of a new class of "CCII" filters that use the current-conveyor element. Basic information is available in the April 1991, volume 38, number 4 edition of the IEEE Transactions on Circuits and Systems journal, pages 456 through 461 of the article "The Single CCII Biquads with High-Input Impedance", by Shen-Iuan Liu and Hen-Wai Tsao.

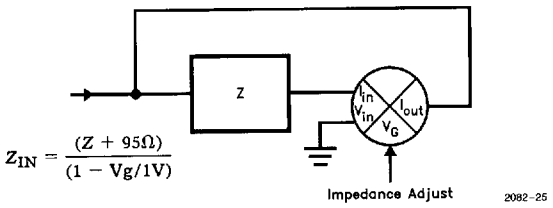


This interesting filter uses the current output of the EL2082 to generate a bandpass voltage output and the intermediate node provides a second-order low-pass filter output. Both outputs should be buffered so as not to warp characteristics, although the V_{IN} of the next EL2082 can be driven directly in the case of cascaded filters. The V_{GAIN} input acts as a Q and peaking adjust point around the nominal 1V value. The resistor at I_{OUT} could serve as the frequency trim, and Q trimmed subsequently with V_{GAIN}.

Negative Components

The following circuit converts a component or two-terminal network to a variable and even negative replica of that impedance:

Variable or Negative Impedance Converter



$$Z_{IN} = \frac{(Z + 95\Omega)}{(1 - Vg/1V)}$$

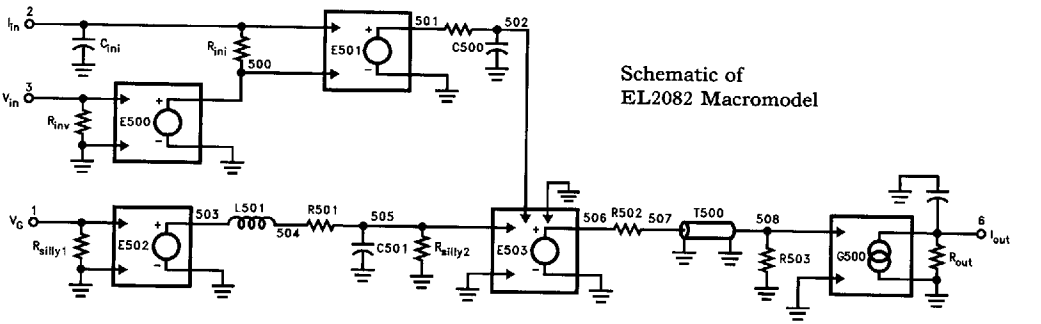
Applications Information — Contd.

A negative impedance is simply an impedance whose current flows reverse to the normal sense. In the above circuit, the current through Z is replicated by the EL2082 and inverted (I_{OUT} flows inverted to the sense of I_{IN} in the EL2082) and summed back to the input. When Vg = 0 or Vg < 0, the input impedance is simply Z + 95Ω. When Vg = 1V, the negative of the current through Z is summed with the input and the input impedance is "infinite". When Vg = 2V, twice the negative of the current through Z is summed with the input resulting in an input impedance of −Z−95Ω.

Thus variable capacitors can be simulated by substituting the capacitor as Z. "Negative" capacitors result for Vg > 1V, and capacitance needs to be present in parallel with the input to prevent oscillations. Inductors or complicated networks also work for Z, but a net negative impedance will result in oscillations.

EL2082 Macromodel

This macromodel has been designed to work with PSPICE (copywritten by the Microsim Corporation). E500 buffers in the V_{IN} voltage and presents it to the R_{INI} resistor to emulate the I_{IN} pin. E501 supplies the non-linearity of the current channel and replicates the I_{IN} current to a ground referenced voltage. R500 and C500 provide the bandwidth limitation on the current signal. E502 supplies the V_{GAIN} non-linearity and drives the L501/R501/C501 to shape the gain control frequency response. E503 does the actual gain-control multiplication, and drives delay line T500 to better simulate the actual phase characteristics of the part G500 creates the current output, and R_{OUT} with C_{OUT} provide proper output parasitics.



Schematic of EL2082 Macromodel

The model is good at frequency and linearity estimates around Vg = 1V and nominal temperatures, but has several limitations:

The Vg channel does not give zero gain for Vg < 0; the output gain reverses–don't use Vg < 0
The Vg channel is not slew limited
Frequency response does not vary with supply voltage
The V_{IN} channel is not slew limited
Noise is not modeled
Temperature effects are not modeled
CMRR and PSRR are not modeled
Frequency response does not vary with Vg

Unfortunately, the polynomial expressions and two-input multiplication may not be available on every simulator. Results have been confirmed by laboratory results in many situations with this macromodel, within its capabilities.

EL2082C
Current-Mode Multiplier

EL2082 Macromodel

```
*:                          Vgain
*                           |    Iin
*                           |    |    Vin
*                           |    |    |                   Iout
*                           |    |    |                   |
.SUBCKT EL2082macro  (1    2    3    4    5    6    7    8)
***
*** I-to-I gain cell macromodel ***
***
******
Cini 2 0 2P
C500 502 0 0.9845P
C501 505 0 1000P
Cout 6 0 5P
******
L501 503 504 0.1U
******
Rsilly1 1 0 1E9
Rsilly2 505 0 1E9
Rini 2 500 95
Rinv 3 0 2Meg
Rout 6 0 1Meg
R500 501 502 1000
R501 504 505 5
R502 506 507 50
R503 508 0 50
******
E500 500 0 3 0 1
E501 501 0 POLY(1) (2,500) 0 2  0 -.8
E502 503 0 POLY(1) (1,0) 0 1.05 -.05
E503 506 0 POLY(2) (505,0) (502,0) 0 0 0 0 1
G500 6 0 508 0 -0.0105
T500 508 0 507 0 Z0=50 TD=1.95N
******
.ENDS
```

Soldering Packages to PC Boards

DIP Packages

Wave soldering is recommended for DIP packages. Solder plated boards are recommended. Rosin mildly activated (RMA) flux is needed. Wave soldering using a dual wave system at 250°C ±10°C for two seconds per wave is preferable. Thorough cleaning of boards after soldering is required.

Hand soldering, Elantec's DIP packages will survive a peak temperature of 300°C (at leads) for a maximum period of 10 seconds.

Surface Mount Packages

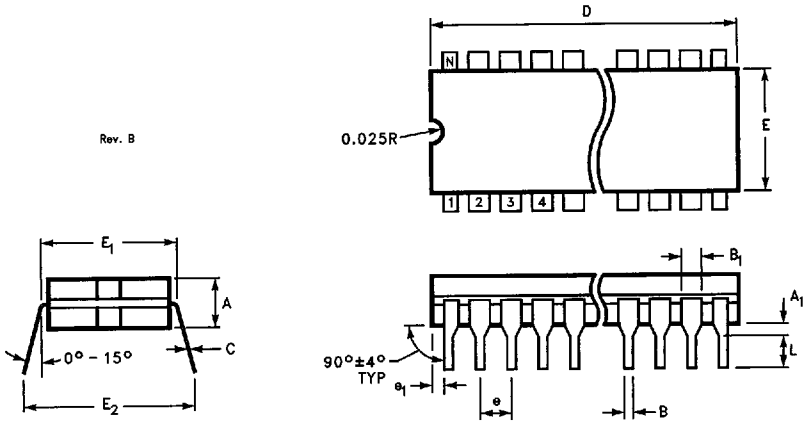
Wave soldering and vapor phase or infrared (IR) reflow can be used for soldering surface mount packages to PC boards. Solder plated boards are recommended for wave soldering and vapor phase or IR reflow methods.

Wave Soldering: Adhesive is used to hold components on the boards during wave soldering. Place components on the board and cure adhesive before wave soldering. Rosin mildly activated (RMA) flux or organic flux is needed. Wave soldering using a dual wave system at 250°C ±10°C for a maximum of two seconds per wave is preferable. Thorough cleaning of boards after soldering is required.

Reflow Soldering: Screen solder paste on board and attach components to board. Solder paste with RMA flux is recommended. Bake boards at 65°C–90°C for 15 minutes. Preheat boards to within 60°C–70°C of the solder temperature. To reflow solder paste with vapor phase method, the solder paste temperature must be maintained at or above 200°C for at least 30 seconds. The components temperature can not exceed 215°C. For the IR reflow method, the solder paste temperature must be maintained at or above 200°C for at least 30 seconds. The components temperature can not exceed 220°C. The temperature/time ramp-up during vapor phase or IR reflow shall be no greater than 2°C/sec.

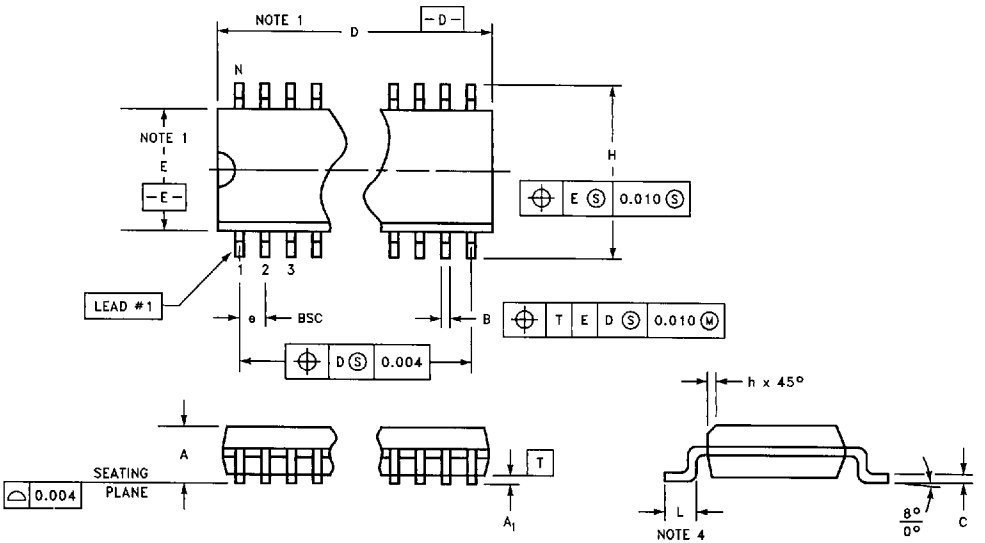
Hand soldering, Elantec's surface mount packages will survive a peak temperature of 260°C (at leads) for a maximum period of 10 seconds.

Package Outlines



MDP0016 Rev. B
CerDIP Package
Lead Finish (Coml)—Tin Plate or Hot Solder DIP
Lead Finish (Mil)—Hot Solder DIP

Common Dimensions	Min	Max	Min	Max	Min	Max	Min	Max
A	0.140	0.160	0.140	0.160	0.140	0.160	0.140	0.160
A_1	0.115	0.055	0.020	0.050	0.015	0.060	0.020	0.050
B	0.016	0.023	0.016	0.021	0.014	0.026	0.016	0.021
B_1	0.050	0.065	0.050	0.060	0.038	0.068	0.050	0.060
C	0.008	0.012	0.008	0.012	0.008	0.018	0.008	0.012
D	0.375	0.395	0.760	0.785	0.940	0.960	1040.925	1.060
E	0.245	0.265	0.220	0.291	0.220	0.310	0.2780	0.298
E_1	0.300	0.320	0.300	0.320	0.290	0.320	0.300	0.320
E_2	0.340	0.390	0.340	0.390	0.360	0.410	0.340	0.390
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
e_1	0.020	0.055	0.078	0.098	0.068	0.098	0.078	0.098
L	0.125	0.150	0.125	0.150	0.125	0.150	0.130	0.150
N	8-Lead		14-Lead		18-Lead		20-Lead	



REV. C

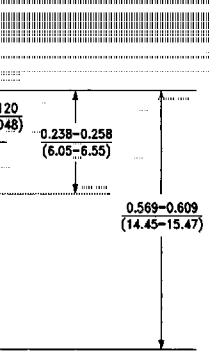
12

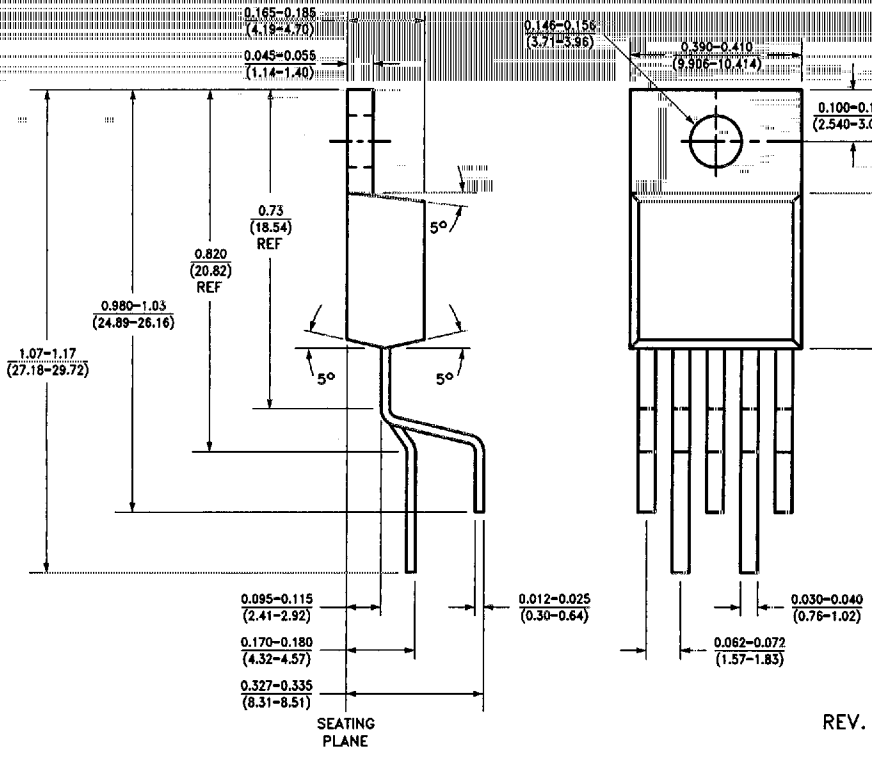
Note 1: These dimensions do not include mold flash or protrusions. Mold flash protrusion shall not exceed .006" on any side.
Note 2: SO-8, SO-14, S0-16 packages are narrow body (0.150").
Note 3: Dimensions and tolerancing per ANSI Y14.5M-1982.
Note 4: Flat area of lead foot.
Note 5: SOL-24T2 (thermal package) has 2 fused leads on each side of package.
Note 6: SOL-20T (thermal package) has 4 fused leads on each side of package.
Note 7: SOL-28T contains a thermal metal slug.

MDP0027 Rev. C
Package Outline—SOIC
Lead Finish—Solder Plate

Symbol	Lead Count													
	SOL-28		SOL-20		SOL-16		SO-16		SO-14		SO-8		SOL-24	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.061	0.068	0.061	0.068	0.061	0.068	0.096	0.104
A_1	0.004	0.011	0.004	0.011	0.004	0.011	0.004	0.010	0.004	0.010	0.004	0.010	0.004	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.008	0.010	0.008	0.010
D	0.696	0.712	0.498	0.510	0.397	0.430	0.386	0.394	0.337	0.344	0.189	0.196	0.598	0.614
E	0.291	0.299	0.291	0.299	0.291	0.299	0.150	0.157	0.150	0.157	0.150	0.157	0.291	0.299
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050	BSC	0.050 BSC		0.050 BSC	
H	0.398	0.414	0.398	0.414	0.398	0.414	0.230	0.244	0.230	0.244	0.230	0.244	0.398	0.414
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024

PACKAGE OU

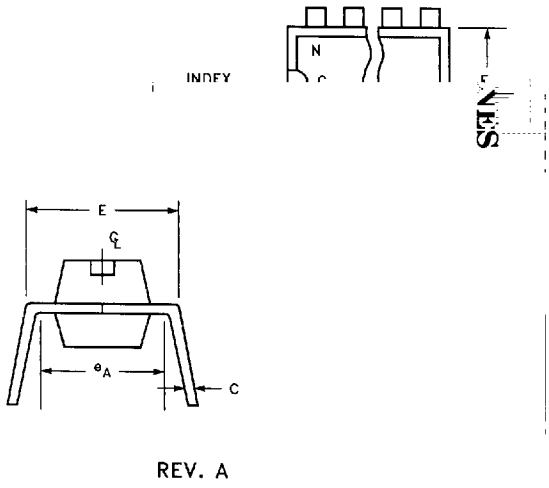


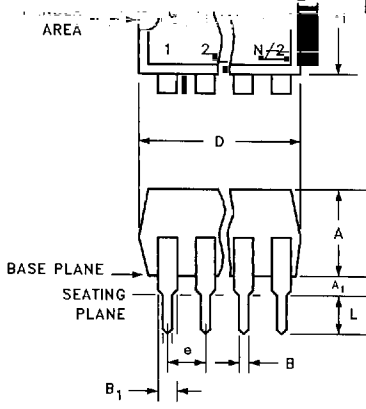


A

REV.

MDP0028 Rev. A
5-Lead TO-220
Lead Finish—Solder Plate





Rev. A
ackage
ot Solder DIP

12

MDP0031
Plastic Pa
Lead Finish—Ho

Min	Max	Min	Max	Min	Max
0.020	0.040	0.020	0.040	0.020	0.040
0.125	0.145	0.125	0.145	0.125	0.145
0.016	0.020	0.016	0.020	0.015	0.021
0.050	0.070	0.050	0.070	0.050	0.070
0.008	0.012	0.008	0.012	0.008	0.012
0.745	0.755	0.875	0.905	0.925	1.045
0.295	0.320	0.295	0.320	0.295	0.320
0.245	0.255	0.245	0.255	0.245	0.255
0.100 Typ		0.100 Typ		0.100 Typ	
ef	0.300 Ref		0.300 Ref		0.300 Ref
0.135	0.115	0.135	0.115	0.135	0.115	0.135
	16		18		20

Mold flash protrusion shall not exceed 0.006" on any side.

Common Dimensions	Min	Max	Min	Max
A_1	0.020	0.040	0.020	0.040
A	0.125	0.145	0.125	0.145
B	0.016	0.020	0.016	0.020
B_1	0.050	0.070	0.050	0.070
C	0.008	0.012	0.008	0.012
D	0.350	0.385	0.745	0.755
E	0.295	0.320	0.295	0.320
E_1	0.245	0.255	0.245	0.255
e	0.100 Typ		0.100 Typ	
e_A	0.300 Ref		0.300 Re	
L	0.115	0.135	0.115	
N	8		14	

Note: Package outline exclusive of any mold flashes. M