HDJD-J822-SCR00

Color Management System Feedback Controller

AVAGO TECHNOLOGIES

Data Sheet

Description

The HDJD-J822 is a CMOS mixed-signal IC designed to be the optical feedback controller of an LED-based lighting system. A typical system consists of an array of red, green and blue LEDs, LED drivers, a tri-color photosensor that samples the light output, and the HDJD-J822. The IC interfaces directly to the photosensor, processes the color information and adjusts the light output from the LEDs until the desired color is achieved. To achieve this, the IC integrates a high-accuracy 10-bit analog-to-digital converter front-end, a color data processing logic core, and a high-resolution 12-bit PWM output generator.

By employing a feedback system and the HDJD-J822, the light output produced by the LED array maintains its color over time and temperature. In addition, the desired color can be specified using a standard CIE color space.

In addition, by incorporating a standard I^2C serial interface, specifying the color of the LED array's light output is as simple as picking the color coordinates from the CIE color space and writing several bytes of data to the device.

The output PWM signals are connected directly to the LED drivers as enable signals. The PWM signals control the on-time duration of the red, green and blue LEDs. That duration is continually adjusted in real-time to match the light output from the LED array to the specified, desired color.

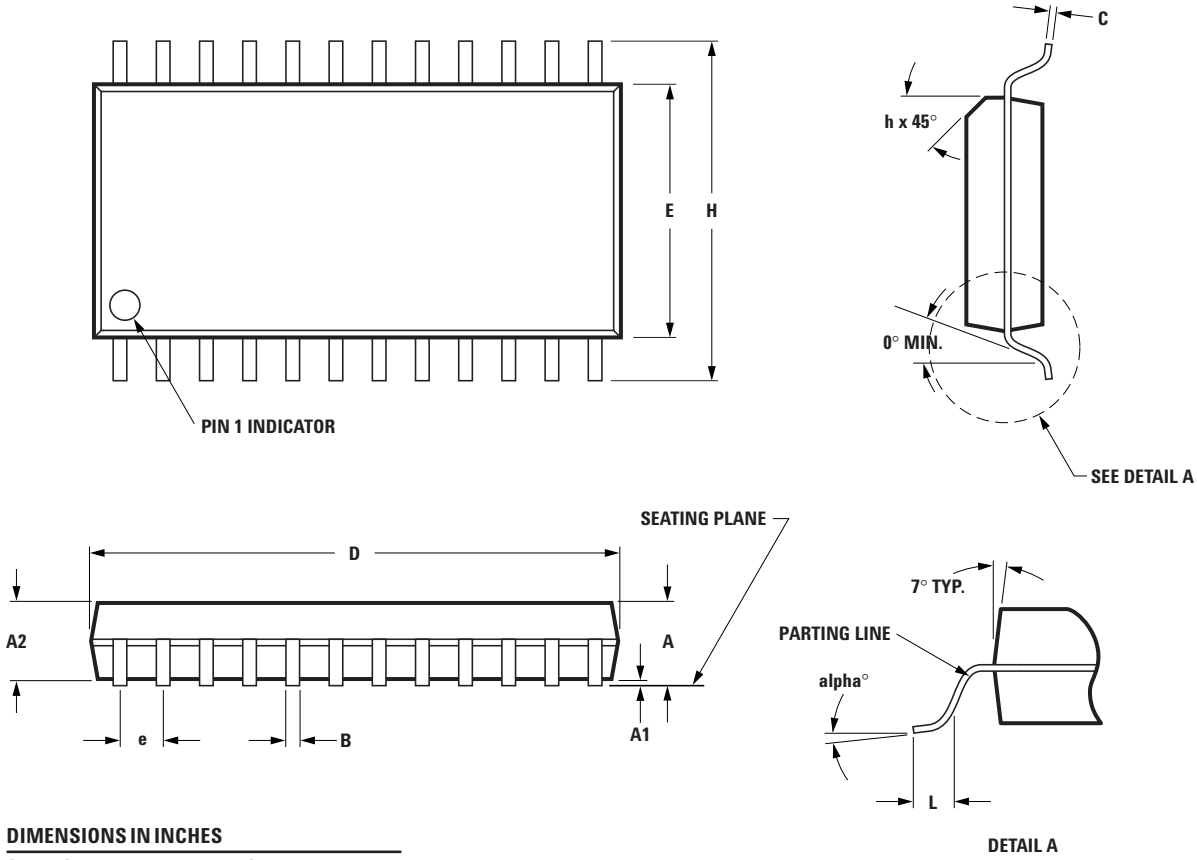
Features

- –40 to 85°C operation
- I^2C serial interface
- Robust CMOS-Schmitt input
- CMOS/TTL compatible output
- Multiple color input formats
  - CIE XYZ, Yxy, Yu'v' and RGB
- 3-channel analog interface to color sensor
  - X, Y and Z channels
- 3-channel 12-bit PWM output
  - Red, Green, and Blue LED channels
- Internal computation of calibration data
- Internal clock generator
- Internal reference voltage generator
- Error flag output
- External push-button interface
- Only passive components required externally

Applications

- Backlighting
- General illumination
- Mood/accent lighting
- Color context sensitive appliances

Package Dimensions



DIMENSIONS IN INCHES

SYMBOL	MIN.	NOM.	MAX.
A	0.093	0.099	0.104
A1	0.004	0.008	0.012
A2	0.088	0.094	0.100
B	0.013	0.016	0.020
C	0.0090	0.0100	0.0125
D	0.599	0.606	0.613
E	0.292	0.296	0.299
e		0.050 BSC.	
H	0.394	0.402	0.419
h	0.010	0.015	0.019
L	0.016	0.033	0.050
alpha	0°	5°	8°

Part Numbering System

HDJD - J822 - XX X XX

Option
00: Default

Packaging Type
R: Tape and Reel Standard Pack

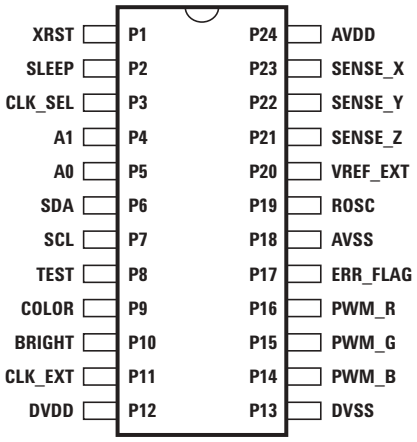
Product Packaging
SC: SOIC

Pinout of HDJD-J822 Color Management System Feedback Controller

Pin	Name	Type
1	XRST	DI
2	SLEEP	DI
3	CLK_SEL	DI
4	A1	DI
5	A0	DI
6	SDA	DIO
7	SCL	DI
8	TEST	DI
9	COLOR	DI
10	BRIGHT	DI
11	CLK_EXT	DI
12	DVDD	DP
13	DVSS	DP
14	PWM_B	DO
15	PWM_G	DO
16	PWM_R	DO
17	ERR_FLAG	DO
18	AVSS	AP
19	ROSC	ANA
20	VREF_EXT	ANA
21	SENSE_Z	ANA
22	SENSE_Y	ANA
23	SENSE_X	ANA
24	AVDD	AP

Legend

DI	Digital input pin
DO	Digital output pin
DIO	Digital bi-directional pin
DP	Digital supply/ground pin
ANA	Analog interface pin
AP	Analog supply/ground pin



Top View
24-Pin SOIC

Pin Descriptions

XRST (Pin 1)

Global, asynchronous, active-low system reset. When asserted low, XRST resets all registers. Minimum reset pulse low is 10 µs and must be provided by external circuitry.

SLEEP (Pin 2)

When asserted high, SLEEP puts the device into sleep mode. In sleep mode, all analog circuits are powered down and the clock signal is gated away from the core logic.

CLK_SEL (Pin 3)

CLK_SEL is used to select between internal and external clock modes. Internal clock mode is selected when CLK_SEL=0 and external clock mode is selected when CLK_SEL=1.

A1, A0 (Pin 4, Pin 5)

A1 (MSB) and A0 (LSB) define the lower two bits of the I^2C slave address.

SDA (Pin 6)

The SDA pin is the I^2C data I/O pin. SDA is a bi-directional pin. The I/O direction is defined by an internal signal generated by the I^2C interface block.

SCL (Pin 7)

The SCL pin is the I^2C clock pin.

TEST (Pin 8)

Connect to digital ground (DVSS).

COLOR, BRIGHT (Pin 9, Pin 10)

COLOR and BRIGHT are button interface pins. Asserting COLOR high with BRIGHT low makes the output color go up a color selection 'slider.' To effect a direction change, COLOR and BRIGHT must be asserted simultaneously for at least 0.1 second. Now, asserting COLOR with BRIGHT low makes the output color go down the color selection slider.

Button brightness control follows a similar procedure. Asserting BRIGHT high with COLOR low increases or decreases brightness depending on the direction. To effect a direction change, COLOR and BRIGHT must be asserted simultaneously for at least 0.1 second. *(*Refer to *Application Note 5070* for color selection 'slider.'*)*

CLK_EXT (Pin 11)

CLK_EXT is the external clock input pin. Users can choose to use an external clock instead of the internal clock generator by setting CLK_SEL to high.

PWM_R, PWM_G, PWM_B (Pin 16, Pin 15, Pin 14)

The PWM_R, PWM_G, and PWM_B output pins drive the external LED drivers that drive the LED arrays. Typically PWM_R drives only the red LEDs, PWM_G drives only the green LEDs and PWM_B drives only the blue LEDs. They are the output enable signals of the red, green and blue LED drivers. So, they control the on-time duration of the LEDs.

The assertion level of the PWM* signals can be toggled by the user to support both active-low and active-high enable input pins at the LED driver side. This is done by configuring the PWML bit of register CONFIG1.

ERR_FLAG (Pin 17)

The ERR_FLAG pin is asserted high when an error condition is detected. The user can determine the type of error by reading the ERROR register. The error conditions are described in the 'High Level Description' section.

SENSE_X, SENSE_Y, SENSE_Z (Pin 23, Pin 22, Pin 21)

The SENSE_X, SENSE_Y and SENSE_Z pins are analog input pins which are tied to the X-channel, Y-channel and Z-channel of the photosensor output respectively. An averaging filter is placed in between the sensor output and the SENSE_X, SENSE_Y and SENSE_Z pins. The filter is typically a 68 kΩ -1 µF single-pole low-pass filter.

VREF_EXT (Pin 20)

The VREF_EXT pin is an analog input pin, which provides an external reference voltage for the ADC. Typically, users will use the internal reference generator to operate the ADC. However, in specific application conditions, an external reference may be required. The external reference is enabled by setting the VREFS bit of register CONFIG1 high.

ROSC (Pin 19)

A 68 kΩ precision 1% resistor is connected from the ROSC to AVSS pin for use by the internal oscillator. In external clock mode, ROSC can be left floating. (Refer to *Application Note 5070* for resistor selection.)

DVDD, DVSS, AVDD, AVSS (Pin 12, Pin 13, Pin 24, Pin 18)

HDJD-J822 has separate power ground nets for the analog and digital section. A star connection from a central power source is recommended when designing the wiring to these supply pins.

DVDD = Digital positive supply

DVSS = Digital ground

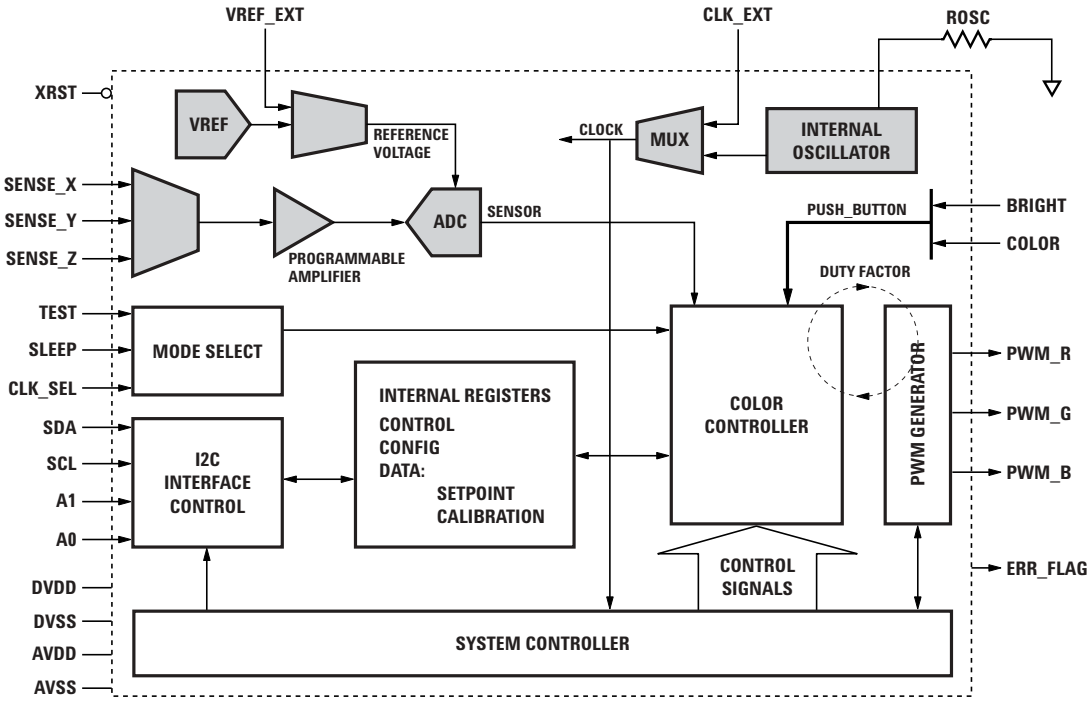
AVDD = Analog positive supply

AVSS = Analog ground

General Specifications

Feature	Value
Interface	I^2C 100 kHz
Input Color Format	CIE XYZ, Yxy, Yu'v' and RGB (illuminant E)
Input Sensor Signal	0 to 2.5 V (typical configuration)
Minimum Dynamic Range	Sensor output > 500 (ADC output code, each channel) during calibration
Output PWM Frequency	610 Hz nominal (typical configuration)
Output PWM Resolution	12 bits
Error Flag	Assertion on ERR_FLAG pin indicates an error condition
Device Address Control	Upper 5 bits 10101 binary, lower 2 bits defined by A1:A0 pins in that order
Supply	5 V digital, 5 V analog (nominal)
I/O	Schmitt-CMOS input and CMOS/TTL compatible output

Block Diagram



HDJD-J822 Block Diagram Description

Function	Description
Programmable Amplifier	If the sensor output is not within the required dynamic range, the amplifier's gain can be changed from unity to 2 to boost the sensor signal.
ADC	Analog-to-digital converter. Converts the sensor signal from analog to digital.
VREF	Reference voltage generator. Provides a stable voltage level to the ADC. Can be bypassed with anexternal reference generator.
Internal Oscillator	Generates a clock signal for the logic circuits. Can be bypassed with an external clock signal.
Mode Select	The device operation mode (normal, sleep, internal/external clock) is determined by the status of the SLEEP and CLK_SEL pins.
I^2C Interface Control	Serial interface controller. Manages the I^2C communications protocol.
Internal Registers	The primary method in which the device is configured. Contains a bank of registers. Each bit is mapped to a specification, function or mode of operation. The internal registers also contain a range of calibration registers. (Refer to the 'High Level Description' section and the *Application Note 5070* for calibration procedures).
Color Controller	Contains the color processing algorithms that operate on the sensor data. The algorithms correct the PWM output duty factors if there is a mismatch between the desired color and actual color produced. Converts the input color coordinates into an internally understood format. Default input format is CIE RGB (illuminant E).
PWM Generator	Receives the duty factor values from the Color Controller and generates 3 PWM signals.
System Controller	Performs internal functions – housekeeping, interfacing between blocks, generating control signals, etc.

High Level Description

A hardware reset (by asserting XRST) should be performed before starting any operation. It is assumed that factory calibration was performed prior to deployment of HDJD-J822. Calibration is discussed at the end of this section.

The user controls and configures HDJD-J822 by programming a set of internal registers. The registers are programmed through the I^2C protocol – a standard, synchronous, serial interface. The registers define operation modes such as sensor slope, reference voltage selection, color space format, PWM assertion level, etc. Selection between internal and external clock can only be made through pin setup.

A typical set-up would be:

- Positive sensor slope
- Internal reference voltage
- 100 Hz (nominal) sensor sample rate
- 610 Hz PWM (nominal)
- Active-high PWM output
- 2.5 MHz (nominal) internal oscillator

HDJD-J822 resets into an "idle" mode and the PWM outputs are held low.

If the PWM assertion level bit (PWML) of register CONFIG1 is changed to high, the PWM outputs will then be held high. However, since the reset condition for that register bit is low, HDJD-J822 always resets with the PWM outputs held low.

The next step after setting up the device is to write the calibration data to the calibration registers (address **0x8A to 0xA8**). The calibration data is typically stored in an external non-volatile memory. After writing the data, the user can set the PWM enable bit (PWME) of register CTRL1 to begin normal operation.

The operation begins with the processor taking in the tri-color sensor's digitized readings from the internal ADC. That data is compared to the desired color/ brightness setting. The PWM duty factor is adjusted in response to any error signal generated by that comparison operation. The user can change the color/ brightness setting at any time by writing to the appropriate device registers (address **0xE8 to 0xED** during normal operation).

The feedback and processing operation is repeated at a rate of 100 Hz (nominal).

The PWM signal is applied to the LED drivers and controls the on-time duration of the red, green and blue LEDs.

The user can input the desired color/brightness in a variety of color formats such as CIE XYZ, Yxy, Yu'v' and RGB (illuminant E).

There are three indicators in register ERROR that monitor the status of the color management system. Refer to *Application Note 5070*.

Factory calibration is needed at a system level to create a 'snapshot' of the initial conditions of the system. The color management algorithm references the snapshot data. In effect, the calibration data trims out variation in the entire signal chain from LEDs to sensor to filter to ADC. The calibration discussion below is brief. Refer to Application Note 5070 for detailed calibration procedures.

First, the device is put into "open loop" mode by setting the OPMD bit of register CONFIG1 to high. In open loop mode, the color management algorithm is turned off.

Second, all LEDs are switched on to maximum PWM. During this, the ADC output is read out to check if the sensor output is within the dynamic range of the system i.e., 400 < pass < 800. An optional internal 2x gain **(1)** can be selected if the ADC reading is less than 400. This procedure is performed for each sensor channel.

Next, only the RED LEDs are switched on. An external camera must be set up to capture the CIE co-ordinates (preferably XYZ) of the RED LEDs. The scaled XYZ readings are then sent to the RED LED camera calibration registers (address 0xE8 to 0xED during calibration mode). Next, the GSSR bit of register CTRL2 is set to capture the sensor readings of the RED LEDs. The readings are stored in the ADC reading registers (SENSOR_ADCZ, SENSOR_ADCY, SENSOR_ADCX registers). The user must read those registers and transfer them to the RED LED sensor calibration registers (address 0xFA to 0xFF).

This is repeated for GREEN and BLUE LEDs.

The RCAL bit of register CTRL2 is then set, after which HDJD-J822 will compute the 31 bytes of calibration data :

CAL_DATA0 to CAL_DATA30 (2)

The 2 pieces of calibration data is noted as **(1)**, and **(2)** above. The user will need to read them from the device registers via I^2C and store them in an external non-volatile memory. They will have to be written to the appropriate registers prior to the start of normal operation, and should be part of the system boot-up sequence.

Electrical Specifications

Absolute Maximum Ratings (Note 1 & 2)

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{STG_ABS}	-65	150	°C	
Digital Supply Voltage, DVDD to DVSS	V_{DDD_ABS}	-0.3	6.0	V	
Analog Supply Voltage, AVDD to AVSS	V_{DDA_ABS}	-0.3	6.0	V	
Input Voltage	V_{IN_ABS}	-0.3	V_{DDD} + 0.3	V	All I/O pins
Solder Reflow Peak Temperature	T_{L_ABS}		260	°C	
Latch-Up Current	I_{L_ABS}	-100	100	mA	
Human Body Model ESD Rating	ESD_{HBM_ABS}		2	kV	All pins, human body model MIL883 Method 3015
Machine Model ESD Rating	ESD_{MM_ABS}		200	V	

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Free Air Operating Temperature	T_A	-40	25	85	°C	
Digital Supply Voltage, DVDD to DVSS	V_{DDD}	4.5	5	5.5	V	
Analog Supply Voltage, AVDD to AVSS	V_{DDA}	4.5	5	5.5	V	
HIGH Level Output Current	I_{OH}			3	mA	
LOW Level Output Current	I_{OL}			3	mA	
External Clock Frequency	f_{CLK_EXT}	1.8	2.5	3.3	MHz	
ROSC Resistor	R_{osc}		68		kΩ	(Note 3)
VREF_EXT Analog Input Pin Input Voltage	V_{REF_EXT}	2.5		4.0	V	
SENSE_* Input Pins Input Voltage	V_{SENSE}	0.0		V_{REF}	V	(Note 4)
VDDD or VDDA Minus SENSE_*	V_{DIFF_SENSE}	1.0			V	(Note 5)
Internal Reference Nominal Voltage	V_{REF_INT}	2.45	2.5	2.55	V	(Note 6)
Internal Oscillator Nominal Frequency with R_{osc} = 68 kΩ	f_{CLK_INT}	1.8	2.5	3.3	MHz	(Note 6)
Internal Oscillator Frequency Variation over Temperature with R_{osc} = 68 kΩ		-5		5	%	

DC Electrical Specifications

Over Recommended free air Operating Temperature Range, and $V_{DDD} = V_{DDA} = 4.5\ V/5\ V/5.5\ V$ (unless otherwise specified).

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Minimum HIGH Level Input Voltage (Note 7)	V_{IH}		0.7 V_{DDD}		V_{DDD}	V
Maximum LOW Level Input Voltage (Note 7)	V_{IL}		0		0.3 V_{DDD}	V
Digital Input Pin Schmitt +ve Threshold (Note 7)	V_{IPOS}				0.8 V_{DDD}	V
Digital Input Pin Schmitt -ve Threshold (Note 7)	V_{INEG}		0.2 V_{DDD}			V
Digital Input Pin Schmitt Hysteresis (Note 7) (Note 8)	V_{IHYS}		1.0			V
Minimum HIGH Level Output Voltage (Note 9)	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = 3$ mA	0.9 V_{DDD}		V_{DDD}	V
Maximum LOW Level Output Voltage (Note 10)	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 3$ mA	0		0.4	V
Dynamic Digital Supply Current (Note 11)	I_{DDD_DYN}	CLK_SEL=1 $f_{CLK\_EXT} = 3.3$ MHz			4	mA
Sleep-Mode Digital Supply Current	I_{DDD_SLP}				15	µA
Standby Digital Supply Current	I_{DDD_STNBY}	CLK_SEL=1			15	µA
Dynamic Analog Supply Current (Note 11)	I_{DDA_DYN}	CLK_SEL=1 $f_{CLK\_EXT} = 3.3$ MHz			3	mA
Sleep-mode Analog Supply Current	I_{DDA_SLP}				15	µA
Standby Analog Supply Current	I_{DDA_STNBY}	CLK_SEL=1			15	µA

I²C Timing (SDA, SCL)

Symbol	Parameter	Min.	Max.	Units
f_{scl}	SCL clock frequency	0	100	kHz
$t_{HD:STA}$	(Repeated) START condition hold time	4.0	-	µs
$t_{HD:DAT}$	Data hold time	0 (note 12)	3.45	µs
t_{LOW}	SCL clock low period	4.7	-	µs
t_{HIGH}	SCL clock high period	4.0	-	µs
$t_{SU:STA}$	Repeated START condition setup time	4.7	-	µs
$t_{SU:DAT}$	Data setup time	250	-	ns
$t_{SU:STO}$	STOP condition setup time	4.0	-	µs
t_{BUF}	Bus free time between START and STOP conditions	4.7	-	µs

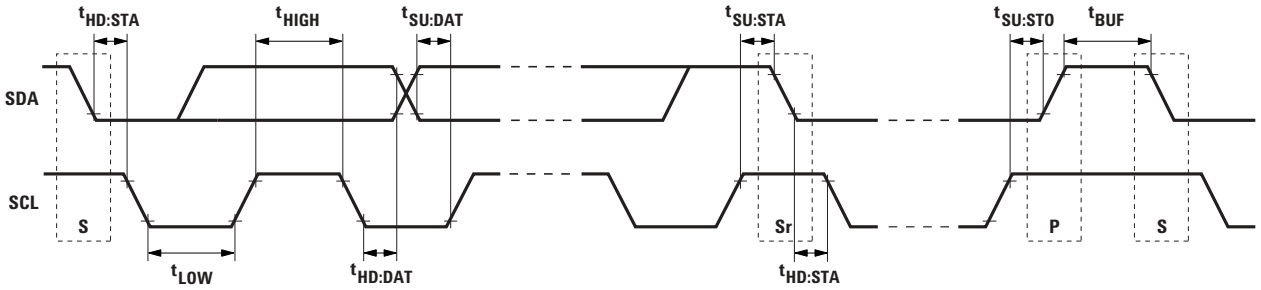


Figure 1. I²C bus timing waveforms.

Notes:

1. The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
2. Unless otherwise specified, all voltages are referenced to ground.
3. A 1% precision resistor is recommended. This resistor is tied from the ROSC pin to ground.
4. $V_{REF} = V_{REF\_INT}$ in internal reference configuration. $V_{REF} = V_{REF\_EXT}$ in external reference configuration.
5. The voltage level at any of the SENSE_* pins must be lower than V_{DDD} or V_{DDA} (whichever is lower) by at least V_{DIFF_SENSE} volts.
6. $T_A = 25°C$. Room temperature.
7. Applies to all DI pins.
8. Guaranteed by design.
9. Applies to all DO pins. SDA is an open-drain NMOS. Minimum V_{OH} depends on the pull-up resistor value.
10. Applies to all DO and DIO pins.
11. Dynamic testing is performed when the IC is operating in a mode representative of typical operation.
12. A hold time of at least 300ns must be provided internally by a device for the SDA signal (with reference to the minimum VIH of SCL) to bridge the undefined region of the falling edge of SCL.

Notes on Sampling Frequency and PWM Output Frequency

The sampling frequency, f_{SAMP}, which is the frequency at which HDJD-J822 samples the tricolor photosensor, is related to the system clock frequency, f_{CLK}. The output PWM frequency, f_{PWM}, is also related to f_{CLK}. The system clock is sourced from either the internal oscillator or an external clock.

Calculation example:

f_{CLK} = 2.5 MHz (nominal)

$f_{SAMP} = f_{CLK}/25087 = 100$ Hz (nominal)

$f_{PWM} = f_{CLK}/4095 = 610$ Hz (nominal)

The internal oscillator frequency varies from part-to-part but it will not vary significantly during operation.

Register Description

The user controls and configures HDJD-J822 by programming a set of internal registers, through the I2C protocol. Refer to Application Note 5070 for programming guide and register description.

I²C Interface

Description

The programming interface to HDJD-J822 is a standard 2-wire serial bus, which follows the I²C data transmission protocol. This protocol defines a *transmitter* as a device that sends data to the bus and a *receiver* as a device that receives data from the bus.

A *master* is a device that initiates a data transfer on the bus, generates the clock signal and terminates the data transfer. A device addressed by the master is called a *slave*. Both master and slave can act as a transmitter or a receiver but the master controls the direction for data transfer.

The bus consists of a serial clock (SCL) and a serial data (SDA) line. Both lines are bi-directional and connected to the positive power supply through a pull-up resistor. When the bus is free, both lines are HIGH.

HDJD-J822's I²C bus interface *always* operates as a slave transceiver in standard mode. Standard mode has a data transfer rate of up to 100 kbit/s.

START/STOP Condition

To begin an I²C data transfer, the master must send a unique signal to the bus called a *START* condition. This is defined as a HIGH to LOW transition on the SDA line while SCL is HIGH.

The master terminates the transfer by sending another unique signal to the bus called a *STOP* condition. This is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH.

The bus is considered to be busy after a START (S) condition. It will be considered free a certain time after the STOP (P) condition. The bus stays busy if a repeated START (Sr) is sent instead of a STOP condition.

The START and repeated START conditions are functionally identical.

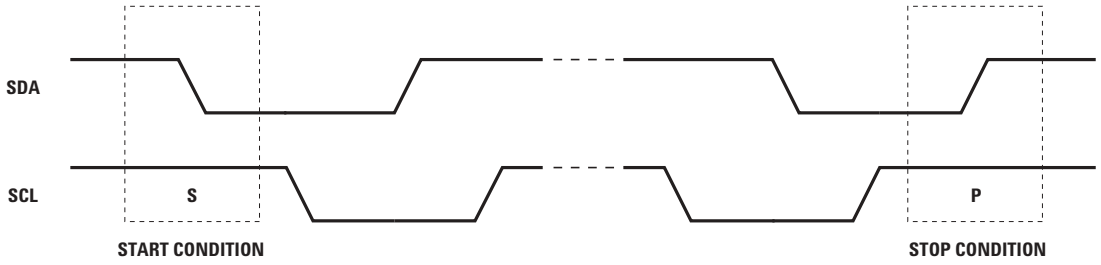


Figure 2. START/STOP condition.

Data Transfer

The master initiates data transfer after a START condition. Data is transferred in bits with the master generating one clock pulse for each bit sent. For a data bit to be valid, the SDA data line must be stable during the HIGH period of the SCL clock line. Only during the LOW period of the SCL clock line can the SDA data line change state to either HIGH or LOW.

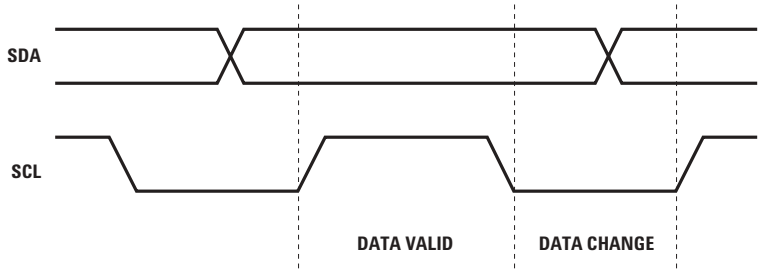


Figure 3. Data bit transfer.

A complete data transfer is 8-bits long or 1-byte. Each byte is sent most significant bit (MSB) first followed by an acknowledge or not acknowledge bit. Each data transfer can send an unlimited number of bytes.

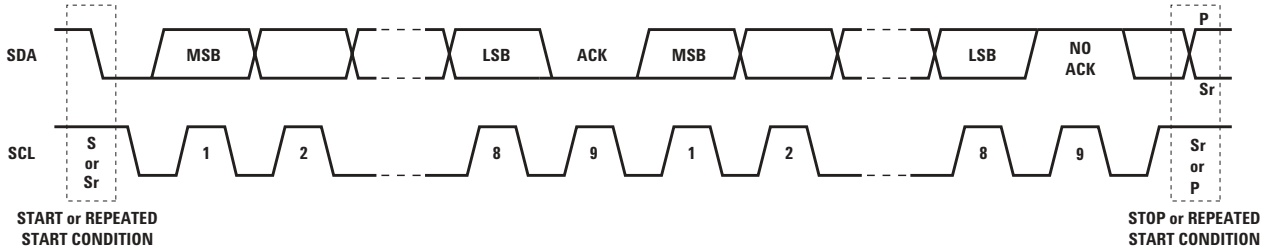


Figure 4. Data byte transfer.

Acknowledge/Not Acknowledge

The receiver must always acknowledge each byte sent in a data transfer. In the case of the slave-receiver and master-transmitter, if the slave-receiver does not send an acknowledge bit, the master-transmitter can either STOP the transfer or generate a repeated START to start a new transfer.

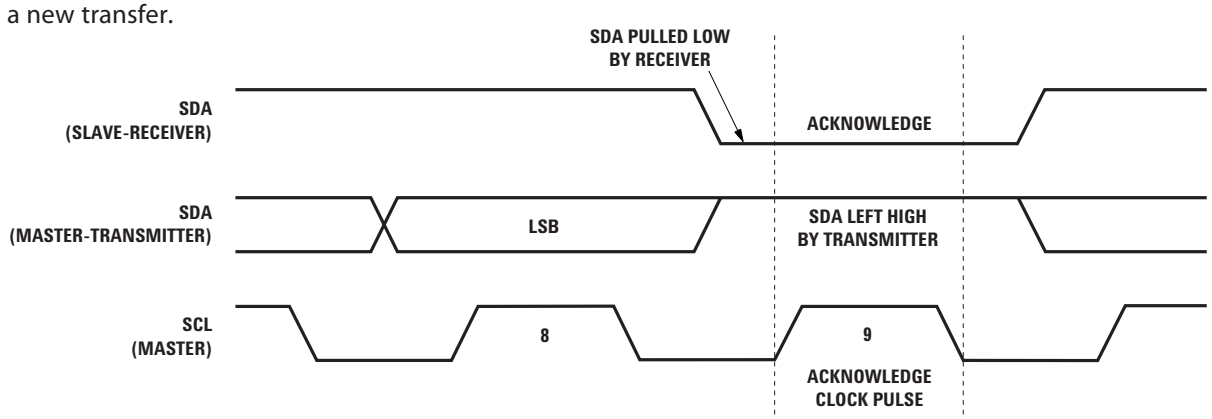


Figure 5. Slave-receiver acknowledge.

In the case of the master-receiver and slave-transmitter, the master generates a not acknowledge to signal the end of the data transfer to the slave-transmitter. The master can then send a STOP or repeated START condition to begin a new data transfer.

In all cases, the master generates the acknowledge or not acknowledge SCL clock pulse.

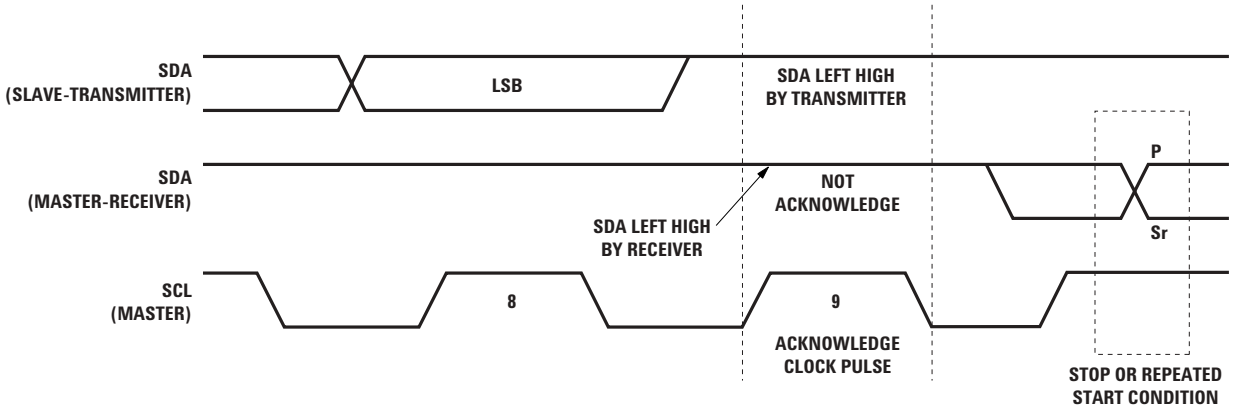


Figure 6. **Master-receiver acknowledge.**

Addressing

Each device on the I²C bus needs to have a unique address. This is the first byte that is sent by the master-transmitter after the START condition. The protocol defines the address as the first seven bits of the first byte.

The eighth bit or least significant bit (LSB) determines the direction of data transfer. A 'one' in the LSB of the first byte indicates that the master will read data from the addressed slave (master-receiver and slave-transmitter). A 'zero' in this position indicates that the master will write data to the addressed slave (master-transmitter and slave-receiver).

A device whose address matches the address sent by the master will respond with an acknowledge for the first byte and set itself up as a slave-transmitter or slave-receiver depending on the LSB of the first byte.

The slave address in HDJD-J822 is made up of a fixed part and a programmable part. The fixed part is A6 to A2 and is set as shown in Figure 7. The programmable part is A1 and A0, which is set by external package pins. The programmable address pins allows a maximum of four HDJD-J822 chips on the same I²C bus to be addressed (address range from 54h to 57h).

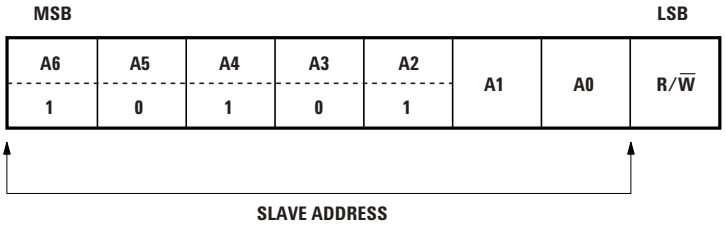


Figure 7**. Slave addressing.**

Data Format

HDJD-J822 uses a register-based programming architecture. Each register has a unique address and controls a specific function inside the chip.

To write to a register, the master first generates a START condition. Then it sends the slave address for the device it wants to communicate with. The least significant bit (LSB) of the slave address must indicate that the master wants to write to the slave. The addressed device will then acknowledge the master.

The master writes the register address it wants to access and waits for the slave to acknowledge. The master then writes the new register data. Once the slave acknowledges, the master generates a STOP condition to end the data transfer.

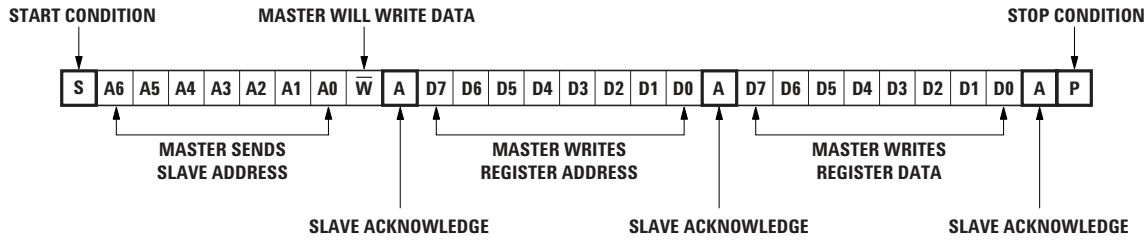


Figure 8. Register byte write protocol.

To read from a register, the master first generates a START condition. Then it sends the slave address for the device it wants to communicate with. The least significant bit (LSB) of the slave address must indicate that the master wants to write to the slave. The addressed device will then acknowledge the master.

The master writes the register address it wants to access and waits for the slave to acknowledge. The master then generates a repeated START condition and resends the slave address sent previously. The least significant bit (LSB) of the slave address must indicate that the master wants to read from the slave. The addressed device will then acknowledge the master.

The master reads the register data sent by the slave and sends a no acknowledge signal to stop reading. The master then generates a STOP condition to end the data transfer.

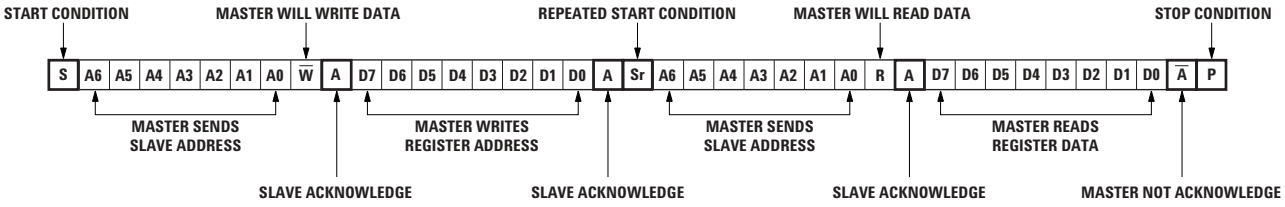
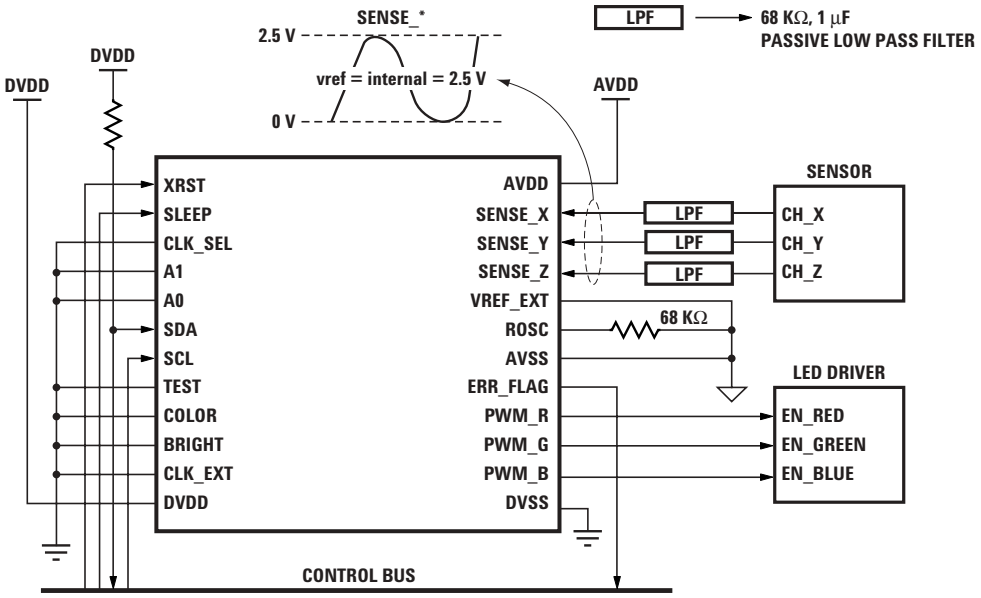
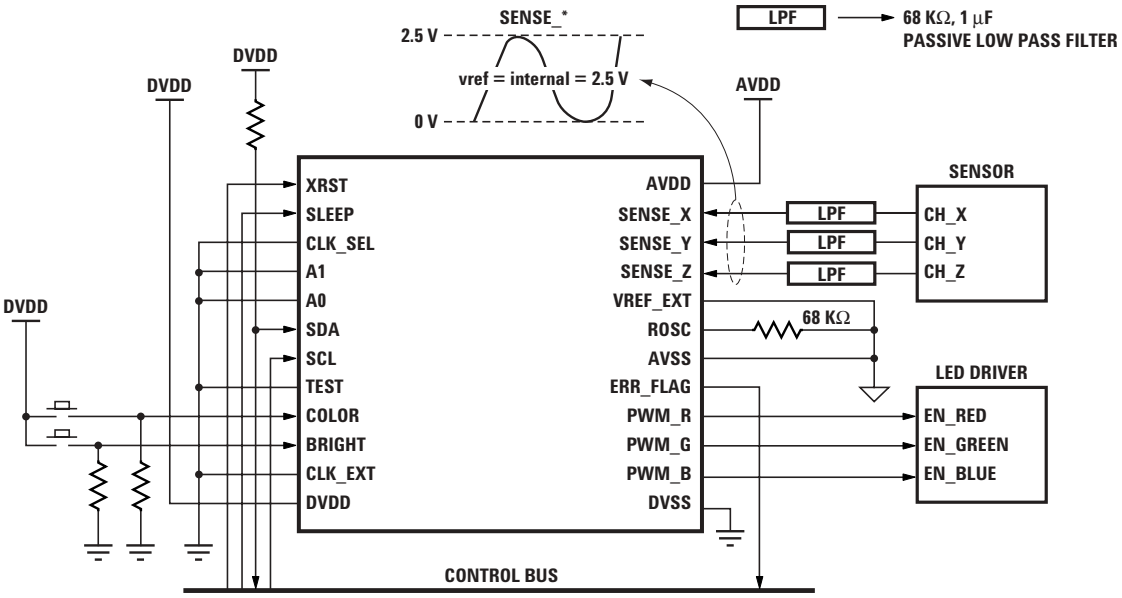


Figure 9. Register Byte Read Protocol.

Application Diagrams



Typical Operation*



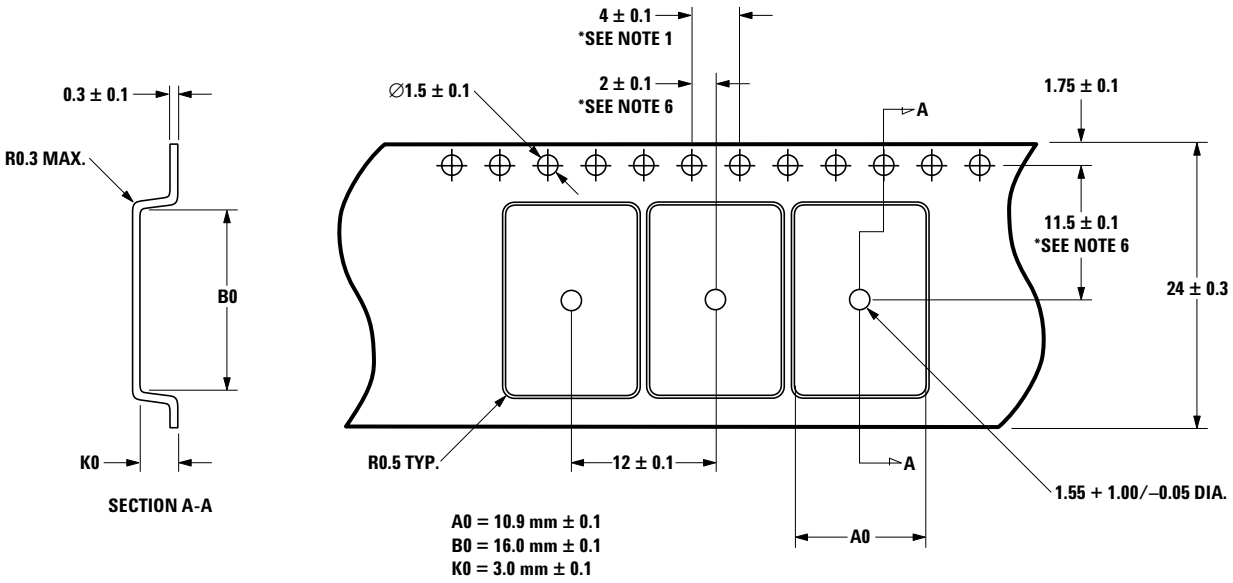
Button Mode Operation*

Refer to Application Note 5070 for implementation details.

*The SDA pull-up is only required at system level. It is shown in the diagram for reference only.

Package Tape and Reel Dimensions

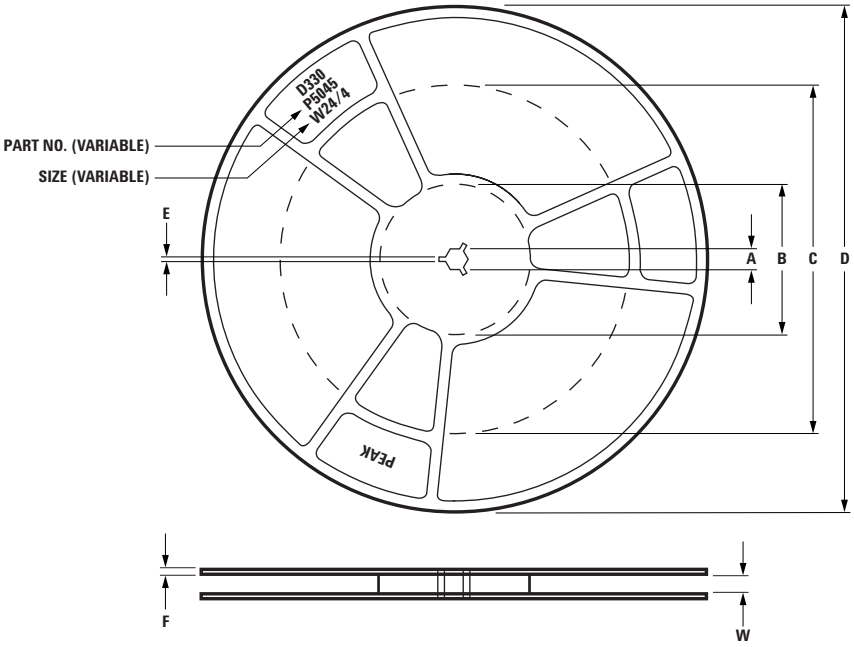
24 Pin Wide Body Carrier Tape



Notes:

1. 10 sprocket hole pitch cumulative tolerance is ± 0.2mm.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: Black Conductive Advantek Polystyrene.
4. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.
5. K0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. Dimensions are in millimeters.

Peak Fixed Reels



LEGEND
W – Width
A – Shaft Diameter
B – Hub Diameter
C – Window Size
D – Total Reel Diameter
E –Shaft Key Hole
F –Reel Thickness

Notes:
1. Material: Polystyrene (Blue).
2. Antistatic coated.
3. Flange warpage: 3 mm maximum.
4. All dimensions are in millimeters.
5. ESD – Surface resistivity: 10^5 to 10^{11} ý/sq.

W		A		B		C		D		E		F	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
24.4	26.4	12.80	13.20	98	102	225.75	226.25	326	330.25	1.95	2.45	2	2.8

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