

MC10E016, MC100E016

5.0 V ECL 8-Bit Synchronous Binary Up Counter

The MC10E/100E016 is a high-speed synchronous, presettable, cascadable 8-bit binary counter. Architecture and operation are the same as the MC10H016 in the MECL 10H™ family, extended to 8-bits, as shown in the logic symbol.

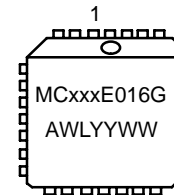
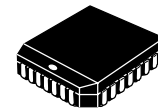
The counter features internal feedback of \overline{TC} , gated by the TCLD (terminal count load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the \overline{TC} feedback is disabled, and counting proceeds continuously, with \overline{TC} going LOW to indicate an all-one state. When TCLD is HIGH, the \overline{TC} feedback causes the counter to automatically reload upon $\overline{TC} = \text{LOW}$, thus functioning as a programmable counter. The Q_n outputs do not need to be terminated for the count function to operate properly. To minimize noise and power, unused Q outputs should be left unterminated.

The 100 series contains temperature compensation.

- 700 MHz Min. Count Frequency
- 1000 ps CLK to Q, \overline{TC}
- Internal \overline{TC} Feedback (Gated)
- 8-Bit
- Fully Synchronous Counting and \overline{TC} Generation
- Asynchronous Master Reset
- PECL Mode Operating Range: $V_{CC} = 4.2 \text{ V}$ to 5.7 V with $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0 \text{ V}$ with $V_{EE} = -4.2 \text{ V}$ to -5.7 V
- Pb-Free Packages are Available*



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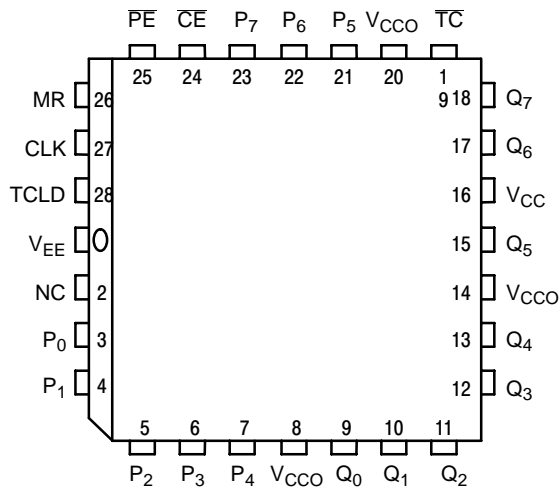


xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

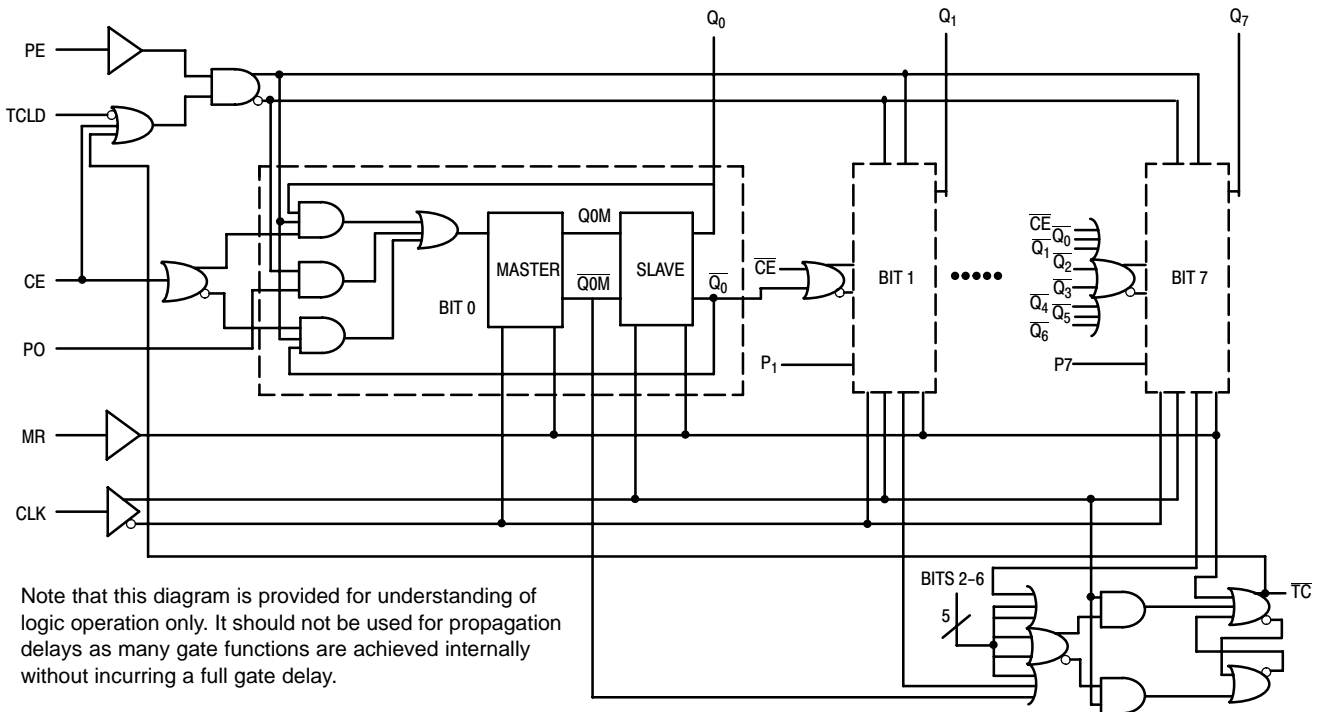
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



P0 - P7	ECL Parallel Data (Preset) Inputs
Q0 - Q7	ECL Data Outputs
CE	ECL Count Enable Control Input
PE	ECL Parallel Load Enable Control Input
MR	ECL Master Reset
CLK	ECL Clock
TC	ECL Terminal Count Output
TCLD	ECL TC-Load Control Input
NC	No Connect
VCC, VCCO	Positive Supply
VEE	Negative Supply

All VCC and VCCO pins are tied together on the die.
 Warning: All VCC, VCCO, and VEE pins must be externally connected to Power Supply to guarantee proper operation.

(Top View)



Note that this diagram is provided for understanding of logic operation only. It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

Load Parallel (P _n to Q _n)	X	L	X	L	Z
Continuous Count	L	H	L	L	Z
Count; Load Parallel on TC = LOW	L	H	H	L	Z
Hold	H	H	X	L	Z
Masters Respond, Slaves Hold	X	X	X	L	ZZ
Reset (Q _n : = LOW, TC : = HIGH)	X	X	X	H	X

Z = clock pulse (low to high);
 ZZ = clock pulse (high to low)

		-					-					
Load Count	L X L X Z	H	H	H	L	L	H	H	H	L	L	H
	H L L L Z	X	X	X	X	X	H	H	H	L	H	H
	H L L L Z	X	X	X	X	X	H	H	H	H	H	L
	H L L L Z	X	X	X	X	X	L	L	L	L	L	H
Load Hold	L X L X Z	H	H	H	L	L	H	H	H	L	L	H
	H H L X Z	X	X	X	X	X	H	H	H	L	L	H
Load On Terminal Count	H L L H Z	H	L	H	H	L	H	H	H	L	H	H
	H L L H Z	H	L	H	H	L	H	H	H	H	L	H
	H L L H Z	H	L	H	H	L	H	H	H	H	H	L
	H L L H Z	H	L	H	H	L	H	L	H	H	L	H
Reset	H L L H Z	H	L	H	H	L	H	H	L	L	L	H
	X X H X X	X	X	X	X	X	L	L	L	L	L	H

Internal Input Pulldown Resistor		50 kΩ	
Internal Input Pullup Resistor		50 kΩ	
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg	
	PLCC-28	Level 1	Level 3
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
Transistor Count	592 Devices		
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

V_{CC}	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	PLCC-28 PLCC-28	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	PLCC-28	22 to 26	°C/W
T_{sol}	Wave Solder Pb Pb-Free			265 265	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

$$V_{CCx} = 5.0\text{ V}; V_{EE} = 0.0\text{ V (Note 1)}$$

		°			°			°			
I_{EE}	Power Supply Current		151	181		151	181		151	181	mA
V_{OH}	Output HIGH Voltage (Note 2)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.

$V_{CC} = 0.0\text{ V}; V_{EE} = -5.0\text{ V}$ (Note 3)

o

$V_{CCx} = 0.0 \text{ V}; V_{EE} = -5.0 \text{ V}$ (Note 7)

		○			○			○			
I_{EE}	Power Supply Current		151	181		151	181		174	208	mA
V_{OH}	Output HIGH Voltage (Note 8)	-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
V_{OL}	Output LOW Voltage (Note 8)	-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
V_{IH}	Input HIGH Voltage	-1165	-1025	-880	-1165	-1025	-880	-1165	-1025	-880	mV
V_{IL}	Input LOW Voltage	-1810	-1645	-1475	-1810	-1645	-1475	-1810	-1645	-1475i	

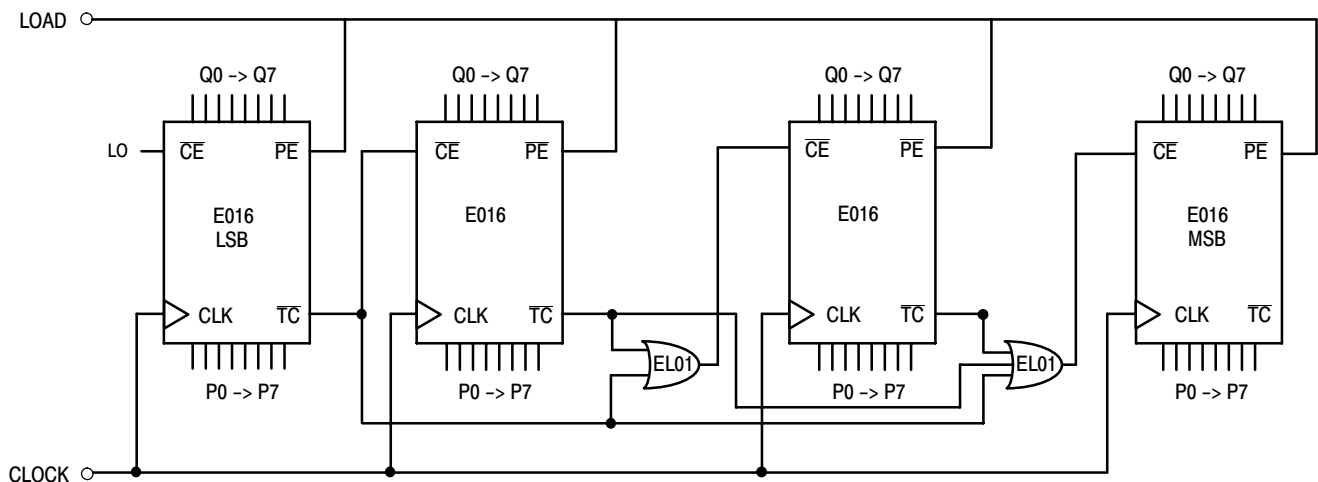
For applications which call for larger than 8-bit counters multiple E016s can be tied together to achieve very wide bit width counters. The active low terminal count (\overline{TC}) output and count enable input (\overline{CE}) greatly facilitate the cascading of E016 devices. Two E016s can be cascaded without the need for external gating, however for counters wider than 16 bits external OR gates are necessary for cascade implementations.

Figure 3 below pictorially illustrates the cascading of 4 E016s to build a 32-bit high frequency counter. Note the E101 gates used to OR the terminal count outputs of the lower order E016s to control the counting operation of the higher order bits. When the terminal count of the preceding device (or devices) goes low (the counter reaches an all 1s state) the more significant E016 is set in its count mode and will count one binary digit upon the next positive clock transition. In addition, the preceding devices will also count one bit thus sending their terminal count outputs back to a high state disabling the count operation of the more significant counters and placing them back into hold modes.

Therefore, for an E016 in the chain to count, all of the lower order terminal count outputs must be in the low state. The bit width of the counter can be increased or decreased by simply adding or subtracting E016 devices from Figure 3 and maintaining the logic pattern illustrated in the same figure.

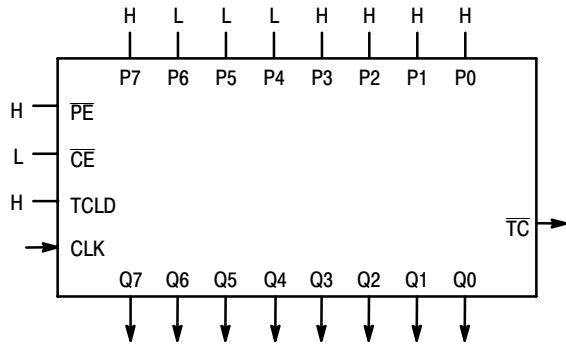
The maximum frequency of operation for the cascaded counter chain is set by the propagation delay of the \overline{TC} output and the necessary setup time of the \overline{CE} input and the propagation delay through the OR gate controlling it (for 16-bit counters the limitation is only the \overline{TC} propagation delay and the \overline{CE} setup time). Figure 3 shows EL01 gates used to control the count enable inputs, however, if the frequency of operation is lower a slower, ECL OR gate can be used. Using the worst case guarantees for these parameters from the ECLinPS data book, the maximum count frequency for a greater than 16-bit counter is 500 MHz and that for a 16-bit counter is 625 MHz.

Note that this assumes the trace delay between the \overline{TC} outputs and the \overline{CE} inputs are negligible. If this is not the case estimates of these delays need to be added to the calculations.



(continued)

The E016 has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count) when asserted reloads the data present at the parallel input pin (Pn's) upon reaching terminal count (an all 1s state on the outputs). Because this feedback is built internal to the chip, the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 4 below illustrates the input conditions necessary for utilizing the E016 as a programmable divider set up to divide by 113.



To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

$$Pn's = 256 - 113 = 8F_{16} = 1000\ 1111$$

where:

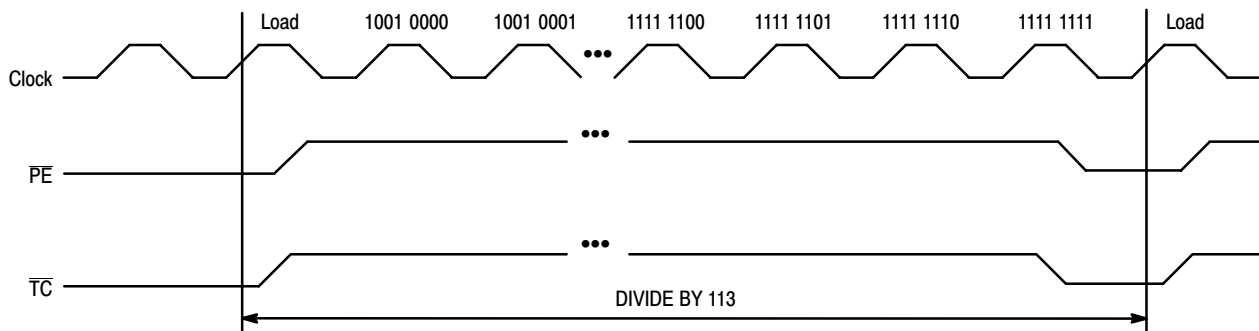
P0 = LSB and P7 = MSB

Forcing this input condition as per the setup in Figure 4 will result in the waveforms of Figure 5. Note that the \overline{TC} output is used as the divide output and the pulse duration is

equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the E016 and the \overline{TC} output can feed the clock input of a toggle flip flop to create a signal divided as desired with a 50% duty cycle.

2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
w	w	•	•	•	•	•	•	•
w	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

A single E016 can be used to divide by any ratio from 2 to 256 inclusive. If divide ratios of greater than 256 are needed multiple E016s can be cascaded in a manner similar to that already discussed. When E016s are cascaded to build larger dividers the TCLD pin will no longer provide a means for reloading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the \overline{TC} pins must be used for multiple E016 divider chains.



(continued)

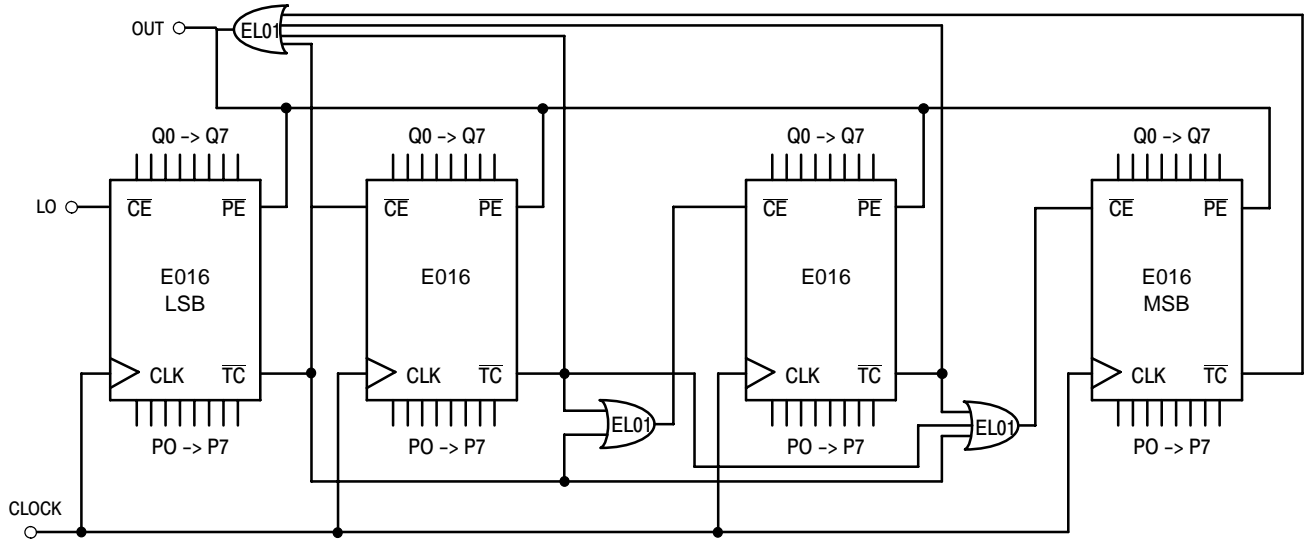
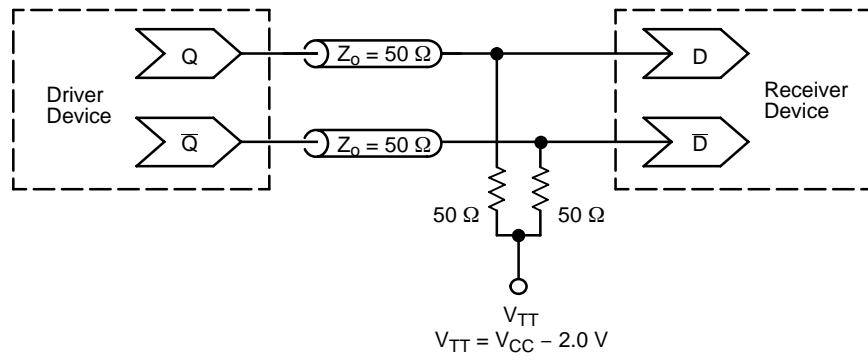


Figure 6 shows a typical block diagram of a 32-bit divider chain. Once again to maximize the frequency of operation EL01 OR gates were used. For lower frequency applications a slower OR gate could replace the EL01. Note that for a 16-bit divider the OR function feeding the \overline{PE} (program enable) input CANNOT be replaced by a wire OR tie as the \overline{TC} output of the least significant E016 must also feed the \overline{CE} input of the most significant E016. If the two \overline{TC} outputs were OR tied the cascaded count operation would not operate properly. Because in the cascaded form the \overline{PE} feedback is external and requires external gating, the maximum frequency of operation will be significantly less than the same operation in a single device.

The E016 device produces 9 fast transitioning single-ended outputs, thus V_{CC} noise can become significant in situations where all of the outputs switch simultaneously in the same direction. This V_{CC} noise can negatively impact the maximum frequency of operation of the device. Since the device does not need to have the Q outputs terminated to count properly, it is recommended that if the outputs are not going to be used in the rest of the system they should be left unterminated. In addition, if only a subset of the Q outputs are used in the system only those outputs should be terminated. Not terminating the unused outputs will not only cut down the V_{CC} noise generated but will also save in total system power dissipation. Following these guidelines will allow designers to either be more aggressive in their designs or provide them with an extra margin to the published data book specifications.

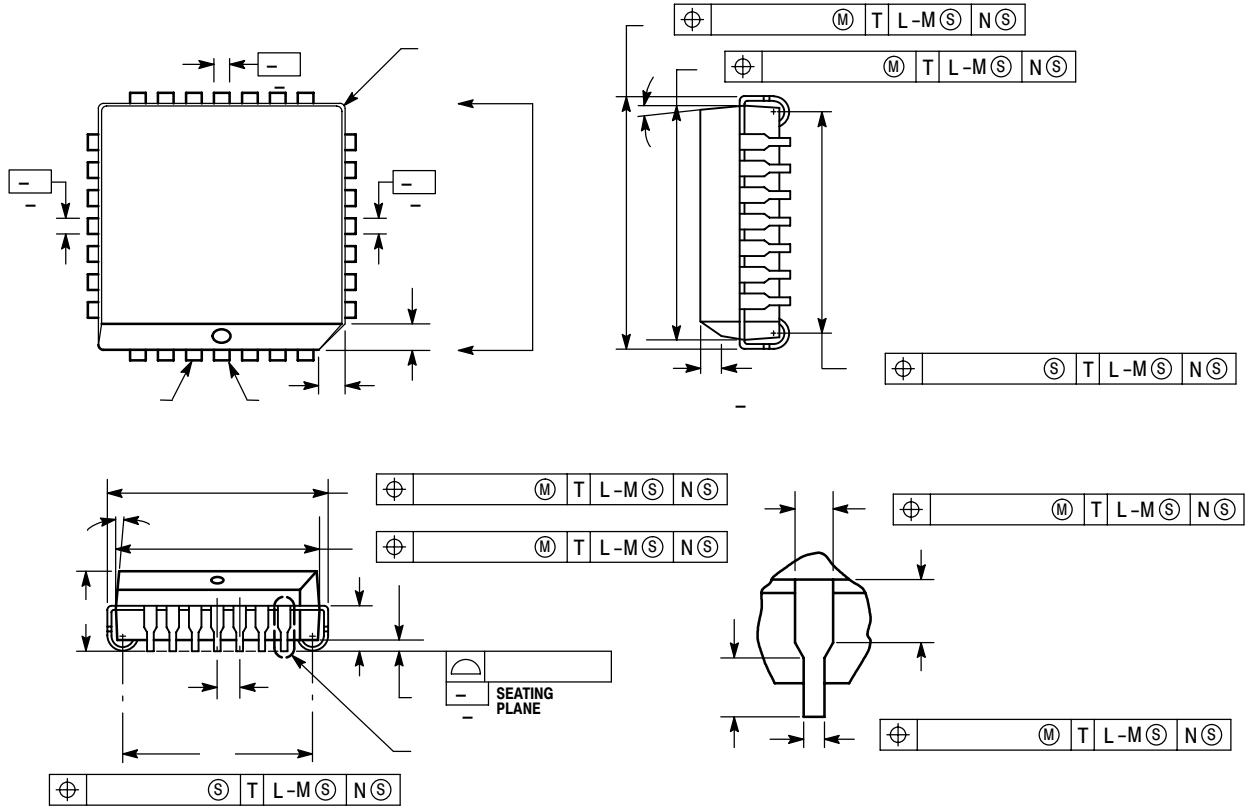


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MC10E016FN	PLCC-28	37 Units/Rail
MC10E016FNG	PLCC-28 (Pb-Free)	37 Units/Rail
MC10E016FNR2	PLCC-28	500 Units/Reel
MC10E016FNR2G	PLCC-28 (Pb-Free)	500 Units/Reel
MC100E016FN	PLCC-28	37 Units/Rail
MC100E016FNG	PLCC-28 (Pb-Free)	37 Units/Rail
MC100E016FNR2	PLCC-28	500 Units/Reel
MC100E016FNR2G	PLCC-28 (Pb-Free)	500 Units/Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E




NOTES:

1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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