STRUCTURE Silicon Monolithic Integrated Circuit
TYPE 1ch Series Regulator Driver IC
PRODUCT SERIES **BD35221EFV**
FEATURES
- High Accuracy Voltage Regulator (0.650V±1%)
- Non Rush Current on Start up (NRCS)
- Built in Super low ON resistance (28mΩtyp) Nch PowerMOSFET
- UVLO・SCP Function
- Maximum Output Current : 4A

○Absolute Maximum Ratings (Ta=25℃)

PARAMETER	SYMBOL	RATING	UNIT
Input Voltage 1	V_{CC}	+6.0 *1	V
Input Voltage 2	V_{IN}	+6.0 *1	V
Input Voltage 3	V_D	+6.0 *1	V
Enable Input Voltage	V_{EN}	-0.3～+6.0	V
Output Current	I_O	4.0 *1	A
Power Dissipation 1	Pd1	1.0 *2	W
Power Dissipation 2	Pd2	1.45 *3	W
Power Dissipation 3	Pd3	2.31 *4	W
Power Dissipation 4	Pd4	3.20 *5	W
Operating Temperature Range	Topr	-10～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Should not exceed Pd.
*2 Reduced by 8mW/℃ for each increase in Ta≧25℃ (when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 1-layer)
*3 Reduced by 11.6mW/℃ for each increase in Ta≧25℃ (when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 2-layer)
copper foil area : 15mm×15mm
*4 Reduced by 18.5mW/℃ for each increase in Ta≧25℃ (when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 2-layer)
copper foil area : 70mm×70mm
*5 Reduced by 25.6mW/℃ for each increase in Ta≧25℃ (when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 4-layer)
copper foil area : 70mm×70mm

○Operating Conditions (Ta=25℃)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Voltage 1	V_{CC}	4.3	5.5	V
Input Voltage 2	V_{IN}	1.25	V_{CC}-1 *6	V
Input Voltage 3	V_D	1.25	V_{CC}-1 *6	V
Enable Input Voltage	V_{EN}	-0.3	5.5	V

*6 VCC and VIN do not have to be implemented in the order listed.

★This product is not designed for use in radioactive environments.

Status of this document
The Japanese version of this document is the official specification.
This translated version is intended only as a reference, to aid in understanding the official version.
If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

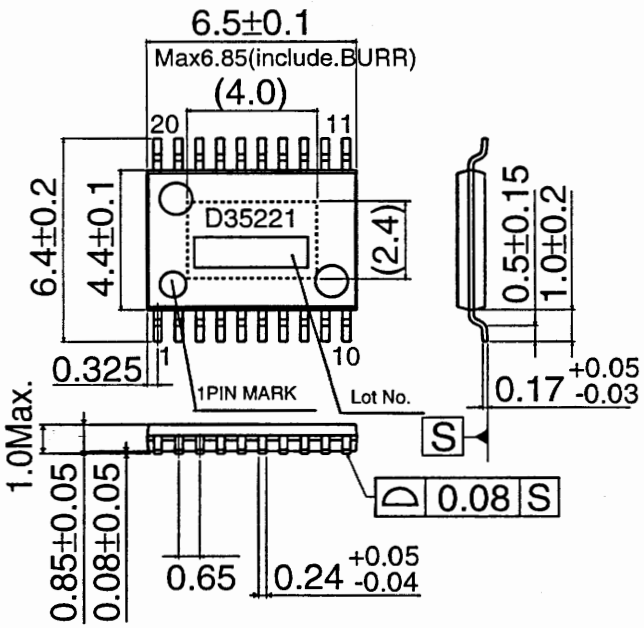
Application example
- **ROHM cannot provide adequate confirmation of patents.**
- **The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).**
  Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.
- **ROHM assumes no responsibility for use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.**

○ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃ V_{CC}=5V V_{EN}=3V V_{IN}=1.7V)

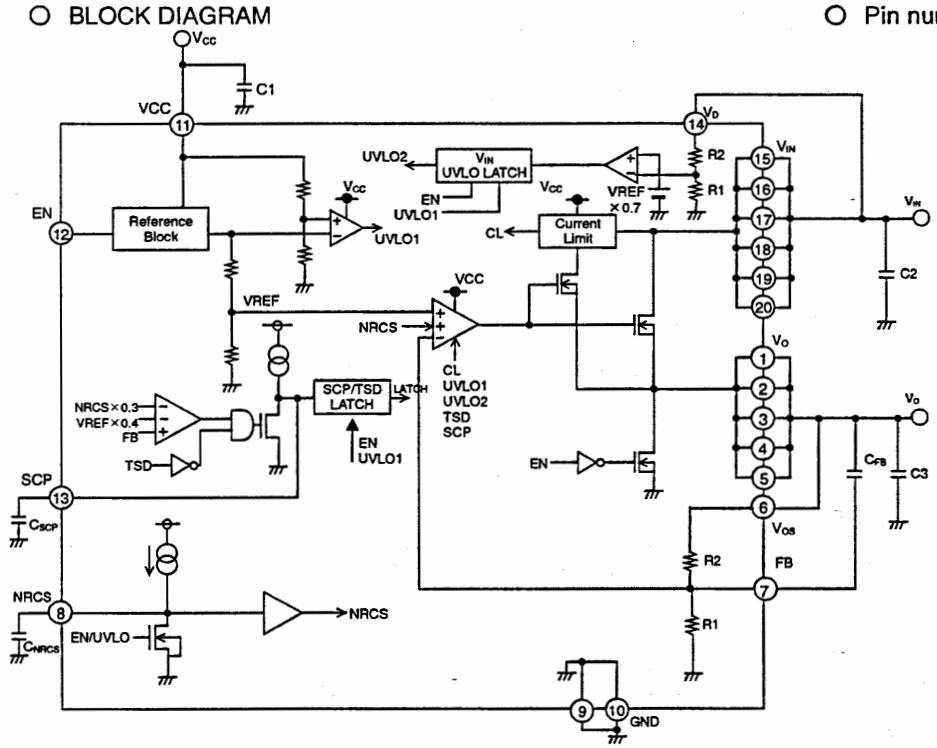
PARAMETER	SYMBOL	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
Bias current	I_{CC}	-	1.4	2.2	mA	
Shut-Down Mode Current	I_{ST}	-	0	10	μA	V_{EN}=0V
Maximum Output Current	I_O	4.0	-	-	A	
Output Voltage 1	$V_{OS}1$	1.188	1.200	1.212	V	
Output Voltage 2	$V_{OS}2$	1.176	1.200	1.224	V	Tj=-10 to 100℃
Line Regulation 1	REG.I1	-	0.1	0.5	%/V	V_{CC}=4.3V to 5.5V
Line Regulation 2	REG.I2	-	0.1	0.5	%/V	V_{IN}=1.25V to 3.3V
Load Regulation	REG.L	-	0.5	10	mV	I_O=0 to 4A
Output ON Resistance	Ron	-	28	50	mΩ	I_O=4A,V_{IN}=1.2V Tj=-10 to 100℃
Standby Discharge Current	I_{DEN}	1	-	-	mA	V_{EN}=0V, V_O=1V
[Enable]						
High level Enable Input Voltage	EN_{HIGH}	2	-	-	V	
Low level Enable Input Voltage	EN_{LOW}	-0.2	-	0.8	V	
Enable pin Input Current	I_{EN}	-	6	10	μA	V_{EN}=3V
[NRCS]						
NRCS Charge Current	I_{NRCS}	12	20	28	μA	
NRCS Standby Voltage	V_{STB}	-	0	50	mV	V_{EN}=0V
[UVLO]						
VCC UVLO Threshold Voltage	V_{CC}UVLO	3.5	3.8	4.1	V	V_{CC}:Sweep-up
VCC UVLO Hysterisis Voltage	V_{CC}HYS	100	160	220	mV	V_{CC}:Sweep-down
VD UVLO Threshold Voltage	V_DUVLO	V_O×0.6	V_O×0.7	V_O×0.8	V	V_D:Sweep-up
[SCP]						
SCP Start-up Voltage	V_{OSCP}	V_O×0.3	V_O×0.4	V_O×0.5	V	
SCP Threshold Voltage	V_{SCPTH}	1.05	1.15	1.25	V	
SCP Charge Current	I_{SCP}	2	4	6	μA	
SCP Standby Voltage	$V_{SCPSTBY}$	-	-	50	mV	

O PHYSICAL DIMENSIONS



(UNIT : mm)
HTSSOP-B20

O BLOCK DIAGRAM



O Pin number Pin name

PIN No.	Pin name
1	V_O
2	V_O
3	V_O
4	V_O
5	V_O
6	V_{OS}
7	FB
8	NRCS
9	GND
10	GND
11	V_{CC}
12	EN
13	SCP
14	V_D
15	V_{IN}
16	V_{IN}
17	V_{IN}
18	V_{IN}
19	V_{IN}
20	V_{IN}
-	FIN

ONOTES FOR USE

(1) Absolute maximum range

Although the quality of this product is rigorously controlled, and circuit operation is guaranteed within the operation ambient temperature range, the device may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because the failure mode (such as short mode or open mode) cannot be identified in this instance, it is important to take physical safety measures such as fusing if a specific mode in excess of absolute rating limits is considered for implementation.

(2) Ground potential

Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode, including transient conditions.

(3) Thermal Design

Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.

(4) Using in the strong electromagnetic field

Use in strong electromagnetic fields may cause malfunctions.

(5) ASO

Be sure that the output transistor for this IC does not exceed the absolute maximum ratings or ASO value.

(6) Thermal shutdown circuit

The IC is provided with a built-in thermal shutdown (TSD) circuit. When chip temperature reaches the threshold temperature shown below, output goes to a cut-off state. (This IC latches output to off mode when the temperature recedes to the specified level. To release latch mode, EN or Vcc is re-operated.) Note that the TSD circuit is designed exclusively to shut down the IC in abnormal thermal conditions. It is not intended to protect the IC or guarantee performance when extreme heat occurs. Therefore, the TSD circuit should not be employed with the expectation of continued use or subsequent operation once TSD is operated.

TSD ON temperature [°C] (typ.)
175

(7) GND pattern

When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

(8) Output Capacitor (C3)

Mount an output capacitor between Vo and GND for stability purposes. The output capacitor is for the open loop gain phase compensation and reduces the output voltage load regulation. If the capacitor value is not large enough, the output voltage may oscillate. And if the equivalent series resistance (ESR) is too large, the output voltage rise/drop increases during a sudden load change. A Low ESR22uF capacitor is recommended. However, the stability depends on the characteristics of temperature and load. And if several kinds of capacitors are utilized in parallel, the output voltage may oscillate due to lack of phase margin. Please confirm operation across a variety of temperature and load conditions.

(9) Input Capacitor (C1, C2)

The input capacitor reduces the output impedence of the voltage supply source connected in the V_{CC} and V_{IN}. If the output impedence of this power supply increases, the input voltage (V_{CC},V_{IN}) may become unstable. This may result in the output voltage oscillation or lowering ripple rejection. Stability depends on power supply characteristics and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.

(10) NRCS (Non Rush Current on Start-up) Setting(C_{NRCS})

The NRCS function is built in this IC to prevent rush current from going through the load (V_{IN} to V_O) for start-up. The constant current comes from the NRCS pin when EN is high or UVLO function is deactivated. Temporary reference voltage is made proportional to time due to current charge the NRCS pin capacitor and make output voltage start up proportional to this reference volatge. To obtain a stable NRCS delay time, a 0.001 μF~1 μF capacitor (X5R or X7R) with susceptiblity to temperature is recommended.

(11) SCP (Short Circuit Protection) Setting (C_{SCP})

Timer latch short circuit protection function is built in the IC. (NRCS is also working at the same time.) to protect the break down of the power MOSFET caused by rush current when the output is shorted to GND. This function becomes active when the output voltage level goes under by 40% of specified Vo. The constant current comes from the NRCS pin in this case. When the reference voltage mede by the current charge of the SCP pin hits 1.15V (Typ.), the output is turned off. To obtain a stable SCP delay time, a capacitor (B) above 330pF with susceptiblity to temperature is recommended.

(12) Input Terminal (V_{CC},V_{IN},V_D,EN)

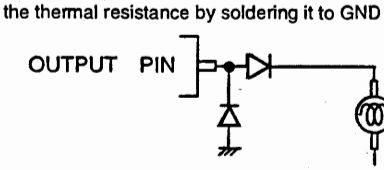
The EN, V_D, V_{IN}, and V_{CC} are isolated. The UVLO protects incorrect operation when the voltage level of V_D and V_{CC} are low. The output becomes high when these pins reach the individual threshold level independent of the start-up pin order. However, if VIN shut down while the IC works under the normal operation, SCP function becomes active and latches the status. And the output does not come back active even though V_{IN} goes up high again. In this case, start V_{CC} or EN up again to deactive this latch function.

(13) Heat sink (FIN)

Since the heat sink (FIN) is connected with the Sub, short it to the GND. It is possible to minimize the thermal resistance by soldering it to GND plane of PCB.

(14) Please add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at startup or in output OFF condition.

(Example)



(15) Short-circuits between pins and and mounting errors

Do not short-circuit between output pin (V_O) and supply pin (V_{CC}) or ground (GND), or between supply pin (V_{CC}) and ground (GND). Mounting errors, such as incorrect positioning or orientation, may destroy the device.

(16) Each block of this IC contains logic circuits which can pull an instantaneous amount of rush current when switching. Therefore, special consideration should be given to the power supply coupling capacitance and the width of power supply and ground traces. Avoid excessively long or convoluted trace patterns.