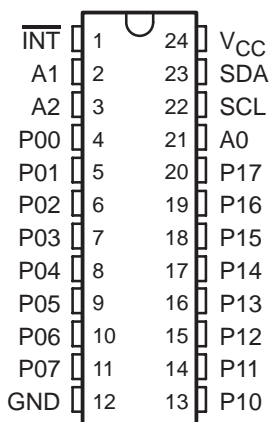


# PCF8575 REMOTE 16-BIT I<sup>2</sup>C AND SMBus I/O EXPANDER WITH INTERRUPT OUTPUT

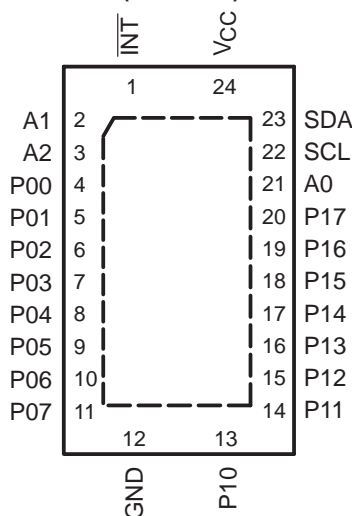
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- Low Standby-Current Consumption of 10  $\mu$ A Maximum
- I<sup>2</sup>C to Parallel-Port Expander
- Open-Drain Interrupt Output
- Compatible With Most Microcontrollers
- 400-kHz Fast I<sup>2</sup>C Bus
- Address by Three Hardware Address Pins for Use of Up To Eight Devices
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Current Source to V<sub>CC</sub> for Actively Driving a High at the Output
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

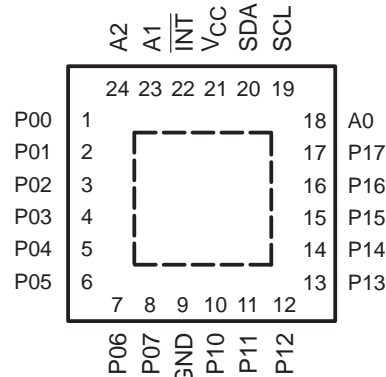
DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



RHL PACKAGE  
(TOP VIEW)



RGE PACKAGE  
(TOP VIEW)



## description/ordering information

This 16-bit I/O expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 2.5-V to 5.5-V V<sub>CC</sub> operation.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DB	Reel of 2500	PCF8575DBR	PF575
		Reel of 250	PCF8575DBT	
	QSOP – DBQ	Reel of 2500	PCF8575DBQR	PCF8575
	TVSOP – DGV	Reel of 2000	PCF8575DGVR	PF575
	SOIC – DW	Tube of 25	PCF8575DW	PCF8575
		Reel of 2000	PCF8575DWR	
	TSSOP – PW	Tube of 60	PCF8575PW	PF575
		Reel of 1200	PCF8575PWR	
		Reel of 250	PCF8575PWT	
QFN – RGE	Reel of 3000	PCF8575RGER	PF575	
QFN – RHL	Reel of 1000	PCF8575RHRL	PF575	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
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# PCF8575

## REMOTE 16-BIT I<sup>2</sup>C AND SMBus I/O EXPANDER WITH INTERRUPT OUTPUT

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### description/ordering information (continued)

The PCF8575 provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface serial clock (SCL) and serial data (SDA).

The device features a 16-bit quasi-bidirectional input/output (I/O) port (P07–P00; P17–P10), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source ( $I_{OH}$ ) to  $V_{CC}$  is active. An additional strong pullup to  $V_{CC}$  ( $I_{OHT}$ ) allows fast rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs. After power on, as all the I/Os are set high, all of them can be used as inputs. Any change in setting of the I/Os as either input or outputs can be done with the write mode. If a high is applied externally to an I/O that has been written earlier to low, a large current ( $I_{OL}$ ) will flow to GND.

The PCF8575 provides an open-drain interrupt output ( $\overline{INT}$ ), which can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time ( $t_{iV}$ ), the signal  $\overline{INT}$  is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal or in the write mode at the ACK bit after the falling edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and transmitted as  $\overline{INT}$ . Reading from or writing to another device does not affect the interrupt circuit.

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Thus, the PCF8575 can remain a simple slave device.

Every data transmission to or from the PCF8575 must consist of an even number of bytes. The first data byte in every pair refers to port 0 (P07–P00), and the second data byte in every pair refers to port 1 (P17–P10). To write to the ports (output mode), the master first addresses the slave device, setting the last bit of the byte containing the slave address to logic 0. The PCF8575 acknowledges, and the master sends the first data byte for P07–P00. After the first data byte is acknowledged by the PCF8575, the second data byte (P17–P10) is sent by the master. Once again, the PCF8575 acknowledges the receipt of the data, after which this 16-bit data is presented on the port lines.

The number of data bytes that can be sent successively is not limited. After every two bytes, the previous data is overwritten. When the PCF8575 receives the pairs of data bytes, the first byte is referred to as P07–P00 and the second byte as P17–P10. The third byte is referred to as P07–P00, the fourth byte as P17–P10, and so on.

Before reading from the PCF8575, all ports desired as input should be set to logic 1. To read from the ports (input mode), the master first addresses the slave device, setting the last bit of the byte containing the slave address to logic 1. The data bytes that follow on the SDA are the values on the ports. If the data on the input port changes faster than the master can read, this data may be lost.

When power is applied to  $V_{CC}$ , an internal power-on reset holds the PCF8575 in a reset state until  $V_{CC}$  has reached  $V_{POR}$ . At that time, the reset condition is released, and the device's I<sup>2</sup>C-bus state machine initializes the bus to its default state.

The hardware pins (A0, A1, and A2) are used to program and vary the fixed I<sup>2</sup>C address and allow up to eight devices to share the same I<sup>2</sup>C bus or SMBus. The fixed I<sup>2</sup>C address of the PCF8575 is the same as the PCF8575C, PCF8574, PCA9535, and PCA9555, allowing up to eight of these devices, in any combination, to share the same I<sup>2</sup>C bus or SMBus.



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**PIN FUNCTIONS**

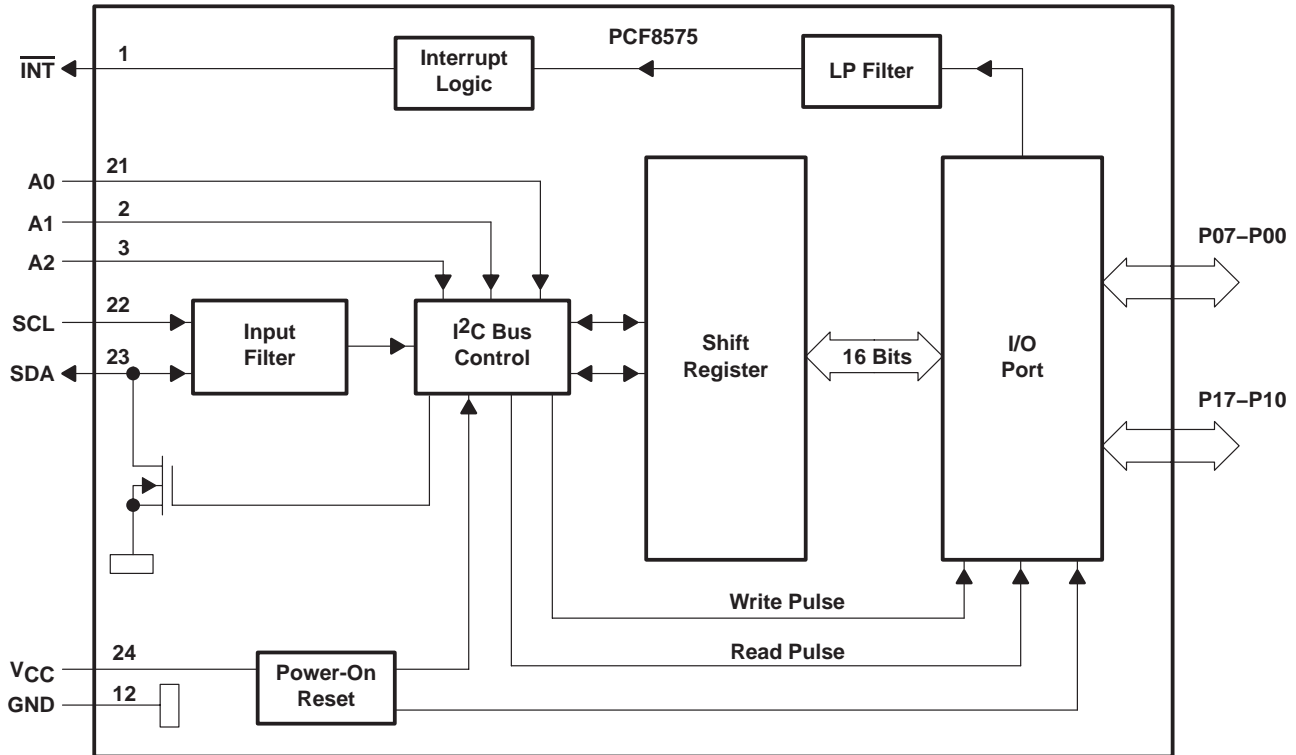
DB, DBQ, DGV, DW, PW, AND RHL PIN NO.	RGE PIN NO.	NAME	FUNCTION
1	22	INT	Interrupt output. Connect to V <sub>CC</sub> through a pullup resistor.
2	23	A1	Address input 1. Connect directly to V <sub>CC</sub> or ground. Pullup resistors are not needed.
3	24	A2	Address input 2. Connect directly to V <sub>CC</sub> or ground. Pullup resistors are not needed.
4	1	P00	P-port input/output
5	2	P01	P-port input/output
6	3	P02	P-port input/output
7	4	P03	P-port input/output
8	5	P04	P-port input/output
9	6	P05	P-port input/output
10	7	P06	P-port input/output
11	8	P07	P-port input/output
12	9	GND	Ground
13	10	P10	P-port input/output
14	11	P11	P-port input/output
15	12	P12	P-port input/output
16	13	P13	P-port input/output
17	14	P14	P-port input/output
18	15	P15	P-port input/output
19	16	P16	P-port input/output
20	17	P17	P-port input/output
21	18	A0	Address input 0. Connect directly to V <sub>CC</sub> or ground. Pullup resistors are not needed.
22	19	SCL	Serial clock line. Connect to V <sub>CC</sub> through a pullup resistor.
23	20	SDA	Serial data line. Connect to V <sub>CC</sub> through a pullup resistor.
24	21	V <sub>CC</sub>	Supply voltage



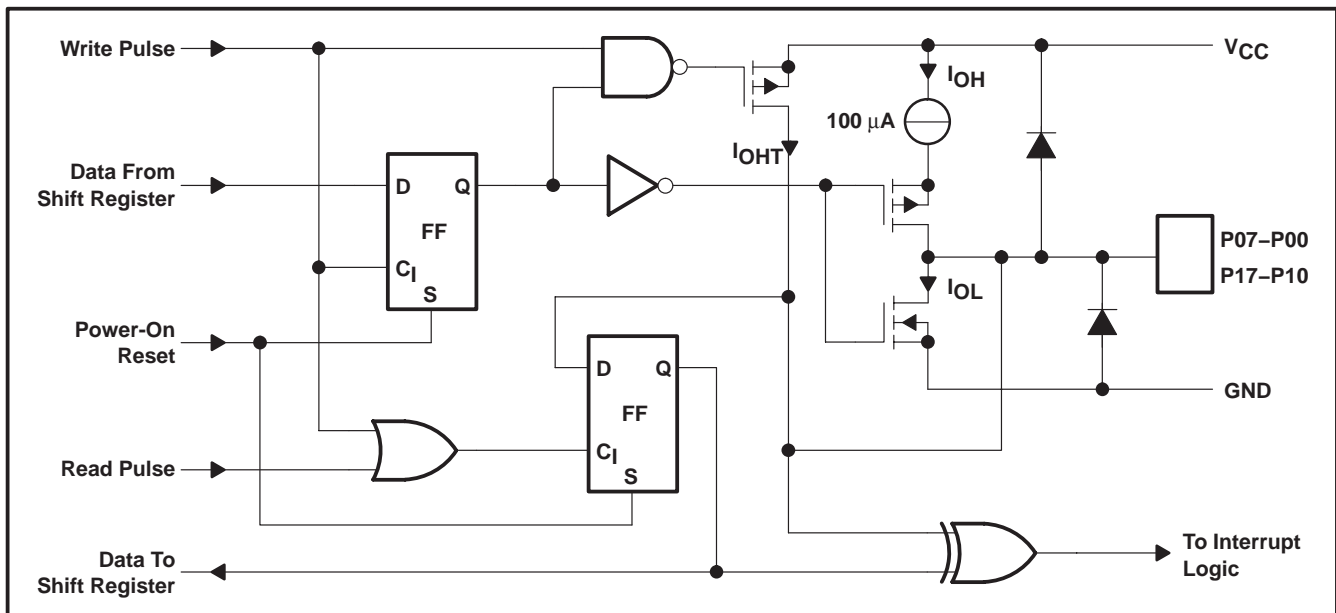
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## logic diagram (positive logic)



## simplified schematic diagram of each P-port input/output



## I<sup>2</sup>C interface

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I<sup>2</sup>C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the start condition, the device address byte is sent, MSB first, including the data direction bit ( $R/\overline{W}$ ). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the start and the stop conditions.

The data byte follows the address ACK. If the  $R/\overline{W}$  bit is high, the data from this device are the values read from the P port. If the  $R/\overline{W}$  bit is low, the data are from the master, to be output to the P port. The data byte is followed by an ACK sent from this device. If other data bytes are sent from the master, following the ACK, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time ( $t_{pv}$ ) after the low-to-high transition of SCL, during the clock cycle for the ACK.

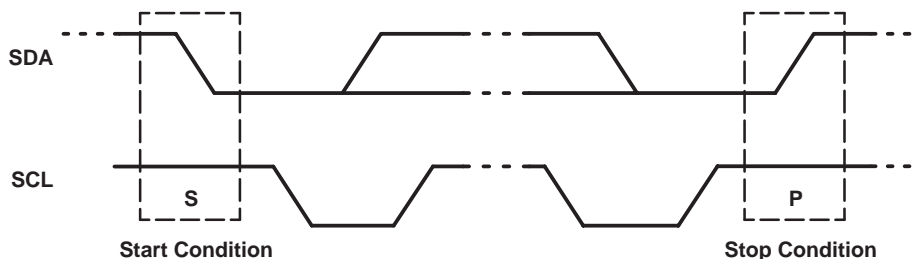
On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see Figure 2).

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). Setup and hold times must be taken into account.

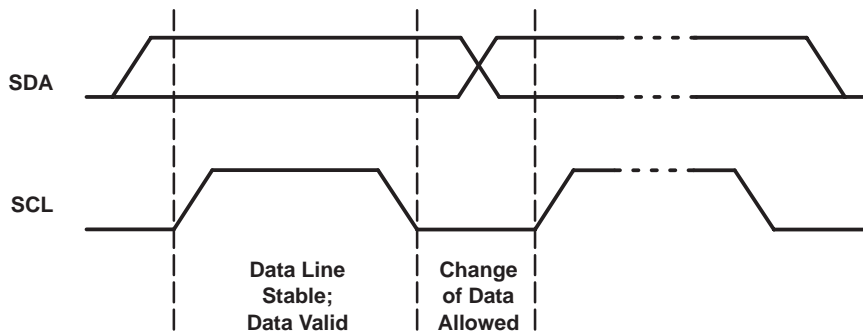
A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.



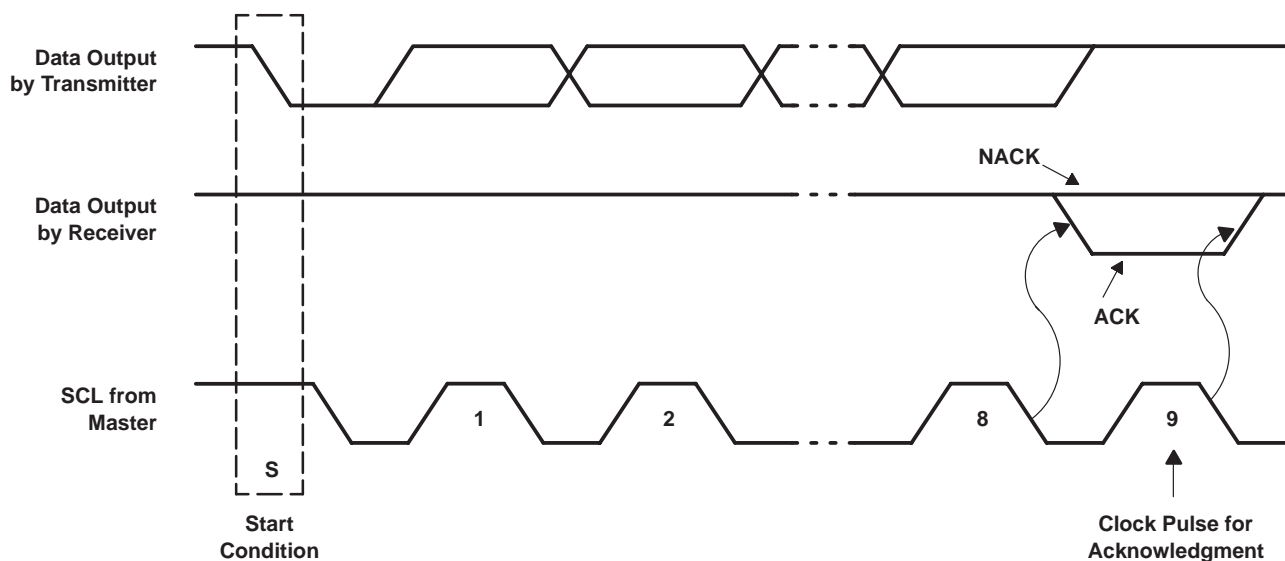
**Figure 1. Definition of Start and Stop Conditions**

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**Figure 2. Bit Transfer**



**Figure 3. Acknowledgment on the I<sup>2</sup>C Bus**

**INTERFACE DEFINITION TABLE**

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C slave address	L	H	L	L	A2	A1	A0	R/ $\bar{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

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Figures 4 and 5 show the address and timing diagrams for the write and read modes, respectively.

### Integral Multiples of Two Bytes

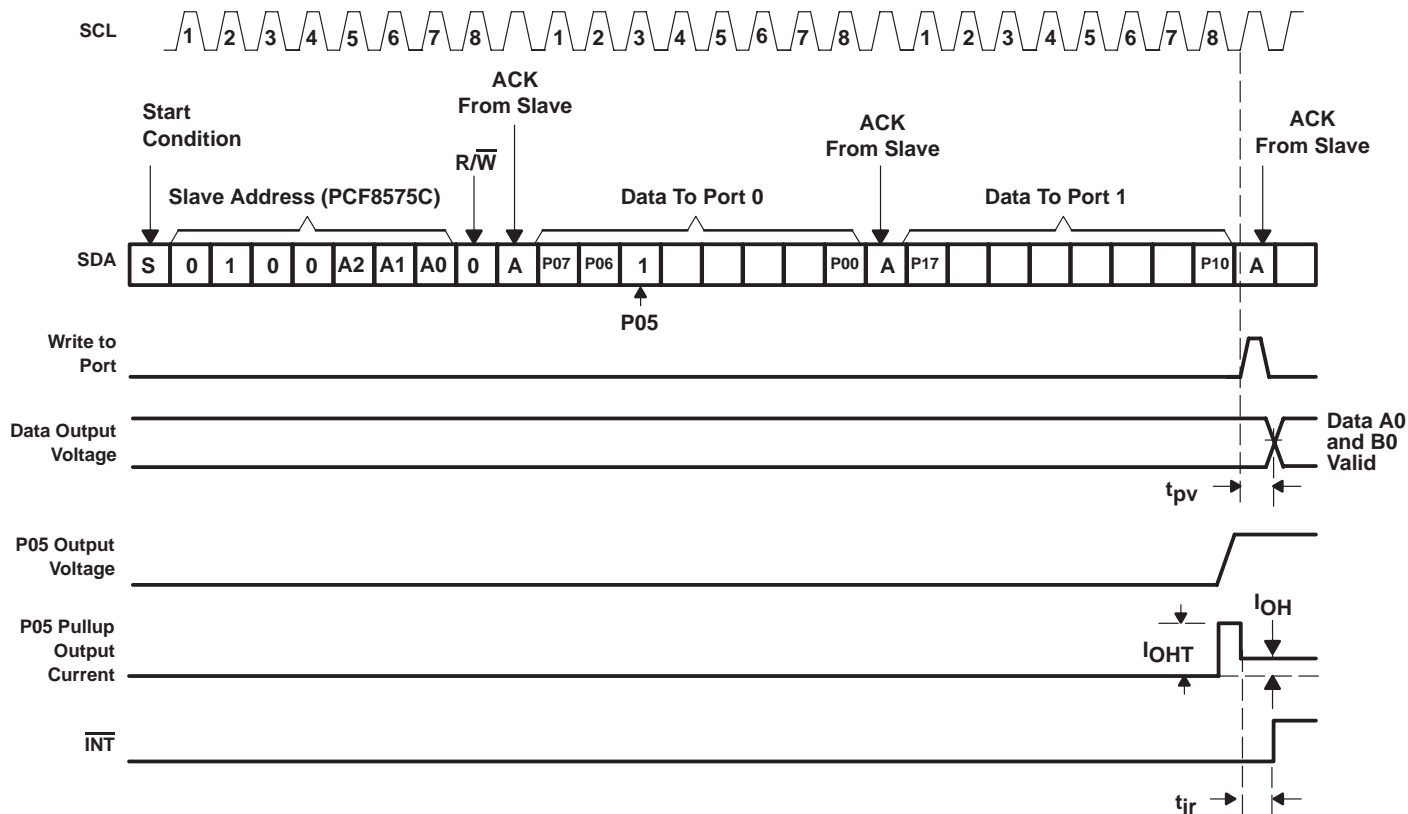
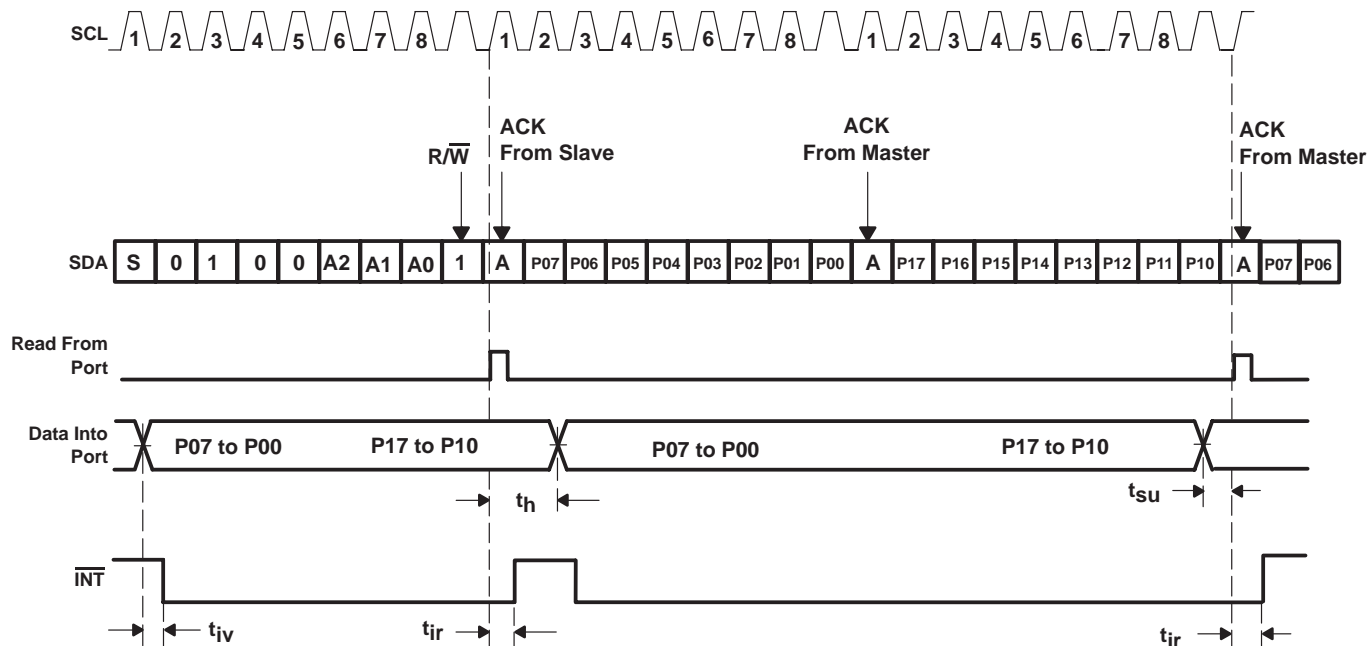


Figure 4. Write Mode (Output)

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A low-to-high transition of SDA while SCL is high is defined as the stop condition (P). The transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the latest ACK phase is valid (output mode). Input data is lost.

Figure 5. Read Mode (Input)

ADDRESS REFERENCE TABLE

INPUTS			I <sup>2</sup> C-BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–20 mA
Input/Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	–20 mA
Continuous output low current, $I_{OL}$ ( $V_O = 0$ to $V_{CC}$ ) .....	50 mA
Continuous output high current, $I_{OH}$ ( $V_O = 0$ to $V_{CC}$ ) .....	–4 mA
Continuous current through $V_{CC}$ or GND .....	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....	63°C/W
DBQ package .....	61°C/W
DGV package .....	86°C/W
DW package .....	46°C/W
PW package .....	88°C/W
RGE package .....	53°C/W
RHL package .....	43°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	2.5	5.5	V
$V_{IH}$ High-level input voltage	$0.7 \times V_{CC}$	$V_{CC} + 0.5$	V
$V_{IL}$ Low-level input voltage	–0.5	$0.3 \times V_{CC}$	V
$I_{OH}$ P-port high-level output current		–1	mA
$I_{OHT}$ P-port transient pullup current		10	mA
$I_{OL}$ P-port low-level output current		25	mA
$T_A$ Operating free-air temperature	–40	85	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	Input diode clamp voltage	I <sub>I</sub> = -18 mA	2.5 V to 5.5 V	-1.2			V
V <sub>POR</sub>	Power-on reset voltage‡	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	V <sub>POR</sub>		1.2	1.8	V
I <sub>OH</sub>	P port	V <sub>O</sub> = GND	2.5 V to 5.5 V	-30		-300	μA
I <sub>OHT</sub>	P-port transient pullup current	High during ACK, V <sub>OH</sub> = GND	2.5 V	-0.5	-1		mA
I <sub>OL</sub>	SDA	V <sub>OL</sub> = 0.4 V	2.5 V to 5.5 V	3			mA
	P port	V <sub>OL</sub> = 0.4 V	2.5 V to 5.5 V	5	15		mA
		V <sub>OL</sub> = 1 V		10	25		
	$\overline{\text{INT}}$	V <sub>OL</sub> = 0.4 V	2.5 V to 5.5 V	1.6			mA
I <sub>I</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V to 5.5 V			±5	μA
	A0, A1, A2					±1	
I <sub>IHL</sub>	P port	V <sub>I</sub> ≥ V <sub>CC</sub> or V <sub>I</sub> ≤ GND	2.5 V to 5.5 V			±400	μA
I <sub>CC</sub>	Operating mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, f <sub>SCL</sub> = 400 kHz	5.5 V	100	200	μA	
			3.6 V	30	75		
			2.7 V	20	50		
	Standby mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, f <sub>SCL</sub> = 0 kHz	5.5 V	2.5	10		
			3.6 V	2.5	10		
			2.7 V	2.5	10		
ΔI <sub>CC</sub>	Supply current increase	One input at V <sub>CC</sub> - 0.6, Other inputs at V <sub>CC</sub> or GND	2.5 V to 5.5 V			200	μA
C <sub>i</sub>	SCL	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V to 5.5 V		3	7	pF
C <sub>io</sub>	SDA	V <sub>IO</sub> = V <sub>CC</sub> or GND	2.5 V to 5.5 V		3	7	pF
	P port				4	10	

† All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5 V V<sub>CC</sub>) and T<sub>A</sub> = 25°C.

‡ The power-on reset circuit resets the I<sup>2</sup>C-bus logic with V<sub>CC</sub> < V<sub>POR</sub> and sets all I/Os to logic high (with current source to V<sub>CC</sub>).



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**I<sup>2</sup>C interface timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6)**

		MIN	MAX	UNIT
f <sub>scl</sub>	I <sup>2</sup> C clock frequency		400	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	0.6		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	1.3		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time		50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time	100		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time	0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time	20 + 0.1C <sub>b</sub> <sup>§</sup>	300	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time	20 + 0.1C <sub>b</sub> <sup>§</sup>	300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time (10-pF to 400-pF bus)		300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start	1.3		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup	0.6		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold	0.6		μs
t <sub>sps</sub>	I <sup>2</sup> C stop condition setup	0.6		μs
t <sub>vd</sub>	Valid-data time	SCL low to SDA output valid		1.2
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400	pF

§ C<sub>b</sub> = total bus capacitance of one bus line in pF

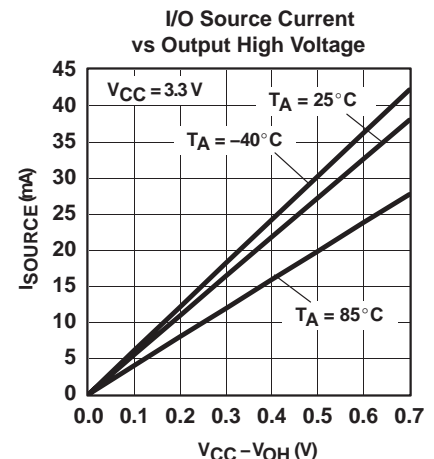
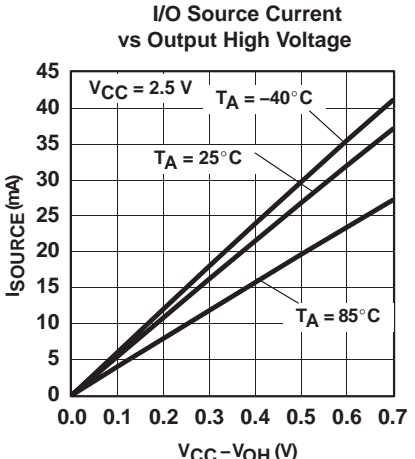
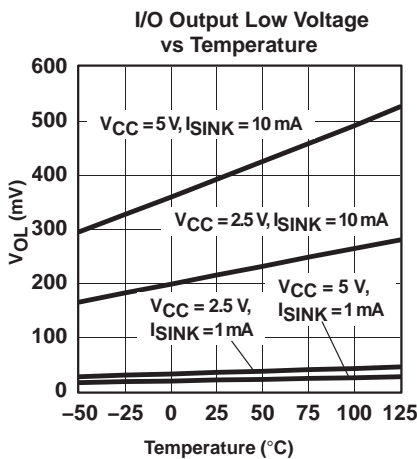
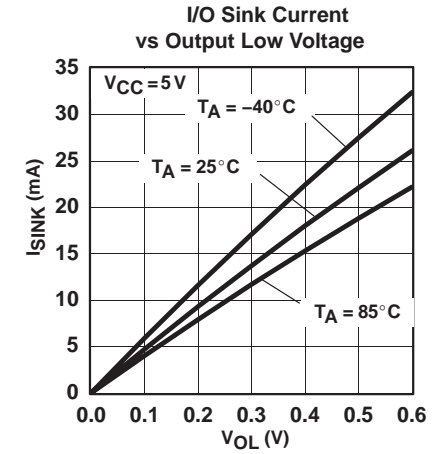
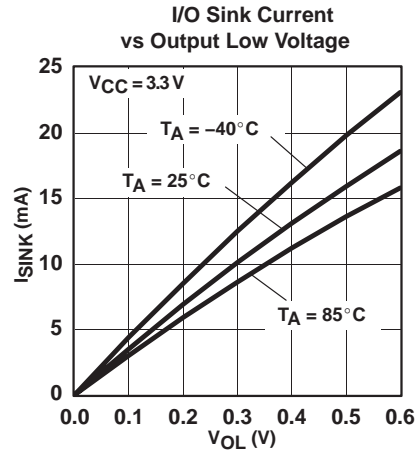
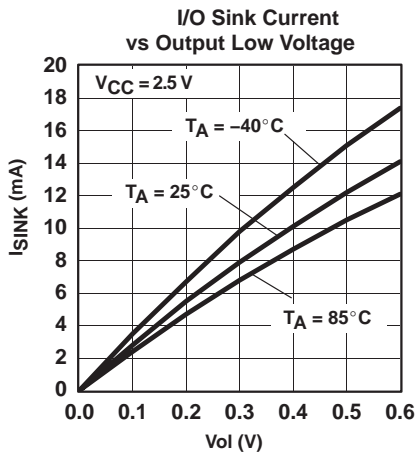
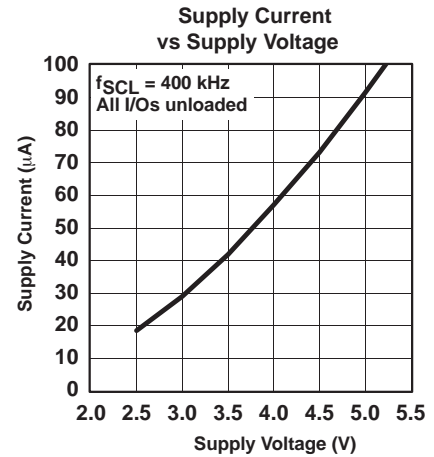
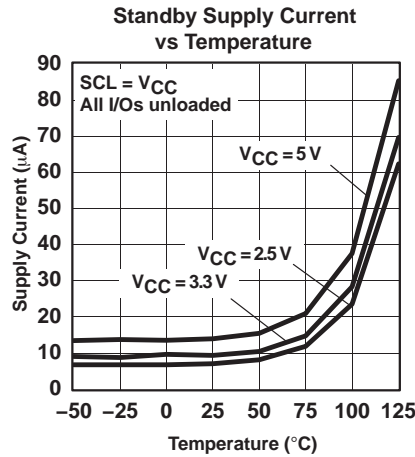
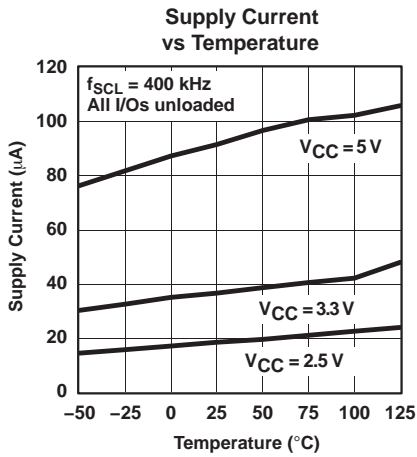
**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> ≤ 100 pF (unless otherwise noted) (see Figures 7 and 8)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t <sub>iv</sub>	Interrupt valid time	P port			4	μs
t <sub>ir</sub>	Interrupt reset delay time	SCL			4	μs
t <sub>pv</sub>	Output data valid	SCL			4	μs
t <sub>su</sub>	Input data setup time	P port	0			μs
t <sub>h</sub>	Input data hold time	P port	4			μs

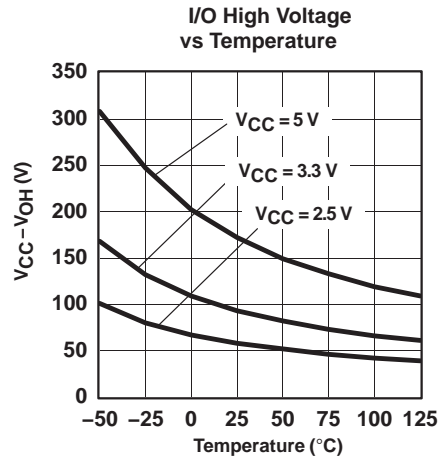
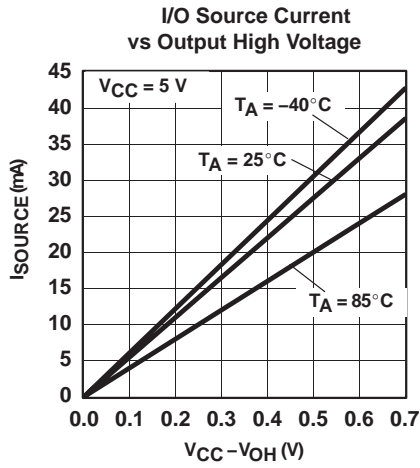
# PCF8575 REMOTE 16-BIT I<sup>2</sup>C AND SMBus I/O EXPANDER WITH INTERRUPT OUTPUT

SCPS121B – JANUARY 2005 – REVISED SEPTEMBER 2005

## TYPICAL OPERATING CHARACTERISTICS T<sub>A</sub> = 25°C (unless otherwise noted)



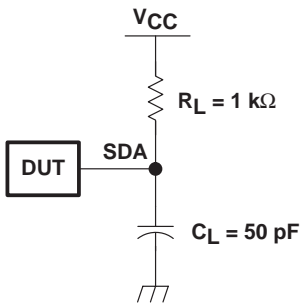
**TYPICAL OPERATING CHARACTERISTICS**  
**T<sub>A</sub> = 25°C (unless otherwise noted) (continued)**



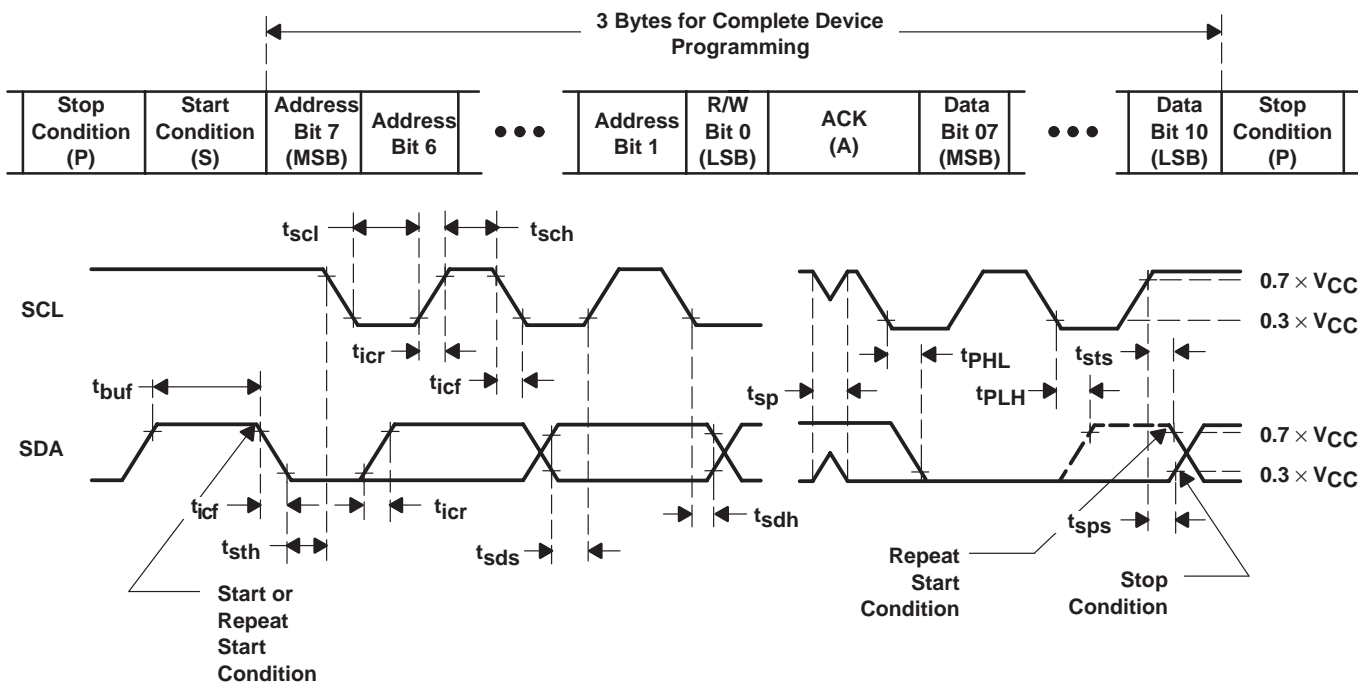
**PCF8575**  
**REMOTE 16-BIT I<sup>2</sup>C AND SMBus I/O EXPANDER**  
**WITH INTERRUPT OUTPUT**

SCPS121B – JANUARY 2005 – REVISED SEPTEMBER 2005

**PARAMETER MEASUREMENT INFORMATION**



**SDA LOAD CONFIGURATION**

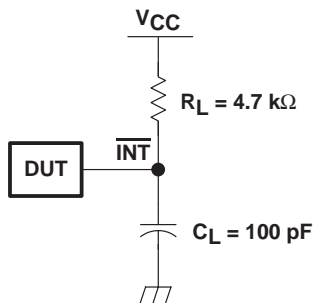


**VOLTAGE WAVEFORMS**

BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2, 3	P port data

**Figure 6. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION



INTERRUPT LOAD CONFIGURATION

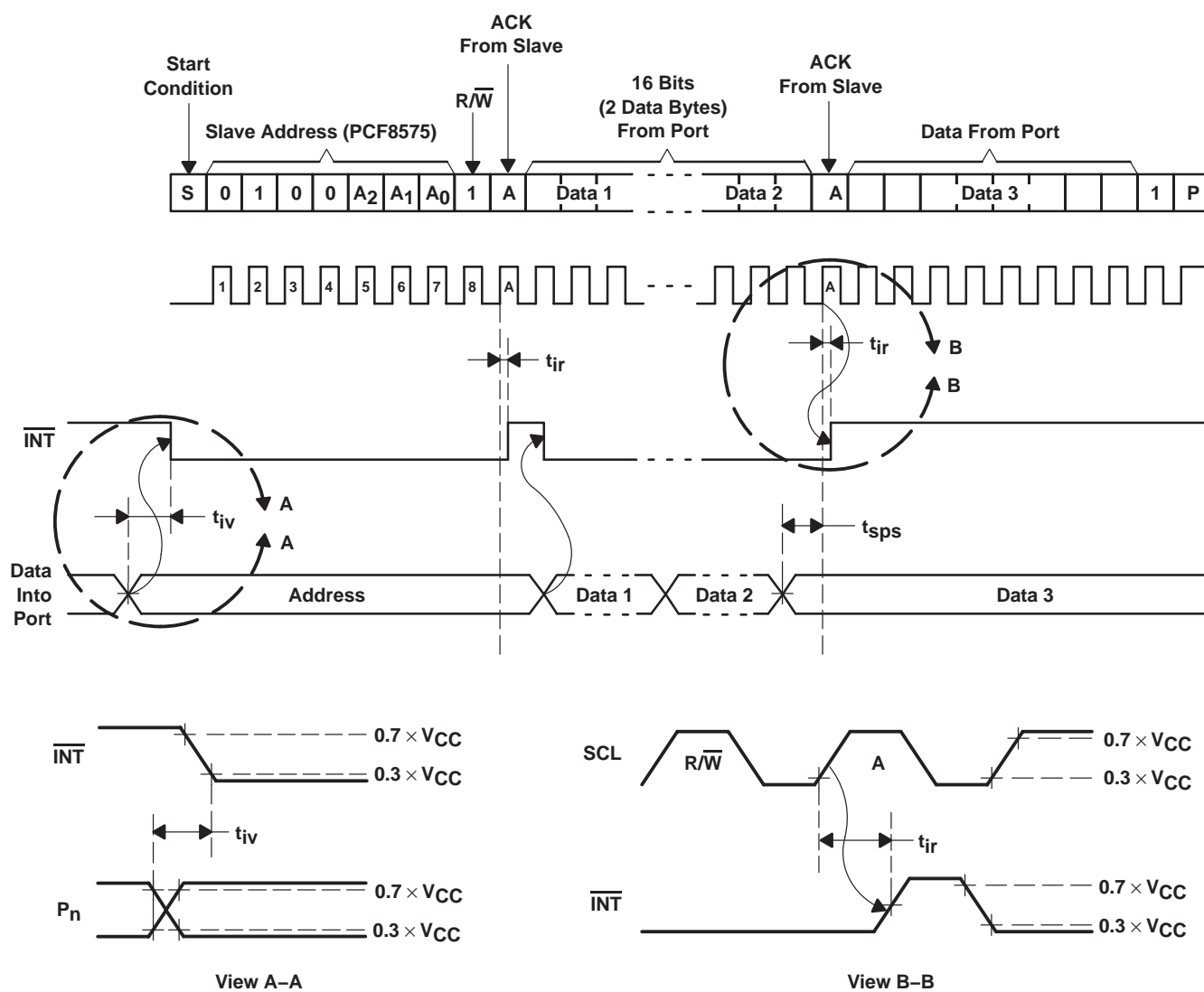
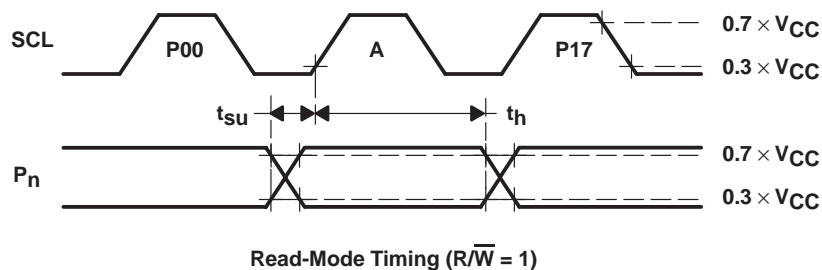
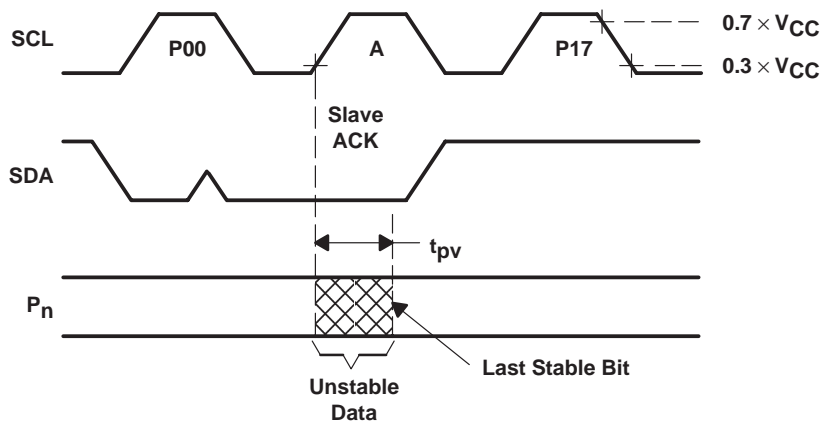
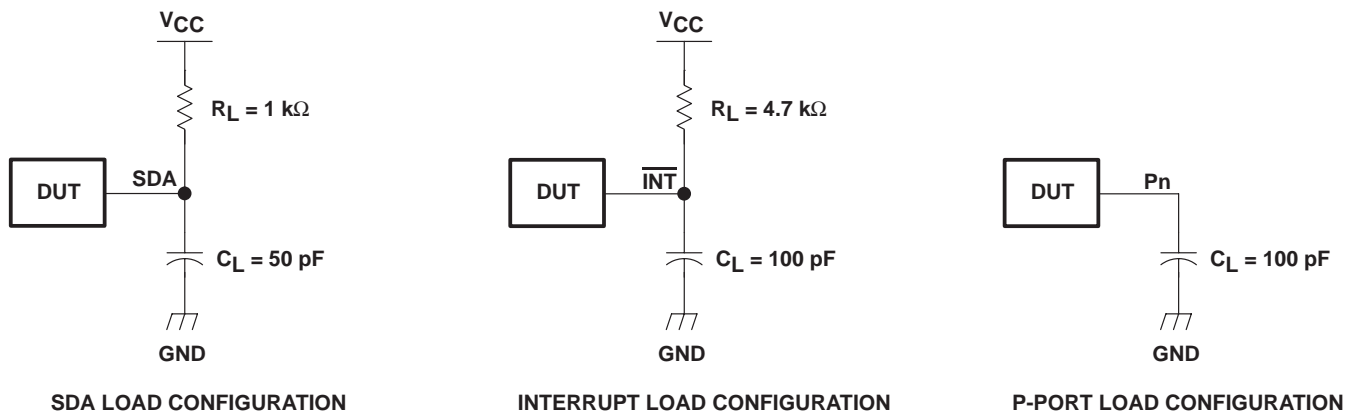


Figure 7. Interrupt Load Circuits and Voltage Waveforms

**PCF8575**  
**REMOTE 16-BIT I<sup>2</sup>C AND SMBus I/O EXPANDER**  
**WITH INTERRUPT OUTPUT**

SCPS121B – JANUARY 2005 – REVISED SEPTEMBER 2005

**PARAMETER MEASUREMENT INFORMATION**



**Figure 8. P-Port Timing Waveforms**



THERMAL PAD MECHANICAL DATA

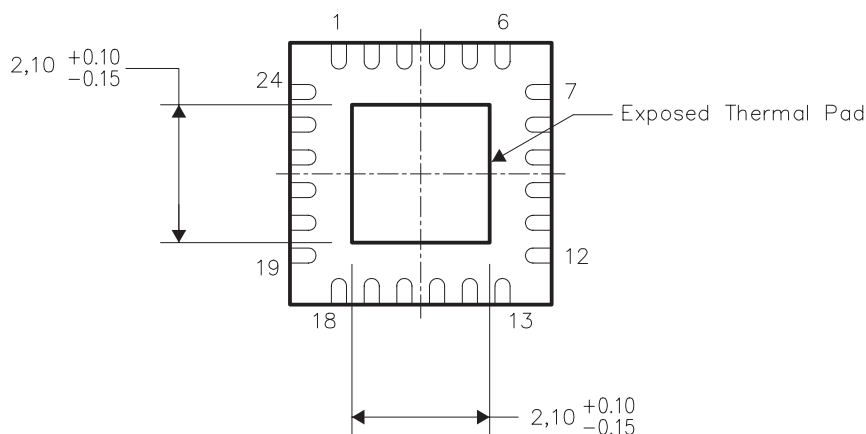
RGE (S-PQFP-N24)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206344-3/B 04/05

# PCF8575 REMOTE 16-BIT I<sup>2</sup>C AND SMBus I/O EXPANDER WITH INTERRUPT OUTPUT

SCPS121B – JANUARY 2005 – REVISED SEPTEMBER 2005

## THERMAL PAD MECHANICAL DATA

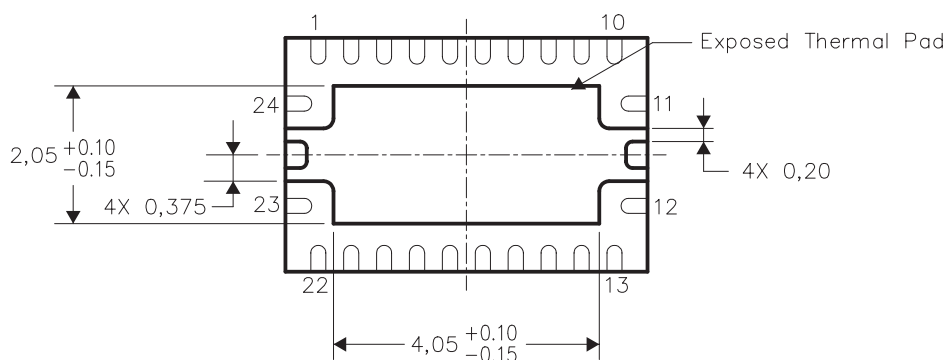
RHL (R-PQFP-N24)

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206363-3/A 01/05



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
PCF8575DB	PREVIEW	SSOP	DB	24	60	TBD	Call TI	Call TI
PCF8575DBQR	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
PCF8575DBQRE4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
PCF8575DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCF8575DBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCF8575DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCF8575DGVRE4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCF8575DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCF8575DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCF8575PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCF8575PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCF8575PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCF8575PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCF8575RGER	PREVIEW	QFN	RGE	24	3000	TBD	Call TI	Call TI
PCF8575RHLR	PREVIEW	QFN	RHL	24	1000	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



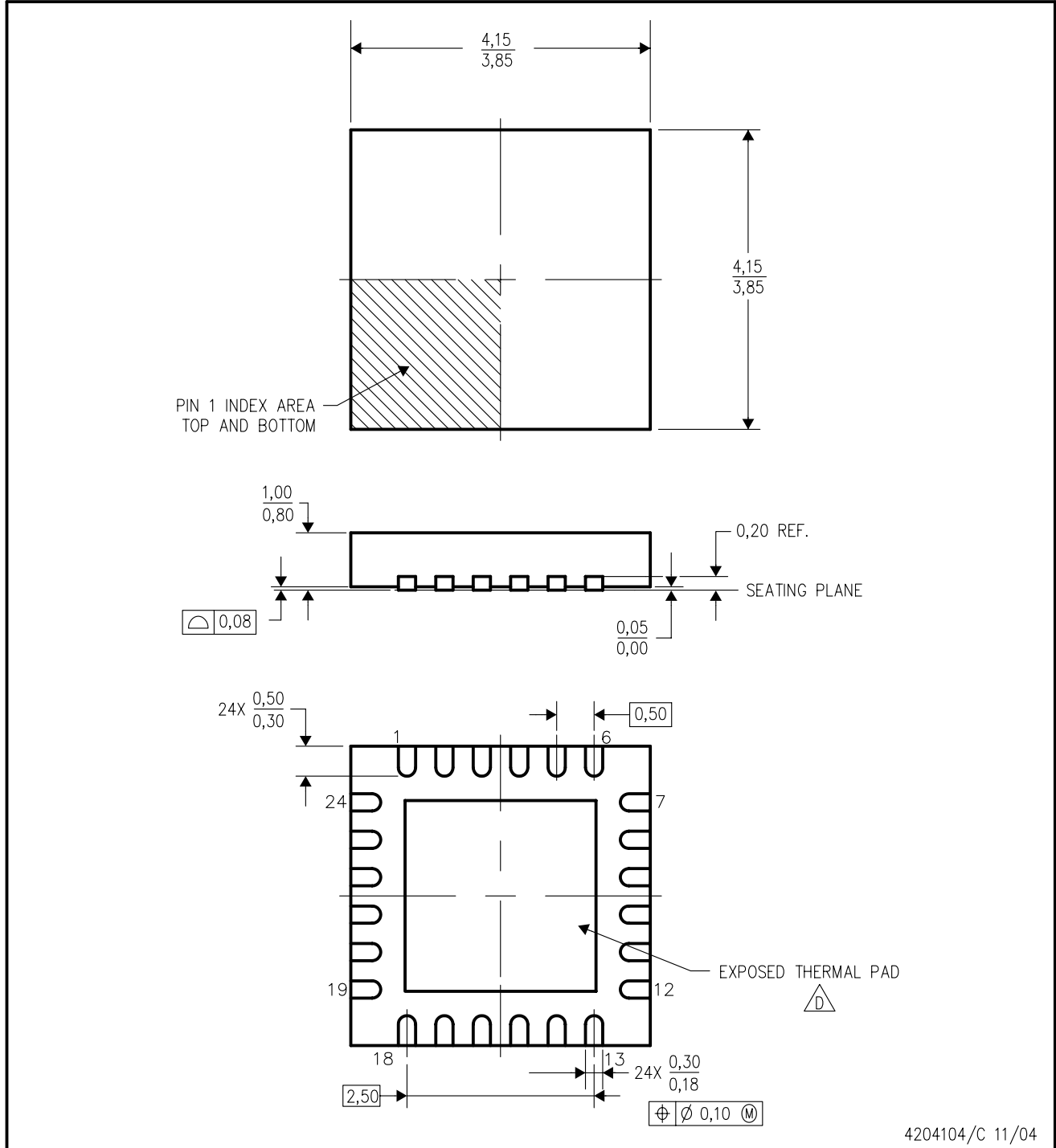
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194






RGE (S-PQFP-N24)

PLASTIC QUAD FLATPACK



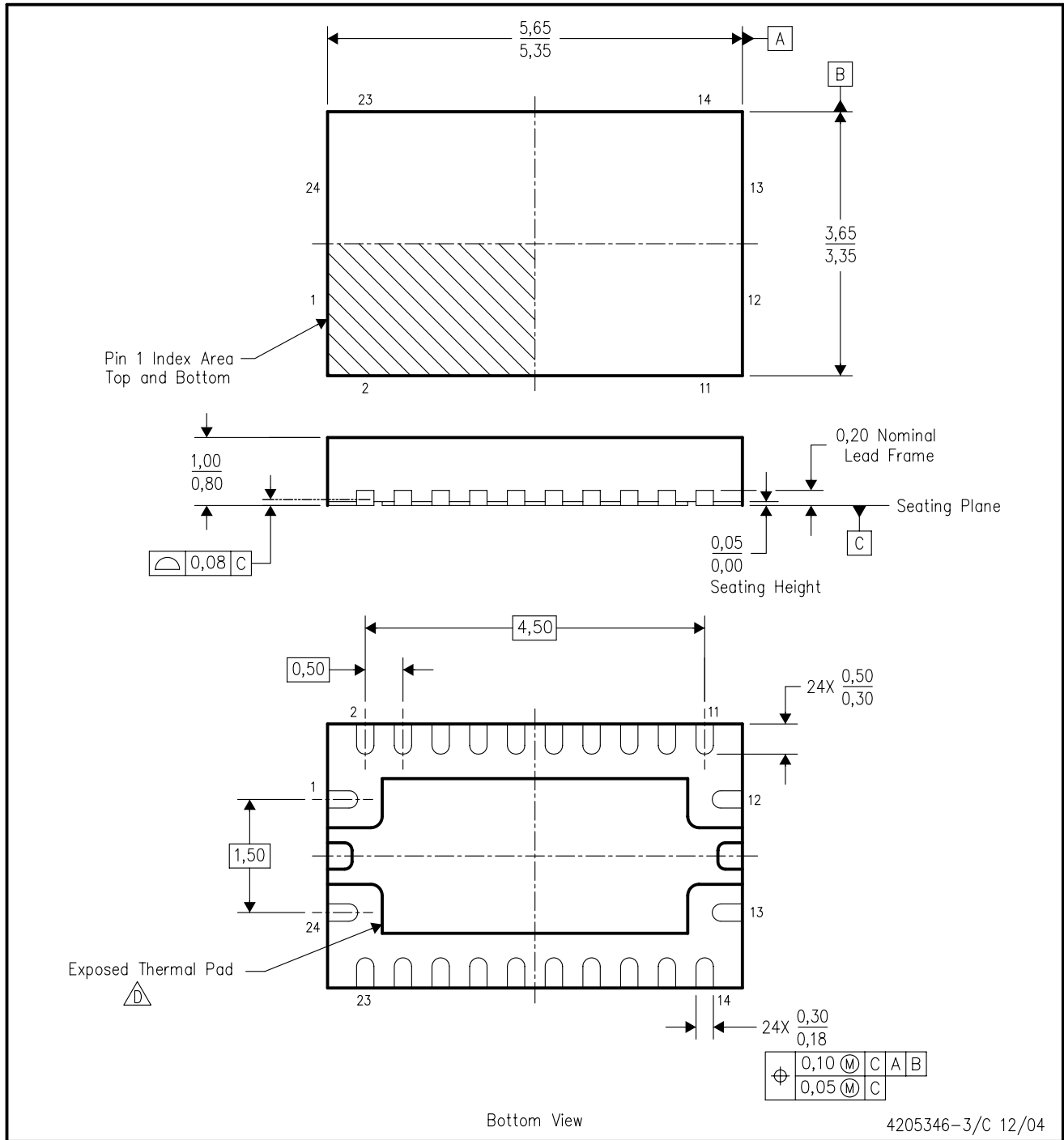
4204104/C 11/04

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.



RHL (R-PQFP-N24)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. JEDEC MO-241 package registration pending.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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