

# ADSP-BF526 EZ-Board™ Evaluation System Manual

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The EZ-Board evaluation system is warranted against defects in materials and workmanship for a period of one year from the date of purchase from Analog Devices or from an authorized dealer.

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## Regulatory Compliance

The ADSP-BF526 EZ-Board is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-BF526 EZ-Board is currently being processed for certification that it complies with the essential requirements of the European EMC directive 89/336/EEC amended by 93/68/EEC and therefore carries the “CE” mark.



The EZ-Board evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-Board boards in the protective shipping package.





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# PREFACE

Thank you for purchasing the ADSP-BF526 EZ-Board™, Analog Devices, Inc. evaluation system for Blackfin® processors.

Blackfin processors embody a new type of embedded processor designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. They deliver breakthrough signal-processing performance and power efficiency within a reduced instruction set computing (RISC) programming model.

Blackfin processors support a media instruction set computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics. Blackfin processors deliver signal-processing performance in a microprocessor-like environment.

Based on the Micro Signal Architecture (MSA), Blackfin processors combine a 32-bit RISC instruction set, dual 16-bit multiply accumulate (MAC) DSP functionality, and eight-bit video processing performance that had previously been the exclusive domain of very-long instruction word (VLIW) media processors.

The evaluation board is designed to be used in conjunction with the VisualDSP++<sup>®</sup> development environment to test the capabilities of the ADSP-BF526 Blackfin processors. The VisualDSP++ development environment aids advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-BF526 assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-BF526 processor from a personal computer (PC) is achieved through a USB port or an external JTAG emulator. The USB interface of the standalone debug agent gives unrestricted access to the ADSP-BF526 processor and evaluation board's peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. To learn more about Analog Devices emulators and processor development tools, go to <http://www.analog.com/dsp/tools/>.

The ADSP-BF526 EZ-Board provides example programs to demonstrate the capabilities of the product.



The ADSP-BF526 EZ-Board installation is part of the VisualDSP++ installation. As an EZ-KIT Lite, an EZ-Board is a licensed product that offers an unrestricted evaluation license for the first 90 days. For details about evaluation license restrictions after the 90 days, refer to “[Evaluation License Restrictions](#)” on [page 1-9](#) and the *VisualDSP++ Installation Quick Reference Card*.

The board features:

- Analog Devices ADSP-BF526 Blackfin processor
  - ✓ Core performance up to 400 MHz
  - ✓ External bus performance up to 80 MHz
  - ✓ 208-pin BGA package
  - ✓ 25 MHz crystal
- Programmable VDDINT core power
  - ✓ Analog Devices AD5258 TWI digital potentiometer
  - ✓ Analog Devices ADP1715 low dropout linear regulator
- Battery-powered operation
  - ✓ Panasonic CR1632 740 mAh lithium ion battery
  - ✓ Analog Devices ADP2291 battery charge circuit
  - ✓ Benchmarq BQ27500 fuel gauge for battery monitoring
- Mobile synchronous dynamic random access memory (SDRAM)
  - ✓ Micron MT48H32M16 – 64 MB (8M x 16-bits x 4 banks)
- Parallel flash memory
  - ✓ Numonyx M58WR032KB – 32 Mb (2M x 16-bits)
- NAND flash memory
  - ✓ Numonyx NAND02 – 2 Gb
- SPI flash memory
  - ✓ SST SST25WF040 – 4 Mb

- Analog audio interface
  - ✓ Wolfson WM8731L low power audio codec
  - ✓ 1 stereo LINE OUT jack
  - ✓ 1 headphone LINE IN
  - ✓ 1 input MIC jack
  - ✓ 1 input stereo LINE IN jack
- Ethernet interface
  - ✓ SMSC LAN8700 PHY device
  - ✓ 10-BaseT and 100-BaseTX Ethernet controller
  - ✓ Auto-MDIX
- Thumbwheel
  - ✓ Panasonic EVQ-WKA001 rotary encoder
- Universal asynchronous receiver/transmitter (UART)
  - ✓ ADM1385 RS-232 line driver/receiver
  - ✓ DB9 female connector
- LEDs
  - ✓ Nine LEDs: one board reset (red), three general-purpose (amber), one PHY link (amber), one PHY activity (green), one battery charging (amber), one battery low (amber), and one battery good (green)
- Push buttons
  - ✓ Five push buttons: one reset, two programmable flags with debounce logic, wake and sleep with debounce logic

- Expansion interface II™:
  - ✓ Next generation of the expansion interface design, provides access to most of the ADSP-BF526 processor signals
- Land grid array
  - Easy probing of all port pins and most EBIU signals
- Other features
  - ✓ JTAG ICE 14-pin header
  - ✓ USB on-the-go (OTG) connector
  - ✓ Host interface connector
  - ✓ Blackfin and SDRAM power measurement jumpers

For information about the hardware components of the EZ-Board, refer to “[ADSP-BF526 EZ-Board Hardware Reference](#)” on page 2-1.

## Purpose of This Manual

The *ADSP-BF526 EZ-Board Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF526 EZ-Board. Finally, a schematic and a bill of materials are provided as a reference for future designs.

The product software installation is detailed in the *VisualDSP++ Installation Quick Reference Card*.

# Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set. Programmers who are unfamiliar with Analog Devices processors can use this manual, but should supplement it with other texts (such as the *ADSP-BF52x Blackfin Processor Hardware Reference* and *Blackfin Processor Instruction Set Reference*) that describe your target architecture.

Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and user's or getting started guides. For the locations of these documents, see "[Related Documents](#)".

# Manual Contents

The manual consists of:

- Chapter 1, "[Using ADSP-BF526 EZ-Board](#)" on page 1-1  
Describes EZ-Board functionality from a programmer's perspective and provides an easy-to-access memory map.
- Chapter 2, "[ADSP-BF526 EZ-Board Hardware Reference](#)" on page 2-1  
Provides information on the EZ-Board hardware components.
- Appendix A, "[ADSP-BF526 EZ-Board Bill Of Materials](#)" on page A-1  
Provides a list of components used to manufacture the EZ-Board.
- Appendix B, "[ADSP-BF526 EZ-Board Schematic](#)" on page B-1  
Provides the resources to allow EZ-Board board-level debugging or to use as a reference design. Appendix B is part of the online Help.



## What's New in This Manual

This is the first revision of the ADSP-BF526 EZ-Board Evaluation System Manual.

## Technical or Customer Support

You can reach Analog Devices, Inc. Customer Support in the following ways:

- Visit the Embedded Processing and DSP products Web site at [http://www.analog.com/processors/technical\\_support](http://www.analog.com/processors/technical_support)
- E-mail tools questions to [processor\\_tools.support@analog.com](mailto:processor_tools.support@analog.com)
- E-mail processor questions to [processor.support@analog.com](mailto:processor.support@analog.com) (World wide support)  
[processor.europe@analog.com](mailto:processor.europe@analog.com) (Europe support)  
[processor.china@analog.com](mailto:processor.china@analog.com) (China support)
- Phone questions to **1-800-ANALOGD**
- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:  
Analog Devices, Inc.  
One Technology Way  
P.O. Box 9106  
Norwood, MA 02062-9106  
USA

# Supported Processors

This evaluation system supports Analog Devices ADSP-BF526 Blackfin embedded processors.

## Product Information

Product information can be obtained from the Analog Devices Web site, VisualDSP++ online Help system, and a technical library CD.

## Analog Devices Web Site

The Analog Devices Web site, [www.analog.com](http://www.analog.com), provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to [http://www.analog.com/processors/technical\\_library](http://www.analog.com/processors/technical_library). The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, [MyAnalog.com](http://MyAnalog.com) is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. [MyAnalog.com](http://MyAnalog.com) provides access to books, application notes, data sheets, code examples, and more.

Visit [MyAnalog.com](http://MyAnalog.com) to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

## VisualDSP++ Online Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, Dinkum Abridged C++ library, and FLEXnet License Tools software documentation. You can search easily across the entire VisualDSP++ documentation set for any topic of interest.

For easy printing, supplementary Portable Documentation Format (.pdf) files for all manuals are provided on the VisualDSP++ installation CD.

Each documentation file type is described as follows.

File	Description
.chm	Help system files and manuals in Microsoft help format
.htm or .html	Dinkum Abridged C++ library and FLEXnet License Tools software documentation. Viewing and printing the .html files requires a browser, such as Internet Explorer 6.0 (or higher).
.pdf	VisualDSP++ and processor manuals in PDF format. Viewing and printing the .pdf files requires a PDF reader, such as Adobe Acrobat Reader (4.0 or higher).

## Technical Library CD

The technical library CD contains seminar materials, product highlights, a selection guide, and documentation files of processor manuals, VisualDSP++ software manuals, and hardware tools manuals for the following processor families: Blackfin, SHARC, TigerSHARC, ADSP-218x, and ADSP-219x.

To order the technical library CD, go to [http://www.analog.com/processors/technical\\_library](http://www.analog.com/processors/technical_library), navigate to the manuals page for your processor, click the request CD check mark, and fill out the order form.

## Product Information

Data sheets, which can be downloaded from the Analog Devices Web site, change rapidly, and therefore are not included on the technical library CD. Technical manuals change periodically. Check the Web site for the latest manual revisions and associated documentation errata.

## Related Documents

For information on product related development software, see the following publications.

Table 1. Related Processor Publications

Title	Description
<i>ADSP-BF526 Blackfin Embedded Processor Data Sheet</i>	General functional description, pinout, and timing.
<i>ADSP-BF52x Blackfin Processor Hardware Reference</i>	Description of internal processor architecture and all register functions.
<i>Blackfin Processor Programming Reference</i>	Description of all allowed processor assembly instructions.

Table 2. Related VisualDSP++ Publications

Title	Description
<i>ADSP-BF526 EZ-Board Evaluation System Manual</i>	Description of the hardware capabilities of the evaluation system; description of how to access these capabilities in the VisualDSP++ environment.
<i>VisualDSP++ User's Guide</i>	Description of VisualDSP++ features and usage.
<i>VisualDSP++ Assembler and Preprocessor Manuals</i>	Description of the assembler function and commands.
<i>VisualDSP++ C/C++ Compiler and Library Manual for Blackfin Processors</i>	Description of the compiler function and commands for Blackfin processors.
<i>VisualDSP++ Linker and Utilities Manual</i>	Description of the linker function and commands.

Table 2. Related VisualDSP++ Publications (Cont'd)




Title	Description
<i>VisualDSP++ Loader and Utilities Manual</i>	Description of the loader/splitter function and commands.
<i>VisualDSP++ Device Drivers and System Services Manual for Blackfin Processors</i>	Description of the device drivers' and system services' functions and commands.

## Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
<b>Close</b> command ( <b>File</b> menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the <b>Close</b> command appears on the <b>File</b> menu).
{this   that}	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as this or that. One or the other is required.
[this   that]	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional this or that.
[this, ...]	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipsis; read the example as an optional comma-separated list of this.
.SECTION	Commands, directives, keywords, and feature names are in text with letter gothic font.
<i>filename</i>	Non-keyword placeholders appear in text with italic style format.

## Notation Conventions

Example	Description
	<p><b>Note:</b> For correct operation, ...</p> <p>A Note provides supplementary information on a related topic. In the online version of this book, the word <b>Note</b> appears instead of this symbol.</p>
	<p><b>Caution:</b> Incorrect device operation may result if ...</p> <p><b>Caution:</b> Device damage may result if ...</p> <p>A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word <b>Caution</b> appears instead of this symbol.</p>
	<p><b>Warning:</b> Injury to device users may result if ...</p> <p>A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word <b>Warning</b> appears instead of this symbol.</p>

# 1 USING ADSP-BF526 EZ-BOARD

This chapter provides specific information to assist you with development of programs for the ADSP-BF526 EZ-Board evaluation system.

The following topics are covered.

- “Package Contents” on page 1-3
- “Default Configuration” on page 1-4
- “EZ-Board Installation” on page 1-4
- “EZ-Board Session Startup” on page 1-7
- “Evaluation License Restrictions” on page 1-9
- “Memory Map” on page 1-9
- “SDRAM Interface” on page 1-12
- “Parallel Flash Memory Interface” on page 1-12
- “NAND Flash Interface” on page 1-13
- “SPI Interface” on page 1-14
- “Parallel Peripheral Interface (PPI)” on page 1-15
- “Rotary Encoder Interface” on page 1-16
- “Ethernet Interface” on page 1-17
- “Audio Interface” on page 1-18

- “USB OTG Interface” on page 1-19
- “UART Interface” on page 1-20
- “RTC Interface” on page 1-21
- “LEDs and Push Buttons” on page 1-22
- “JTAG Interface” on page 1-24
- “Land Grid Array” on page 1-24
- “Expansion Interface II” on page 1-25
- “Power Architecture” on page 1-26
- “Power Setup” on page 1-28
- “Power Saving Features” on page 1-30
- “Power Measurements” on page 1-31
- “Power-On-Self Test” on page 1-32
- “Example Programs” on page 1-32
- “Background Telemetry Channel” on page 1-32
- “Design Reference Information” on page 1-33

For information about VisualDSP++, including the boot loading, target options, and other facilities, refer to the online Help.

For more information about the ADSP-BF526 Blackfin processor, see documents referred to as “[Related Documents](#)”.



## Package Contents

Your ADSP-BF526 EZ-Board evaluation system package contains the following items.

- ADSP-BF526 EZ-Board
- *VisualDSP++ Installation Quick Reference Card*
- CD containing:
  - ✓ VisualDSP++ software
  - ✓ ADSP-BF526 EZ-Board debug software
  - ✓ USB driver files
  - ✓ Example programs
  - ✓ *ADSP-BF526 EZ-Board Evaluation System Manual*
- Universal 5.0V DC power supply
- 7-foot Ethernet patch cable
- Two 6-foot 3.5 mm male-to-male audio cables
- Two 10-foot mini USB 2.0 cables for USB on-the-go (OTG)

If any item is missing, contact the vendor where you purchased your EZ-Board or contact Analog Devices, Inc.

# Default Configuration

The ADSP-BF526 EZ-Board board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

The EZ-Board evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-Board in the protective shipping package.



When removing the EZ-Board from the package, handle the board carefully to avoid the discharge of static electricity, which can damage some components. [Figure 1-1](#) shows the default jumper and switch settings, connector locations, and LEDs used in installation. Confirm that your board is in the default configuration before using the board.

## EZ-Board Installation

For correct operation, install the software in the order presented in the *VisualDSP++ Installation Quick Reference Card*. Substitute instructions in step 3 with instructions in this section.

There are two options to connect the EZ-Board hardware to a personal computer (PC) running VisualDSP++ 5.0: via an Analog Devices emulator or via a standalone debug agent module. The standalone debug agent allows a debug agent to interface to the ADSP-BF526 EZ-Board. The standalone debug agent is shipped with the kit.

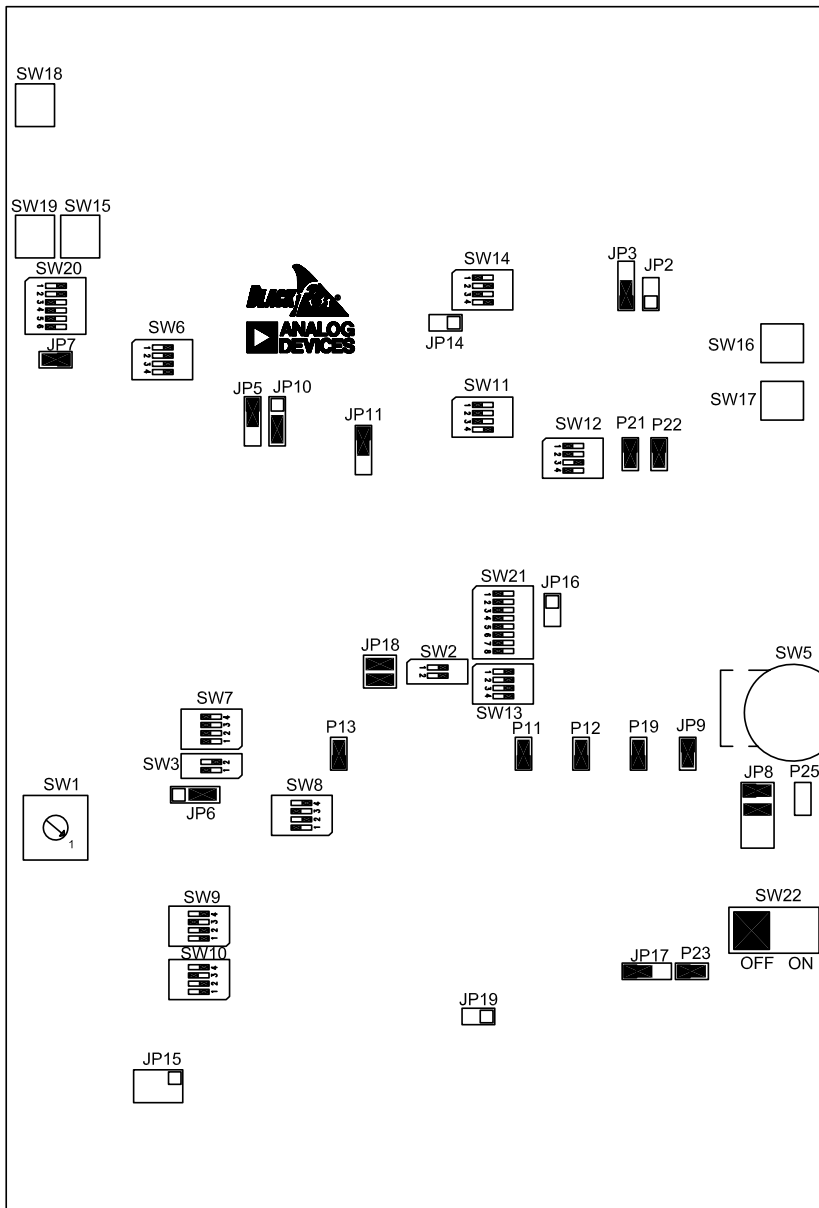


Figure 1-1. Default EZ-Board Hardware Setup

## EZ-Board Installation

### To connect the EZ-Board to a PC via an emulator:

1. Set up the EZ-Board for either battery power or wall/USB power; see [“Power Setup” on page 1-28](#).
2. Attach the emulator header to connector P1 (labeled JTAG) on the back side of the EZ-Board.
3. Depending on the power source for the EZ-Board, do one of the following.
  - Turn ON switch SW22 (battery)
  - Plug the 5V wall adaptor into connector P14 (labeled 5.0V)
4. Plug the mini plug of the provided USB cable into connector P8 (labelled USB OTG). Plug the standard USB plug into a USB port of the PC running VisualDSP++ 5.0 update 4 or newer.

### To connect the EZ-Board to a PC via a standalone debug agent:



The debug agent can be used only when power is supplied from the wall adaptor.

1. Attach the standalone debug agent to connectors P1 (labeled JTAG) and ZP1 on the backside of the EZ-Board, watching for the keying pin of P1 to connect correctly. Plug the 5V adaptor into connector P14 (labeled 5.0V).
2. Plug one side of the provided USB cable into the USB connector (ZP1) of the standalone debug agent. Plug the other side of the cable into a USB port of the PC running VisualDSP++ 5.0 update 4 or newer.

The other USB connector on the ADSP-BF526 EZ-Board (labelled USB OTG, P8) is for applications use.

3. Verify that the yellow USB monitor LED on the standalone debug agent (LED4, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and ready to run VisualDSP++.

## EZ-Board Session Startup

1. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start**→**Programs** menu. The main window appears. Note that VisualDSP++ is not connected to any session. Skip the rest of this step to step 2.

If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 3.

2. To connect to a new EZ-KIT Lite session, start **Session Wizard** by selecting one of the following.
  - From the **Session** menu, **New Session**.
  - From the **Session** menu, **Session List**. Then click **New Session** from the **Session List** dialog box.
  - From the **Session** menu, **Connect to Target**.
3. The **Select Processor** page of the wizard appears on the screen. Ensure **Blackfin** is selected in **Processor family**. In **Choose a target processor**, select **ADSP-BF526**. Click **Next**.

## EZ-Board Session Startup


4. The **Select Connection Type** page of the wizard appears on the screen. For standalone debug agent connection, select **EZ-KIT Lite** and click **Next**. For emulator connection select **Emulator**, and click **Next**
5. The **Select Platform** page of the wizard appears on the screen. For standalone debug agent connection, ensure that the selected platform is **ADSP-BF526 EZ-KIT Lite via Debug Agent**. For emulator connection chose the type of emulator that is connected. Specify your own **Session name** for the session or accept the default name.

The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and to open a new session.

Click **Next**.

6. The **Finish** page of the wizard appears on the screen. The page displays your selections. Check the selections. If you are not satisfied, click **Back** to make changes; otherwise, click **Finish**. VisualDSP++ creates the new session and connects to the EZ-Board. Once connected, the main window's title is changed to include the session name set in step 5.



To disconnect from a session, click the disconnect button  or select **Session**→**Disconnect from Target**.

To delete a session, select **Session** → **Session List**. Select the session name from the list and click **Delete**. Click **OK**.

## Evaluation License Restrictions

The ADSP-BF526 EZ-Board installation is part of the VisualDSP++ installation. The EZ-Board is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ restricts a connection to the ADSP-BF526 EZ-Board via the USB port of the standalone debug agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a user's program to 20 KB of memory for code space with no restrictions for data space.
- The EZ-Board hardware must be connected and powered up to use VisualDSP++ with a valid evaluation or permanent license.

Refer to the *VisualDSP++ Installation Quick Reference Card* for details.

## Memory Map

The ADSP-BF526 processor has internal static random access memory (SRAM) used for instructions and data storage. See [Table 1-1](#). The internal memory details can be found in the *ADSP-BF52x Blackfin Processor Hardware Reference*.

The ADSP-BF526 EZ-Board includes four types of external memory: synchronous dynamic random access memory (SDRAM), serial peripheral interconnect (SPI), parallel flash, and NAND flash. See [Table 1-2](#). For more information about a specific memory type, go to the respective section in this chapter.

# Memory Map

Table 1-1. EZ-Board Internal Memory Map

Start Address	Content
0xEF00 0000	BOOT ROM (32K BYTE)
0xEF00 8000 0xFEBO 0000 0xFEB2 0000 0xFF40 0000 0xFF40 4000 0xFF40 8000 0xFF50 0000 0xFF50 4000 0xFF50 8000 0xFF60 0000 0xFF60 4000 0xFF60 8000 0xFF60 C000 0xFF61 0000 0xFF61 4000 0xFF70 0000 0xFF70 1000	Reserved
0xFF80 0000	L1 DATA BANKA SRAM (16K BYTE)
0xFF80 4000	L1 DATA BANKA SRAM/CACHE (16K BYTE)
0xFF80 8000	Reserved
0xFF90 0000	L1 DATA BANKB SRAM (16K BYTE)
0xFF90 4000	L1 DATA BANKB SRAM/CACHE (16K BYTE)
0xFF90 8000	Reserved
0xFFA0 0000	L1 INSTRUCTION BANKA LOWER SRAM (16K BYTE)
0xFFA0 4000	L1 INSTRUCTION BANKA UPPER SRAM (16K BYTE)
0xFFA0 8000	L1 INSTRUCTION BANKB LOWER SRAM (16K BYTE)
0xFFA0 C000	Reserved
0xFFA1 0000	L1 INSTRUCTION SRAM/CACHE (16K BYTE)



Table 1-1. EZ-Board Internal Memory Map (Cont'd)

Start Address	Content
0xFFA1 4000 0xFFA1 8000 0xFFA1 C000 0xFFA2 0000 0xFFA2 4000	Reserved
0xFFB0 0000	L1 SCRATCHPAD SRAM (4K BYTE)
0xFFB0 1000	Reserved
0xFFC0 0000	SYSTEM MMR REGISTERS
0xFFE0 0000	CORE MMR REGISTERS

Table 1-2. EZ-Board External Memory Map

Start Address	End Address	Content
0x0000 0000	0x03FF FFFF	SDRAM bank 0 (SDRAM)
0x2000 0000	0x200F FFFF	ASYNC memory bank 0 (flash)
0x2010 0000	0x201F FFFF	ASYNC memory bank 1 (flash)
0x2020 0000	0x202F FFFF	ASYNC memory bank 2 (flash)
0x2030 0000	0x203F FFFF	ASYNC memory bank 3 (flash)
0x2040 0000	0xEEFF FFFF	Reserved

# SDRAM Interface

The ADSP-BF526 processor connects to a 64 MB Micron MT48H32M16-75 chip through the external bus interface unit (EBIU). The SDRAM chip can operate at a maximum clock frequency of 80 MHz, which is the ADSP-BF526 processor limitation.

With a VisualDSP++ session running and connected to the EZ-Board via the USB standalone debug agent, the SDRAM registers are configured automatically each time the processor is reset. The values are used whenever SDRAM is accessed through the debugger (for example, when viewing memory windows or loading a program).

To disable the automatic setting of the SDRAM registers, select **Target Options** from the **Settings** menu in VisualDSP++ and uncheck **Use XML reset values**. For more information on changing the reset values, refer to the online Help.

An example program is included in the EZ-Board installation directory to demonstrate how to setup and access the SDRAM interface. For more information on how to initialize the registers after a reset, search the VisualDSP++ online Help for “reset values”.

## Parallel Flash Memory Interface

The parallel flash memory interface of the ADSP-BF526 EZ-Board contains a 4 MB (2M x 16 bits) 1.8V Numonyx M58WR032KB chip. Flash memory connects to the 16-bit data bus and address lines 1 through 19. Chip enable is decoded by the  $AMS0-3$  select lines through NAND and AND gates. The address range for flash memory is  $0x2000000$  to  $0x203FFFF$ .

Flash memory is pre-loaded with boot code for the blink and power-on-self test (POST) programs. For more information, refer to [“Power-On-Self Test” on page 1-32](#). Flash memory also is preloaded with configuration flash information, which contains board revision, BOM revision, and other data.

By default, the EZ-Board boots from the 16-bit parallel flash memory. The processor boots from flash memory if the boot mode select switch (SW1) is set to a position of 1 (see [“Boot Mode Select Switch \(SW1\)” on page 2-10](#)).

Flash memory code can be modified. For instructions, refer to the online Help and example program included in the EZ-Board installation directory.

## NAND Flash Interface

The ADSP-BF526 processor is equipped with an internal NAND flash controller, which allows the 2 Gb 1.8V ST Micro’s NAND02 device to be attached gluelessly to the processor. NAND flash is attached via the processor’s specific NAND flash control and data lines. NAND flash shares pins with the Ethernet PHY, host connector, and expansion interface II.

The NAND chip enable signal (NDCE#\_HOSTD10) can be disconnected from NAND flash by turning SW13.4 (switch 13 position 4) OFF. This ensures that NAND flash is not driving data when HOSTD10 changes state. See [“Rotary/NAND Enable Switch \(SW13\)” on page 2-14](#) for more information.

## SPI Interface

The Ethernet PHY (U29) must be disabled in order for NAND flash to function properly. This is accomplished by setting switch SW12 to OFF, OFF, ON, OFF.

For more information about the NAND02 device, refer to the Numonyx Web site:

<http://www.numonyx.com/en-US/MemoryProducts/NAND/Pages/SLCLargePage.aspx>.

An example program is included in the EZ-Board installation directory to demonstrate how to setup and access the NAND flash interface.

## SPI Interface

The ADSP-BF526 processor has one serial peripheral interface (SPI) port with multiple chip select lines. The SPI port connects directly to serial flash memory, audio codec, and expansion interface II.

Serial flash memory is a 4 Mb SST SST25WF040 device, which is selected using the SPI SEL1 line of the processor.

SPI flash memory is factory programmed with Das U-Boot—the universal boot loader. Das U-Boot (*U-Boot* for short) is open source firmware for embedded processors, including the ADSP-BF526 Blackfin processors. U-Boot can load files from a variety of peripherals, such as a serial connection, an Ethernet network connection, or flash memories. U-Boot is executed at system reset, which automatically loads up another application (such as the Linux kernel or a stand alone application). U-Boot can parse many types of files on many types of storage devices.

U-Boot is controlled via a serial communications, the default setting is 56700 baud, 8 data bits, No parity, 1 stop bit. See “[RS-232 Connector \(J2\)](#)” on page 2-33 for information on the serial connector.

For more information about U-Boot, refer to the online documentation: <http://docs.blackfin.uclinux.org/doku.php?id=bootloaders:u-boot>. For U-Boot support on the Blackfin processors, refer to the online help forums:

[http://blackfin.uclinux.org/gf/project/u-boot/forum/?action=ForumBrowse&forum\\_id=51](http://blackfin.uclinux.org/gf/project/u-boot/forum/?action=ForumBrowse&forum_id=51).

SPI flash can be modified. For instructions, refer to the VisualDSP++ online Help, example program included in the EZ-Board installation directory, and U-Boot documentation. U-Boot includes an SPI flash driver and can be used to download a new file over Ethernet or serial connection, and write that to SPI flash.

By default, the EZ-Board boots from the 16-bit flash parallel memory. SPI flash can be selected as the boot source by setting the boot mode select switch (SW1) to position 3 (see “[Boot Mode Select Switch \(SW1\)](#)” on [page 2-10](#)).

By default, the audio codec is set up to use the SPI SEL5 signal as the SPI chip select when configuring the codec. The chip select is shared with the HOSTD9 signal. For more information, refer to “[Audio Interface](#)” on [page 1-18](#).

## Parallel Peripheral Interface (PPI)

The ADSP-BF526 processor provides a parallel peripheral interface (PPI), supporting data widths up to 16 bits. The PPI interface provides three multiplexed frame syncs, a dedicated clock input, and 16 data lines. The full PPI port is accessible on the expansion interface II connector (P3).

## Rotary Encoder Interface

The PPI signals connect to multi-function pins; the upper eight data bit signals are configured for the rotary, SPI, UART1, and LED0 interfaces. To use the upper eight PPI data lines at connector P3, change the board as follows: disable rotary switch (SW13 positions 1–3 OFF) and disable the UART1 interface (remove a jumper from JP3). LED0 mimics the PPI D8 data pin.

The PPI has a dedicated clock, generated from the expansion interface II. The PPI is not used on the EZ-Board, intended for use on the expansion interface II.

## Rotary Encoder Interface

The ADSP-BF526 processor has a built-in, up-down counter with support for a rotary encoder. The three-wire rotary encoder interface connects to the thumbwheel rotary switch (SW13) and expansion interface II connector (P3). The rotary encoder can be turned clockwise for the up function, counter clockwise for the down function, or can be pushed towards the center of the board to clear the counter.

The rotary switch is a two-bit quadrature (gray code) counter with a detent, meaning that both the down signal (CDG) and up signal (CUD) toggle when the count register increases on a rotation to the right. Upon rotating to the left, CDG and CUD toggle, and the overall count decreases.

If the processor pins are needed for the expansion interface II, disconnect the rotary encoder switch via the four-position rotary/NAND enable switch (SW13). [For more information, see “Rotary/NAND Enable Switch \(SW13\)” on page 2-14.](#)

An example program is included in the EZ-Board installation directory to demonstrate how to set up and access the rotary encoder interface.

## Ethernet Interface

The ADSP-BF526 processor has an integrated Ethernet MAC with media independent interface (MII) and reduced media independent interface (RMII), which connects to an external PHY. The EZ-Board provides a SMSC LAN8700 RMII Ethernet PHY with Auto-MDIX, fully compliant with IEEE 802.2/802.2u standards. The SMSC LAN8700 chip supports 10BASE-T and 100BASE-TX operations. The part is attached gluelessly to the processor.

The Ethernet signals are shared with NAND flash; by default, the Ethernet mode is set OFF (SW12 OFF, OFF, ON, OFF). See [“ETH Enable Switch \(SW12\)” on page 2-14](#) for more information.



It is important not to run code that accesses NAND flash while using the Ethernet interface.

The Ethernet mode is set by the SW11 switch and defaults to all capable, auto negotiation with settings OFF, OFF, OFF, ON. See [“ETH Mode Flash CS Switch \(SW11\)” on page 2-13](#) for more information.

The Ethernet chip is pre-loaded with a MAC address. The MAC address for the EZ-Board is stored in the configuration flash section of the parallel flash memory and can be found on a sticker on the bottom side of the board.

The PHY portion of the Ethernet chip connects to a Pulse HX1188 magnetics (U28), then to a standard RJ-45 Ethernet connector (J5). [For more information, see “Ethernet Connector \(J5\)” on page 2-34.](#)

Example programs are included in the EZ-Board installation directory to demonstrate how to use the Ethernet interface.

In low-power consumption applications that do not require Ethernet, the P21–22 jumpers can be removed to disconnect the power from the LAN8700 PHY and Ethernet oscillator. [For more information, see “ETH PWR Jumpers \(P21–22\)” on page 2-27.](#)

# Audio Interface

The audio interface of the EZ-Board consists of a low-power stereo codec, WM8731L, with an integrated headphone driver and associated passive components. There are two inputs, a stereo line in, and a mono microphone, as well as two outputs, a headphone, and a stereo line out. The codec has integrated stereo analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) and requires minimal external circuitry.

The codec connects to the ADSP-BF526 processor via the processor's serial port 0A (alternate). The `SPORT0A` port is disconnected from the codec by turning switches `SW2` and `SW7` OFF, which enable `SPORT0A` on the expansion interface II. See [“SPORT0A ENBL Switches \(SW2 and SW7\)” on page 2-11](#) for more information.

The control interface for the codec is selected by switching `SW8` and `SW10` between the 2-wire interface (TWI) and SPI. The board default is SPI mode, set by the `SW10` switch (ON, OFF, ON, OFF) and `SW8` switch (positions 3 ON and 4 OFF). To select TWI mode, set `SW8` position 3 OFF and position 4 ON, as well as `SW19` OFF, ON, OFF, ON. Refer to [“Mic/HP LPBK, Audio Mode Switch \(SW10\)” on page 2-13](#) and [“SPI/TWI Switch \(SW8\)” on page 2-12](#) for more information.

Mic gain values of 14 dB, 0 dB, or -6 dB are selectable through the `SW9` switch by turning ON position 1, 2, or 3 (respectively). All other positions must be OFF to achieve the desired gain. For more information, see [“MIC Gain Switch \(SW9\)” on page 2-12](#).

Microphone bias is provided through a low-noise reference voltage. A jumper on positions 2&3 of `JP6` connects the `MICBIAS` signal to the audio jack. Placing a jumper on positions 1&2 of `JP6` connects the bias directly to the mic signal. For more information, see [“MIC Select Jumper \(JP6\)” on page 2-22](#).




J3 and J4 are 3.5 mm connectors for the audio portion of the board. J4 connects the mic on the top portion and line-in on the bottom. J3 connects the headphone on the top portion and line-out on the bottom. If there is no 3.5 mm cable plugged into the bottom of either J3 or J4, the signals are looped back inside the connector. [For more information, see “Dual Audio Connectors \(J3–4\)” on page 2-33.](#)

For testing, SW10 positions 1&2 connect the MIC IN signal to either the left or right headphone. Do not connect the left and right to the MIC IN signal at the same time—only position 1 or 2 of SW10 should be ON at the same time. [For more information, see “Mic/HP LPBK, Audio Mode Switch \(SW10\)” on page 2-13.](#)

The EZ-Board is shipped with two 3.5 mm cables, which allow you to run the example programs provided in the EZ-Board installation directory and learn about the audio interface.

## USB OTG Interface

The ADSP-BF526 processor has a built-in, high-speed USB OTG interface and integrated PHY. The interface connects to a 24 MHz crystal (Y2), has a surge protector, and can be configured as a host or a device. When in device mode, the USB 5V FET switch (U23) is turned OFF. When in host mode, the ADSP-BF526 EZ-Board can supply 5V to a device, if desired.

 A 5V, 500 mA current can be supplied only when the EZ-Board is powered from the 5V wall source.

The 5V supplied to an external USB device is controlled by the PG13 flag pin of the processor. PG13 must be connected on the board to signal USB\_VRSEL through switch SW20. The USB\_VRSEL signal controls an Analog Devices ADM869L p-channel FET, which has an active low ON pin. By default, USB\_VRSEL is held high or a logic ‘1’ via a pull-up resistor and disconnects the 5V wall supply to VBUS. To set host mode and provide 5V to

## UART Interface

a device, set SW20 positions 2&5 OFF and position 6 ON. This disables push button 2. Note that signal HOSTADDR is shared with push button 2; do not use the push button when controlling the USB\_VRSEL signal.

By default, SW20 positions 2, 5, and 6 are ON, OFF, and OFF (respectively) and shut off the p-channel FET (U23). For more information, see “GPIO Enable Switch (SW20)” on page 2-17.

The USB OTG interface has a mini-AB connector (P8); a cable that plugs into P8 is shipped with the EZ-Board.

Use the example programs in the EZ-Board installation directory to learn about the ADSP-BF526 processor’s device and host modes. For more information about the USB interface, refer to the *ADSP-BF52x Blackfin Processor Hardware Reference*.

## UART Interface

The ADSP-BF526 processor has two built-in universal asynchronous receiver transmitters (UARTs). UART0–1 share the processor pins with other peripherals on the EZ-Board.

UART1 has full RS-232 functionality via the Analog Devices 3.3V ADM1385 line driver and receiver (U21). The ADSP-BF526 processor is running at the VDDEXT voltage of 1.8V, requiring a voltage translator (U32) to translate the 1.8V processor signals to the UART 3.3V line transceiver.

The UART1 interface is disconnected from the ADM1385 transceiver by ensuring that no jumper is installed on JP3. The ADM1385 transceiver is shut down by placing a jumper on JP14. The UART1 interface is controlled by the inverted WAKEUP\_OUT signal,  $\sim$ WAKEUP\_OUT. To set up  $\sim$ WAKEUP\_OUT, place a jumper on the JP3 positions 1&2. A jumper on positions 1&2 of JP3 disables the voltage translator, disconnecting the ADM1385 device from the UART1 interface of the processor. This JP3 setting does not shut


down the transceiver. For more information on power saving capabilities of the EZ-Board, see “[UART Enable Jumper \(JP3\)](#)” on page 2-21 and “[UART SD Jumper \(JP14\)](#)” on page 2-24.

SW14 allows the flow control signals to be looped back. See “[UART Setup Switch \(SW14\)](#)” on page 2-15 for more information.

When using UART1, do not install jumper JP2. JP2 is a UART loopback jumper and should be installed only when running the POST program. If signals RTS and CTS are needed for flow control, the UART1RTS port pin PF10 can be configured as a general-purpose I/O (GPIO) pin for RTS. The HWAIT port pin PG0 can be used for CTS by setting up the pin accordingly; see “[UART Loopback Jumper \(JP2\)](#)” on page 2-21 and “[UART Enable Jumper \(JP3\)](#)” on page 2-21 for more information.

UART0 and UART1 are connected to the expansion interface II at connectors P2 and P4. For more information, see “[Expansion Interface II Connectors \(P2 and P4\)](#)” on page 2-35.

Example programs are included in the EZ-Board installation directory to demonstrate UART and RS-232 operations.

 On the processor, UART1 shares pins with the PPI interface; consequently, do not use UART1 at the same time as the PPI interface. To disable the UART line drive, ensure that JP3 has no jumpers on.

For more information on the UART interface, refer to the *ADSP-BF52x Blackfin Processor Hardware Reference*.


## RTC Interface

The ADSP-BF526 processor has a real-time clock (RTC) and a watchdog timer. Typically, the RTC interface is used to implement a real-time watchdog or a life counter of the time elapsed since the last system reset. The EZ-Board is equipped with a Panasonic CR1632 lithium coin, 3V battery supplying 125 mAh. The 3V battery and 3.3V supply of the board

## LEDs and Push Buttons

connect to the `RTC` power pin of the processor. When the EZ-Board is powered, the RTC circuit uses the board power to supply voltage to the `RTC` pin. When the EZ-Board is not powered, the RTC circuit uses the lithium battery to maintain the power to the `RTC` pin. After removing the mylar, the battery lasts for about one year with the EZ-Board unpowered.

Example programs are included in the EZ-Board installation directory to demonstrate the RTC features.

 The EZ-Board is shipped with a protective Mylar sheet placed between the coin battery and positive pin of the battery holder. Remove the Mylar sheet before using the RTC in the processor.

For more information on the RTC and watchdog timer, refer to the *ADSP-BF52x Blackfin Processor Hardware Reference*.

## LEDs and Push Buttons

The EZ-Board provides two push buttons and three LEDs for general-purpose I/O, as well as two additional push buttons intended for power down and wake functionality, which also can be used as GPIO flag pins.

The three LEDs, labeled `LED0` through `LED2`, are accessed via the `PF8`, `PG11`, and `PG12` pins of the processor (respectively). For information on how to program the flag pins, refer to the *ADSP-BF52x Blackfin Processor Hardware Reference*.

`LED1` is shared with the `HOSTWR#` signal, while `LED2` is shared with the `HOS-TACK` signal. The `LED0` signal is shared with the `PPI D8` signal. When using the PPI 16-bit data interface, `LED0` mimics `PPI D8`.

The `LED1` and `LED2` signals also connect to the expansion interface II (connectors `J1`, `P2`, and `P4`). See [“Expansion Interface II Connector \(J1\)” on page 2-33](#) and [“Expansion Interface II Connectors \(P2 and P4\)” on page 2-35](#) for more information.

The two general-purpose push buttons are labeled PB1 and PB2. The status of each individual button can be read through programmable flag inputs PGO and PG13. The flag reads '1' when a corresponding switch is being pressed. When the switch is released, the flag reads '0'. A connection between the push buttons and processor inputs is established through positions 1&2 of the DIP switch, SW20.

Push buttons 1 and 2 of SW20 are used as GPIO signals on the expansion interface II connectors (J1, P2, P4). To use the PGO and PG13 port pins as GPIO signals on the expansion interface II, turn SW20 positions 1&2 OFF.

Push button 1 cannot be used when PGO is set up to control the charge rate, when charging the battery over USB. To set this up, turn SW20. 1 OFF. See [“CHG GPIO Jumper \(JP15\)” on page 2-24](#) for more information.

Push button 2 can be connected to the USB\_VRSEL signal by setting switches SW13. 2 OFF, SW20. 5 OFF, and SW20. 6 ON. The USB\_VRSEL signal allows the USB OTG interface to power an external USB device with 5V. Push button 2 also can be connected to the OTP\_FLAG signal, which is necessary to supply 7V for writing to OTP. To set up the EZ-Board to control the OTP\_FLAG signal, set switches SW13. 2 OFF, SW20. 5 ON, and SW20. 6 OFF. Push button 2 is shared with signal HOSTADDR. See [“USB OTG Interface” on page 1-19](#) and [“GPIO Enable Switch \(SW20\)” on page 2-17](#) for more information.

For a power down interrupt, signal LED2\_HOSTACK is wired to SW20. 3 (GPIO enable switch), which allows a push button (SW16) to drive an interrupt to the ADSP-BF526 processor. The PG12 port pin of the processor should be set up as a GPIO pin. Turning switch SW20. 3 ON connects the push button (SW16) to the processor. By default, SW20. 3 is OFF.

A wake interrupt can be set up by turning switch SW20. 4 ON and setting the processor's flag pin PG15 as the wake interrupt. When push button SW17 (labelled WAKE) is pressed, PG15 receives a low-to-high transition. The PG15

## JTAG Interface

processor pin is shared with the audio codec (U31), Ethernet PHY (U29), and HOSTCE signal. Do not use these features when using the wake interrupt push button.

An example program is included in the ADSP-BF526 installation directory to demonstrate functionality of the LEDs and push buttons.

## JTAG Interface

The JTAG connector (P1) allows the standalone debug agent to connect a debug session to the ADSP-BF526 processor. The debug agent operates only when the external 5V wall adaptor is used (P14). When operating the EZ-Board from a battery or USB bus power, the debug agent is not powered.

The standalone debug agent can be removed, and an external emulator can be attached to the EZ-Board. Be careful not to damage the connectors when removing the debug agent. The emulator connects to P1 on the back side of the board. See “EZ-Board Installation” on page 1-4 for more information. for more information.

For more information about emulators, contact Analog Devices or go to: <http://www.analog.com/processors/blockfi n/evaluation/development/crosscore/>.

## Land Grid Array

The ADSP-BF526 EZ-Board has provisions for probing every port pin and the EBIU interface of the processor on connectors P5, P6, and P7. The connector locations are intended for use with a Tektronix DMAX logic analyzer connector, but can be probed with any oscilloscope or logic analyzer. Connectors P5 and P6 require the primary retention posts, while

connector P7 can use either the primary or secondary retention post. For pinout information, refer to “[ADSP-BF526 EZ-Board Schematic](#)” on [page B-1](#).

For more information on the Tektronix DMAX logic analyzer interface, go to the Tektronix Web site.

## Expansion Interface II

The expansion interface II allows an Analog Devices EZ-Extender or a custom-design daughter board to be tested across various hardware platforms that have the same expansion interface.

The expansion interface II implemented on the ADSP-BF526 EZ-Board consists of four connectors, three of which are 0.1 in. shrouded headers (P2–4) and the last of which is a Samtec QMS series header (J1). The connectors contain a majority of the ADSP-BF526 processor signals. For the pinout of the connectors, go to “[ADSP-BF526 EZ-Board Schematic](#)” on [page B-1](#). The mechanical dimensions of the expansion connectors can be obtained by contacting [Technical or Customer Support](#).


For more information about daughter boards, visit the Analog Devices Web site at:

<http://www.analog.com/processors/blockfi n/evaluation/development/crosscore/>.

Limits to current and interface speed must be taken into consideration when using the expansion interface II. Current for the expansion interface II is sourced from the EZ-Board, therefore, the current should be limited to 1A for 5V and 500 mA for the 1.8V planes. When a battery supplies power to the EZ-Board, the expansion interface II 5V current is reduced to 400mA. If more current is required, then a separate power connector

## Power Architecture

and a regulator must be designed on a daughter card. Additional circuitry can add extra loading to signals, decreasing their maximum effective speed.

 Analog Devices does not support and is not responsible for the effects of additional circuitry.

## Power Architecture

The ADSP-BF526 EZ-Board has three primary voltage sources, a lithium ion battery (740 mAh), a 5V wall adaptor, and  $V_{BUS}$  supplied over a USB cable. There is an OR'ing opamp circuit, which allows the board to draw power from any supply source that has the highest voltage potential. For example, if the battery is turned on while the board is plugged into the 5V wall adaptor (P14), the board runs from the 5V wall adaptor.

The VDDEXT, VDDMEM, and SDRAM power are 1.8V and supplied by an ADP2105 regulator (VR3).

The ADSP-BF526 core voltage, VDDINT, is selected via the I<sup>2</sup>C interface of the processor. The default is 1.4V. An I<sup>2</sup>C voltage translator (U39) interfaces the 1.8V signals SDA and SCL of the processor to the AD5258 digipot (U34). The digipot sets the feedback resistors for a low drop-out (LDO) regulator ADP1715 (VR5). See the POST example located in the ADSP-BF526 directory of VisualDSP++ to learn how to change the VDDINT voltage.


The 3.3V power for the board is regulated by an ADP2105 converter (VR2).

The expansion interface II is equipped with three voltage domains: 5V, 3.3V, and 1.8V. The 1.8V and 3.3V are provided directly through the VR2 and VR3 regulators. The 5V is sourced from the wall adaptor when jumper JP8 is set to positions 1&2, 3&4, and JP9 is ON. The 5V also can be pro-




vided by the on-board ADP1611 converter when using the lithium ion battery. To set up the ADP1611 converter (VR7), install jumpers on positions 5&6, and 7&8 of JP8 and ensure JP9 is OFF.

To write to the OTP memory inside the processor, turn SW20. 2 OFF, SW20. 5 ON, and SW20. 6 OFF. Also install a jumper on JP16. Now the PG13 flag pin of the processor, when driven high, provides a precise 7.0V for OTP writes. Ensure that the PG13 flag pin is driven low when not writing to the OTP memory: there is a limited amount of time that the OTP circuit can be supplied 7V. Refer to the *ADSP-BF52x Blackfin Processor Hardware Reference* for more information.

 Leaving JP16 ON when not writing to the OTP memory can damage the processor. See the *ADSP-BF52x Blackfin Processor Hardware Reference* for more information.

In USB host mode, if the host must provide 5V to a device, the PG13 flag pin must be set low to turn on the p-channel mosfet (U23). To connect PG13 of the processor to the mosfet, set SW20. 2 OFF, SW20. 5 OFF, and SW20. 6 ON.

The lithium ion battery leads are inserted into the P24 connector. The SW22 switch connects the battery to the EZ-Board when SW22 is ON. To change the battery, press in the white tabs and slide out the battery lead.

 The EZ-Board is intended to be used at room temperature (approximately 21°C)

An ADP2291 lithium ion battery charger IC charges the 740 mAh battery. The charge rate is selected based on a jumper placement and whether the battery is charging from a wall adaptor or from a USB port. See [Table 1-3](#) for details.

The lithium battery is monitored by the BQ27500 fuel gauge (U38). All battery statistics can be read from the fuel gauge, including time to empty, current voltage, and current consumption rate. To access the fuel gauge, use the I<sup>2</sup>C interface: ensure that JP18 has jumpers on positions 1&2


## Power Setup

Table 1-3. Charge Rate Selection

Mode	WALL	USB	JP17	P23	Resistance	Charge Rate
Full Charge	YES	NO	X <sup>1</sup>	X	OPEN	750 mA
Low	NO	YES	OFF	OFF	32K	100 mA
Medium	NO	YES	2&3	X	169K	375 mA
Selectable <sup>2</sup>	NO	YES	1&2	OFF	32/169K	100/375 mA
Shutdown	NO	YES	OFF	ON	0	NONE
Control Shut-down <sup>3</sup>	NO	YES	1&2	ON	0/169K	0/375mA


- 1 Any jumper setting has no affect.
- 2 Rate is selectable by the processor's flag: use JP15 to chose the flag pin. Setting the flag high selects 83 mA and setting the flag low selects 375 mA charge rates.
- 3 JP15 needs to be set to positions 1&2 (PG0), 3&4 (PG11), or 5&6 (PG12), selecting the processor port pin to control the selection. See [“CHG GPIO Jumper \(JP15\)” on page 2-24](#) for more information.

and 3&4. See [“Gauge I2C Jumper \(JP18\)” on page 2-26](#) for more information. An example program in the POST directory of the ADSP-BF526 installation demonstrates how to use the fuel gauge.

 Change jumper and switch settings only when power is OFF.

## Power Setup

The EZ-Board is shipped with the default configuration for 5V power from a wall adaptor or a USB port (see [Table 1-4](#)).

 Change jumper and switch settings only when power is OFF.

To set up the board for battery operation, the settings in [Table 1-5](#) are a good starting point.

Table 1-4. 5V Power Settings

Switch/Jumper	5V Setting
JP8	Positions 1&2, 3&4
JP9	Installed
JP10	Positions 2&3
JP15	Uninstalled
P17	Positions 1&2
P23	OFF
P25	OFF
SW22	OFF

Table 1-5. Battery Power Settings

Switch/Jumper	Battery Setting
JP8 (if 5V needed on the expansion interface II)	Positions 5&6, 7&8
JP9 (if 5V needed on expansion interface II)	Uninstalled
JP10	Positions 1&2
JP15	See <a href="#">Table 1-3</a>
P17	See <a href="#">Table 1-3</a>
P23	OFF; see <a href="#">Table 1-3</a>
P25	ON
SW22	ON

Refer to the individual switch and jumper descriptions for alternate settings.



Note that complying with USB current limitations requires limiting the charging rate and implementation of power saving features.

# Power Saving Features

The ADSP-BF526 EZ-Board is designed for low-power application evaluations; use the following settings to enable the board's power saving features.

- Jumper-controlled power savings:
  - ✓ The Ethernet PHY (SMSC LAN8700) can be totally powered down by removing jumpers P21 and P22.
  - ✓ The UART line drivers can be powered down by placing a jumper on JP14 and then removing any jumper from JP3.
  - ✓ The reset and Ethernet LED voltage translator can be disabled by removing any jumper from JP11.
  - ✓ The GPIO LED's and OTP flag voltage translator can be disabled by removing any jumper from JP5.
- Processor-controlled power savings:

The VDDINT regulator (VR5) can be shut down with the EXT\_WAKE signal of the processor. EXT\_WAKE also controls:

- ✓ the OTP flag and LED voltage translator (U3) via JP5
- ✓ the Ethernet LED and reset voltage translator (U4) via JP11
- ✓ the UART1 voltage translator (U32) via JP3

Refer to the *ADSP-BF52x Blackfin Processor Hardware Reference* for more information about EXT\_WAKE; refer to [“Jumpers” on page 2-20](#) for more information about the jumpers.

- Low-power mode capable ICs of the EZ-Board:
  - ✓ Wolfson WM8731L audio codec (U31)
  - ✓ Micron MT48H32M16-75 SDRAM memory (U14)
  - ✓ Numonyx M58WR032KB parallel flash (U16)
  - ✓ SST 25WF040 SPI flash memory (U6)
  - ✓ Numonyx NAND02 flash memory (U15)

Some of the low-power modes are entered by inactivity on-chip select lines. Consult the product data sheets for details.

## Power Measurements

Several locations are provided for measuring the current draw from various power planes. Precision 0.1 ohm shunt resistors are available on the VDDINT, VDDEXT, VDDMEM, and SDRAM voltage domains. For current draw measurements, the associated jumper (P13, P11, P12, or P19) should be removed. Once the jumper is removed, the voltage across the resistor can be measured using an oscilloscope. Once voltage is measured, current can be calculated by dividing the voltage by 0.1. For the highest accuracy, a differential probe should be used for measuring voltage across the resistor.

For more information, see [“VDDINT Power Jumper \(P13\)”](#) on page 2-27, [“VDDEXT Power Jumper \(P11\)”](#) on page 2-26, [“VDDMEM Power Jumper \(P12\)”](#) on page 2-27, and [“PCA9306 Jumper \(JP19\)”](#) on page 2-26.

# Power-On-Self Test

The power-on-self-test program (POST) tests all EZ-Board peripherals and validates functionality as well as connectivity to the processor. Once assembled, each EZ-Board is fully tested for an extended period of time with a POST; all EZ-Boards are shipped with the POST preloaded into one of its on-board flash memories. The POST is executed by resetting the board and pressing the proper push button(s). The POST also can be used as a reference for a custom software design or hardware troubleshooting. Note that the source code for the POST program is included in the VisualDSP++ installation directory, along with the readme text file, which describes how the EZ-Board is configured to run POST.

## Example Programs

Example programs are provided with the ADSP-BF526 EZ-Board to demonstrate various capabilities of the product. The programs are installed with the VisualDSP++ software and can be found in the `<install_path>\Blackfin\Examples\ADSP-BF526 EZ-KIT Lite` directory. Refer to the readme file provided with each example for more information.

## Background Telemetry Channel

The USB debug agent supports the background telemetry channel (BTC), which facilitates data exchange between VisualDSP++ and the processor without interrupting processor execution.

The BTC allows you to read and write data in real time while the processor continues to execute. For increased performance of the BTC, including faster reading and writing, please check our latest line of processor emulators at:

<http://www.analog.com/en/embedded-processing-dsp/sharc/USB-EMU-LATOR/products/product.html> . For more information about BTC, see the online help.

## Design Reference Information

A design reference info package is available for download on the Analog Devices Web site. The package provides information on the design, layout, fabrication, and assembly of the EZ-KIT Lite and EZ-Board products.

The information can be found at:

<http://www.analog.com/en/embedded-processing-dsp/blackfin/BF526-EZBRD/processors/product.html> .

## Design Reference Information



# 2 ADSP-BF526 EZ-BOARD HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF526 EZ-Board board.

The following topics are covered.

- [“System Architecture” on page 2-2](#)  
Describes the ADSP-BF526 EZ-Board configuration and explains how the board components interface with the processor.
- [“Programmable Flags” on page 2-3](#)  
Shows the locations and describes the programming flags (PFs).
- [“Push Button and Switch Settings” on page 2-9](#)  
Shows the locations and describes the push buttons and switches.
- [“Jumpers” on page 2-20](#)  
Shows the locations and describes the configuration jumpers.
- [“LEDs” on page 2-29](#)  
Shows the locations and describes the LEDs.
- [“Connectors” on page 2-32](#)  
Shows the locations and provides part numbers for the on-board connectors. In addition, the manufacturer and part number information is provided for the mating parts.

## System Architecture

This section describes the processor's configuration on the EZ-Board (Figure 2-1).

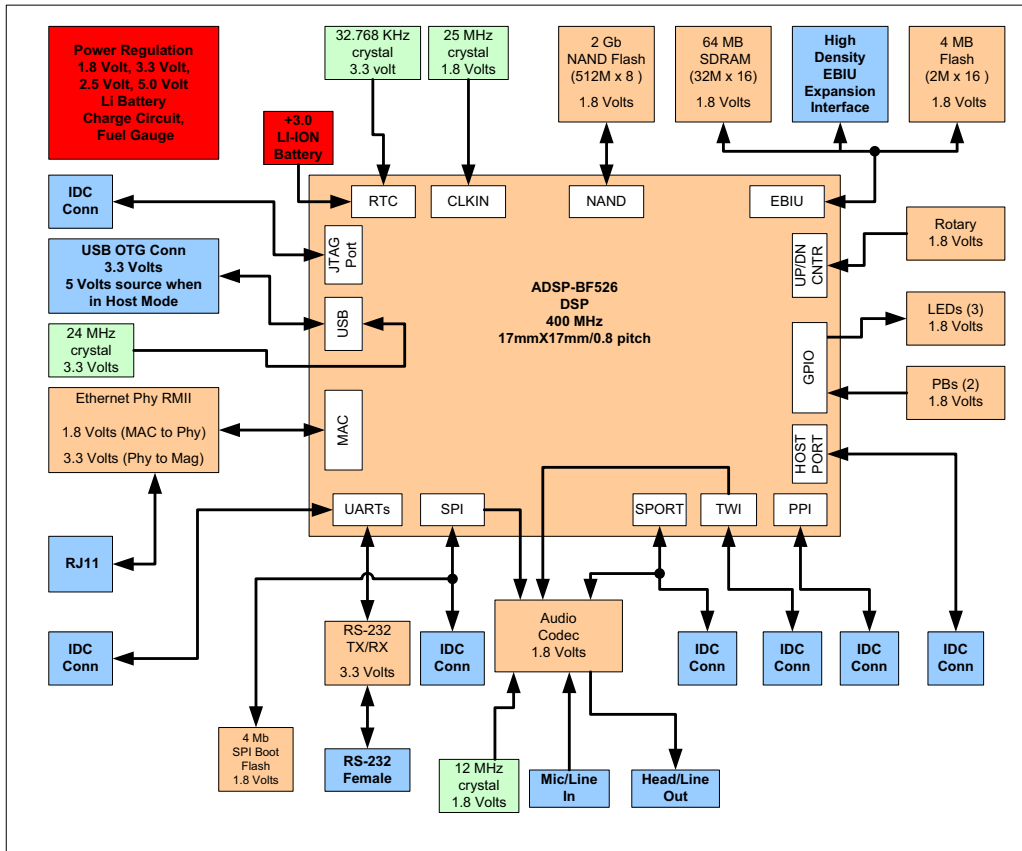


Figure 2-1. System Architecture

This EZ-Board is designed to demonstrate the capabilities of the ADSP-BF526 Blackfin processors. The processor has an I/O voltage of 1.8V. The core voltage of the processor is controlled by an Analog Devices

ADP1715 low dropout regulator (LDO) and an Analog Devices AD5258 digipot, which is configurable over the 2-wire interface (TWI) signals. Refer to the power-on-self test (POST) example in the ADSP-BF526 installation directory of VisualDSP++ for information on how to set up the TWI interface.

The core voltage and clock rate can be set on the fly by the processor. The input clock is 25 MHz. A 32.768 kHz crystal supplies the real-time clock (RTC) inputs of the processor. The default boot mode for the processor is external parallel flash boot. See [“Boot Mode Select Switch \(SW1\)” on page 2-10](#) for information on how to change the default boot mode.

## Programmable Flags

The processor has 50 general-purpose input/output (GPIO) signals spread across four ports (PF, PG, PH, and PJ). The pins are multi-functional and depend on the ADSP-BF526 processor setup. The following tables show how the programmable flag pins are used on the EZ-Board.

- PF programmable flag pins – [Table 2-1](#)
- PG programmable flag pins – [Table 2-2](#)
- PH programmable flag pins – [Table 2-3](#)
- PJ programmable flag pins – [Table 2-4](#)

Table 2-1. PF Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-Board Function
PFO	PPI D0/DROPRI /ND_DOA	Default: PPI D0 on P3. 18 via RN1 Land grid array P7. A
PF1	PPI D1/RFS0/ND_D1A	Default: PPI D1 on P3. 17 via RN1 Land grid array P7. A2

## Programmable Flags

Table 2-1. PF Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-Board Function
PF2	PPI D2/RSCLK0/ND_D2	Default: PPI D2 on P3. 20 via RN1 Land grid array P7. A4
PF3	PPI D3/DTOPRI /ND_D3A	Default: PPI D3 on P3. 19 via RN1 Land grid array P7. A5
PF4	PPI D4/TFS0/ND_D4A/ TACLK0	Default: PPI D4 on P3. 22 via RN1 Land grid array P7. A10
PF5	PPI D5/TSCLK0/ND_D5A/ TACLK1	Default: PPI D5 on P3. 21 via RN1 Land grid array P7. A11
PF6	PPI D6/DTOSEC/ND_D6A/ TACIO	Default: PPI D6 on P3. 24 via RN1 Land grid array P7. A13
PF7	PPI D7/DR0SEC/ND_D7A/ TACI1	Default: PPI D7 on P3. 23 via RN1 Land grid array P7. A14
PF8	PPI D8/DR1PRI	Default: LED0 via RN2 Expansion interface II P3. 26 (PPI D8), P4. 14 via SW21. 8, land grid array P7. A16
PF9	PPI D9/RSCLK1/SPI SEL6#	Default: PPI D9 via RN2 Expansion interface II (P3. 25, P4. 18) via SW21. 7, land grid array P7. A17
PF10	PPI D10/PRFS1/SPI SEL7#	Default: UART1RTS (U21) via U32, SW14. 3 and RN2 Expansion interface II (P3. 28, P4. 20) via SW21. 6, land grid array P7. A17
PF11	PPI D11/TFS1/CZM	Default: CZM rotary (SW5) via SW13. 3 and RN2 Expansion interface II (P3. 27, P4. 19) via SW21. 5, land grid array P7. A20
PF12	PPI D12/DT1PRI / SPI SEL2#/CDG	Default: CDG rotary (SW5) via SW13. 2 and RN2 Expansion interface II (P3. 30, P4. 13) via SW21. 4, land grid array P7. A22
PF13	PPI D13/TSCLK1/ SPI SEL3#/CUD	Default: CUD rotary (SW5) via SW13. 1 and RN2 Expansion interface II (P3. 29, P4. 17) via SW21. 3, land grid array P7. A23

## ADSP-BF526 EZ-Board Hardware Reference

**Table 2-1. PF Port Programmable Flag Connections (Cont'd)**

<b>Processor Pin</b>	<b>Other Processor Function</b>	<b>EZ-Board Function</b>
PF14	PPI D14/DT1SEC/UART1TX	<b>Default: UAR1TX (U21) via U32 and RN2</b> <b>Expansion interface II (P3. 32, P4. 15) via SW21. 2, land grid array P7. A25</b>
PF15	PPI D15/DR1SEC/UART1RX/TAC1 3	<b>Default: UAR1RX (U21) via U32, SW14. 2 and RN2</b> <b>Expansion interface II (P3. 31, P4. 16 via SW21. 1, P4. 32) via SW21. 1, land grid array P7. A26</b>

**Table 2-2. PG Port Programmable Flag Connections**

<b>Processor Pin</b>	<b>Other Processor Function</b>	<b>EZ-Board Function</b>
PG0	HWAI T	<b>Default: PB1 via SW21. 1 and RN5</b> <b>UART1 CTS (HWAI T) via U32, SW14. 1, host connector P9. 12, CHG GPIO JP15. 1, expansion interface II (P2. 37, P4. 37, J1. 52), land grid array P7. B27</b>
PG1	SPI SS#/SPI SEL1#	<b>Default: SPI flash (U6) CS via SW1. 4 and RN3</b> <b>Expansion interface II (P2. 21, P4. 21, P4. 26, P2. 26), land grid array P7. B26</b>
PG2	SPI SCK	<b>Default: SPI flash (U6), codec (U2) via SW8. 3</b> <b>Expansion interface II (P2. 24, P4. 24), land grid array P7. B9</b>
PG3	SPI MI S0/DROSECA	<b>Default: SPI flash (U6) via RN3</b> <b>Expansion interface II (P2. 16, P2. 27, P4. 27), land grid array P7. B23</b>
PG4	SPI MOSI /DT0SECA	<b>Default: SPI flash (U6), codec (U31) via SW8. 1</b> <b>Expansion interface II (P2. 15, P2. 25, P4. 25), land grid array P7. B24</b>
PG5	TMR1/PPI FS2/TFS0A	<b>Default: PPI FS2 P3. 14</b> <b>Land grid array P7. B17</b>
PG6	DTOPRI A/TMR2/PPI FS3	<b>Default: DTOPRI A codec (U31) via SW7. 2</b> <b>Expansion interface II (P2. 13, P3. 15), land grid array P7. B18</b>

## Programmable Flags

Table 2-2. PG Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-Board Function
PG7	TMR3/DROPRI A/UARTOTX	<b>Default:</b> DROPRI A codec (U31) via SW7. 3 <b>Expansion interface II</b> (P2. 14, P2. 31, P3. 36), land grid array P7. B14
PG8	TMR4/RFSOA/UARTORX/ TAC1 4	<b>Default:</b> RFSOA codec (U31) via SW7. 4 <b>Expansion interface II</b> (P3. 35, P2. 20, P2. 32), land grid array P7. B15
PG9	TMR5/RSCLKOA/TAC1 5	<b>Default:</b> RSCLKOA codec (U31) via SW2. 2 <b>Expansion interface II</b> (P2. 18, P3. 38), land grid array P7. B11
PG10	TMR6/TSCLKOA/TAC1 6	<b>Default:</b> TSCLKOA codec (U31) via SW2. 1 <b>Expansion interface II</b> P2. 17, land grid array P7. B12
PG11	TMR7/HOST_WR#	<b>Default:</b> LED1 via U3 and RN5 CHG GPIO JP15. 3, host connector P9. 4, expansion interface II (J1. 51, P2. 28, P2. 38, P4. 28, P4. 38), land grid array P7. B6
PG12	DMAR1/UART1TXA/ HOST_ACK	<b>Default:</b> LED2 via U3 and RN5 <b>Power down PB</b> via SW20. 3, CHG GPIO JP15. 5, host connector P9. 10, expansion interface II (J1. 54, P2. 39, P4. 39), land grid array P7. B8
PG13	DMAR0/UART1RXA/ HOST_ADDR/TAC1 2	<b>Default:</b> PB2 via SW21. 2 and RN5 OTP_FLAG_1P8V via SW20. 5, USB_VRSEL via SW20. 6, host connector P9. 8, expansion interface II (J1. 53, P2. 40, P4. 40), land grid array P7. B5
PG14	TSCLKOA/MDC/HOST_RD#	<b>Default:</b> host connector P9. 2 MDC PHY (U29) via SW12. 2, land grid array P7. B2
PG15	TFSOA/MI1PHY1NT#/ RMI1MDI1NT#/HOST_CE#	<b>Default:</b> TFSOA codec (U31) via SW7. 1 and RN5 RMI1MDI1NT# PHY (U29), wake via SW20. 4, host connector P9. 6, expansion interface II P2. 19, land grid array P7. B3

## ADSP-BF526 EZ-Board Hardware Reference

**Table 2-3. PH Port Programmable Flag Connections**

<b>Processor Pin</b>	<b>Other Processor Function</b>	<b>EZ-Board Function</b>
PH0	ND_D0/MI I CRS/ RMI I CRSDV/HOST_D0	<b>Default: NAND data 0 (U15) via RN4</b> RMI I carrier sense/receive data valid (U29. 36), host connector data 0 (P9. 31), land grid array P6. B3
PH1	ND_D1/ERXER/HOST_D1	<b>Default: NAND data 1 (U15) via RN4</b> PHY receive error (U29. 21), host connector data 1 (P9. 29), land grid array P6. B2
PH2	ND_D2/MDI O/HOST_D2	<b>Default: NAND data 2 (U15) via RN4</b> PHY management bus MDI O U29 via SW12. 1, host connector data 2 (P9. 27), land grid array P6. B6
PH3	ND_D3/ETXEN/HOST_D3	<b>Default: NAND data 3 (U15) via RN4</b> PHY transmit enable (U29. 6), host connector data 3 (P9. 25), land grid array P6. B5
PH4	ND_D4/MI I TXCLK/ RMI I REF_CLK/HOST_D4	<b>Default: NAND data 4 (U15) via RN4</b> PHY RMII ref clock U29 via SW12. 3 and U20, host connector data 4 (P9. 23), land grid array P6. B9
PH5	ND_D5/ETXD0/HOST_D5	<b>Default: NAND data 5 (U15) via RN4</b> PHY RMII transmit data 0 (U29. 23), host connector data 5 (P9. 21), land grid array P6. B8
PH6	ND_D6/ERXD0/HOST_D6	<b>Default: NAND data 6 (U15) via RN4</b> PHY RMII receive data 0 (U29. 18), PHY mode via SW11. 3, host connector data 6 (P9. 19), land grid array P6. B11
PH7	ND_D7/ETXD1/HOST_D7	<b>Default: NAND data 7 (U15) via RN4</b> PHY RMII transmit data 1 (U29. 24), host connector data 7 (P9. 17), land grid array P6. B12
PH8	SPI SEL4#/ERXD1/ HOST_D8/TACLK2	<b>Default: PHY RMII receive data 1 (U29. 17) via RN5</b> PHY mode via SW11. 2, host connector data 8 (P9. 15), expansion interface II (P2. 22, P4. 22), land grid array P6. B15
PH9	SPI SEL5#/ETXD2/ HOST_D9/TACLK3	<b>Default: SPI SEL5 codec U31 via RN3 and SW3. 1</b> Host connector P9. 13, expansion interface II P2. 23, P4. 23, land grid array P6. B27

## Programmable Flags

Table 2-3. PH Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-Board Function
PH10	ND_CE#/ERXD2/HOST_D10	Default: NAND chip (U15) enable via SW13. 4 Host connector data 10 (P9. 11), land grid array P6. B26
PH11	ND_WE/ETXD3/HOST_D11	Default: NAND write enable (U15) Host connector data 11 (P9. 9), land grid array P6. B24
PH12	ND_RE/ERXD3/HOST_D12	Default: NAND output enable (U15) Host connector data 12 (P9. 7), land grid array P6. B21
PH13	ND_BUSY/ERXCLK/ HOST_D13	Default: NAND busy (U15) Host connector data 13 (P9. 5), land grid array P6. B23
PH14	ND_CLE/ERXDV/HOST_D14	Default: NAND command latch enable (U15) Host connector data 14 (P9. 3), land grid array P6. B18
PH15	ND_ALE/COL/HOST_D15	Default: NAND address latch enable (U15) Host connector data 15 (P9. 1), land grid array P6. B17

Table 2-4. PJ Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-Board Function
PJ0	PPI FS1/TMRO	Default: PPI FS1 P3. 13 Land grid array P7. B21
PJ1	PPI CLK/TMRCLK	Default: PPI CLK P3. 16 Land grid array P7. A7
PJ2	SCL	Default: fuel gauge U38, digipot U34 via U39 via RN5 Codec via SW8. 4, expansion interface II (P2. 29, P3. 63, P4. 29)
PJ3	SDA	Default: fuel gauge U38, digipot U34 via U39 via RN5 Codec via SW8. 2, expansion interface II (P2. 30, P3. 61, P4. 30)



## Push Button and Switch Settings

This section describes operation of the push buttons and switches. The push button and switch locations are shown in [Figure 2-2](#).

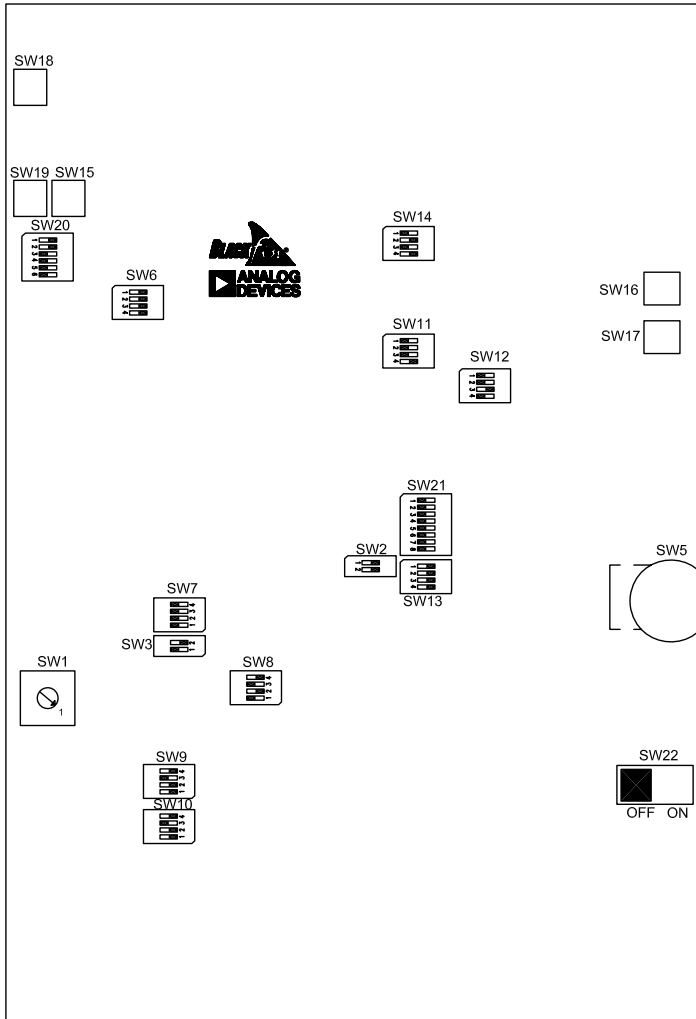


Figure 2-2. Push Button and Switch Locations

### Boot Mode Select Switch (SW1)

The rotary switch (SW1) determines the boot mode of the processor. [Table 2-5](#) shows the available boot mode settings. By default, the ADSP-BF526 processor boots from the on-board parallel flash memory.


 The selected position of SW1 is marked by the notch down the entire rotating portion of the switch, not the small arrow.

Table 2-5. Boot Mode Select Switch (SW1)

SW1 Position	Processor Boot Mode
0	Reserved
<b>1</b>	<b>Boot from 8-bit external flash memory (default)</b>
2	Boot from 16-bit asynchronous FIFO
3	Boot from serial SPI memory
4	Boot from SPI host device
5	Boot from serial TWI memory
6	Boot from TWI host
7	Boot from UART0 host
8	Boot from UART1 host
9	Reserved
A	Boot from SDRAM
B, C, D	Reserved
E	Boot from 16-bit host DMA
F	Boot from 8-bit host DMA

## SPORT0A ENBL Switches (SW2 and SW7)

The SPORT0A enable switches (SW2 and SW7) connect the SPORT0A interface of the processor to the audio codec, WM8731L (U31). When the SPORT0A interface is used on the expansion interface II, turn SW2 and SW7 all OFF. By default, SW2 and SW7 are set to all ON.

## SPI Codec CS (SW3)

The SPI codec CS switch (SW3) position 1 (ON) connects the SPI SEL5 pin to the WM8731L audio codec (U31) when the SPI interface is used. SW3 position 2 (ON) connects the expansion interface II connector P4 to the SPI SEL5 pin. By default, SW3 is set to ON, OFF.

## Rotary Encoder with Momentary Switch (SW5)

The rotary encoder (SW5) can be turned clockwise for an up count or counter-clockwise for a down count. The encoder also features a momentary switch, activated by pushing the switch towards the processor, which resets the counter to zero. The rotary encoder is a two-bit quadrature (gray code) encoder. Refer to the Rotary Counter section of the *ADSP-BF52x Blackfin Processor Hardware Reference* for more information.

The rotary encoder is disconnected from the processor by setting SW13 positions 1, 2 and 3 to OFF. See [“Rotary/NAND Enable Switch \(SW13\)” on page 2-14](#) for more information.

## Flash Enable Switch (SW6)

The flash enable switch (SW6) disconnects the  $\sim$ AMSx signals from parallel flash memory (U16), allowing other devices to utilize the signals via the expansion interface II. For each switch listed in [Table 2-6](#) that is turned OFF, the size of available flash memory is reduced by 1 MB.

## Push Button and Switch Settings

Table 2-6. Flash Enable Switch (SW6)

SW6 Switch Position (Default)	Processor Signal
1 (ON)	~AMS0
2 (ON)	~AMS1
3 (ON)	~AMS2
4 (ON)	~AMS3

### SPI/TWI Switch (SW8)

The SPI/TWI switch (SW8) selects the control interface for the WM8731L audio codec. By default, SW8 is ON, OFF, ON, OFF and selects the SPI interface. TWI is selected by setting the SW8 switch to OFF, ON, OFF, ON. See [“Mic/HP LPBK, Audio Mode Switch \(SW10\)” on page 2-13](#) for more information on how to setup the audio interface.

### MIC Gain Switch (SW9)

The microphone gain switch (SW9) sets the gain of the MIC signal, which is connected to the top 3.5 mm jack (J4). The gain can be set to 14 dB, 0 dB, or -6 dB by turning ON position 1, 2, or 3 of SW9 (see [Table 2-7](#)). When the corresponding position for the desired gain is ON, the remaining positions must be OFF. Refer to [“Audio Interface” on page 1-18](#) for more information about the audio codec.

Table 2-7. MIC Gain Switch (SW9)

Gain	SW9 Switch Settings
5 (14 dB)	ON, OFF, OFF, OFF
1 (0 dB)	OFF, ON, OFF, OFF
0.5 (-6 dB)	<b>OFF, OFF, ON, OFF (default)</b>
Unused	OFF, OFF, OFF, OFF

## Mic/HP LPBK, Audio Mode Switch (SW10)

The SW10 switch places the EZ-Board in a loopback to test the board for signal/circuit continuity and functionality. SW10 positions 1&2 connect the MIC IN signal to the headphone's left and right outputs for audio loopback. Do not turn SW10 positions 1&2 ON at the same time. See [“Power-On-Self Test” on page 1-32](#) for more information.

SW10 positions 3&4 select the control interface for the audio codec.

SW10 positions 3 ON and 4 OFF select the SPI interface, while position 3 OFF and position 4 ON select TWI mode. By default, SW8 is OFF, OFF, ON, OFF. See [“SPI/TWI Switch \(SW8\)” on page 2-12](#) for more information.

## ETH Mode Flash CS Switch (SW11)

The Ethernet mode flash CS switch (SW11) sets the bootstrapping option for the LAN8700 RMII PHY chip (U29). The mode settings for the PHY utilize internal chip pull-ups. Setting a position 1–3 of SW11 ON connects a pull-down resistor. [Table 2-8](#) shows the default as well as the alternate switch settings.

SW11 position 4 disconnects the SPI SEL1 pin from the SPI flash chip (U6). Setting SW11 position 4 OFF is useful when using SPI SEL1 on the expansion interface II. By default, SW11 is set to OFF, OFF, OFF, ON,

Table 2-8. ETH Mode Flash CS Switch (SW11)

MODE[2:0] Setting	Mode Definitions
111	All capable, auto negotiation (default)
110	Power down mode
101	Repeater mode, auto negotiation
100	100Base-TX half duplex advertised, auto negotiation
011	100Base-TX full duplex
010	100Base-TX half duplex

## Push Button and Switch Settings

Table 2-8. ETH Mode Flash CS Switch (SW11) (Cont'd)

MODE[2:0] Setting	Mode Definitions
001	10Base-T full duplex
000	10Base-T half duplex

## ETH Enable Switch (SW12)

The Ethernet enable switch (SW12) enables the Ethernet interface. The Ethernet and NAND flash share the same lines and cannot operate at the same time. By default, the SW12 settings are OFF, OFF, ON, OFF (see [Table 2-9](#)). Ethernet is enabled by setting the switch to ON, ON, OFF, ON. SW12 positions 1&2 connect the PHY management bus (MDIO and MDC). SW12 position 3 ON enables the 50 MHz RMII clock. SW12 position 4 holds the PHY in reset (set to OFF) or connects the PHY reset to the EZ-Board reset (set to ON).

Table 2-9. ETH Enable Switch (SW12)

SW12 Switch Setting	Ethernet Mode
OFF, OFF, ON, OFF	OFF (default)
ON, ON, OFF, ON	ON

## Rotary/NAND Enable Switch (SW13)

The rotary/NAND enable switch (SW13) disconnects the rotary encoder signals from the GPIO pins of the processor. When SW13 is OFF, its associated GPIO signals can be used on the expansion interface II (see [Table 2-10](#)). Position 4 of SW13 disconnects the chip enable for the NAND flash memory (U4).

Table 2-10. Rotary NAND Enable Switch (SW13)

SW13 Position (Default)	From	To
1 (ON)	Encoder (SW5)	Processor (U1, PF13)
2 (ON)	Encoder (SW5)	Processor (U1, PF12)
3 (ON)	Encoder (SW5)	Processor (U1, PF11)
4 (ON)	Processor (U1, PH10)	NAND (U15)

## UART Setup Switch (SW14)

The UART setup switch (SW14) configures the UART1 signals from the GPIO pins of the processor. By default, SW14 is OFF, ON, OFF, ON. Flow control is not implemented in the POST program, so SW14 positions 1 and 3 should be OFF and position 4 should be ON for loopback flow control. Refer to the ADM1385 data sheet on the Analog Devices Web Site for more information about the UART interface.

## Programmable Flag Push Buttons (SW15 and SW19)

Two momentary push buttons (SW15 and SW19) are provided for general-purpose user input. The buttons connect to the PG0 and PG13 GPIO pins of the processor. The push buttons are active high and, when pressed, send a high (1) to the processor. The GPIO enable switch (SW20) disconnects the push buttons from the corresponding push button signals. Refer to “[GPIO Enable Switch \(SW20\)](#)” on [page 2-17](#) for more information.

## Power-Down and Wake Push Buttons (SW16–17)

Two momentary push buttons (SW16–17) are provided for optional power feature inputs. The buttons connect to the PG12 and PG15 GPIO pins of the processor. The push buttons are active high and, when pressed, send a

## Push Button and Switch Settings

high (1) to the processor. The GPIO enable switch (SW20) disconnects the push buttons from the corresponding push buttons signals. Refer to “GPIO Enable Switch (SW20)” on page 2-17 for more information.

The power-down push button (SW16) is intended as an GPIO input to the processor and can be configured to put the processor in any one of the sleep modes.

The wake push button (SW17) is connected to the flag pin (PG15), which can be configured as the dedicated WAKE input signal from hibernation. Refer to the *ADSP-BF52x Blackfin Processor Hardware Reference Manual* for more information.

### Reset Push Button (SW18)

The reset push button (SW18) resets the following ICs.

- Processor (U1), parallel flash (U16), PHY (U29) if SW12 position 4 is ON, SPI flash (U6)

The reset push button does not reset the following ICs.

- SDRAM (U14), NAND flash (U15)
- Audio codec (U31), UART1 (U21), voltage translators (U3, U4, U32, U39) schmitt trigger hex inverter (U5)
- Fuel gauge (U38), digipot (U34), battery charger (U37), power (VR2–3, VR5, VR9, VR10, U23)

The reset push button does not reset the standalone debug agent once the debug agent is connected to a personal computer (PC). After communication between the debug agent and PC is initialized, pushing a reset button does not reset the USB chip on the debug agent. The only way to reset the USB chip on the debug agent is to power down the EZ-Board.



## GPIO Enable Switch (SW20)

The general-purpose input/output switch (SW20) disconnects the associated push buttons and LED circuits from the GPIO pins of the processor and allows the signals to be used for other purposes. Depending on the switch configuration, the signals can be used as push buttons, one-time-programmable memory (OTP) flag for writing, or on-the-go (OTG) host mode 5V (see [Table 2-11](#)).

Table 2-11. GPIO Enable Switch (SW20)

SW20 Position (Default)	From	To	Function
1 (ON)	Push button 1 (SW19)	Processor (U1, PGO)	ON (PB1) OFF (UART1 CTS U21, host connector P9. 12, expansion interface II P2. 37, P4. 37, J1. 52)
2 (ON)	Push button 2 (SW15)	Processor (U1, PG13)	ON (PB2) OFF (host connector P9. 8, OTP flag for writes SW20. 8, OTG voltage select SW13. 7, expansion interface II P2. 40,P4. 40, J1. 53)
3 (OFF)	Power down push button (SW16)	Processor (U1, PG12)	OFF (LED2 not driven by the power down push button) ON (SW16 drives PG12)
4 (OFF)	Wake push button (SW17)	Processor (U1, PG15)	ON (connects the wake push button SW17 to PG15)
5 (OFF)	OTP_FLAG_1P8V (U3)	Processor (U1, PG13)	ON (PG13 controls the OTP flag for OTP writes) Requires SW20. 2 OFF, SW20. 6 OFF, and JP16 installed
6 (OFF)	USB_VRSEL (U23)	Processor (U1, PG13)	ON (PG13 controls USB_VRSEL PG13 for OTG host power) Requires SW20. 2 OFF and SW20. 5 OFF

## Push Button and Switch Settings

The OTP memory writes require a precise 7V supply, which is turned on by setting high the `OTP_FLAG_1P8V` signal. The OTP flag is connected to the processor by setting positions 2 & 6 of `SW20` to OFF and position 5 ON. These settings connect the `PG13` flag pin of the processor to the shutdown pin of the precise 7V circuit `VR9`.

The `USB_VRSEL` provides 5V to a device connected over the USB OTG interface when running in host mode. A connection to the `USB_VRSEL` signal is set by the `SW13` switch (positions 2&5 OFF and position 6 ON). Then the `PG13` programmable flag pin of the processor can be used to control the p-channel mosfet (`U23`). Refer to [“USB OTG Interface” on page 1-19](#) for more information.

A power-down push button can be connected to the processor’s flag pin `PG12` if position 3 of `SW20` is ON.



Turning `SW20` position 2 ON allows the `SW16` push button to control `LED2`.

A wake signal can be driven to the processor’s dedicated hibernate wake flag `PG15` by turning `SW20` position 4 ON. This setting can conflict with the `SPORT0A`, Ethernet, and host interfaces. See [“Power-Down and Wake Push Buttons \(SW16–17\)” on page 2-15](#) for more information.

The `PG0` flag pin of the processor can be used as an GPIO or other functions if `SW20` position 1 is turned OFF. By default, the `SW20` is set to ON, ON, OFF, OFF, OFF, OFF.

## SPORT1 Enable (SW21)

The `SPORT1` enable switch (`SW21`) disconnects the following processor interfaces from the `P4` connector of the EZ-Board expansion interface II: `UART1RX`, `UART1TX`, `CUD`, `CDG`, `CZM`, `UART1RTS`, `PPI D9`, and `LEDO`. To enable the `SPORT1` interface at `P4`, turn `SW21` all ON. By default, `SW21` is all OFF.

## Battery Switch (SW22)

The battery switch (SW22) connects and disconnects the ADP2291 lithium ion battery from the EZ-board power. When SW22 is ON, the board can run and charge from the battery attached to the back of the board. Jumper P25 should be removed when SW22 is OFF. SW22 is OFF by default.

## Jumpers

This section describes functionality of the configuration jumpers. [Figure 2-2](#) shows the locations of the configuration jumpers.

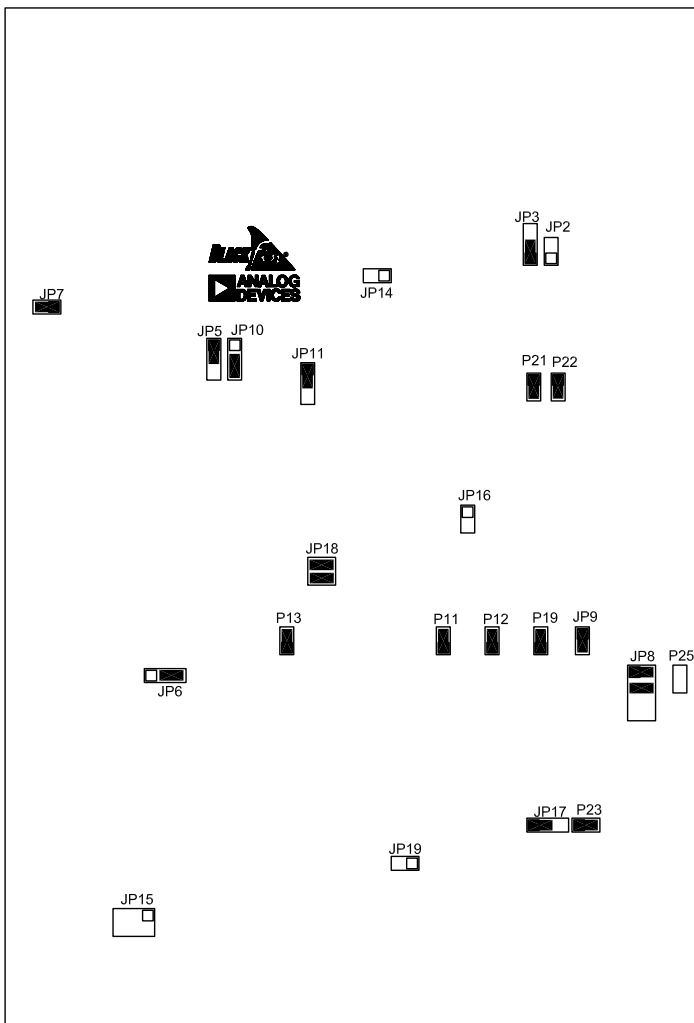


Figure 2-3. Configuration Jumper Locations

## UART Loopback Jumper (JP2)

The UART loopback jumper (JP2) is used to place the UART1 port of the processor in a loopback condition. The jumper connects the UART1\_TX line of the processor to the UART1\_RX signal of the processor. The jumper is required when the POST program is run to test the serial port interface. By default, JP2 is uninstalled.

## UART Enable Jumper (JP3)

The UART enable jumper (JP3) is a three-pin jumper that controls the output enable ( $\text{-OE}$ ) of the UART1 voltage translator. When JP3 is uninstalled, the voltage translator outputs are tri-stated. When a jumper is placed on positions 1&2 of JP3, the inverted copy of the WAKEUP\_OUT signal ( $\text{-WAKEUP\_OUT}$ ) controls the output enable of the voltage translator. When the EZ-board boots, the processor enables the voltage translator; when the processor is in hibernate, the translator outputs are tri-stated. A jumper on positions 2&3 of JP3 allows the translator to drive the outputs. See [“Power Architecture” on page 1-26](#) for more information on power saving capabilities of the ADSP-BF526 EZ-Board. By default, JP3 is installed on positions 1&2.

## LED Enable Jumper (JP5)

The LED enable jumper (JP5) enables the power saving feature of the board through control of the voltage translator's output enable pins. When no jumper is installed on JP5, the voltage translator (U3), which controls the GPIO LEDs, and the OTP\_FLAG signals are tri-stated. Placing a jumper on positions 1&2 of JP5 allows the inverted WAKEUP\_OUT signal ( $\text{-WAKEUP\_OUT}$ ) to control the output enable of the translator. When the processor is not in hibernate, the translator is enabled; when the processor is in hibernate, the translator outputs are tri-stated. Placing a jumper on positions 2&3 of JP5 enables the translator outputs. See [“Power Architec-](#)

## Jumpers

ture” on page 1-26 and “Power Saving Features” on page 1-30 for more information about the power saving capabilities of the EZ-Board. By default, JP5 is installed on positions 1&2.

### MIC Select Jumper (JP6)

The microphone select jumper (JP6) connects the MI CBI AS signal to the MI CI N signal (JP6 on positions 1&2) or connects the MI CBI AS signal to the 3.5 mm connector J4 (JP6 on positions 2&3). By default, JP6 is installed on positions 2&3.

### CFG WP Jumper (JP7)

The CFG WP jumper (JP7) is used to write-protect block 70 of the parallel flash chip. Block 70 contains 64 KB of configuration data at address range 0x203\_F0000–0x203\_FFFFF. When a jumper is installed on JP7, and the parallel flash driver from Analog Devices is used, block 70 is read-only. By default, JP7 is installed.

### EXP 5V Select Jumper (JP8)

The EXP 5V select jumper (JP8) selects the 5V voltage source for the expansion interface II connectors J1, P2, P3, and P4. JP8 must have either no jumpers or two jumpers installed, never one or three jumpers. When jumpers are placed on positions 1&2 and 3&4 of JP8, the 5V power rail for the expansion interface II is sourced from the wall adaptor. When jumpers are placed on positions 5&6 and 7&8 of JP8, 5V is sourced by the boost regulator VR7. By default, JP8 is installed on positions 1&2 and 3&4.

## VR7 Enable Jumper (JP9)

The VR7 enable jumper (JP9) controls the shut-down pin of the ADP1611 boost regulator, which is a 5V source for the expansion interface II. When installed, JP9 disables VR7. Install JP9 when using positions 1&2 and 3&4 of JP8 because the 5V source for the expansion interface II is the wall adaptor. Removing JP9 allows VR7 to drive 5V to the expansion interface II; the battery is providing the input to VR7. This setting drains the battery at a much faster rate. See [“EXP 5V Select Jumper \(JP8\)” on page 2-22](#) for more information. By default, JP9 is installed (VR7 is disabled).

## SENSE2 Select Jumper (JP10)

The SENSE2 select jumper (JP10) selects between the 3.3V regulator (VR2) and battery voltage as a monitored input for the reset signal. When a jumper is on positions 1&2 of JP10, the BAT\_P signal is monitored, which is useful when using the 740 mAh lithium ion battery. When a jumper is on positions 2&3 of JP10, the 3.3V regulator (VR2) is monitored. This setting must be used when no battery is wired to connector P24. The SENSE2 input pin of the ADM13305 voltage reset supervisor is set to drive the `-RESET_3V` signal low when a voltage of less than 3.16V is measured. By default, JP10 is installed on positions 2&3.

## RST/ETH LED Jumper (JP11)

The RST/ETH LED jumper (JP11) enables the power saving feature of the board through control of the voltage translator's output enable pins. When JP11 is not installed, the voltage translator (U4), which controls Ethernet LEDs, and `-RESET_3V` signals are tri-stated. Placing a jumper on positions 1&2 of JP11 allows the inverted `WAKEUP_OUT` signal (`-WAKEUP_OUT`) to control the output enable of the translator. When the processor is not in hibernate, the translator is enabled; when the processor is in hibernate, the translator outputs are tri-stated. Placing a jumper on

## Jumpers

positions 2&3 of JP11 enables the translator outputs. See [“Power Architecture” on page 1-26](#) and [“Power Saving Features” on page 1-30](#) for more information about the power saving capabilities of the EZ-Board. By default, JP11 is installed on positions 1&2.

### UART SD Jumper (JP14)

The UART SD jumper (JP14) enables the power saving feature of the ADM1385 UART line driver by controlling the driver’s shut-down pin. When installed, JP14 disables the transmitters and receivers of the UART line driver. See [“Power Architecture” on page 1-26](#) and [“Power Saving Features” on page 1-30](#) for more information on the power saving capabilities of the EZ-Board. By default, JP14 is uninstalled.

### CHG GPIO Jumper (JP15)

The CHG GPIO jumper (JP15) selects the flag pin of the processor to control the ADP2291 single cell lithium ion charge rate (see [Table 2-12](#)). Note that only settings that are listed in the table are supported. For an explanation of each setting, see [“Power Architecture” on page 1-26](#). JP15 is used in conjunction with the P23 and JP17 jumper settings. See the following sections for more information: [“R274 JMP Jumper \(P23\)” on page 2-27](#), [“CHG Control Jumper \(JP17\)” on page 2-25](#), and [“Power Measurements” on page 1-31](#). By default, JP15 is uninstalled.

Table 2-12. CHG GPIO Settings


JP15 Setting	Signal	FLAG pin
Uninstalled	PUSHBUTTON1_HWAIT	Not applicable (default)
1&2	PUSHBUTTON1_HWAIT	PG0
3&4	LED1_HOSTWR#	PG11
5&6	LED2_HOSTACK	PG12



## OTP Flag Enable Jumper (JP16)

The OTP flag enable jumper (JP16) controls the precise 7V OTP voltage regulator (VR9). When installed, JP16 allows OTP writes. JP16 must be used in conjunction with the SW20 GPIO enable switch. Refer to [“GPIO Enable Switch \(SW20\)” on page 2-17](#) for more information.

JP16 must be installed for OTP writes to be successful. The nominal 2.5V for OTP is temporarily raised to 7V when SW20 is configured properly and PG13 is set high. Care must be taken when SW20 is configured for the OTP\_FLAG signal in order to avoid VR9 driving 7V for an extended amount of time.

 There is a limited amount of time that 7V can be applied to the processor's OTP interface. Violating the specifications listed in the ADSP-BF526 processor datasheet can damage the processor.

Configured properly, SW20 and JP16 connect the processor's PG13 flag pin to the shut-down pin of the ADP1611 switching converter (VR9). Refer to [“GPIO Enable Switch \(SW20\)” on page 2-17](#), the *ADSP-BF52x Blackfin Processor Hardware Reference Manual*, and the *ADSP-BF526 Blackfin Embedded Processor Data Sheet* for more information about OTP writes.

## CHG Control Jumper (JP17)

The CHG control jumper (JP17) selects the control line for the mosfet attached to the charge rate adjustment pin of the ADP2291 linear charger. When no jumper is installed, the on-board pull-up holds the gate of the mosfet ON. Placing a jumper on positions 1&2 of JP17 allows the processor's flag pin, selectable by JP15, to control the gate of the mosfet. Placing a jumper on positions 2&3 of JP17 pulls the mosfet gate to ground, disconnecting the drain and the source. For more information on the ADP2291 single cell lithium ion battery charger, see [“Power Architecture” on page 1-26](#).

## Jumpers

The JP17 jumper is used in conjunction with the P23 and JP15 jumpers; see the following sections for more information: [“R274 JMP Jumper \(P23\)” on page 2-27](#), [“CHG GPIO Jumper \(JP15\)” on page 2-24](#), and [“Power Measurements” on page 1-31](#). By default, JP17 is installed on positions 2&3.

### Gauge I<sup>2</sup>C Jumper (JP18)

The gauge I<sup>2</sup>C jumper (JP18) disconnects the I<sup>2</sup>C bus of the processor from the BQ27500 fuel gauge. The fuel gauge is connected to the I<sup>2</sup>C bus when jumpers are installed on positions 1&2 and 3&4 of JP18. If the I<sup>2</sup>C bus hangs when performing fast bus operations, it may be necessary to remove the jumpers. By default, JP18 is installed on positions 1&2 and 3&4.

### PCA9306 Jumper (JP19)

The PCA9306 jumper (JP19) disables the PCA9306 I<sup>2</sup>C voltage translator and reduces power consumption of the EZ-Board. When a jumper is installed on JP19, the voltage translator is disabled. Disabling the voltage translator removes the ability to control the VDDINT voltage domain. The VDDINT remains at the voltage set before JP19 has been installed. By default, JP19 is uninstalled.

### VDDEXT Power Jumper (P11)

The VDDEXT power jumper (P11) is used to measure the processor's I/O voltage and current. By default, JP11 is ON: the power flows through the two-pin IDC header. To measure power, remove the jumper and measure voltage across the 0.1 ohm resistor. Once voltage is measured, power can be calculated. For more information, refer to [“Power Measurements” on page 1-31](#).

## VDDMEM Power Jumper (P12)

The VDDMEM power jumper (P12) is used to measure the voltage and current supplied to the memory interface of the processor. By default, P12 is ON: the power flows through the two-pin IDC header. To measure power, remove P12 and measure voltage across the 0.1 ohm resistor. Once voltage is measured, power can be calculated. For more information, refer to [“Power Measurements” on page 1-31](#).

## VDDINT Power Jumper (P13)

The VDDINT power jumper (P13) is used to measure the core voltage and current supplied to the processor core. P13 is ON by default, and the power flows through the two-pin IDC header. To measure power, remove P13 and measure voltage across the 0.1 ohm resistor. Once voltage is measured, power can be calculated. For more information, refer to [“Power Measurements” on page 1-31](#).

## ETH PWR Jumpers (P21–22)

The ETH PWR jumpers (P21–22) disconnect the SMSC LAN8700 Ethernet PHY from the 1.8V and 3.3V power supplies. When P21–22 are removed, all power is disconnected from the PHY, which is a great benefit for low-power consumption applications that do not require Ethernet. See [“Power Architecture” on page 1-26](#) and [“Power Saving Features” on page 1-30](#) for more information about the power saving capabilities of the EZ-Board. By default, P21–22 are installed.

## R274 JMP Jumper (P23)

The R274 JMP jumper (P23) provides a means to short out a R274 set resistor in the charge rate circuit of the ADP2291 single cell lithium ion battery. P23 bypasses R274 when installed and effectively makes a zero ohm connection to the WALL\_SENSE signal. For more information on

## Jumpers

the ADP2291 battery charger, see [“Power Architecture” on page 1-26](#).

P23 is used in conjunction with the JP17 and JP15 jumpers; see the following sections for more information: [“CHG Control Jumper \(JP17\)” on page 2-25](#), [“CHG GPIO Jumper \(JP15\)” on page 2-24](#), and [“Power Measurements” on page 1-31](#). By default, P23 is uninstalled.

### **BATT Installed Jumper (P25)**

The BATT installed jumper (P25) serves as an indication to the BQ27500 fuel gauge that a lithium ion battery is installed. When using the battery, install a jumper on P25 before turning ON the battery’s power switch (SW22). By default, P25 is uninstalled.

## LEDs

This section describes the on-board LEDs. [Figure 2-4](#) shows the LED locations.

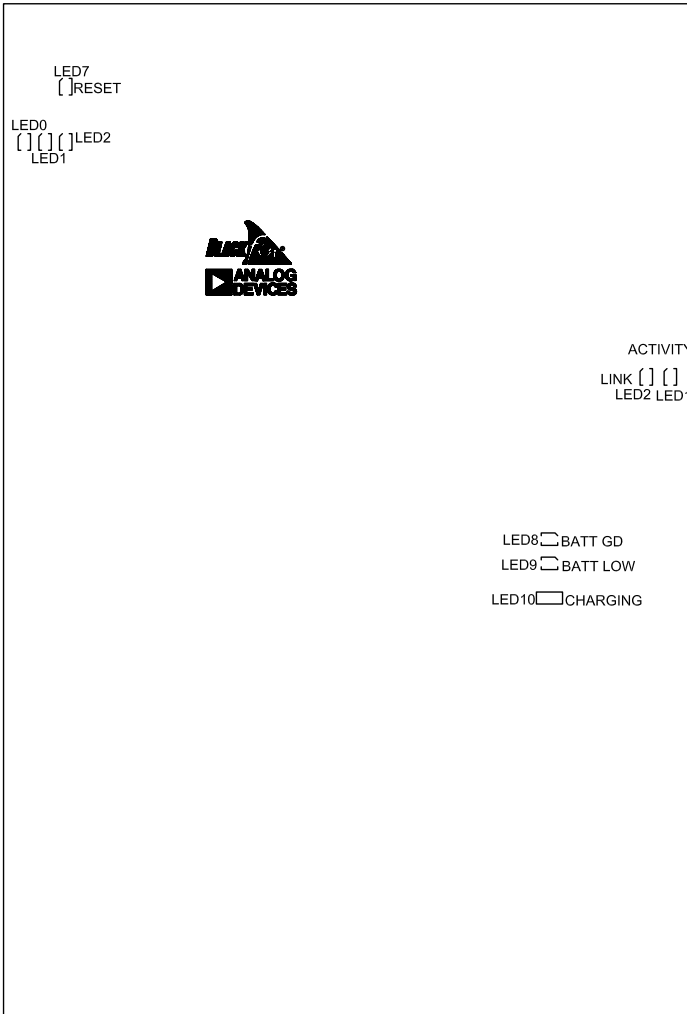


Figure 2-4. LED Locations

## LEDs

### Ethernet LEDs (LED1–2)

When LED2 is lit solid, it indicates that the SMSC LAN8700 chip (U29) detects a valid link. When transmit or receive activity is sensed, LED1 flashes as an activity indicator. For more information on the LEDs, refer to the LAN8700 chip data sheet provided by the product manufacturer.

### GPIO LEDs (LED3–5)

Three LEDs connect to three general-purpose I/O pins of the processor (see [Table 2-13](#)). The LEDs are active high and are lit by writing a 1 to the correct programmable flag signal.

Table 2-13. GPIO LEDs

LED Reference Designator	Processor Programmable Flag Pin
LED0	PF8
LED1	PG11
LED2	PG12

### Reset LED (LED7)

When LED7 is lit, it indicates that the master reset of all major ICs is active. The reset LED is controlled by the Analog Devices ADM13305 supervisory reset circuit. You can assert the reset push button (SW18) to assert the master reset and activate LED7. [For more information, see “Reset Push Button \(SW18\)” on page 2-16.](#)

### Batt GD LED (LED8)

When LED8 is lit (green), it indicates that the BQ27500 fuel gauge (U38) has successfully initialized the lithium ion battery. This is not an indication of the battery capacity. When the battery switch (SW22) is OFF, but the battery installed jumper (P25) is ON, the battery GD LED still illuminates. Ensure that P25 is installed only when SW22 is ON.

### Batt Low LED (LED9)

When LED9 is lit (yellow), it indicates that the BQ27500 fuel gauge (U38) has detected that the lithium ion battery is low. The low threshold can be programmed; for more information, refer to the BQ27500 data sheet provided by the product manufacturer.

### Charging LED (LED10)

When LED10 illuminates, it indicates that the lithium ion battery is receiving a charge from either the 5V wall adaptor (P14) or the USB OTG connector (P8).

## Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in [Figure 2-5](#).

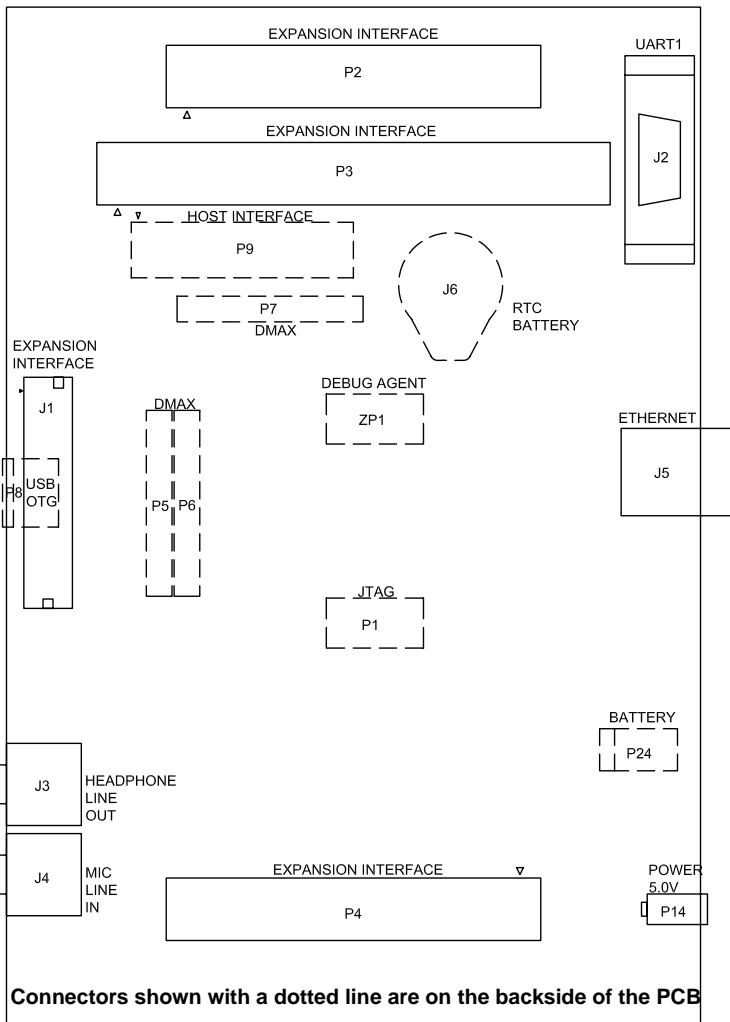


Figure 2-5. Connector Locations



## Expansion Interface II Connector (J1)

J1 is a board-to-board connector providing signals from the external bus interface unit (EBIU) of the processor. The connector is located on the left edge of the board. For more information, see [“Expansion Interface II” on page 1-25](#). For availability and pricing of the connector, contact Samtec.

Part Description	Manufacturer	Part Number
104-position 0.025", SMT header	SAMTEC	QMS-052-11-L-D-A
<b>Mating Connector</b>		
104-position 0.025", SMT socket	SAMTEC	QFS-052-01-L-D-A

## RS-232 Connector (J2)

Part Description	Manufacturer	Part Number
DB9, female, vertical mount	NORCOMP	191-009-213-L-571
<b>Mating Cable</b>		
2m female-to-female cable	DIGI-KEY	AE1020-ND

## Dual Audio Connectors (J3–4)

Part Description	Manufacturer	Part Number
3.5 mm dual stereo jack	SWITCHCRAFT	35RAPC7JS
<b>Mating Cable (shipped with EZ-Board)</b>		
3.5 mm male/male 6' cable	RANDOM	10A3-01106

## Connectors

### Ethernet Connector (J5)

Part Description	Manufacturer	Part Number
RJ-45 Ethernet jack	STEWART	SS-6488-NF
<b>Mating Cable</b> (shipped with EZ-Board)		
Cat 5E patch cable	RANDOM	PC10/100T-007

### Battery Holder (J6)

Part Description	Manufacturer	Part Number
16 mm battery holder	MEMORY PROTECTION	BH600
<b>Mating Battery</b> (shipped with EZ-Board)		
3V 125MAH 16 mm LI-COIN	PANASONIC	CR1632

### JTAG Connector (P1)

The JTAG header is the connecting point for a JTAG connection to the ADSP-BF526 processor. The standalone debug agent requires both connectors P1 and ZP1.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-Board, the standalone debug agent must be removed. Follow the installation instructions provided in [“EZ-Board Installation” on page 1-4](#), using P1 as the JTAG connection point.

## Expansion Interface II Connectors (P2 and P4)

P2 and P4 are board-to-board connectors providing signals for the SPI, TWI, UART, SPORT interfaces and GPIO signals of the processor. The connectors are located on the upper and lower edges of the board. For more information, see [“Expansion Interface II” on page 1-25](#). For availability and pricing of the connectors, contact Samtec.

Part Description	Manufacturer	Part Number
50-position 0.1”, SMT header	SAMTEC	TSSH-125-01-L-DV-A
<b>Mating Connector</b>		
50-position 0.1”, SMT socket	SAMTEC	SSW-125-22-F-D-VS

## Expansion Interface II Connector (P3)

P3 is a board-to-board connector providing signals for the PPI, TWI, and GPIO signals of the processor. The connector is located on the upper edge of the board. For more information, see [“Expansion Interface II” on page 1-25](#). For availability and pricing of the connector, contact Samtec.

Part Description	Manufacturer	Part Number
70-position 0.1”, SMT header	SAMTEC	TSSH-135-01-L-DV-A
<b>Mating Connector</b>		
70-position 0.1”, SMT socket	SAMTEC	SSW-135-22-F-D-VS

## DMAx Land Grid Array Connectors (P5–7)

The land grid array areas (P5–7) are intended for the probing of the processor signals. The pads are exposed and designed to attach a Tektronix logic analyzer to the connectors listed in [Table 2-14](#). P5 and P6 require the

## Connectors

primary retention connectors, while P7 can connect to either the primary or alternate retention connectors. For more information about the land grid array, consult the Tektronix Web site.

Table 2-14. DMAX Land Grid Array Connectors (P5–7)

Part Description	Manufacturer	Part Number
Primary retention	TEKTRONIX	020290800
Alternate retention	TEKTRONIX	020291000

## USB OTG Connector (P8)

The pinout of the P8 connector can be found in [“ADSP-BF526 EZ-Board Schematic” on page B-1.](#)

Part Description	Manufacturer	Part Number
USB 5-pin mini AB	MOLEX	56579-0576
<b>Mating Cable (shipped with EZ-Board)</b>		
3M mini USB 2.0 cable	ASSMANN	AK672M/2-3

## Host Interface Connector (P9)

The pinout of the P9 connector can be found in [“ADSP-BF526 EZ-Board Schematic” on page B-1.](#)

Part Description	Manufacturer	Part Number
IDC header	SAMTEC	TSW-116-26-T-D
<b>Mating Connector</b>		
IDC socket	SAMTEC	TSW-116-01-T-D

## Power Connector (P14)

The power connector (J6) provides all of the power necessary to operate the EZ-Board.

Part Description	Manufacturer	Part Number
0.65 mm power jack	CUI	045-0883R
<b>Mating Power Supply</b> (shipped with EZ-Board)		
5.0VDC@2.5A power supply	CUI STACK	DMS050260-P12P-SZ

## Battery Connector (P24)

P24 is a connection point of a single 3.3V lithium ion battery. Ensure that the positive lead of the battery is inserted to the side labeled “+”, and the negative terminal is inserted to the side labeled “-”. To remove the battery leads, press the white plastic button in and slide out the lead. The battery is not connected until the SW22 switch is ON.

Part Description	Manufacturer	Part Number
Wire to board, push-in, 16–28 AWG	WEIDMULLER	281-2020-ND
<b>Mating Battery</b> (shipped with EZ-Board)		
3.7V lithium ion battery, 740 mAh	MOUSER	5169-UBP543048

## Standalone Debug Agent Connector (ZP1)

ZP1 connects the standalone debug agent to the EZ-Board. The standalone debug agent requires both the ZP1 and P1 connectors. [For more information, see “EZ-Board Installation” on page 1-4.](#)

## Connectors

# A ADSP-BF526 EZ-BOARD BILL OF MATERIALS

The bill of materials corresponds to [“ADSP-BF526 EZ-Board Schematic”](#) on page A-1.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	1	74LVC14A SOIC14	U5	TI	74LVC14AD
2	1	32.768KHZ OSC008	U12	EPSON	MC-156-32.7680KA-A0:RO HS
3	4	SN74LVC1G08 SOT23-5	U24-27	TI	SN74LVC1G08DBVR
4	1	HX1188 ICS007	U28	DIGI-KEY	553-1340-ND
5	1	LAN8700 QFN36	U29	SMSC	LAN8700C-AEZG
6	1	WM8731L ICS009	U31	WOLFSON	WM8731LSEFL
7	1	NJT4030P SOT-223	VR8	ON SEMI	NJT4030PT1G
8	1	50MHZ OSC012	U20	ECS INC	ECS-3518-500-B-TR
9	1	MT48H32M16 VFBGA54_100X1 1	U14	MICRON	MT48H32M16LFCJ-75:A
10	1	SN74AUC1G00 SOT23-5	U9	TI	SN74AUC1G00DBVR
11	1	BF526 M58WR032KB “U16”	U16	ST MICRO	M58WR032KB70ZB6EF

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
12	3	SN74AVC4T245 SOIC16	U3-4,U32	DIGI-KEY	296-17930-1-ND
13	1	BF526 BQ27500 "U33"	U38	DIGI-KEY	296-22633-2-ND
14	1	BF526 SST25WF040 "U6"	U6	SST	SST25WF040-40-5I-SAF
15	1	25MHz OSC013	Y1	DIGI-KEY	535-9140-1-ND
16	1	24MHz OSC013	Y2	DIGI-KEY	535-9138-1-ND
17	1	12MHz OSC014	Y3	DIGI-KEY	535-9100-1-ND
18	1	SI1012R SC-75A	Q1	VISHAY	SI1012R-T1-E3
19	3	SI2333DS SOT23D	Q2-4	VISHAY	SI2333DS-T1-E3
20	1	PCA9306 VSSOP8	U39	DIGI-KEY	568-4213-1-ND
21	1	NAND02 TFBGA63_80_95 X120	U15	ST MICRO	NAND02GR3B2CZA6E
22	1	ADSP-BF526 BGA208	U1	ANALOG DEVICES	ADSP-BF526KBCZENGA
23	2	ADP1611 MSOP8	VR7,VR9	ANALOG DEVICES	ADP1611ARMZ-R7
24	1	ADP1715 MSOP8	VR5	ANALOG	ADP1715ARMZ-R7
25	1	ADP1710 TSOT5	VR10	ANALOG DEVICES	ADP1710AUJZ-R7
26	1	ADR550B SOT23-3	U35	ANALOG DEVICES	ADR550BRTZ-REEL7
27	1	ADP2291 MSOP8	U37	ANALOG DEVICES	ADP2291ARMZ-R7
28	1	ADP2105-1.8V LFCSP16	VR3	ANALOG DEVICES	ADP2105ACPZ-1.8-R7



## ADSP-BF526 EZ-Board Bill Of Materials

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
29	1	ADP2105-3.3V LFCSP16	VR2	ANALOG DEVICES	ADP2105ACPZ-3.3-R7
30	1	ADM13305-4 SOIC8	U22	ANALOG DEVICES	ADM13305-4ARZ
31	1	ADM869L SSOP16	U23	ANALOG DEVICES	ADM869LARQZ
32	1	AD5258 MSOP10	U34	ANALOG DEVICES	AD5258BRMZ10
33	1	ADM1385ARSZ SSOP20	U21	ANALOG DEVICES	ADM1385ARSZ
34	1	AD8619ARUZ TSSOP14	U36	ANALOG DEVICES	AD8619ARUZ
35	1	DIP8 SWT016	SW21	C&K	TDA08H0SB1
36	1	DIP6 SWT017	SW20	CTS	218-6LPST
37	9	DIP4 SWT018	SW6-14	ITT	TDA04HOSB1
38	1	DB9 9PIN CON038	J2	NORCOMP	191-009-213-L-571
39	2	DIP2 SWT020	SW2-3	C&K	CKN9064-ND
40	8	IDC 2X1 IDC2X1	P11-13,P19, P21-23,P25	FCI	90726-402HLF
41	5	IDC 2X1 IDC2X1	JP2,JP7,JP9,JP14, JP16	FCI	90726-402HLF
42	6	IDC 3X1 IDC3X1	JP3,JP5-6,JP10-11, JP17	FCI	90726-403HLF
43	20	IDC 2PIN_JUMPER_S HORT	SJ1-9,SJ11-14, SJ16,SJ21-24,SJ26- 27	DIGI-KEY	S9001-ND
44	1	IDC 2X2 IDC2X2	JP18	FCI	68737-404HLF
45	1	IDC 3X2 IDC3X2	JP15	BURG	54102-T08-03LF

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
46	1	PWR .65MM CON045	P14	CUI	045-0883R
47	1	IDC 4X2 IDC4X2	JP8	SULLINS	GEC04DAAN
48	1	5A RESETABLE FUS005	F1	MOUSER	650-RGEF500
49	1	ROTARY SWT023	SW1	DIGI-KEY	563-1047-ND
50	2	3.5MM DUAL_STEREO CON050	J3-4	SWITCH- CRAFT	35RAPC7JS
51	1	USB_MINI-AB 5PIN CON052	P8	MOLEX	56579-0576
52	1	RJ45 8PIN CON_RJ45_12P	J5	DIGI-KEY	380-1022-ND
53	5	MOMENTARY SWT024	SW15-19	PANASONIC	EVQ-Q2K03W
54	1	ROTARY_ENC_E DGE SWT025	SW5	PANASONIC	EVQ-WKA001
55	1	QMS 52x2 QMS52x2_SMT	J1	SAMTEC	QMS-052-11-L-D-A
56	1	IDC 16x2 IDC16x2_SMT	P9	SAMTEC	TSM-116-01-T-DV
57	2	IDC 25x2 IDC25x2_SMTA	P2,P4	SAMTEC	TSSH-125-01-L-DV-A
58	1	IDC 35x2 IDC35x2_SMTA	P3	SAMTEC	TSSH-135-01-L-DV-A
59	1	IDC 7x2 IDC7x2_SMTA	P1	SAMTEC	TSM-107-01-T-DV-A
60	1	BATT_HOLDER 16MM BATT_COI	J6	MEMORY PROTECTI	BH600

## ADSP-BF526 EZ-Board Bill Of Materials

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
61	1	SPDTSWT026	SW22	NKK SWITCHES	CS12ANW03
62	2	10 1/8W 5% 1206	R154-155	KOA	RK73B2BTDD100J
63	5	YELLOW LED001	LED2-5,LED9	PANASONIC	LN1461C
64	4	100 1/10W 5% 0805	R116,R119,R129, R133	VISHAY	CRCW0805100RJNEA
65	3	600 100MHZ 200MA 0603	FER10-11,FER13	DIGI-KEY	490-1014-2-ND
66	3	600 100MHZ 500MA 1206	FER1,FER17-18	STEWARD	HZ1206B601R-10
67	3	1UF 16V 10% 0805	C97,C196-197	KEMET	C0805C105K4RAC TU
68	1	10 1/10W 5% 0805	R92	VISHAY	CRCW080510R0FKEA
69	2	10UF 16V 20% CAP002	CT1-2	PANASONIC	EEE1CA100SR
70	1	0 1/10W 5% 0805	R65	VISHAY	CRCW08050000Z0EA
71	1	190 100MHZ 5A FER002	FER19	MURATA	DLW5BSN191SQ2
72	1	YELLOW LED009	LED10	PANASONIC	LNJ416Q8YRA
73	4	1UF 10V 10% 0805	C153-155,C159	AVX	0805ZC105KAT2A
74	13	10UF 6.3V 10% 0805	C8,C18,C23,C34, C104,C108,C120, C122,C200,C229, C243-244,C249	AVX	08056D106KAT2A
75	1	4.7UF 6.3V 10% 0805	C99	AVX	08056D475KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
76	25	0.1UF 10V 10% 0402	C5-7,C17,C19-22, C48,C79-80,C87, C93,C105,C109, C119,C121,C144, C147-150,C205, C216,C237	AVX	0402ZD104KAT2A
77	57	0.01UF 16V 10% 0402	C9,C35-42,C51-52,C54-59,C73, C77-78,C81-86, C88-92,C96,C98, C133,C135, C138-141,C146, C151-152,C156-158,C160,C199, C201-204,C212, C214-215,C236, C262-263	AVX	0402YC103KAT2A
78	33	10K 1/16W 5% 0402	R4-5,R36,R58-59, R63,R72,R99-102, R104,R117-118, R121-124,R126, R128,R131,R134, R160,R171,R173, R185,R190,R204, R208,R245-246, R249,R269	VISHAY	CRCW040210K0FKED
79	25	4.7K 1/16W 5% 0402	R20-35,R66-68, R73,R83-85,R95, R169	VISHAY	CRCW04024K70JNED
80	10	0 1/16W 5% 0402	R12,R168, R192-199	PANASONIC	ERJ-2GE0R00X
81	6	33 1/16W 5% 0402	R6,R10-11,R13, R82,R203	Vishay	CRCW040233R0JNEA
82	7	0.1UF 16V 10%0603	C76,C184,C194, C251,C254-255, C257	AVX	0603YC104KAT2A

## ADSP-BF526 EZ-Board Bill Of Materials

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
83	1	10UF 10V +80/-20% 0805	C256	PANASONIC	ECJ-2FF1A106Z
84	8	1UF 16V 10% 0603	C112-114,C239- 240,C245,C259- 260	PANASONIC	ECJ-1VB1C105K
85	4	4.7UF 25V 20% 0805	C178-179, C188-189	AVX	0805ZD475KAT2A
86	1	68PF 50V 5% 0603	C195	AVX	06035A680JAT2A
87	1	150PF 50V 5% 0603	C209	AVX	06035A151JAT2A
88	5	4.7UF 6.3V 20% 0603	C143,C181,C234- 235,C238	PANASONIC	ECJ-1VB0J475M
89	3	470PF 50V 5% 0603	C252,C258,C261	AVX	06033A471JAT2A
90	1	.022UF 16V 10% 0603	C145	AVX	06033C223KAT2A
91	2	220UF 6.3V 20% D2E	CT3-4	SANYO	10TPE220ML
92	1	10M 1/10W 5% 0603	R2	VISHAY	CRCW060310M0FNEA
93	3	100K 1/10W 5% 0603	R277,R279,R290	VISHAY	CRCW0603100KJNEA
94	1	1M 1/10W 5% 0603	R40	VISHAY	CRCW06031M00FNEA
95	9	0 1/10W 5% 0603	R54-55,R248, R250,R261,R265, R286,R289,R299	PHYCOMP	232270296001L
96	10	49.9 1/16W 1% 0603	R74-76,R79-81, R88-91	VISHAY	CRCW060349R9FNEA
97	4	10 1/10W 5% 0603	R115,R127,R130, R135	VISHAY	CRCW060310R0JNEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
98	2	10.0K 1/16W 1% 0603	R294,R297	DALE	CRCW060310K0FKEA
99	2	75.0K 1/16W 1% 0603	R164,R256	VISHAY	CRCW060375K0FKEA
100	8	200.0K 1/16W 1% 0603	R266,R268,R280, R282,R287,R293, R295-296	VISHAY	CRCW0603200KFKEA
101	1	1K 1/10W 5% 0603	R276	DIGI-KEY	311-1.0KGRTR-ND
102	1	49.9K 1/10W 1% 0603	R253	DIGI-KEY	311-49.9KHRTR-ND
103	1	90.9K 1/10W 1% 0603	R175	DIGI-KEY	311-90.9KHRTR-ND
104	4	0.1 1/10W 1% 0603	R156-158,R188	PANASONIC	ERJ-3RSFR10V
105	1	10.0K 1/10W 1% 0603	R259	DIGI-KEY	311-10.0KHRTR-ND
106	1	120PF 50V 5% 0603	C185	AVX	06035A121JAT2A
107	8	100PF 50V 5% 0603	C100-103,C115-118	AVX	06035A101JAT2A
108	2	1000PF 50V 5% 0603	C183,C193	PANASONIC	ECJ-1VC1H102J
109	1	12.4K 1/10W 1% 0603	R93	DIGI-KEY	311-12.4KHRTR-ND
110	1	2200PF 50V 5% 0603	C250	PANASONIC	ECJ-1VB1H222K
111	2	75.0 1/10W 1% 0603	R77-78	DALE	CRCW060375R0FKEA
112	2	100 1/16W 5% 0402	R51,R56	DIGI-KEY	311-100JRTR-ND

## ADSP-BF526 EZ-Board Bill Of Materials

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
113	1	2.05K 1/16W 1% 0402	R187	VISHAY	CRCW04022K05FKED
114	1	4.99K 1/16W 1% 0603	R71	VISHAY	CRCW06034K99FKEA
115	3	511.0 1/16W 1% 0402	R105-107	DIGI-KEY	311-511LCT-ND
116	4	10UF 10V 10% 0805	C94,C142,C206-207	PANASONIC	ECJ-2FB1A106K
117	3	10UF 16V 10% 1210	C191,C246-247	AVX	1210YD106KAT2A
118	2	GREEN LED001	LED1,LED8	PANASONIC	LN1361CTR
119	1	RED LED001	LED7	PANASONIC	LN1261CTR
120	2	1000PF 50V 5% 1206	C180,C182	AVX	12065A102JAT2A
121	2	18K 1/16W 5% 0402	R177,R270	DIGI-KEY	311-18KJRCT-ND
122	10	430 1/16W 1% 0402	R15-16,R109-110, R114,R120,R262-263,R301-302	DIGI-KEY	311-430LRCT-ND
123	2	22000PF 25V 10% 0402	C208,C241	DIGI-KEY	490-3252-1-ND
124	1	5A MBRS540T3G SMC	D7	ON SEMI	MBRS540T3G
125	3	15KV PGB1010603 0603	D8-10	LITTLEFUSE	PGB1010603MR
126	1	VARISTOR V5.5MLA 30A 0603	R1	LITTLEFUSE	V5.5MLA0603
127	1	THERM 0.5A 0.4 1206	R167	LITTLEFUSE	1206L050-C

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
128	1	20MA MA3X717E DIO005	D1	PANASONIC	MA3X717E
129	2	330.0 1/16W 1% 0402	R94,R97	DIGI-KEY	541-330LCT-ND
130	1	33.0K 1/16W 1% 0402	R9	ROHM	MCR01MZPF3302
131	5	47.0K 1/16W 1% 0402	R48,R50,R52-53, R57	ROHM	MCR01MZPF4702
132	1	5.6K 1/16W 5% 0402	R17	PANASONIC	ERJ-2GEJ562X
133	1	1.0K 1/16W 1% 0402	R237	PANASONIC	ERJ-2RKF1001X
134	2	1000PF 2000V 10% 1206	C131-132	AVX	1206GC102KAT1A
135	1	154.0K 1/16W 1% 0402	R165	DIGI-KEY	541-154KLCT-ND
136	5	10.0K 1/16W 1% 0402	R69-70,R86-87, R172	DIGI-KEY	541-10.0KLCT-ND
137	4	5.6K 1/16W 0.5% 0402	R41,R44-46	SUSUMU	RR0510P-562-D
138	2	680 1/16W 1% 0402	R43,R273	BC COMPONENTS	2312 275 16801
139	1	90.9K 1/16W 5% 0402	R42	DIGI-KEY	541-90.9KLCT-ND
140	1	40.2K 1/16W 5% 0402	R49	DIGI-KEY	541-40.2KLCT-ND
141	7	100K 1/16W 5% 0402	R8,R103,R112-113,R125,R132, R207	DIGI-KEY	541-100KJTR-ND
142	1	3.3UF 16V 10% 0805	C125	DIGI-KEY	490-3337-2-ND

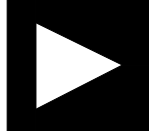


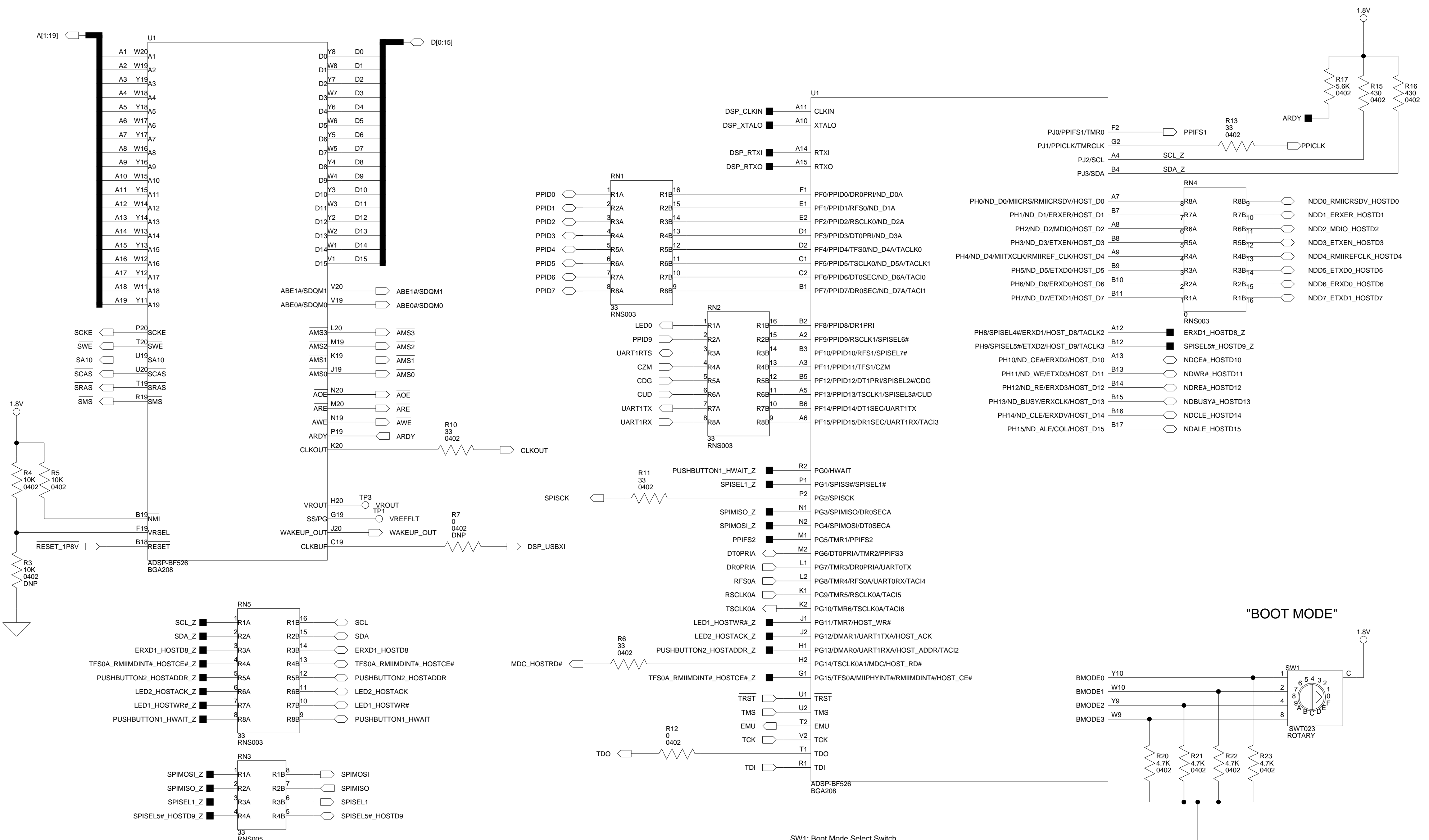
## ADSP-BF526 EZ-Board Bill Of Materials

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
143	1	0 1/16W 5% RNS003	RN4	PANASONIC	EXB-2HVR000V
144	1	2.2UF 25V 10% 0805	C253	DIGI-KEY	490-3331-1-ND
145	3	22UF 16V 10% 1210	C177,C187,C190	YAIYO YUDEN	EMK325BJ226KM-T
146	1	634.001/10W 0.1% 0603	R257	VISHAY	2312 216 76341
147	4	1.00K 1/10W 0.1% 0603	R254,R264,R281, R288	DIGI-KEY	RG16P1.0KBCT-ND
148	1	470 1/10W 1% 0603	R252	DIGI-KEY	311-470HRCT-ND
149	1	21.5K 1/10W 1% 0603	R260	DIGI-KEY	311-21.5KHRCT-ND
150	6	1A MBR130LSFT1G SOD-123FL	D12-17	ON SEMI	MBR130LSFT1G
151	1	22UH 20% IND018	L7	COILCRAFT	MSS4020-223MLB
152	1	1UH 20% IND019	L6	COILCRAFT	ME3220-102MLB
153	1	0.2 1/4W 1% 0805	R285	SUSUMU	RL1220S-R20-F
154	1	40K 1/16W 0.1% 0402	R274	STACKPOLE	RNC 10 T9 40K 0.1% R
155	1	30.9K 1/16W 1% 0402	R174	DIGI-KEY	541-30.9KLCT-ND
156	1	1.8M 1/16W 1% 0402	R271	DIGI-KEY	541-1.80MLCT-ND
157	1	10K 1/100W 1% THERMAT-2	R300	SEMITEC	103AT-2

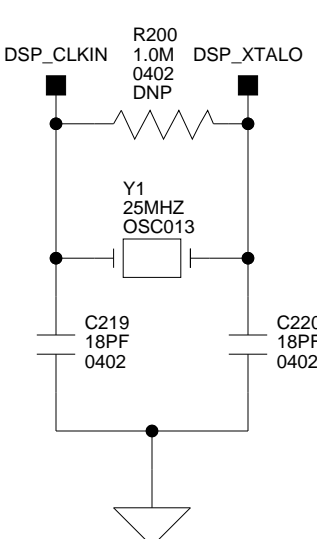
Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
158	3	2.7UH 10.5% IND022	L3-5	COILCRAFT	1812PS-272JLB
159	1	76.8K 1/16W 1% 0402	R178	DIGI-KEY	541-76.8KLCT-ND
160	8	18PF 50V 5% 0402	C2-3,C219-224	PANASONIC	ECJ-0EC1H180J
161	3	33 1/16W 5% RNS003	RN1-2,RN5	PANASONIC	EXB-2HV330JV
162	1	33 1/32W 5% RNS005	RN3	PANASONIC	EXB-28V330JX
163	1	1.2K 1/16W 1% 0402	R234	PANASONIC	ERJ-2RKF1201X
164	2	4.3 1/4W 5% 1206	R233,R236	PANASONIC	ERJ-8GEYJ4R3V
165	1	2.67K 1/16W 1% 0402	R235	PANASONIC	ERJ-2RKF2671X
166	3	909.0K 1/10W 1% 0603	R278,R283,R291	PANASONIC	ERJ-3EKF9093V
167	4	1.0M 1/10W 1% 0603	R267,R284,R292, R298	PANASONIC	ERJ-3EKF1004V
168	1	169.0K 1/16W 1% 0402	R275	VISHAY	CRCW0402169KFKED
169	1	0.02 1/2W 1% 1206	R272	OHMITE	LVK12R020FER

# ADSP-BF526 EZ-BOARD SCHEMATIC

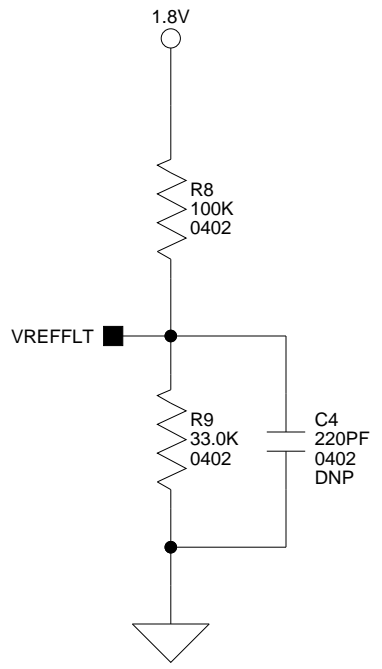
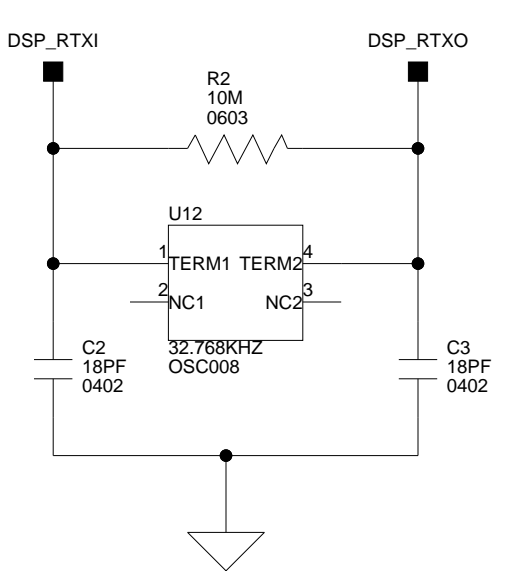
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		<b>Title</b> ADSP-526 EZ-BOARD TITLE	
<b>Size</b> C	<b>Board No.</b> A0212-2007	<b>Rev</b> 0.2A	
<b>Date</b> 8-15-2008_13:19	<b>Sheet</b> 1 of 14		



**"DSP CLK"**



**"RTC "**



SW1: Boot Mode Select Switch

POSITION	BOOT MODE
0	Reserved
1	Boot from 8 or 16-bit external flash memory
2	Boot from 16-bit asynchronous FIFO
3	Boot from serial SPI memory
4	Boot from SPI host device
5	Boot from serial TWI memory
6	Boot from TWI host
7	Boot from UART0 host
8	Boot from UART1Host
9	Reserved
A	Boot from SDRAM
B	Reserved
C	Reserved
D	Reserved
E	Boot from 16-Bit Host DMA
F	Boot from 8-Bit Host DMA

**ANALOG DEVICES**

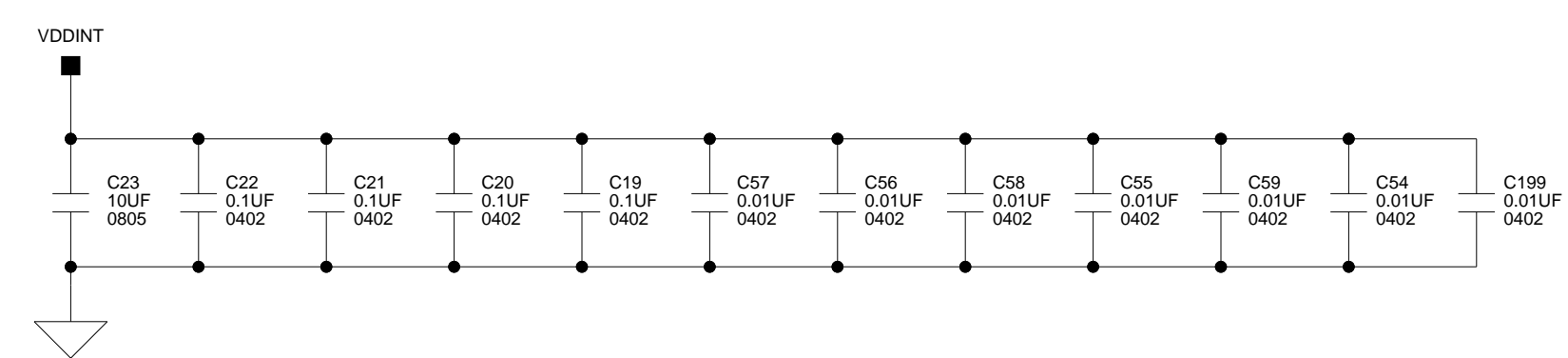
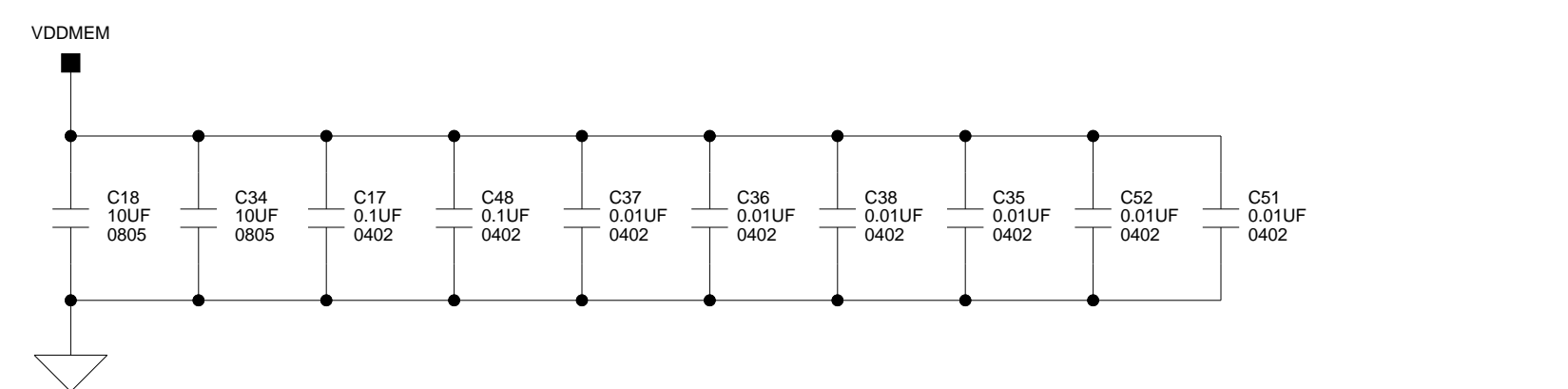
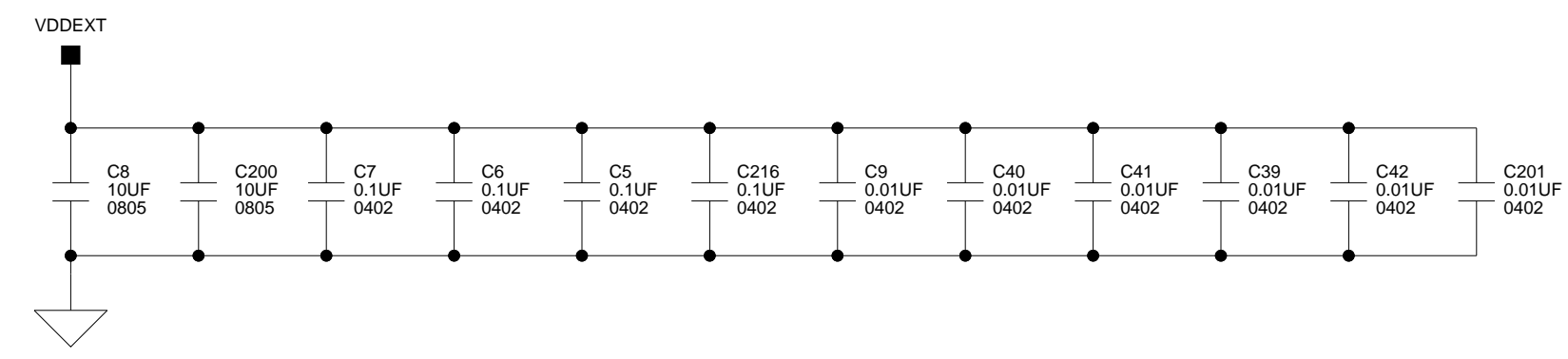
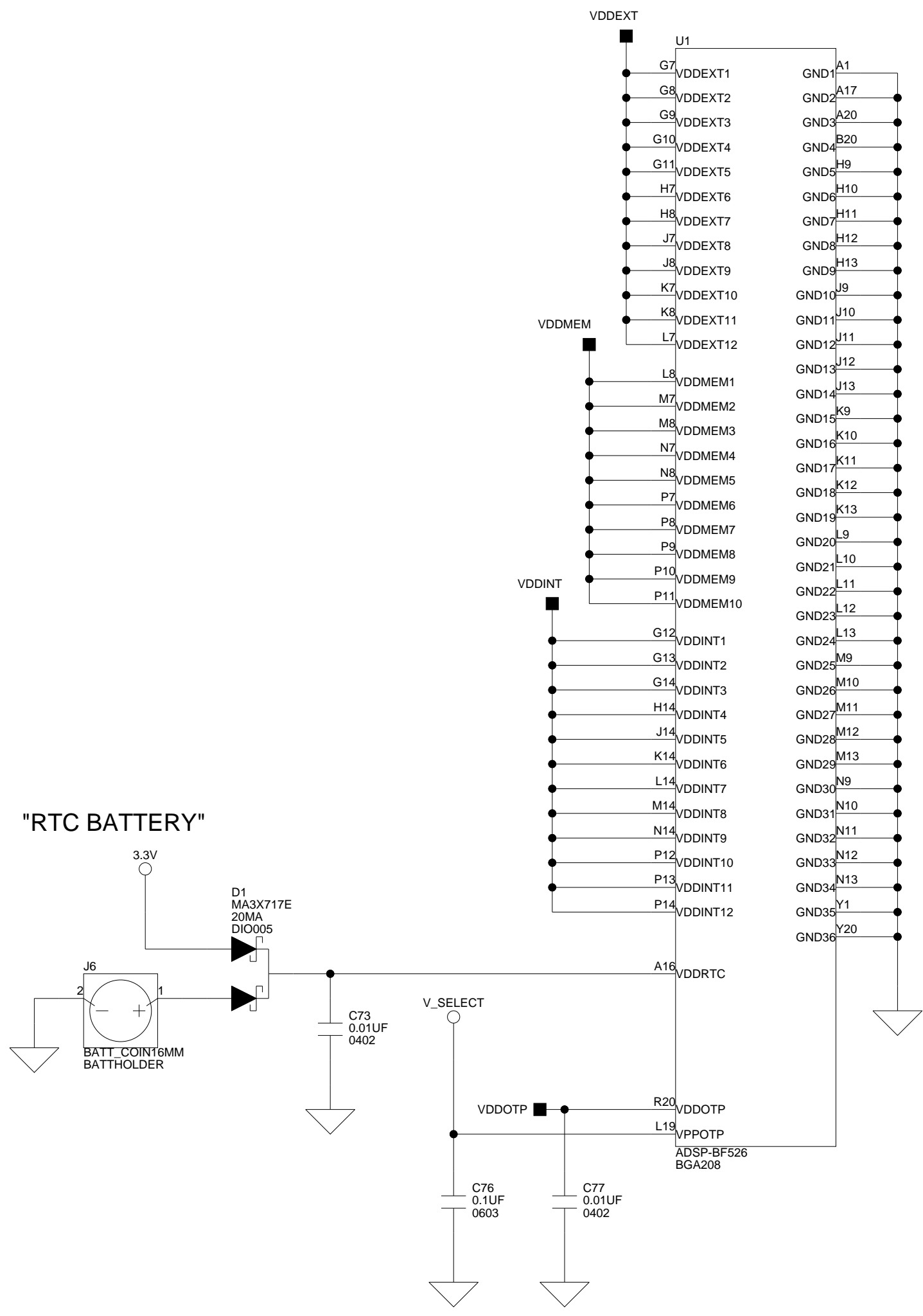
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Nashua, NH 03063  
PH: 1-800-ANALOGD

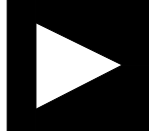
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**Title** ADSP-526 EZ-BOARD  
DSP EBIU + CONTROL

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<b>Size C</b>	<b>Board No.</b> A0212-2007	<b>Rev</b> 0.2A
<b>Date</b> 8-27-2008_9:47	<b>Sheet</b> 2 of 14	



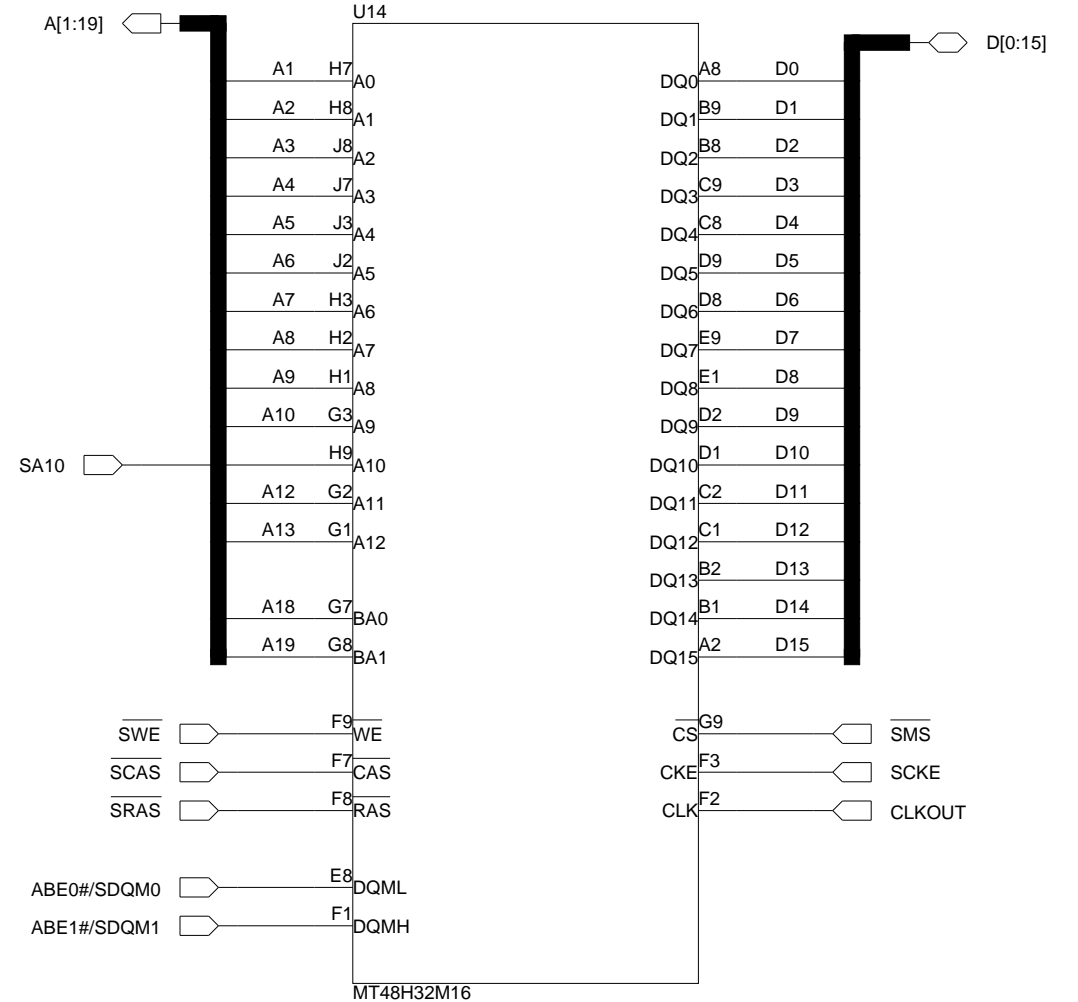
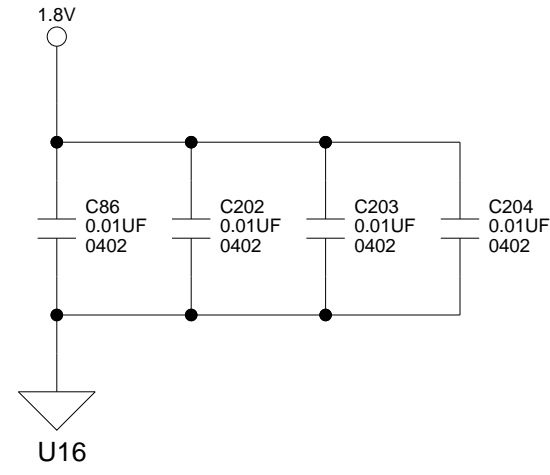
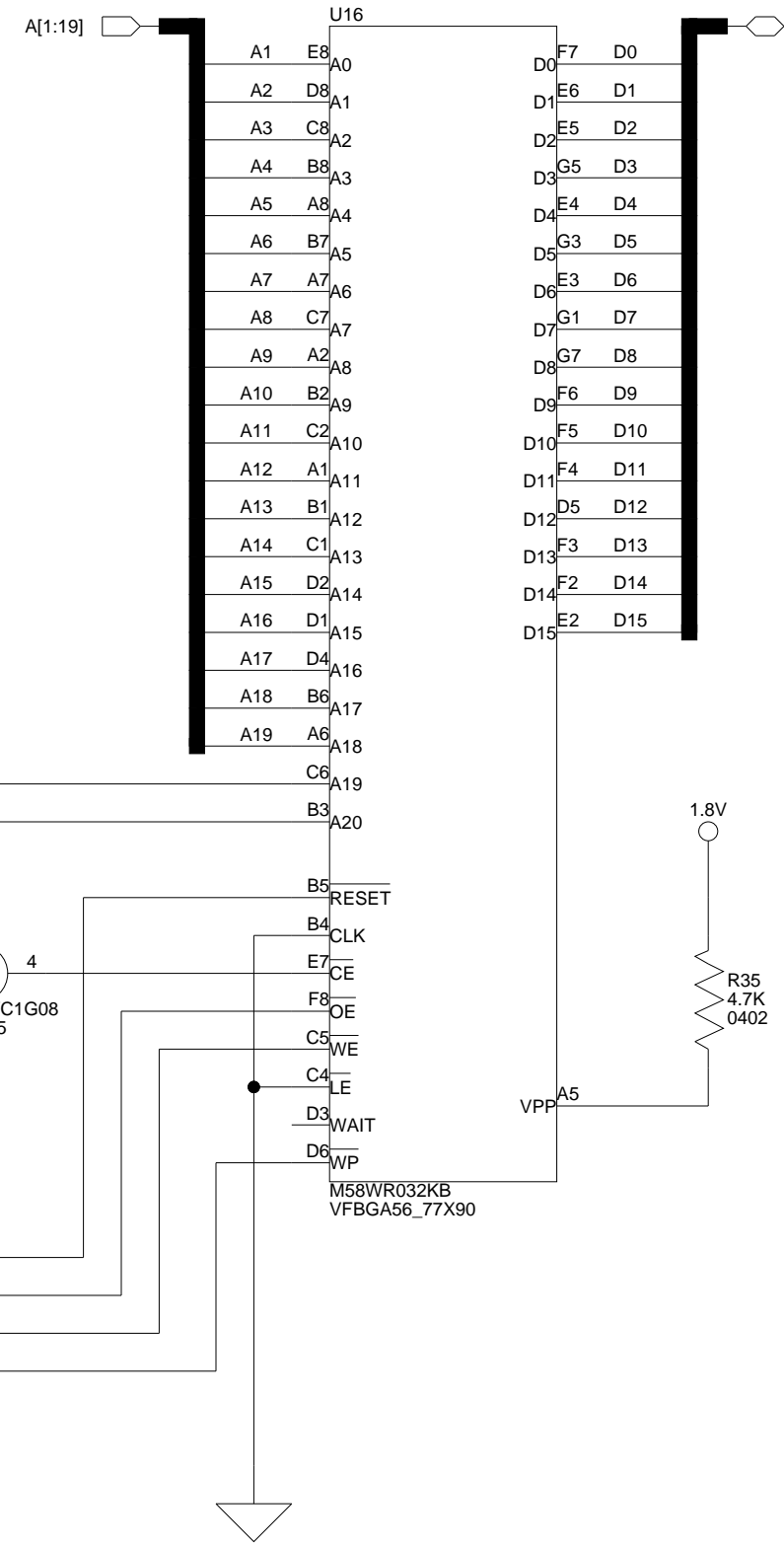
 <b>ANALOG DEVICES</b>		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		<b>Title</b> ADSP-526 EZ-BOARD DSP POWER, BYPASS CAPS	
<b>Size C</b>	<b>Board No.</b> A0212-2007	<b>Rev</b> 0.2A	
<b>Date</b> 8-15-2008_13:19	<b>Sheet</b> 3 of 13		

### 4 MB FLASH (2M x 16)

### 64MB SDRAM (32M x 16)

#### SW6: FLASH Enable

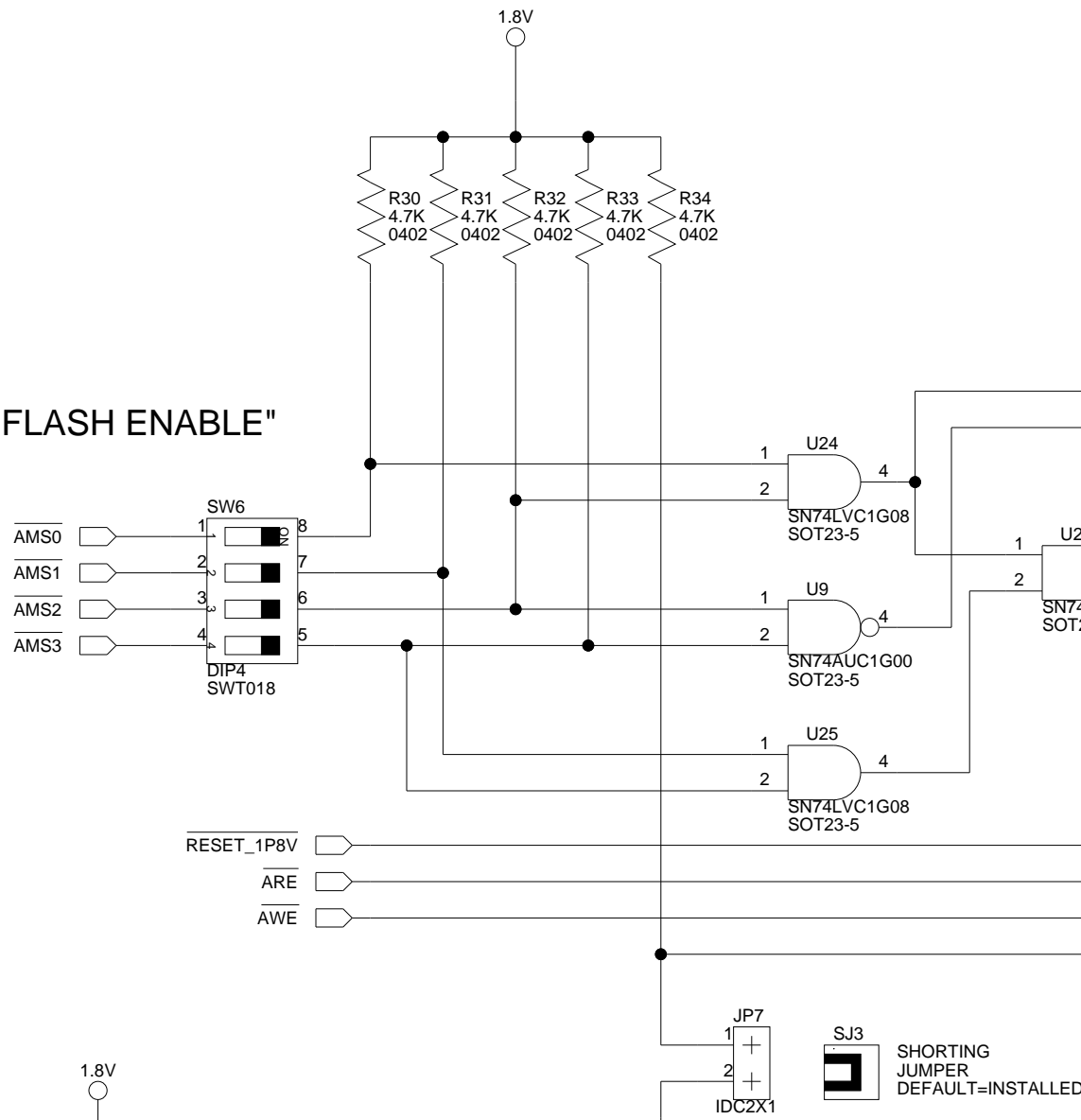
POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION / OFF MODE
SW6.1	DSP (U1)	FLASH (U16)	ON	(Expansion Interface)
SW6.2	DSP (U1)	FLASH (U16)	ON	(Expansion Interface)
SW6.3	DSP (U1)	FLASH (U16)	ON	(Expansion Interface)
SW6.4	DSP (U1)	FLASH (U16)	ON	(Expansion Interface)



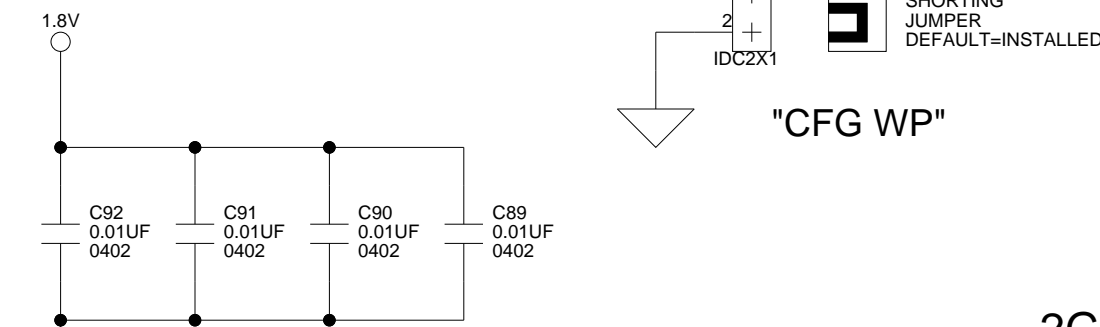
#### MEMORY MAP

ADDRESS RANGE	SELECT LINE	TYPE
0x2030 0000 - 0x203F FFFF	ASYNC BANK 3	FLASH
0x2020 0000 - 0x202F FFFF	ASYNC BANK 2	FLASH
0x2010 0000 - 0x201F FFFF	ASYNC BANK 1	FLASH
0x2000 0000 - 0x200F FFFF	ASYNC BANK 0	FLASH
0x0000 0000 - 0x03FF FFFF	NONE	SDRAM

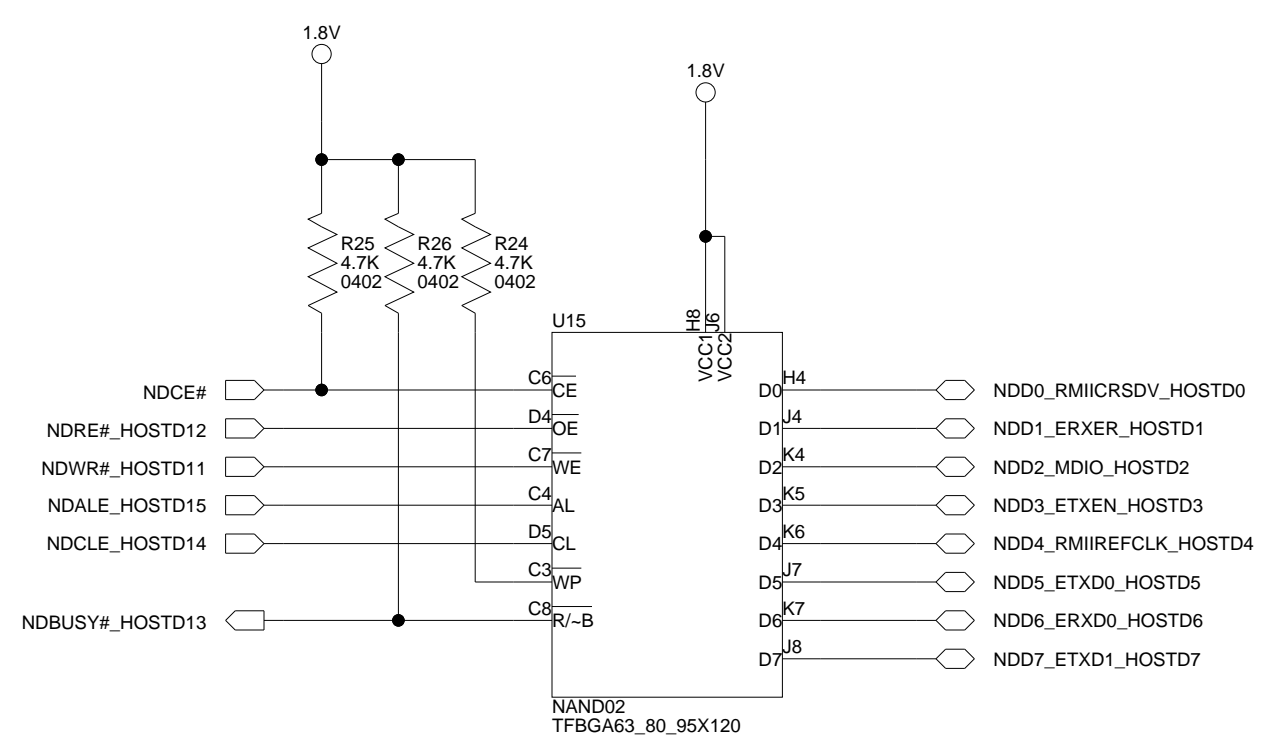
#### "FLASH ENABLE"



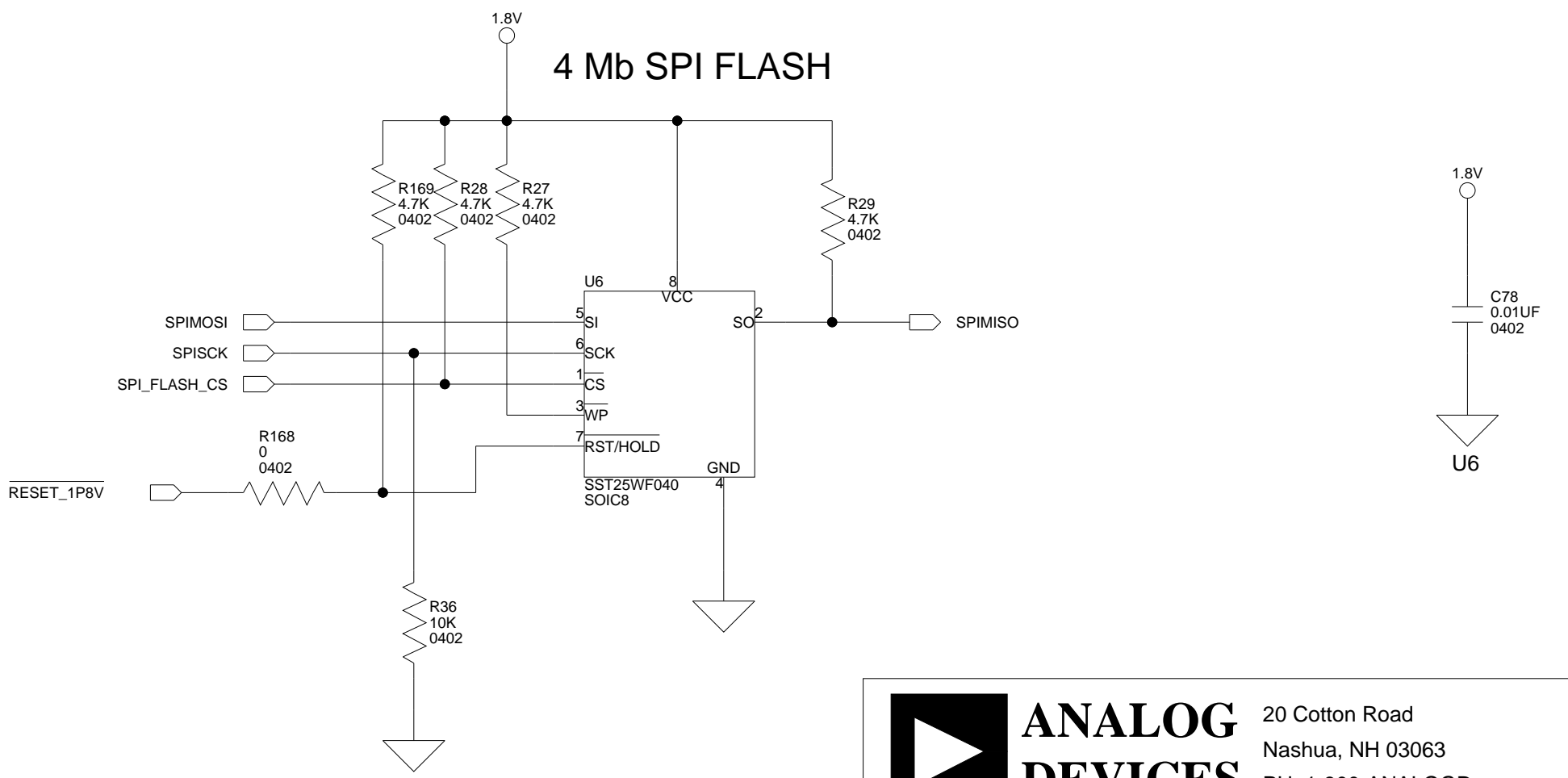
#### "CFG WP"



### 2Gb NAND FLASH

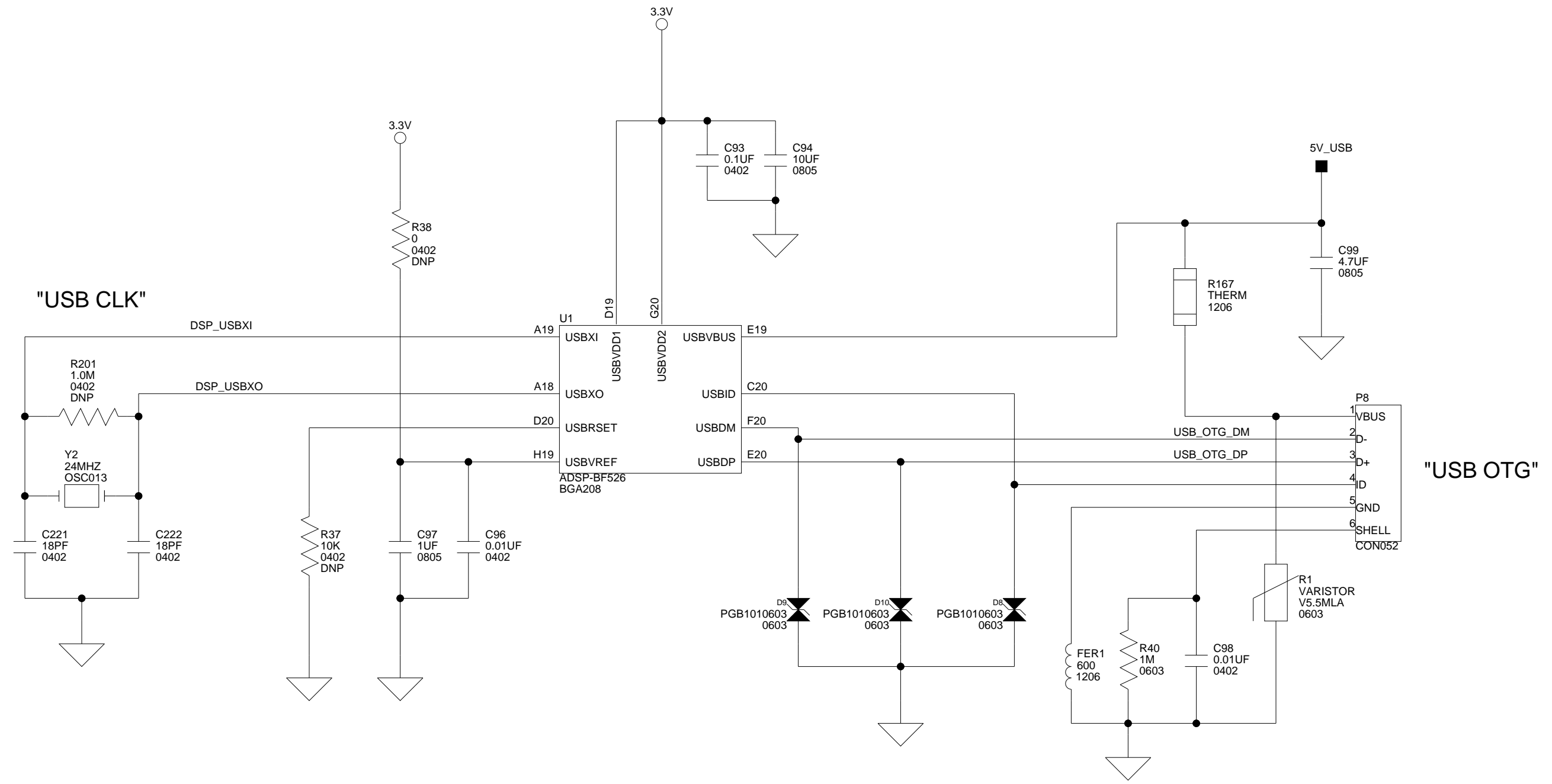


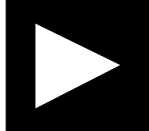
### 4 Mb SPI FLASH

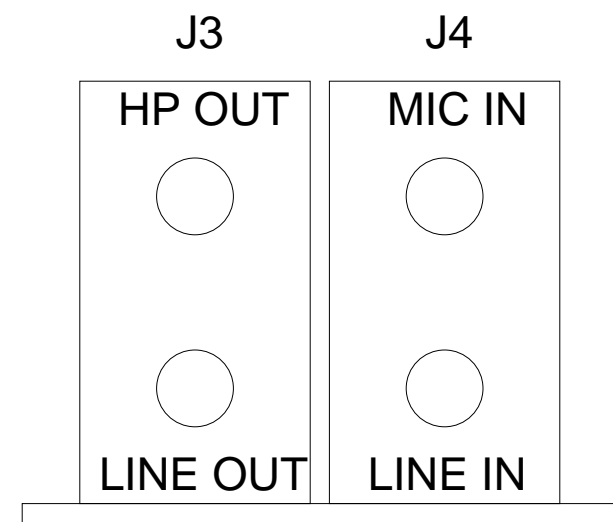


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PH: 1-800-ANALOGD

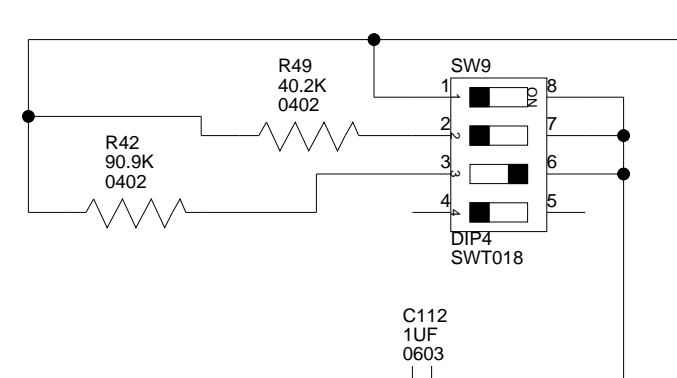
Title			<b>ADSP-526 EZ-BOARD MEMORY</b>		
Size C	Board No.	A0212-2007			Rev
Date	8-15-2008_13:19			Sheet	4 of 14



 <b>ANALOG DEVICES</b>		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		<b>Title</b> ADSP-526 EZ-BOARD DSP USB OTG	
<b>Size</b> C	<b>Board No.</b> A0212-2007	<b>Rev</b> 0.2A	
<b>Date</b> 8-15-2008_13:19	<b>Sheet</b> 5 of 14		



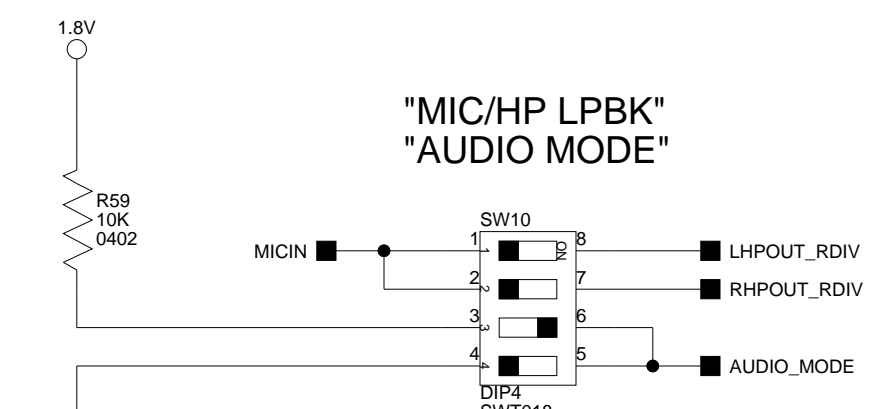
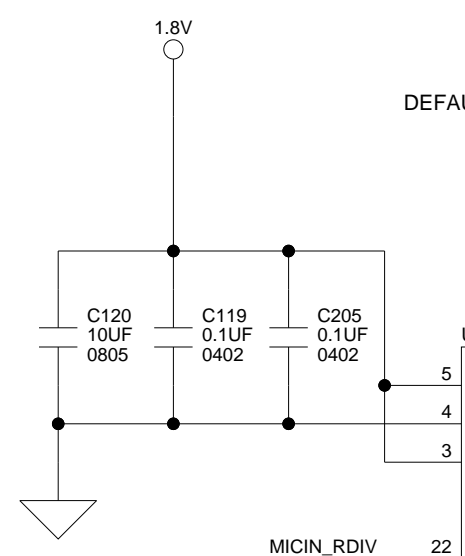
"MIC GAIN"



SW9: MIC GAIN

POS.	GAIN
1	5 (14dB)
2	1 (0dB)
3	0.5 (-6dB)
4	NC

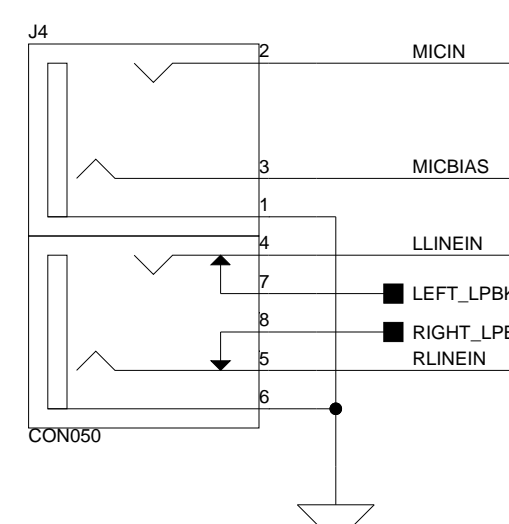
Table shows the gain if switch position in left column is ON, all others OFF.



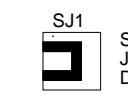
SW10 allows the MICIN signal to be looped back, for test purposes, to the Left and Right headphone. DO NOT switch positions 1 & 2 ON at the same time. Ensure that JP6 is on 2&3 or OFF when using SW10.

AUDIO CODEC INTERFACE MODE:  
 SW10.3 ON and SW10.4 OFF = SPI MODE  
 SW10.3 OFF and SW10.4 ON = TWI MODE

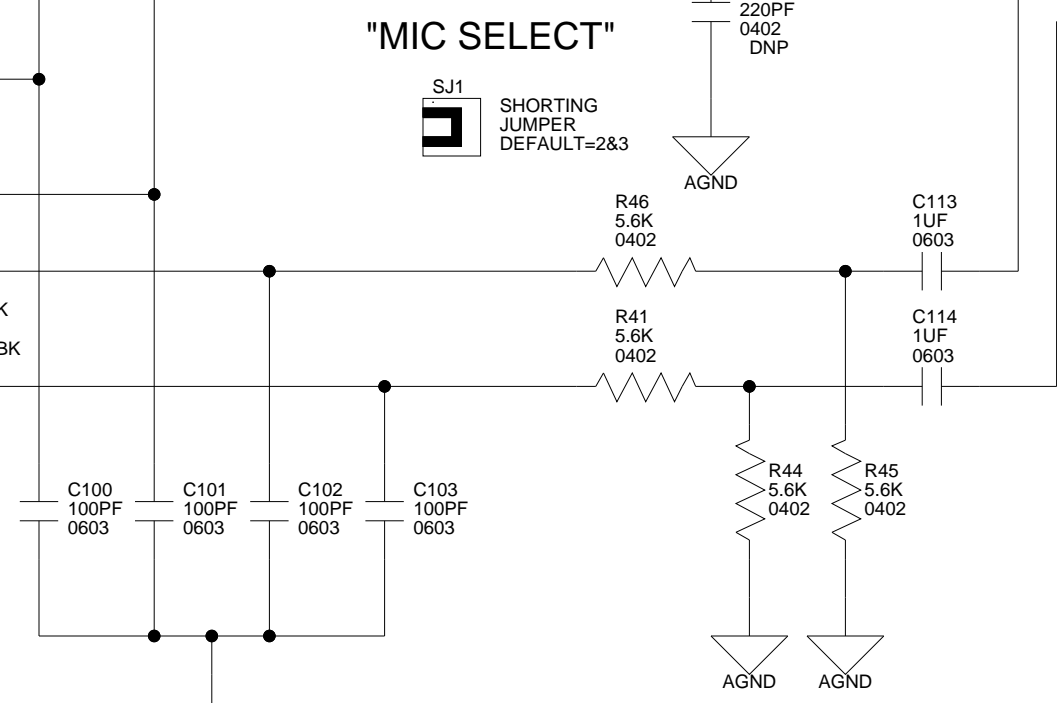
"MIC" "LINE IN"



"MIC SELECT"

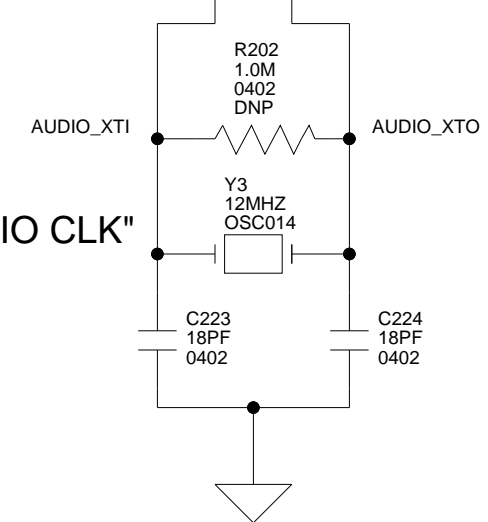


SHORTING JUMPER DEFAULT=2&3

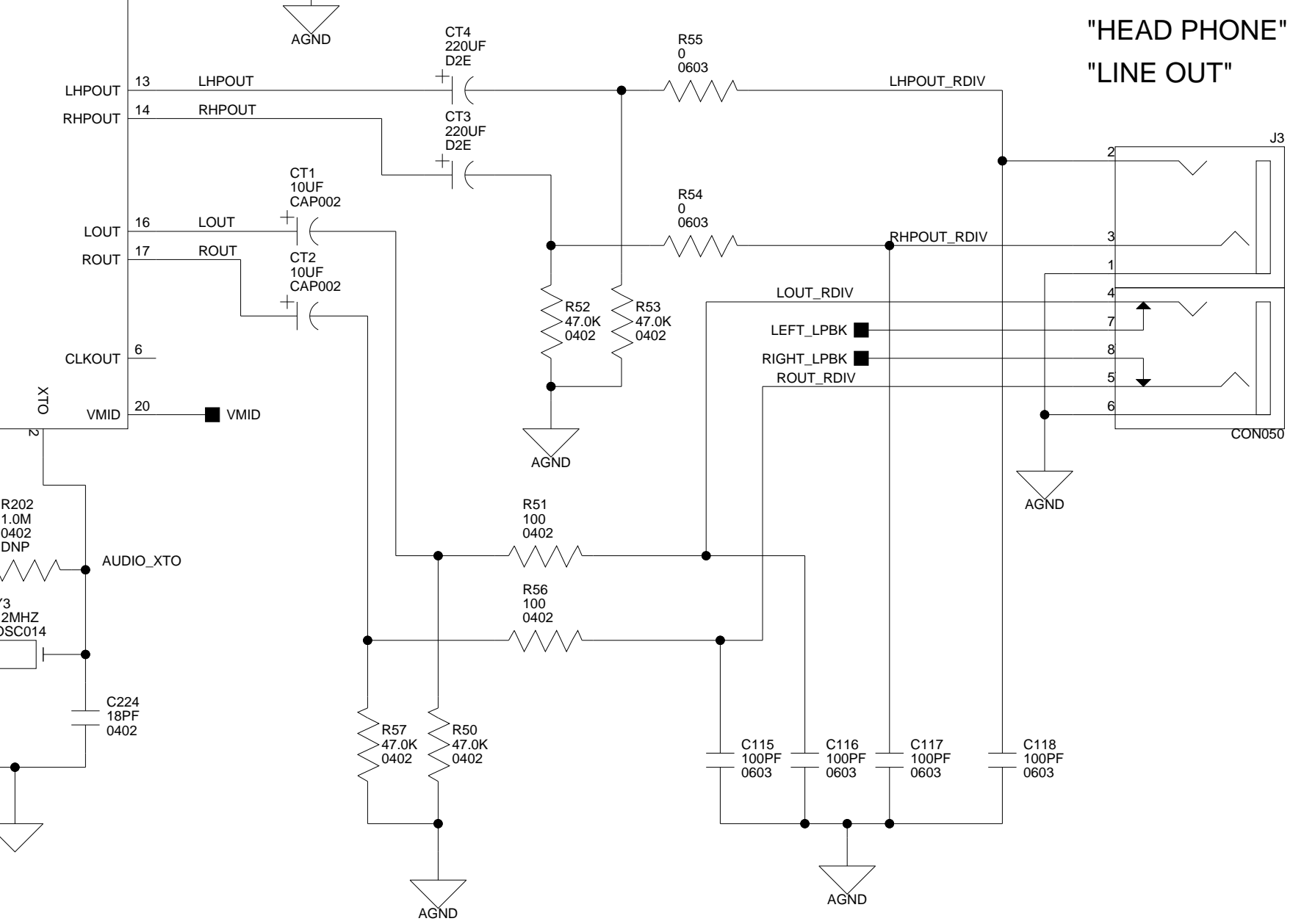


- CODEC\_DACLRC 9
- CODEC\_DACDAT 8
- CODEC\_ADCDAT 10
- CODEC\_ADCLRC 11
- BCLK 7
- AUDIO\_MODE 25
- CSB 26
- SDIN 27
- SCLK 28

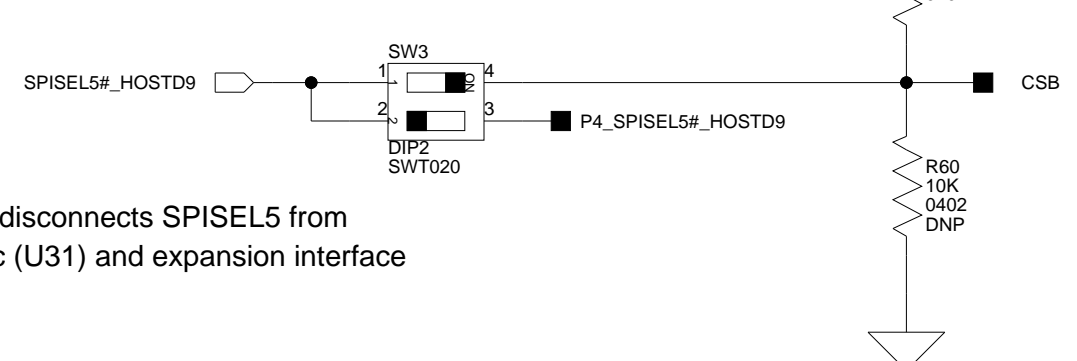
"AUDIO CLK"



"HEAD PHONE" "LINE OUT"

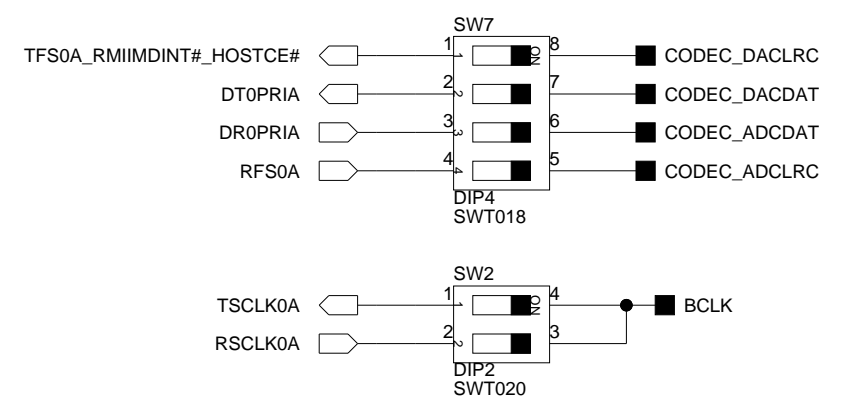


"CODEC CS"



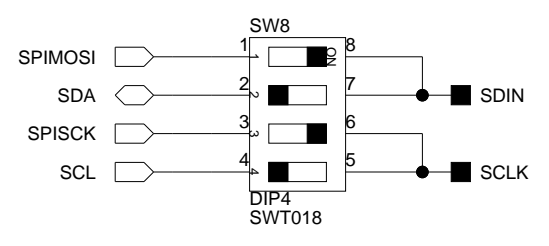
SW3 disconnects SPISEL5 from codec (U31) and expansion interface

"SPORT" "OA" "ENBL"



SW7 and SW2 disconnect DSP from AUDIO CODEC

"SPI/TWI"

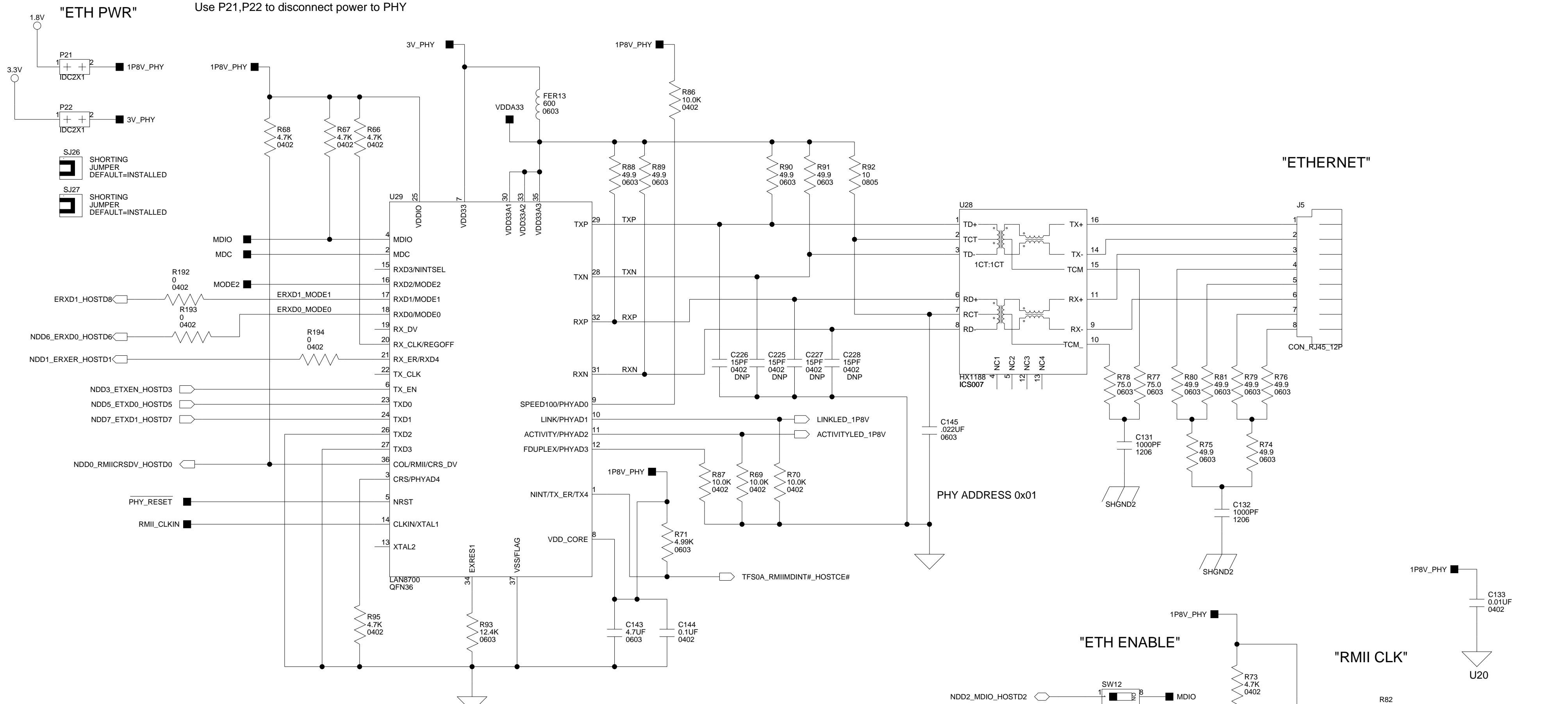


AUDIO CODEC MODE INTERFACE:  
 SPI MODE: ON, OFF, ON, OFF  
 TWI MODE: OFF, ON, OFF, ON

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 PH: 1-800-ANALOGD

Title			ADSP-526 EZ-BOARD AUDIO CODEC		
Size	Board No.				Rev
C	A0212-2007				0.2A
Date	8-28-2008_15:18	Sheet	6 of	14	





"ETH PWR"

Use P21,P22 to disconnect power to PHY

"ETHERNET"

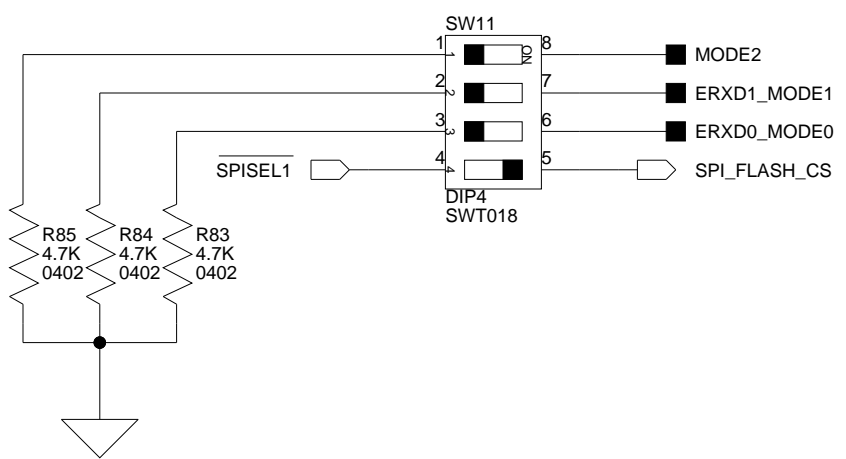
SW11: Ethernet Mode Select (SW9.1, SW9.2, SW9.3)

LAN8700 has internal mode pull-up pins.

MODE[2:0]	MODE DEFINITIONS
111	All Capable, Auto Negotiation <b>DEFAULT</b>
110	Power Down Mode
101	Repeater Mode, Auto Negotiation
100	100Base-TX Half duplex Advertised, Auto Negotiaion
011	100Base-TX Full Duplex
010	100Base-TX Half Duplex
001	10Base-T Full Duplex
000	10Base-T Half Duplex

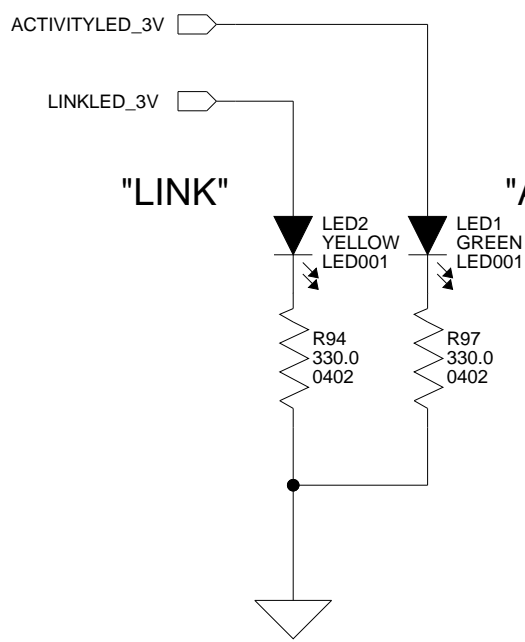
SW11.4 disconnects SPISEL1, for expansion interface (P1.26, P2.21)

"ETH MODE" "FLASH CS"



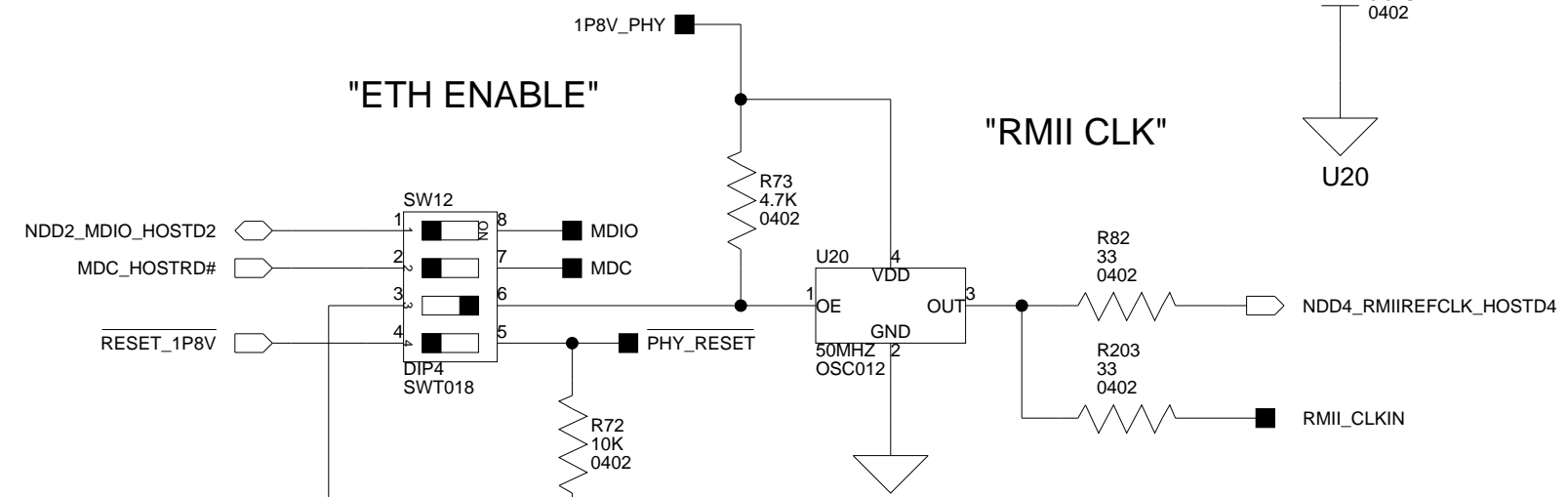
"LINK"

"ACTIVITY"



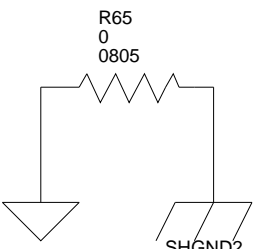
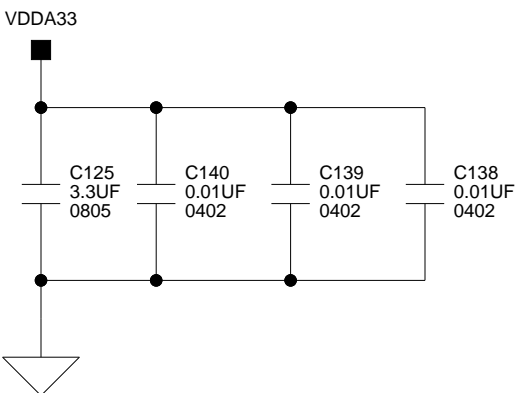
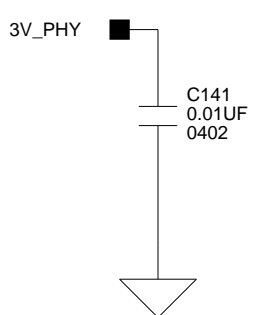
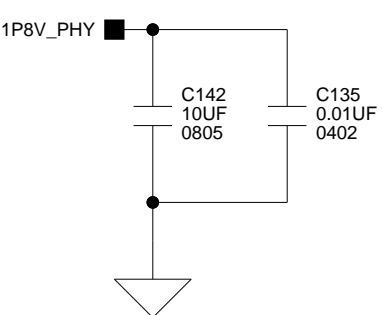
"ETH ENABLE"

"RMI CLK"



SW12: ETH Enable

POS.	FROM	TO	DEFAULT	FUNCTIONS
SW1.1	DSP (U2, PH2)	PHY (U14)	OFF	ON (MDIO PHY U14), OFF (NAND U4, HOST connector P13.27, Expansion Interface J3.42)
SW1.2	DSP (U2, PG14)	PHY (U14)	OFF	ON (MDC PHY U14), OFF ( HOST connector P13.2, Expansion Interface J3.41)
SW1.3	GND	RMI CLK (U24)	ON	ON (RMI CLK disabled), OFF (RMI CLK enabled)
SW1.4	RESET IC (U27)	PHY (U14)	OFF	ON (PHY not held in reset), OFF (PHY held in reset)

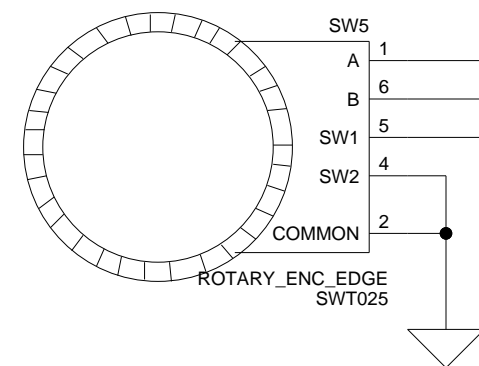


**ANALOG DEVICES**

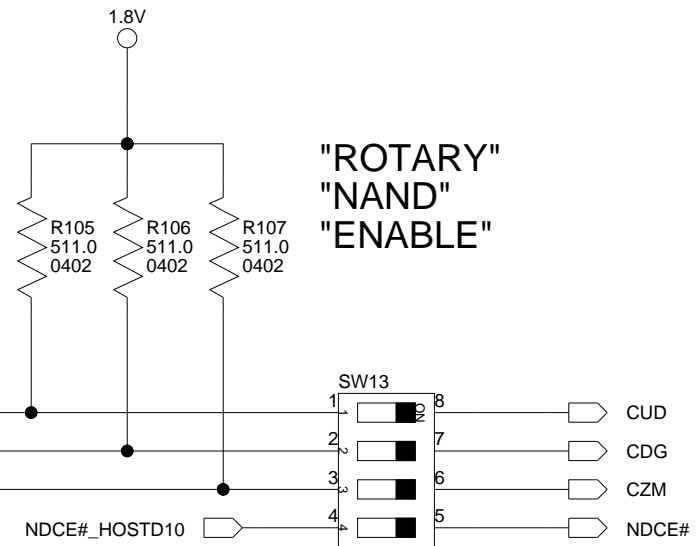
20 Cotton Road  
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PH: 1-800-ANALOGD

<b>Title</b> ADSP-526 EZ-BOARD RMI PHY			
<b>Size C</b>	<b>Board No.</b> A0212-2007	<b>Rev</b> 0.2A	
<b>Date</b> 8-27-2008_9:47	<b>Sheet</b> 7 of 14		

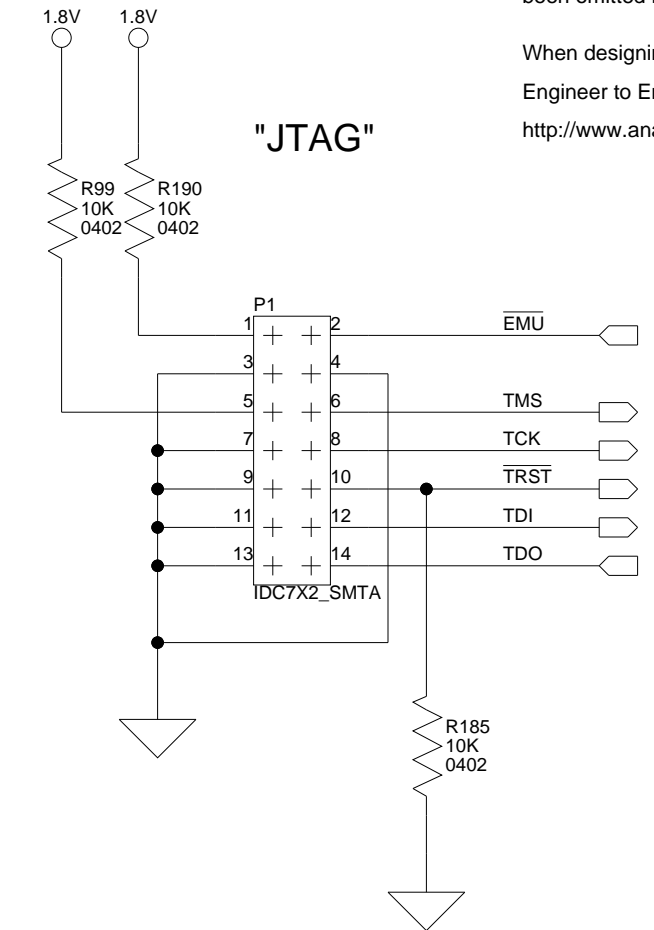
"ENCODER"



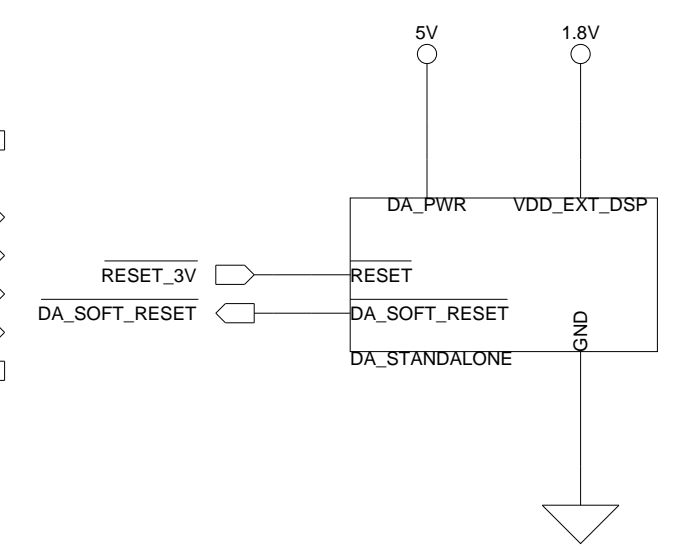
"ROTARY"  
"NAND"  
"ENABLE"



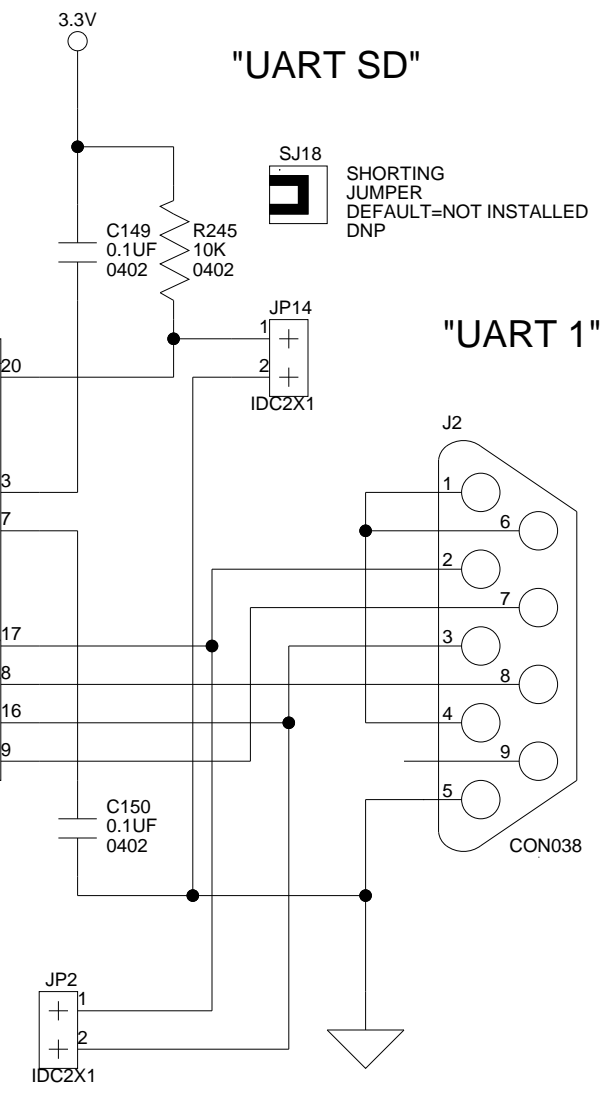
"JTAG"



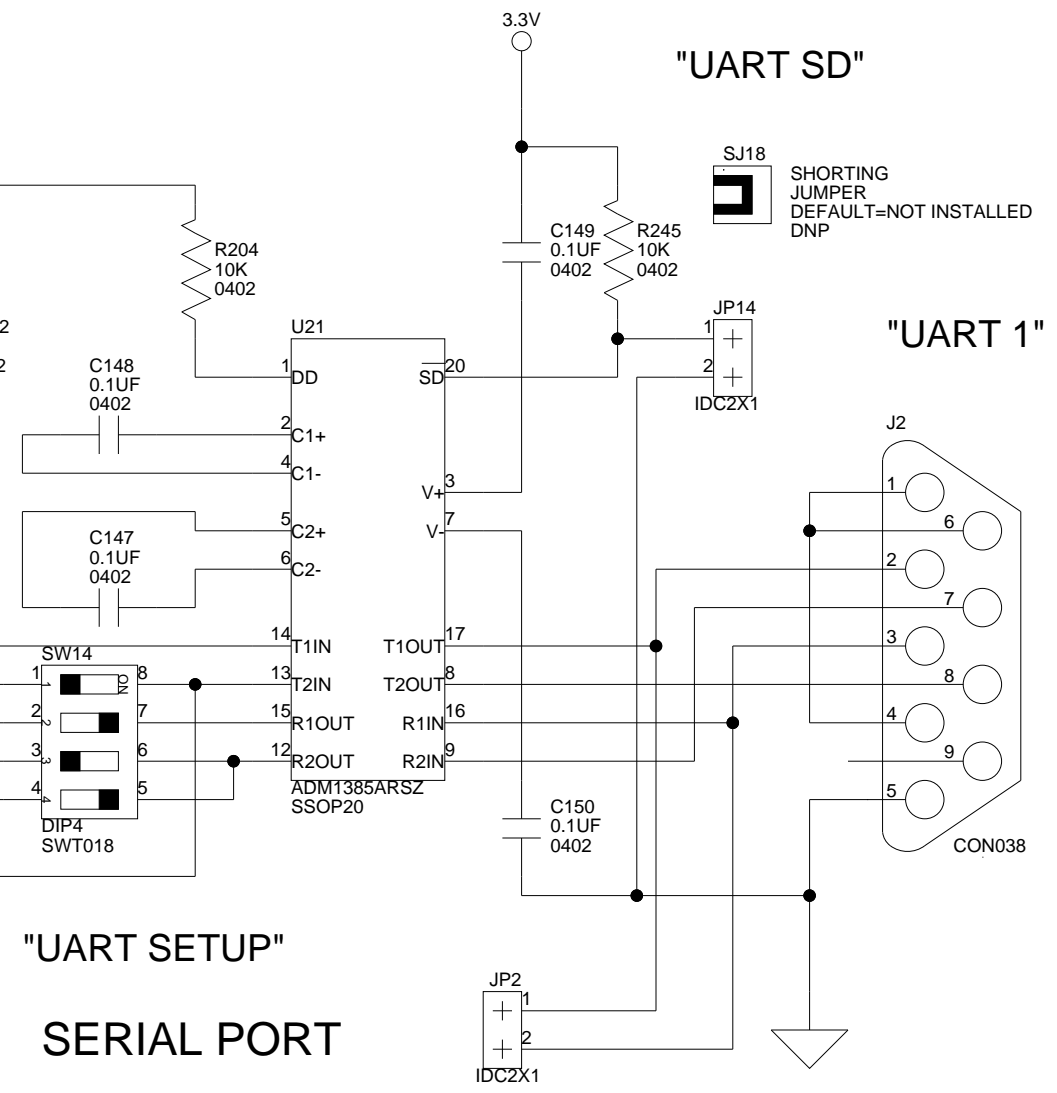
All USB interface circuitry is considered proprietary and has been omitted from this schematic.  
When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at <http://www.analog.com>



"UART SD"

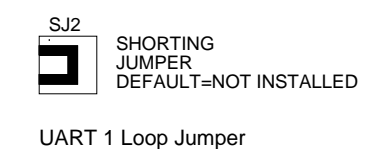


"UART 1"

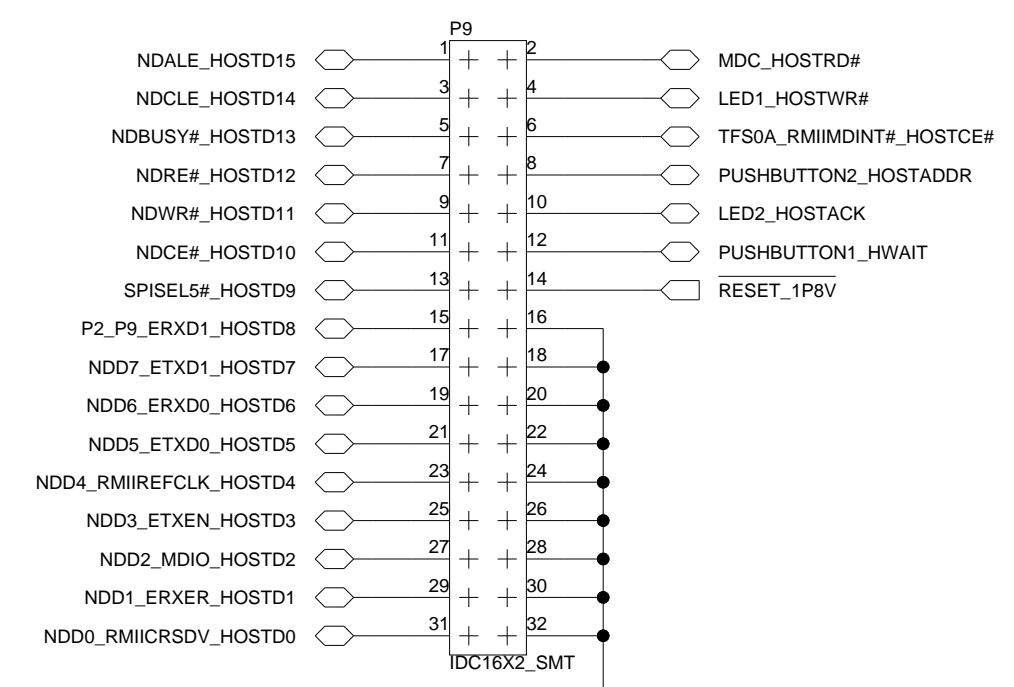


"UART SETUP"  
SERIAL PORT  
(UART 1)

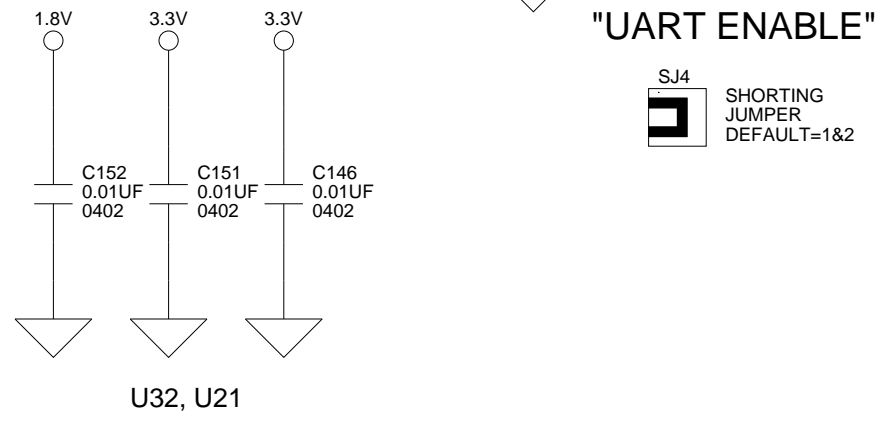
"UART LPBK"



"HOST"

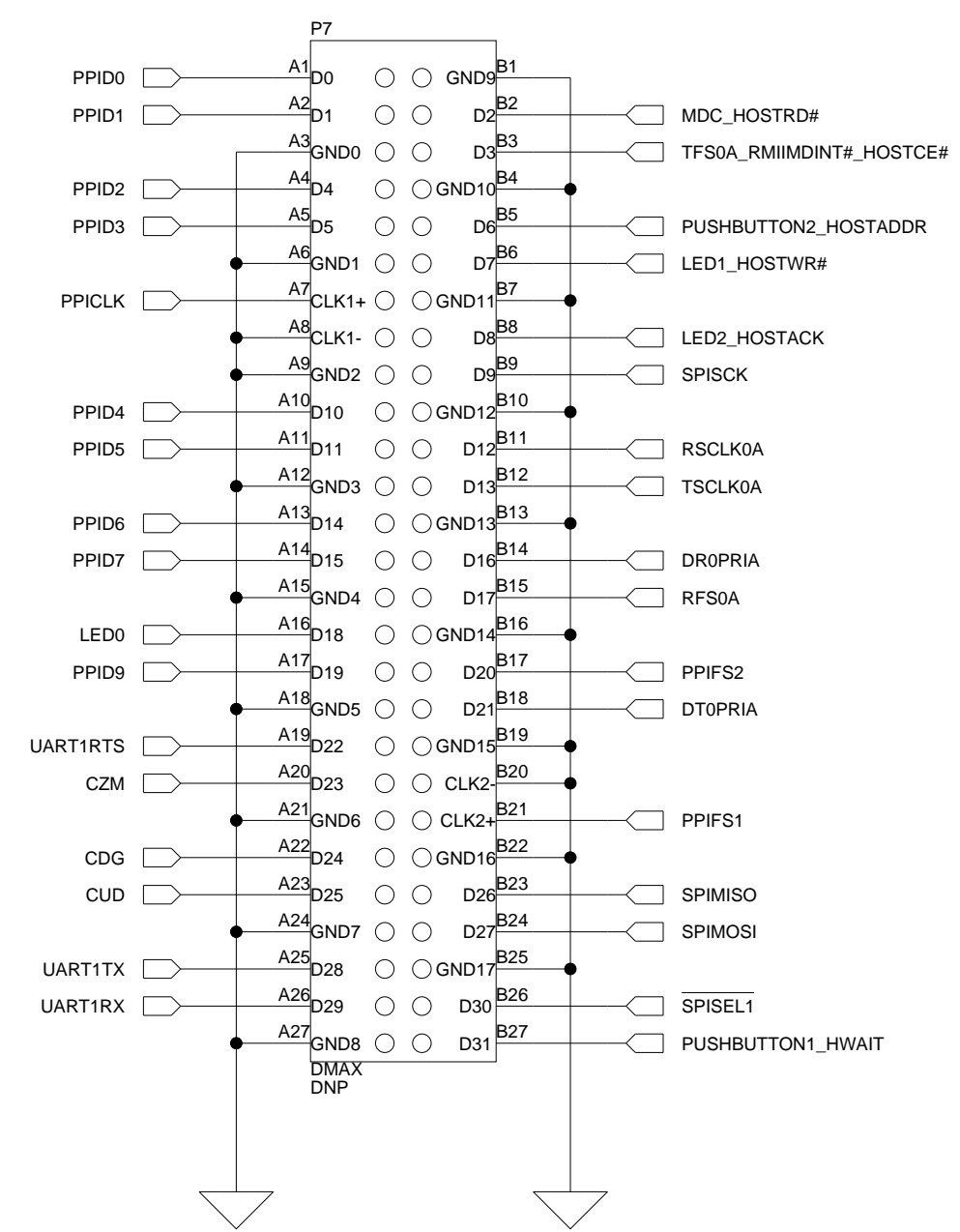
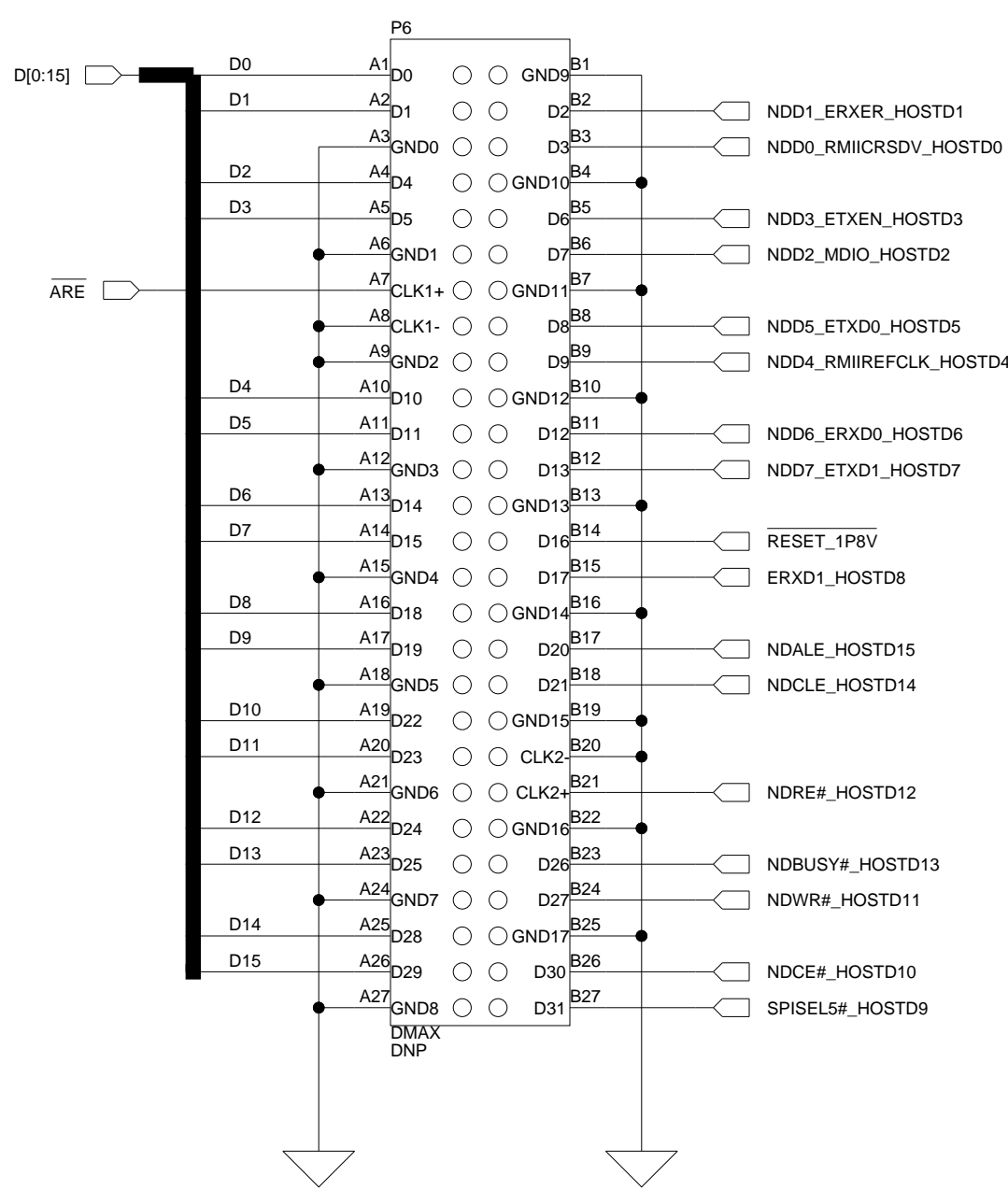
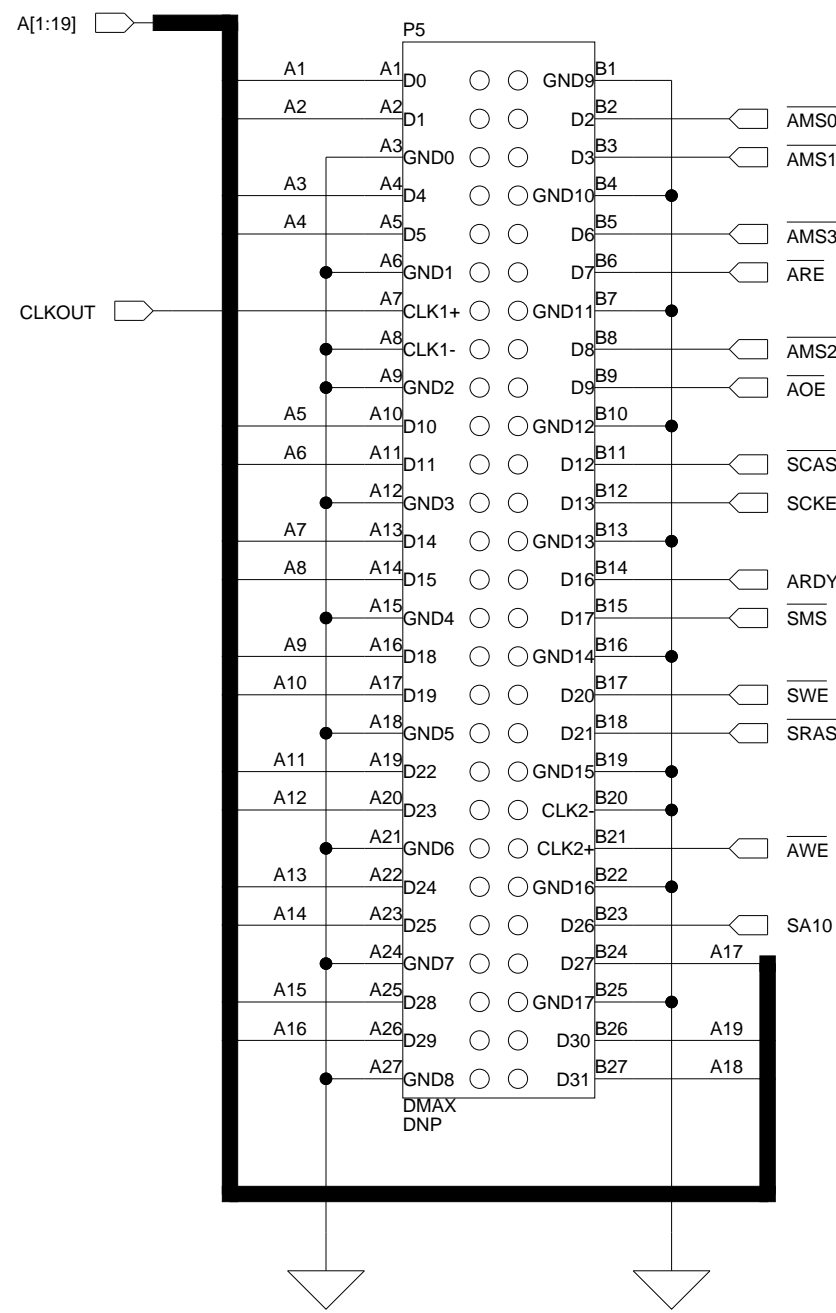


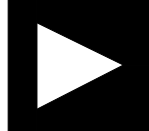
"UART ENABLE"

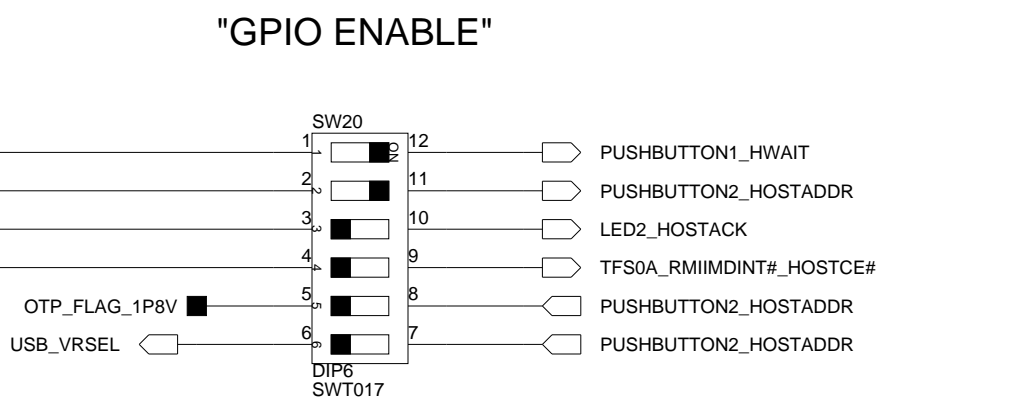
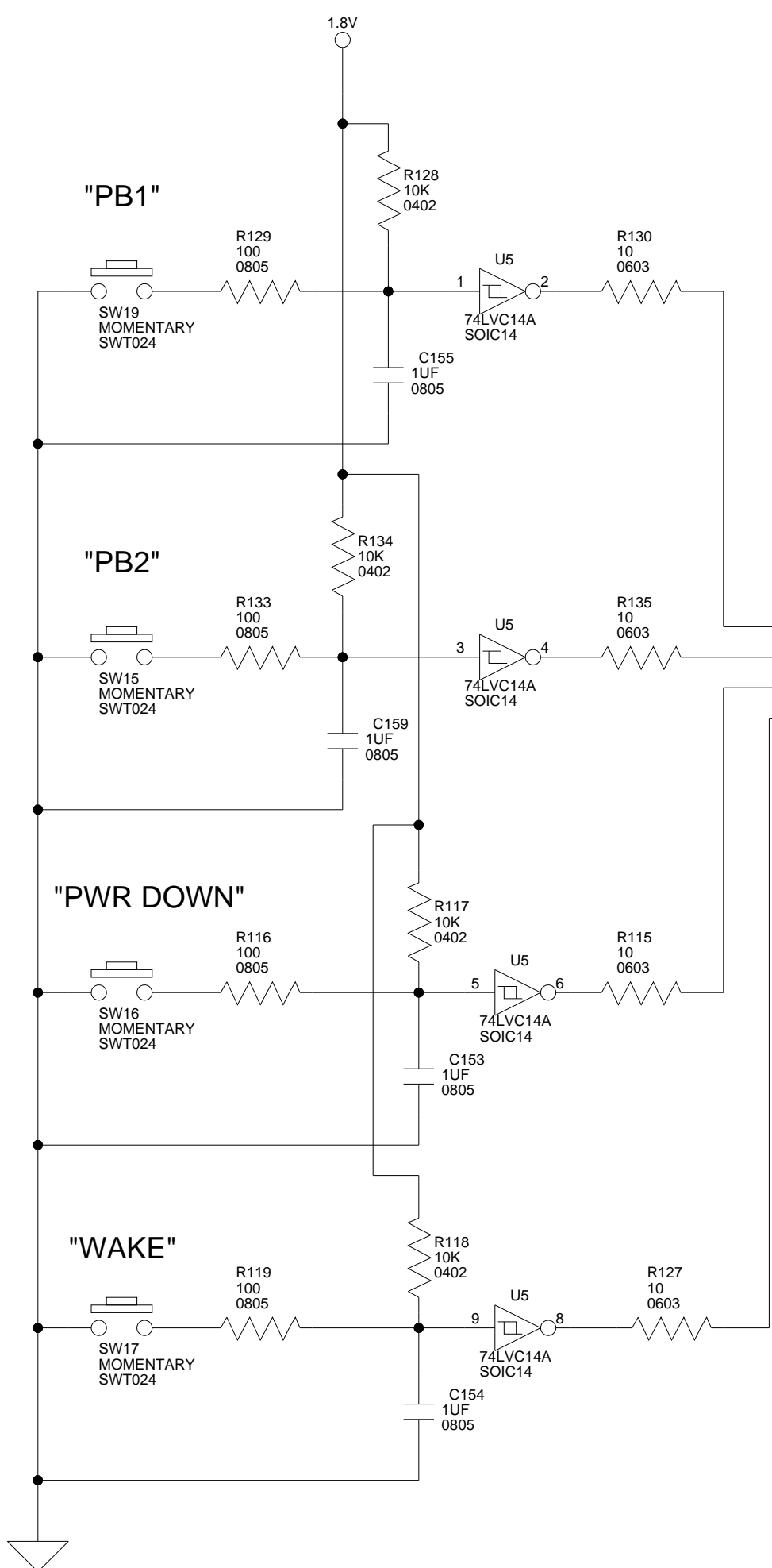


		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
<b>Title</b> ADSP-526 EZ-BOARD ROTARY ENCODER, JTAG, RS232, HOST			
<b>Size</b> C	<b>Board No.</b> A0212-2007	<b>Rev</b> 0.2A	
<b>Date</b> 8-28-2008_11:59	<b>Sheet</b> 8 of 14		

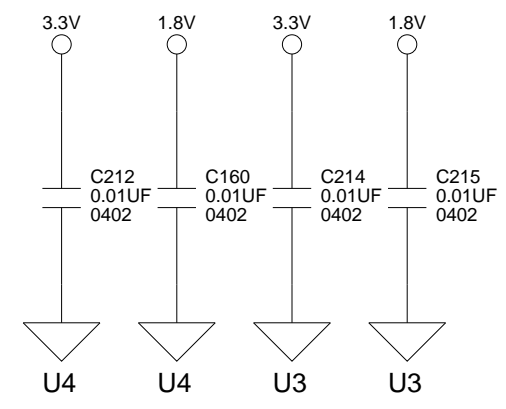
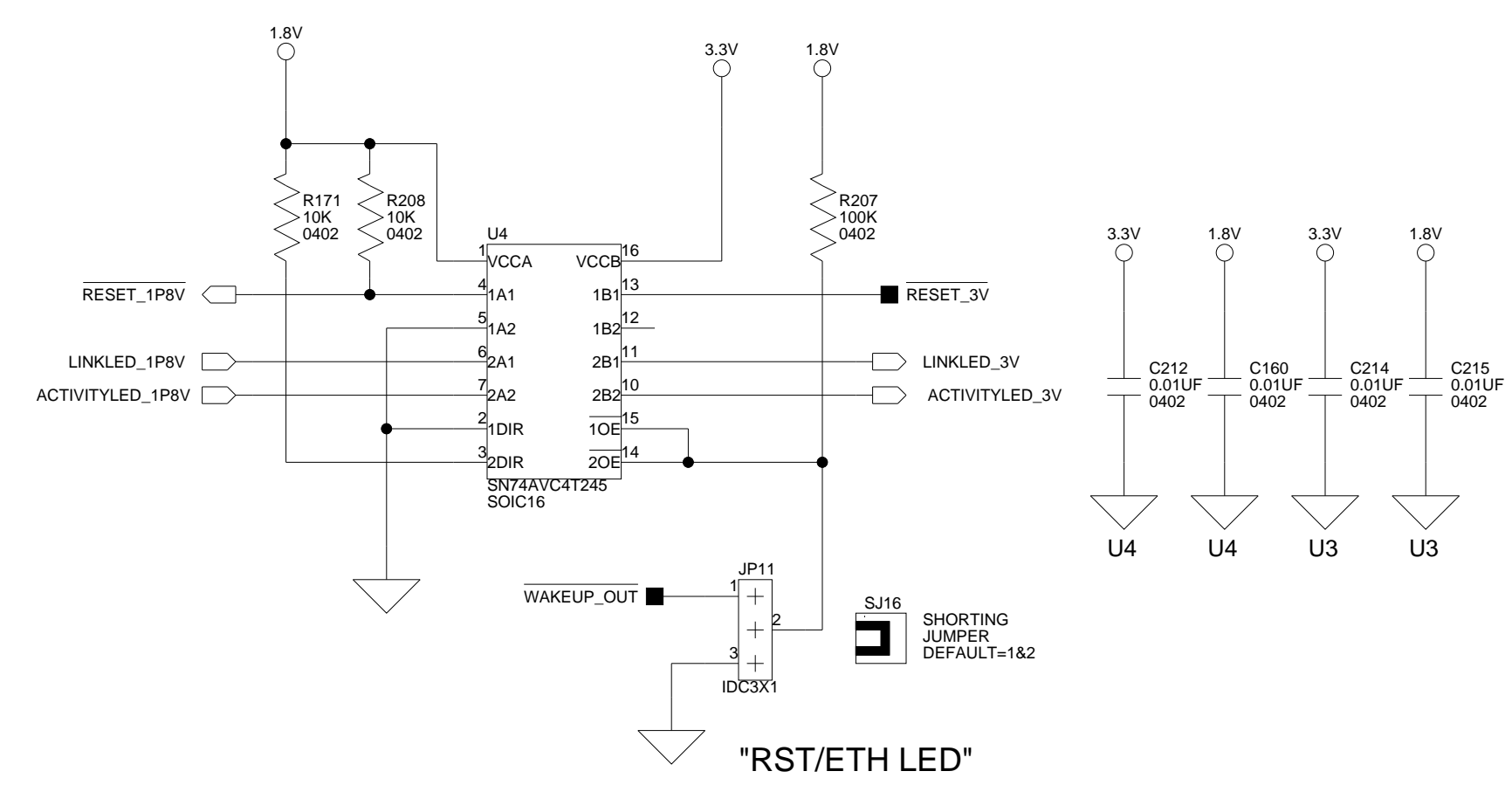
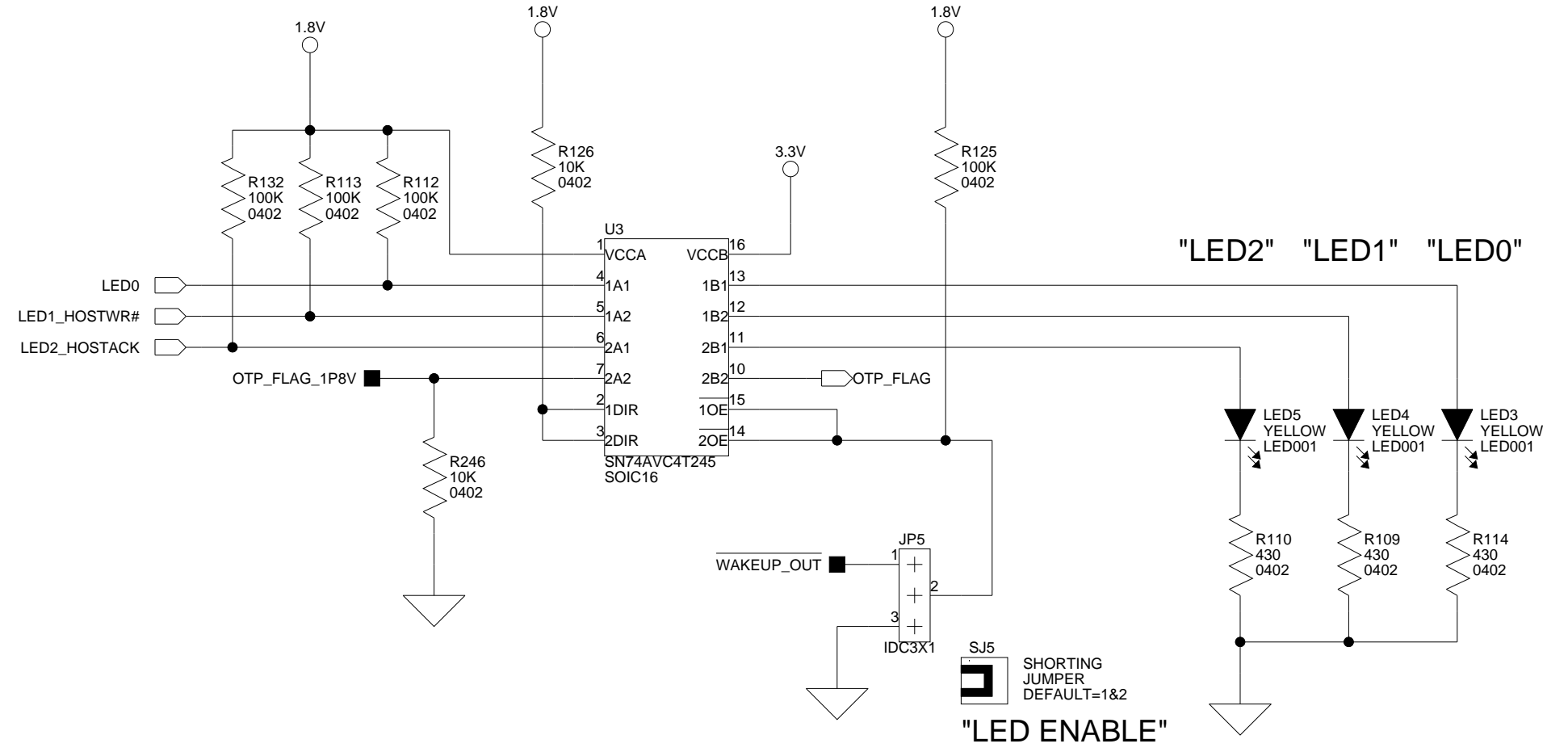
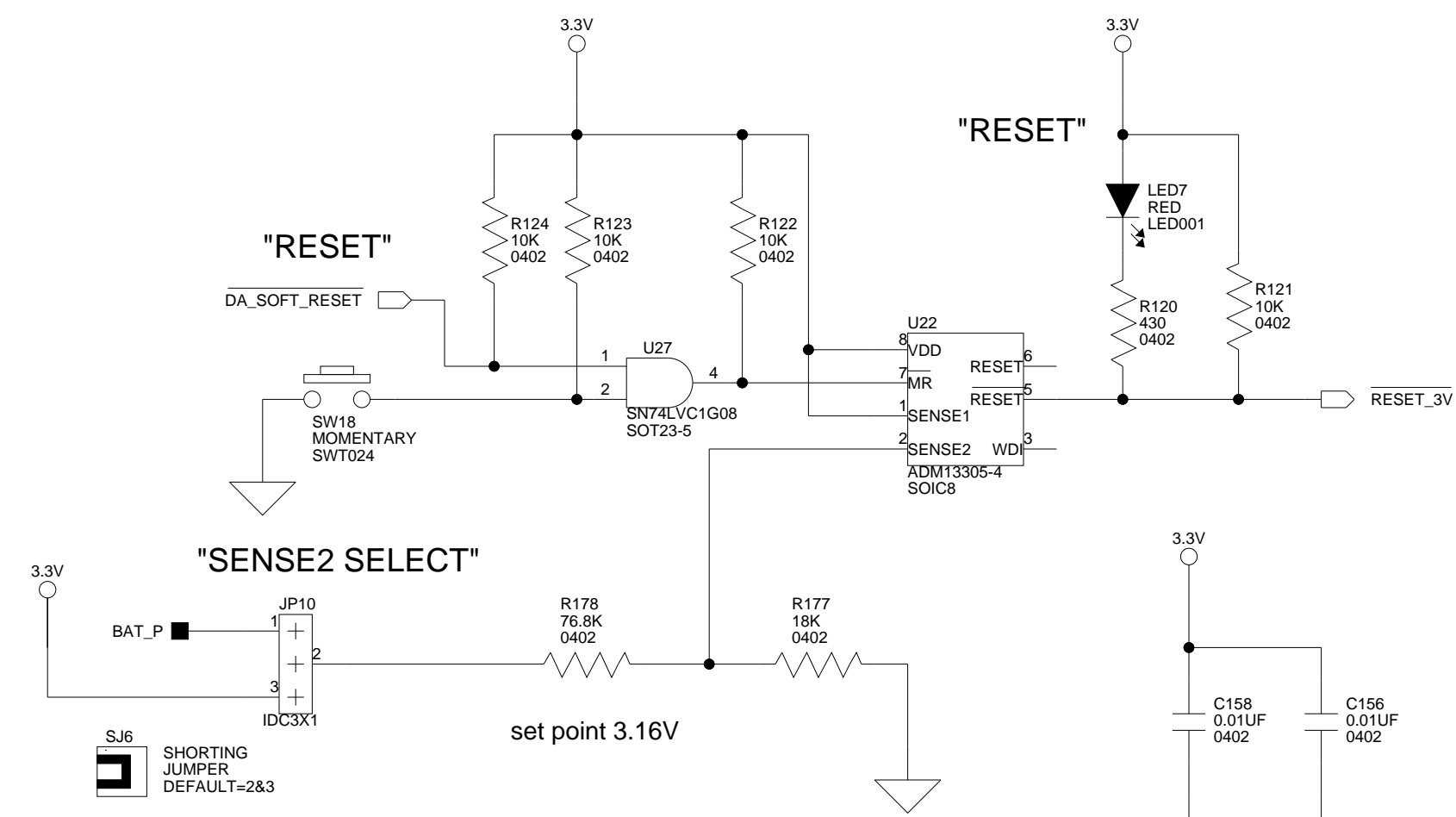
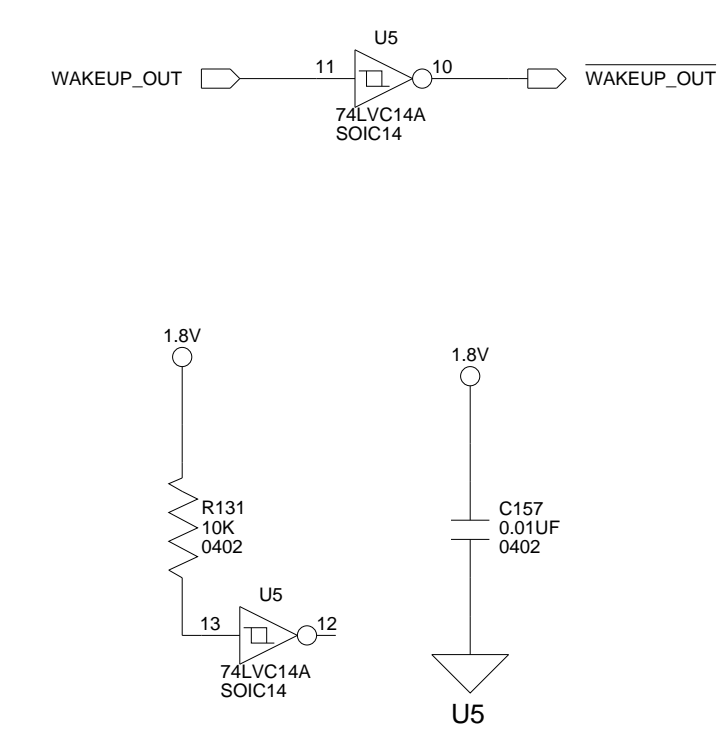
LOGIC ANALYZER COMPRESSION LAND GRID ARRAY



 <b>ANALOG DEVICES</b>		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		<b>Title</b> ADSP-526 EZ-BOARD LOGIC ANALYZER CONN	
<b>Size C</b>	<b>Board No.</b> A0212-2007	<b>Rev</b> 0.2A	
<b>Date</b> 8-15-2008_13:19	<b>Sheet</b> 9 of 14		



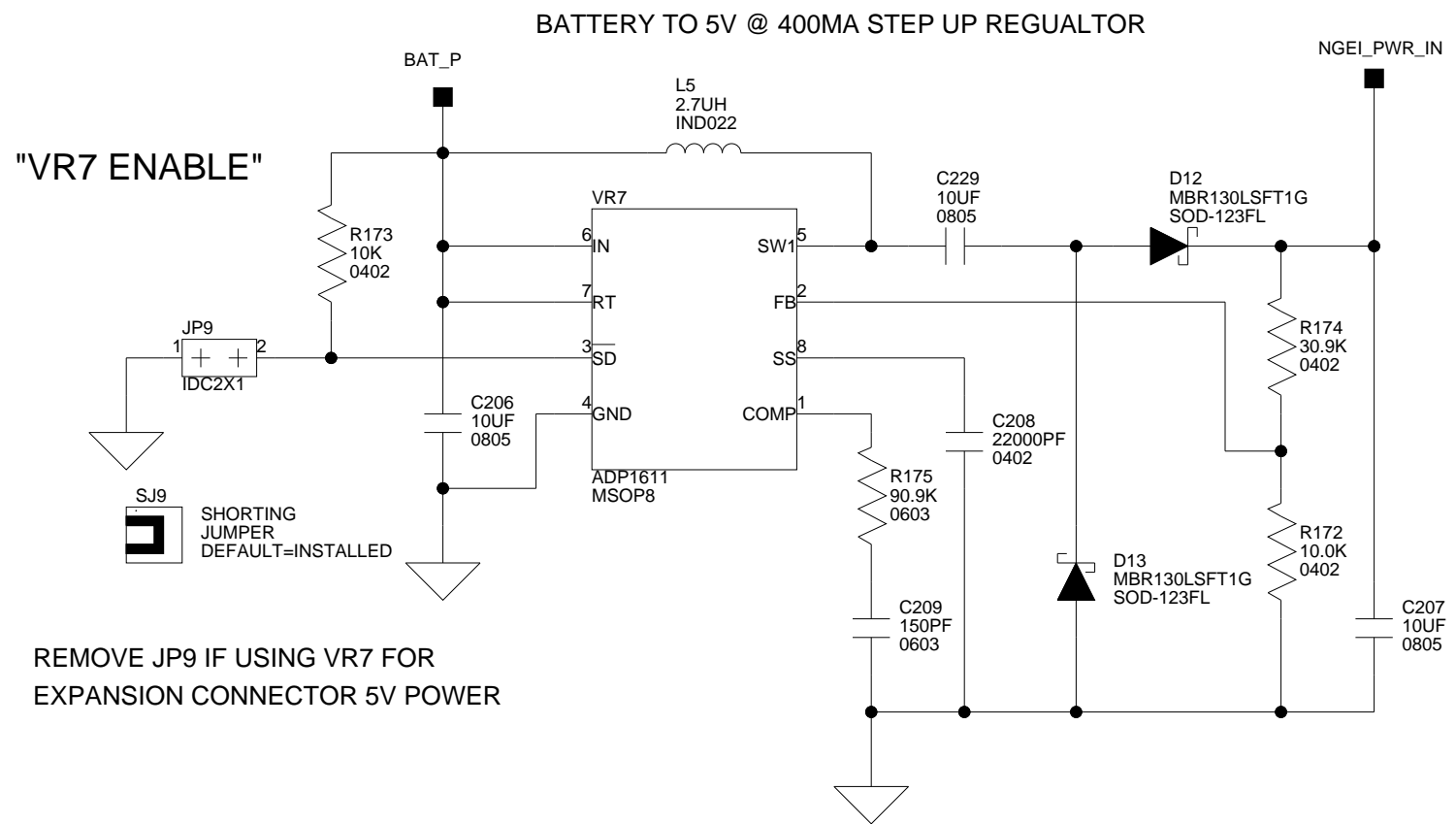
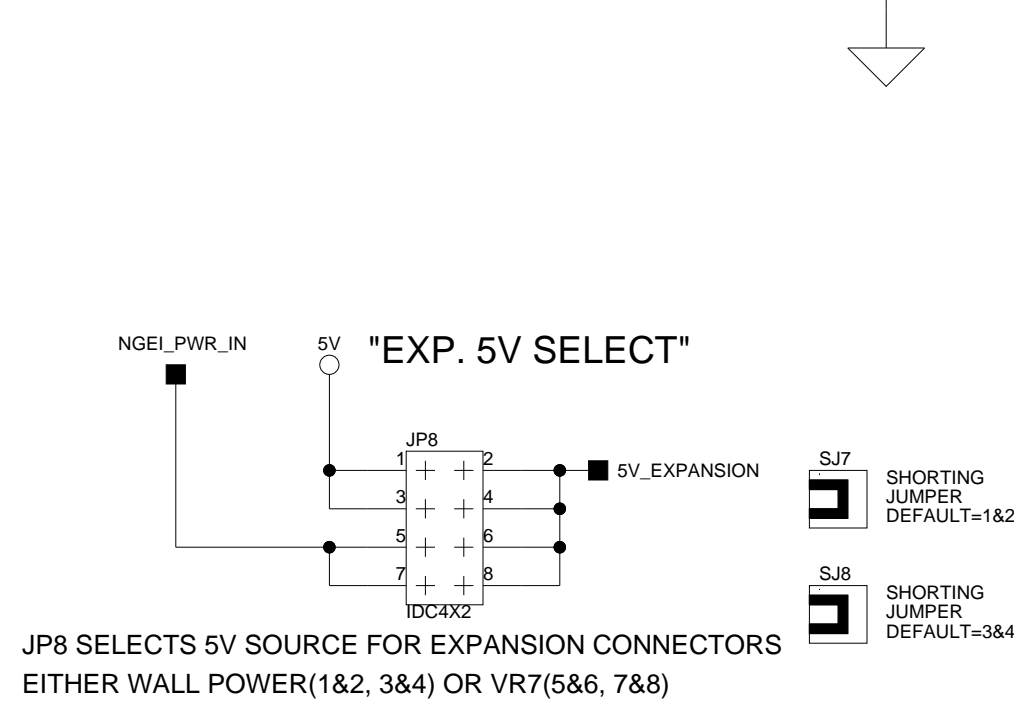
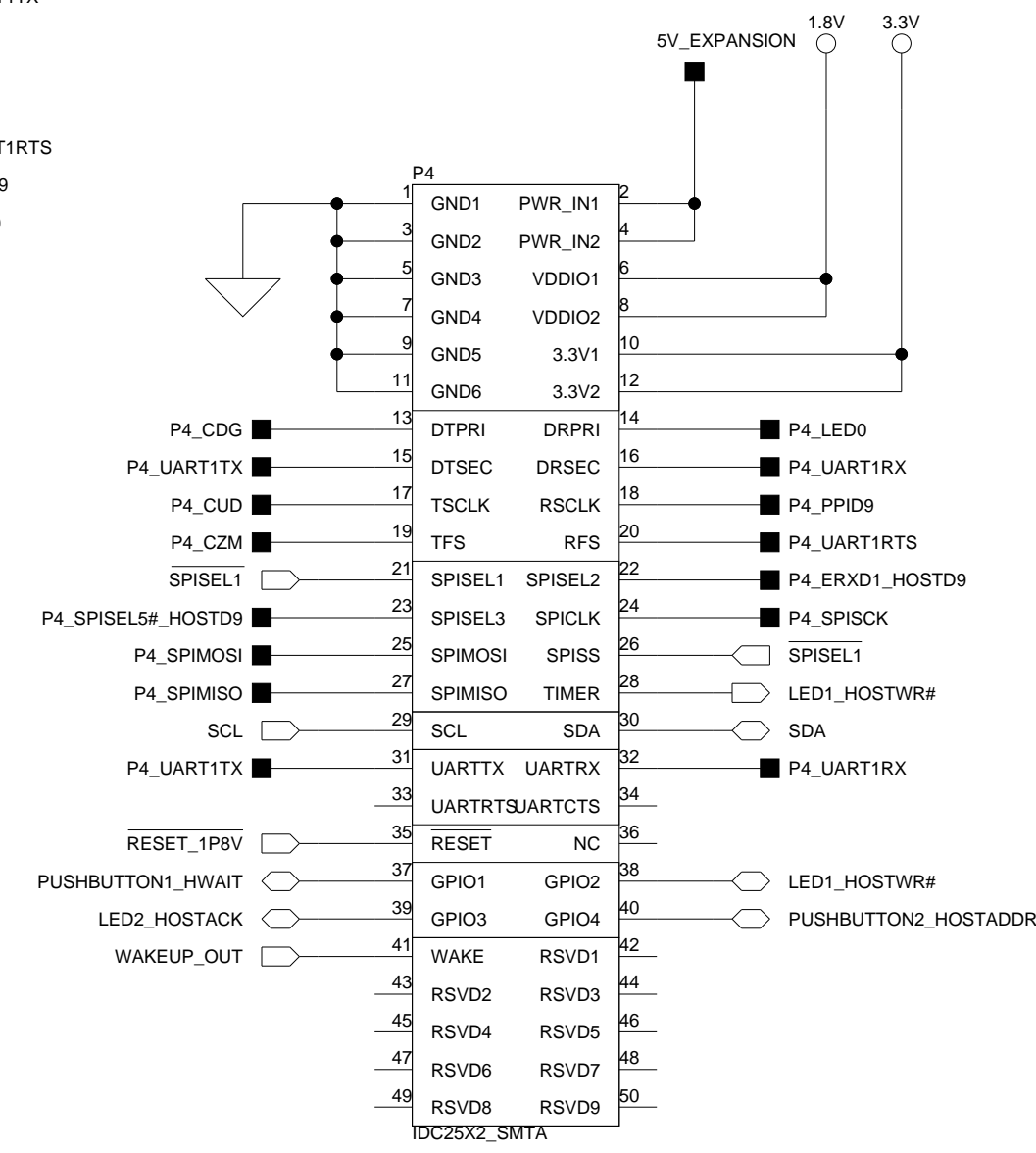
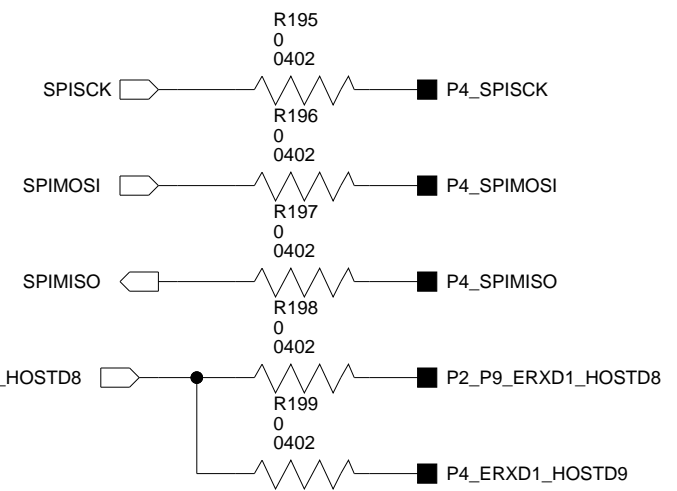
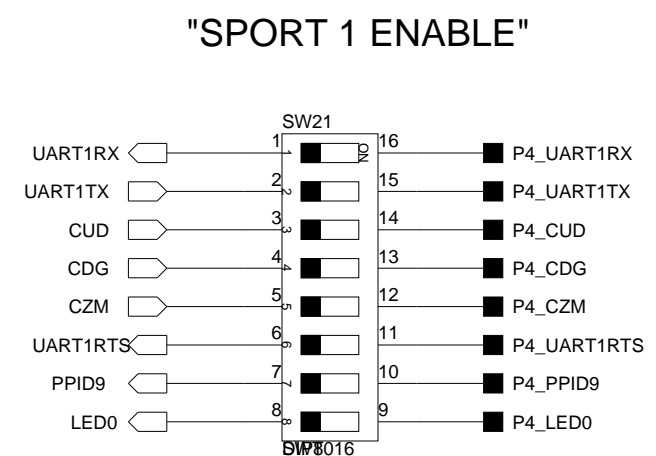
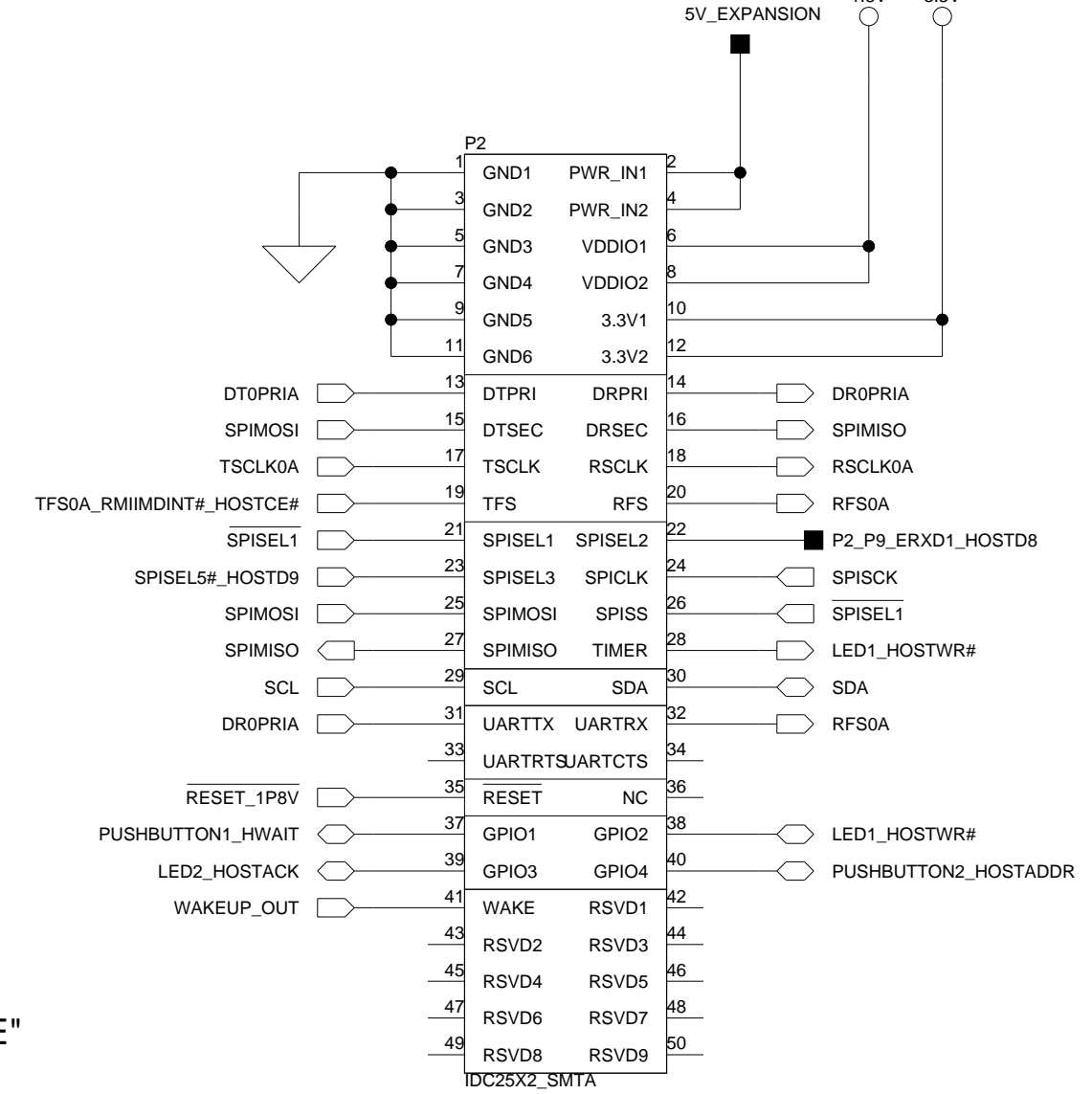
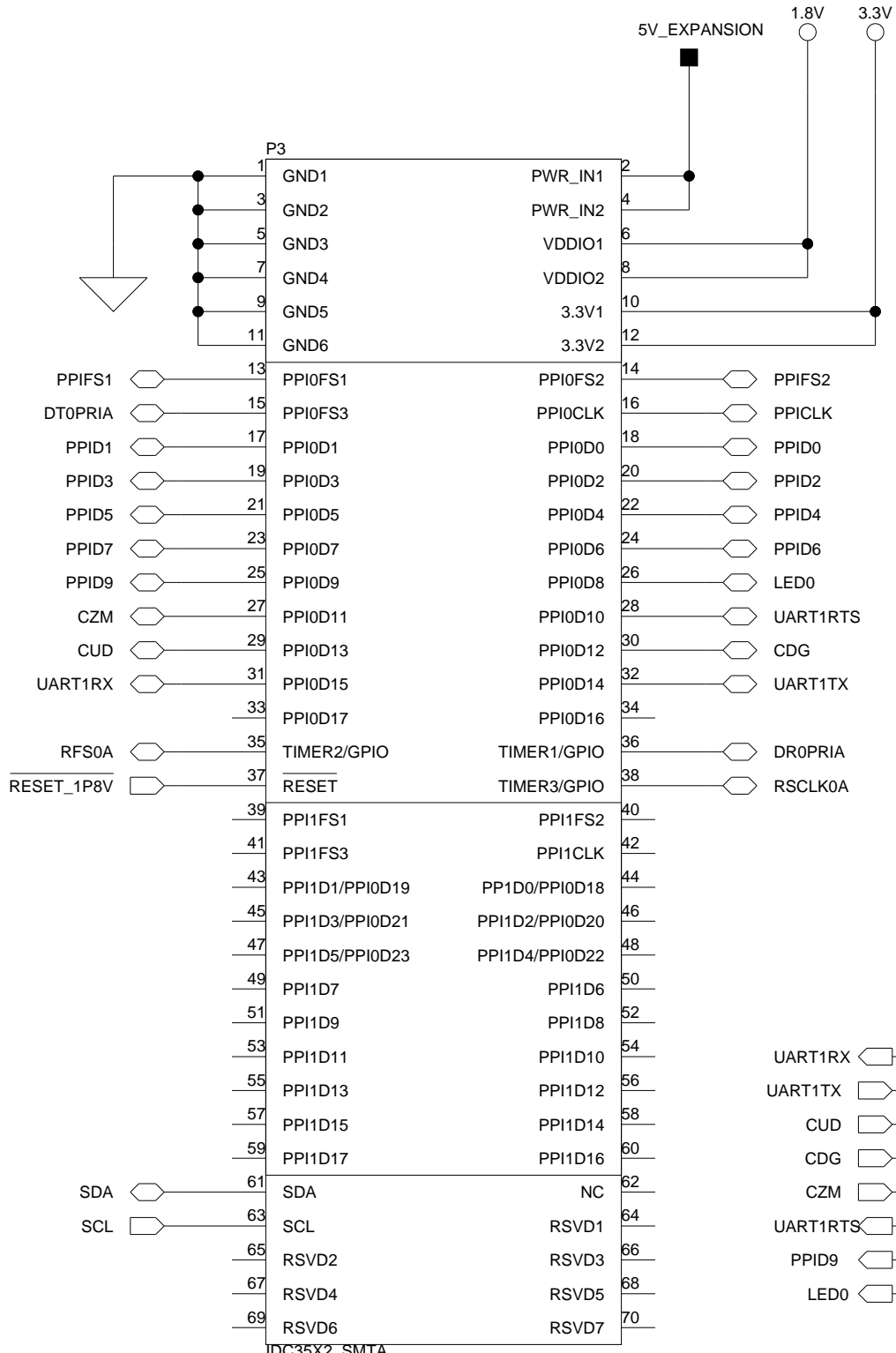
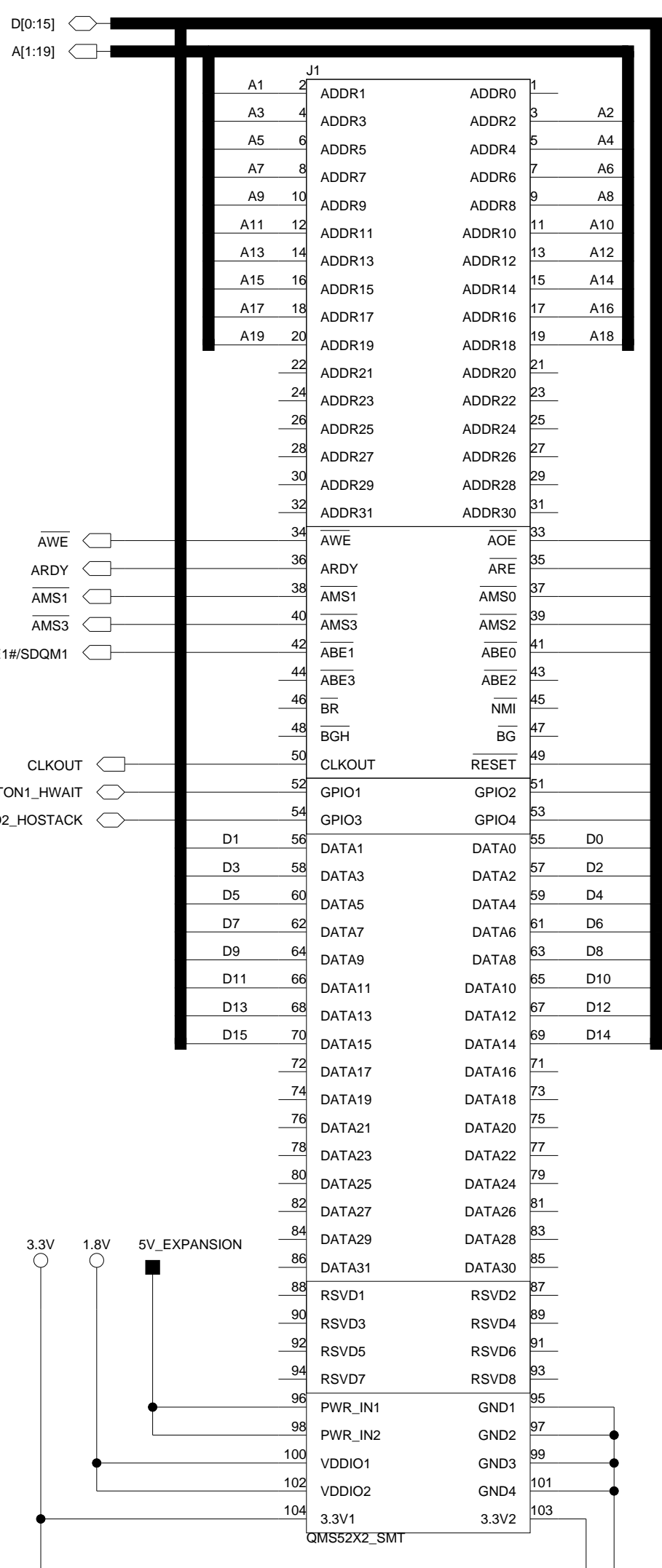
SW20 Position (Default)	FROM	TO	FUNCTION
1 (ON)	Pushbutton 1 (SW19)	DSP (U1, PG0)	ON (PB1), OFF (UART 1 CTS U21, HOST connector P9.12, expansion interface P2.37, P4.37, J1.52)
2 (ON)	Pushbutton 2 (SW15)	DSP (U1, PG13)	ON (PB2), OFF (host connector P9.8, OTP flag for writes SW20.8, OTG voltage select SW13.7, expansion interface P2.40, P4.40, J1.53)
3 (OFF)	Power down pushbutton (SW16)	DSP (U1, PG12)	OFF (LED2 not driven by power down pushbutton). ON (SW16 drives PG12).
4 (OFF)	Wake pushbutton (SW16)	DSP (U1, PG15)	ON (connects wake pushbutton SW17 to PG15).
5 (OFF)	OTP_FLAG_1P8V (U3)	DSP (U1, PG13)	ON (PG13 controls OTP flag for OTP writes. NOTE requires SW20.2 OFF, SW20.6 OFF and JP16 installed.)
6 (OFF)	USB_VRSEL (U23)	DSP (U1, PG13)	ON (PG13 controls USB_VRSEL PG13 for OTG host power. NOTE requires SW20.2 OFF, SW20.5 OFF).

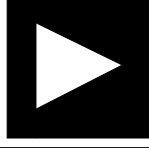


**ANALOG DEVICES**

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PH: 1-800-ANALOGD

Title			<b>ADSP-526 EZ-BOARD RESET, LEDS</b>		
Size C	Board No.	A0212-2007			Rev
		0.2A			
Date	8-28-2008_13:27		Sheet	10 of	14



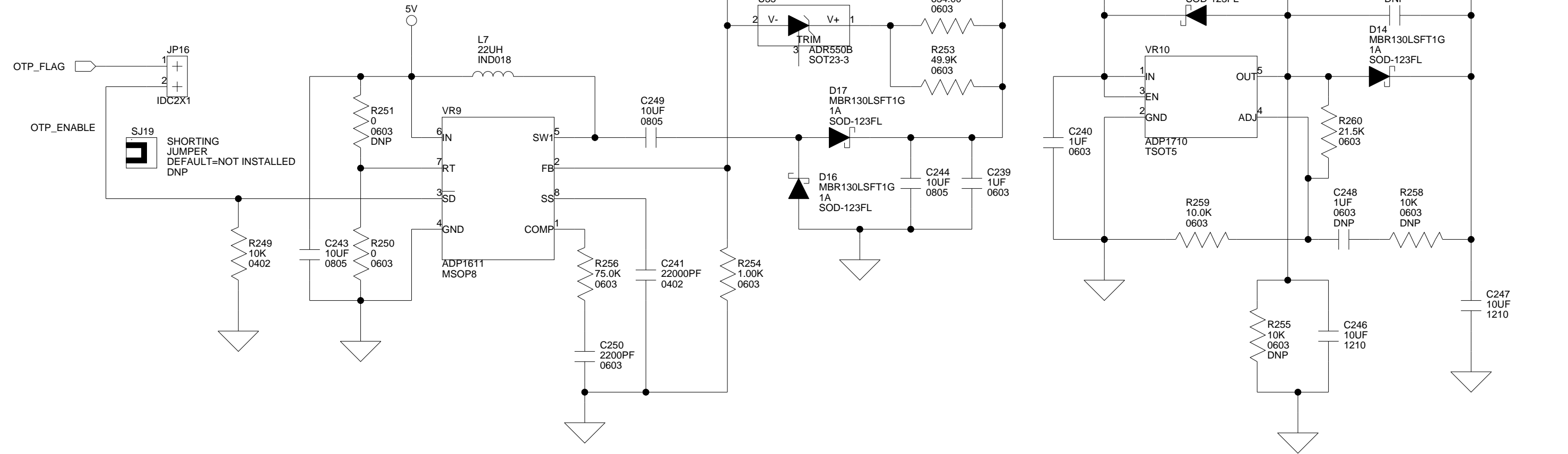


20 Cotton Road  
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PH: 1-800-ANALOGD

Title: ADSP-526 EZ-BOARD EXPANSION INTERFACE		
Size C	Board No. A0212-2007	Rev 0.2A
Date: 8-21-2008_11:10	Sheet 11 of 14	

Warning: Do NOT drive OTP\_Enable high for excessive time. See BF526 datasheet for exact details

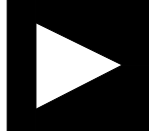
"OTP FLAG ENABLE"

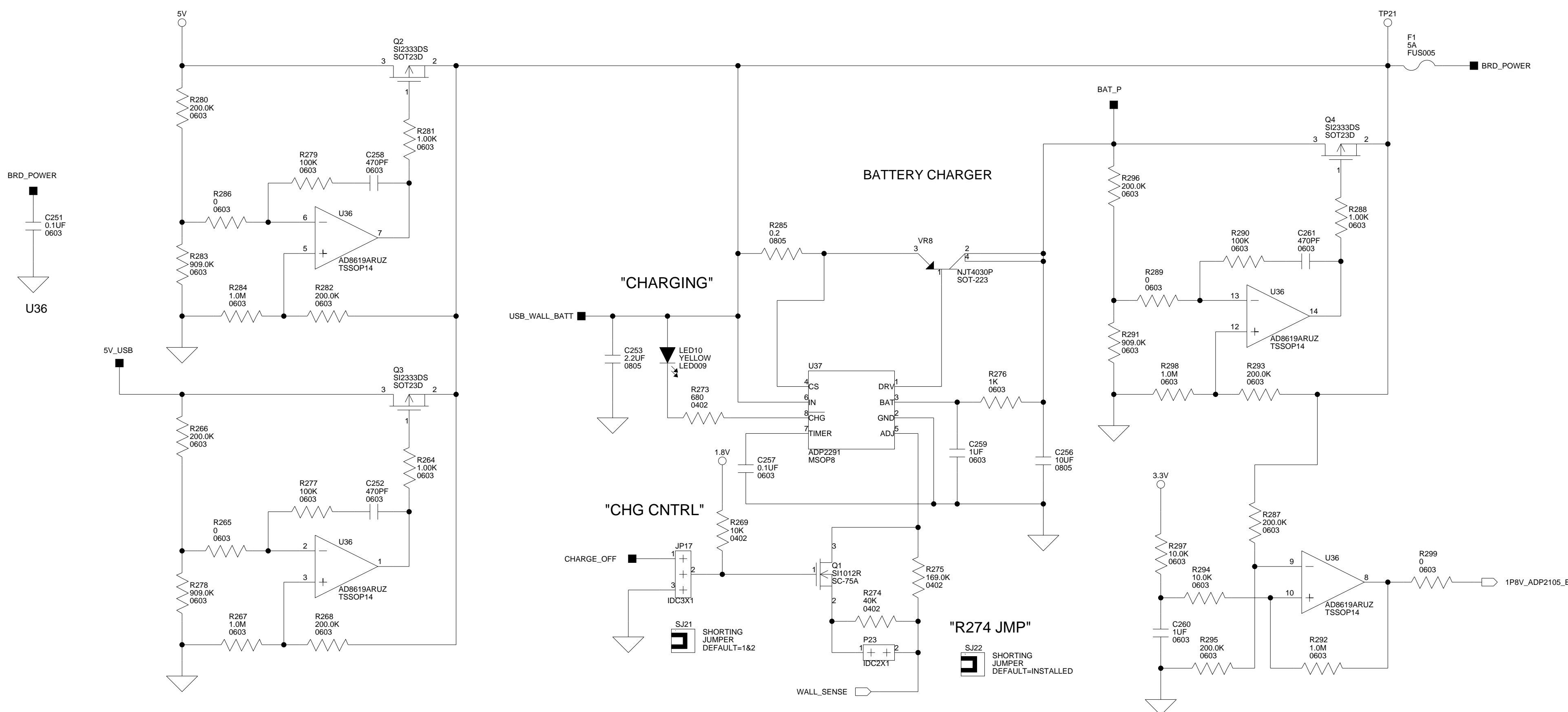


OTP POWER

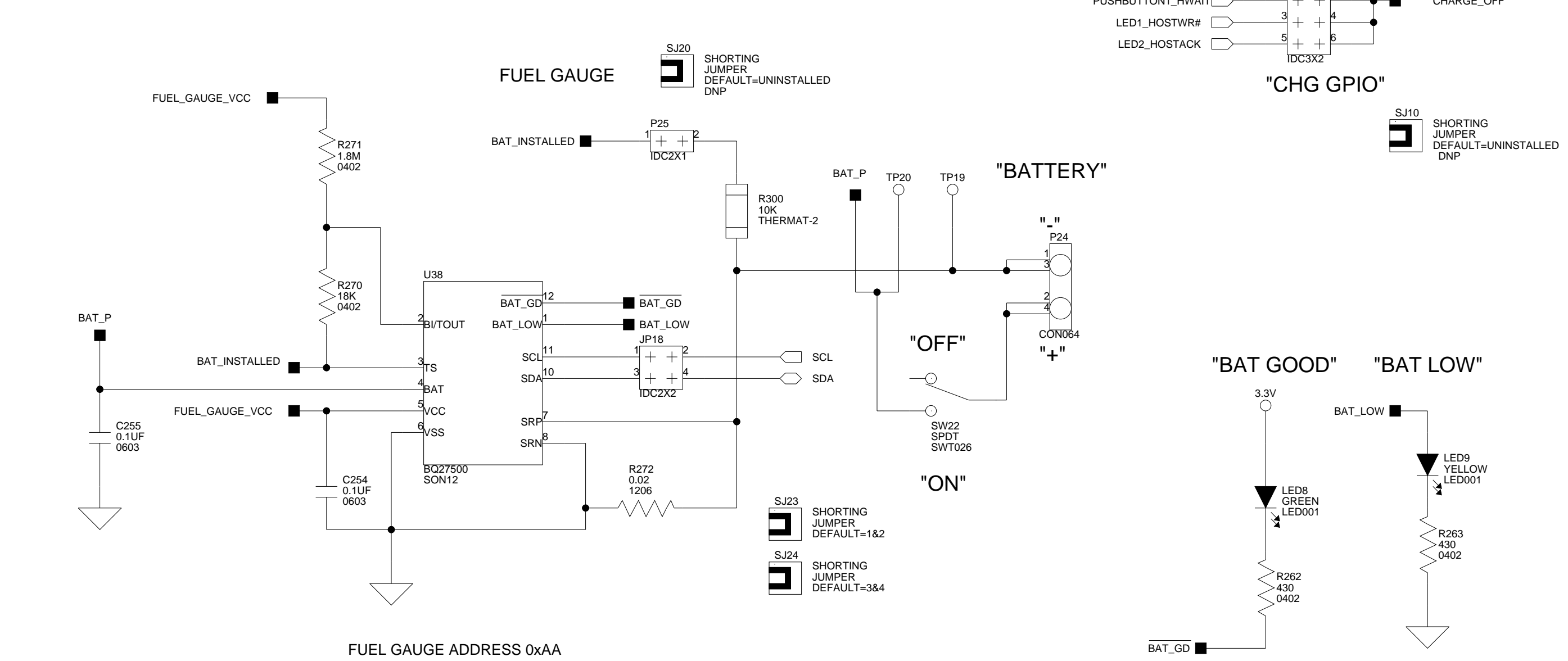
"5V USB"

5V @ 500mA

 <b>ANALOG DEVICES</b>		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title <b>ADSP-526 EZ-BOARD</b> <b>OTP POWER, 5V_USB FET</b>	
Size <b>C</b>	Board No. <b>A0212-2007</b>	Rev <b>0.2A</b>	
Date <b>8-28-2008_11:59</b>		Sheet <b>12</b> of <b>14</b>	



"BATT INSTALLED"



Charge rate selection

MODE	WALL	USB	JP17	P23	Resistance	Charge Rate
Full Charge	YES	NO	X <sup>1</sup>	X	OPEN	750 mA
Low	NO	YES	OFF	OFF	32K	100 mA
Medium	NO	YES	2&3	X	169K	375 mA
Selectable <sup>2</sup>	NO	YES	1&2	OFF	32/169K	100/375 mA
Shutdown	NO	YES	OFF	ON	0	NONE
Control Shutdown <sup>3</sup>	NO	YES	1&2	ON	0/169K	0/375 mA

<sup>1</sup> Any jumper setting has no affect  
<sup>2</sup> Rate is selectable by the processor's flag, use JP15 to chose the flag pin. Setting the flag high selects 83 mA and setting the flag low selects 375 mA charge rates.  
<sup>3</sup> JP15 needs to be set to positions 1&2 (PG0), 3&4 (PG11), or 5&6 (PG12), selecting the processor port pin to control the selection.

**ANALOG DEVICES**

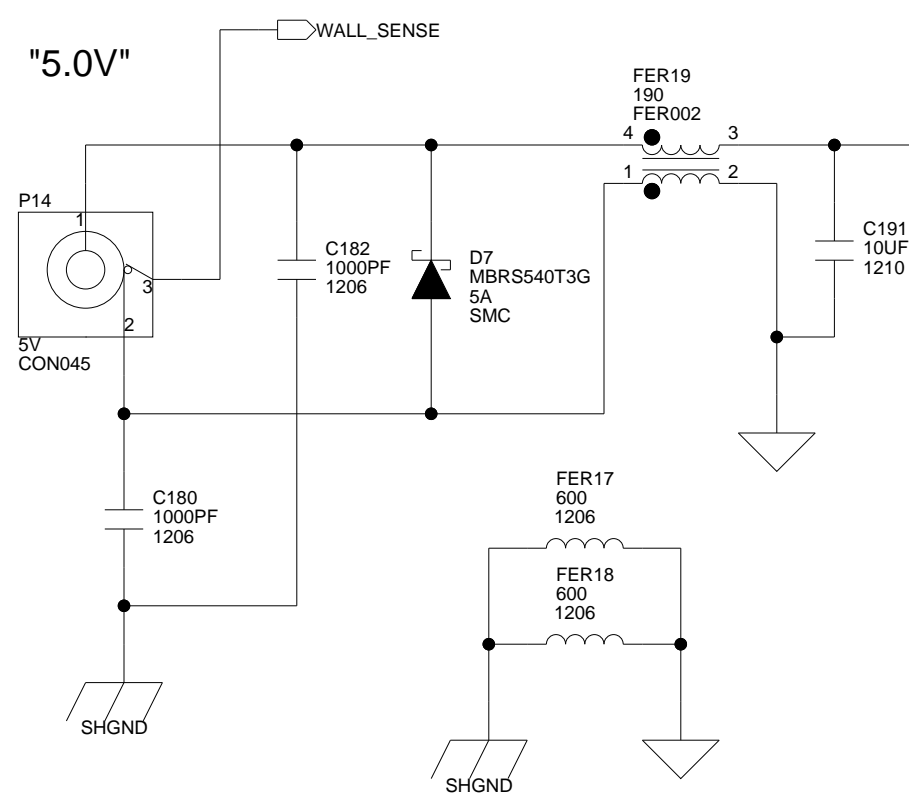
20 Cotton Road  
 Nashua, NH 03063  
 PH: 1-800-ANALOGD

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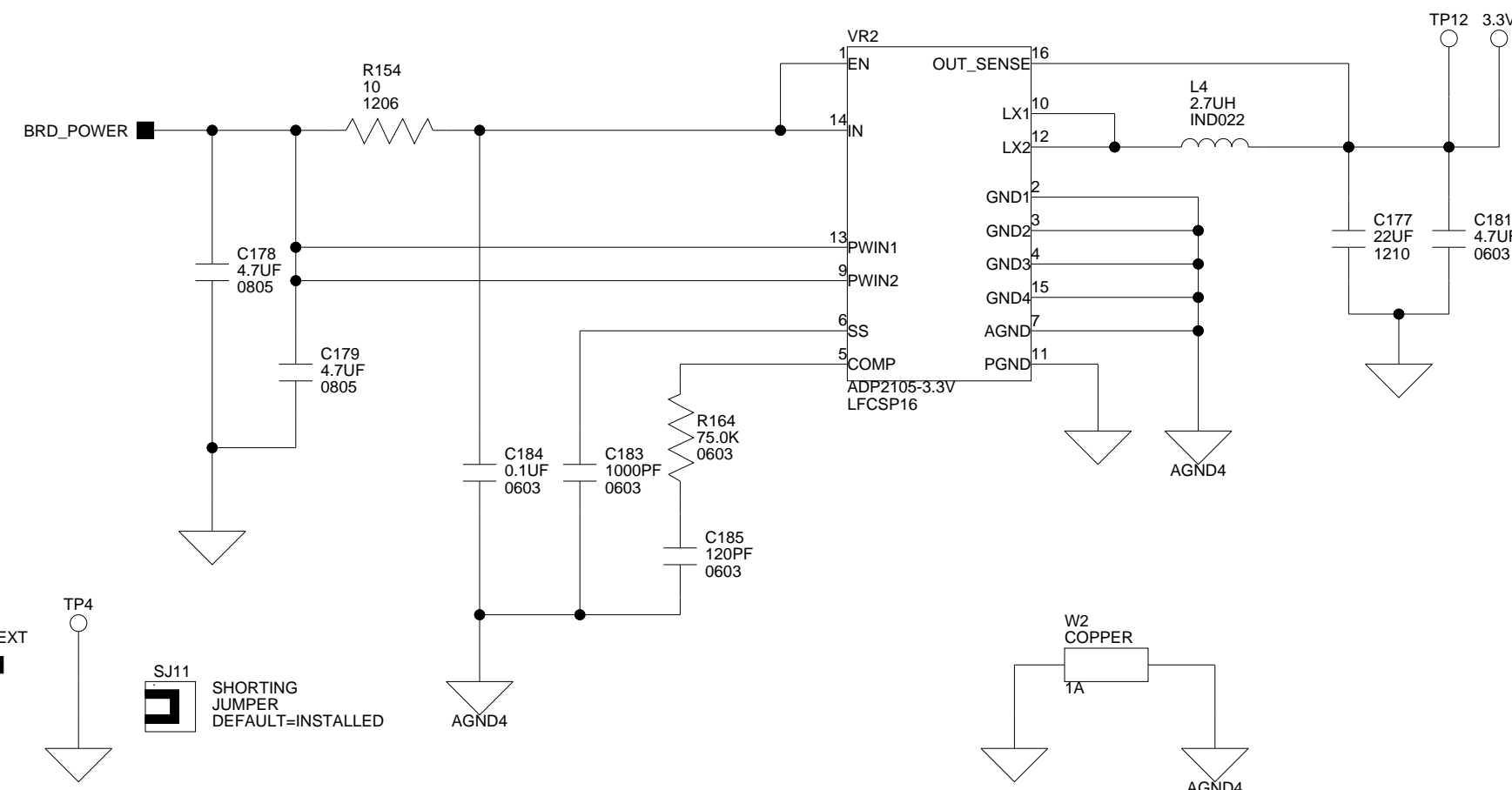
**Title** ADSP-526 EZ-BOARD  
**POWER, INPUT OR'ING, CHARGE, FUEL GAUGE**

<b>Size C</b>	<b>Board No.</b> A0212-2007	<b>Rev</b> 0.2A
<b>Date</b> 8-28-2008_16:17	<b>Sheet</b> 13 of 14	

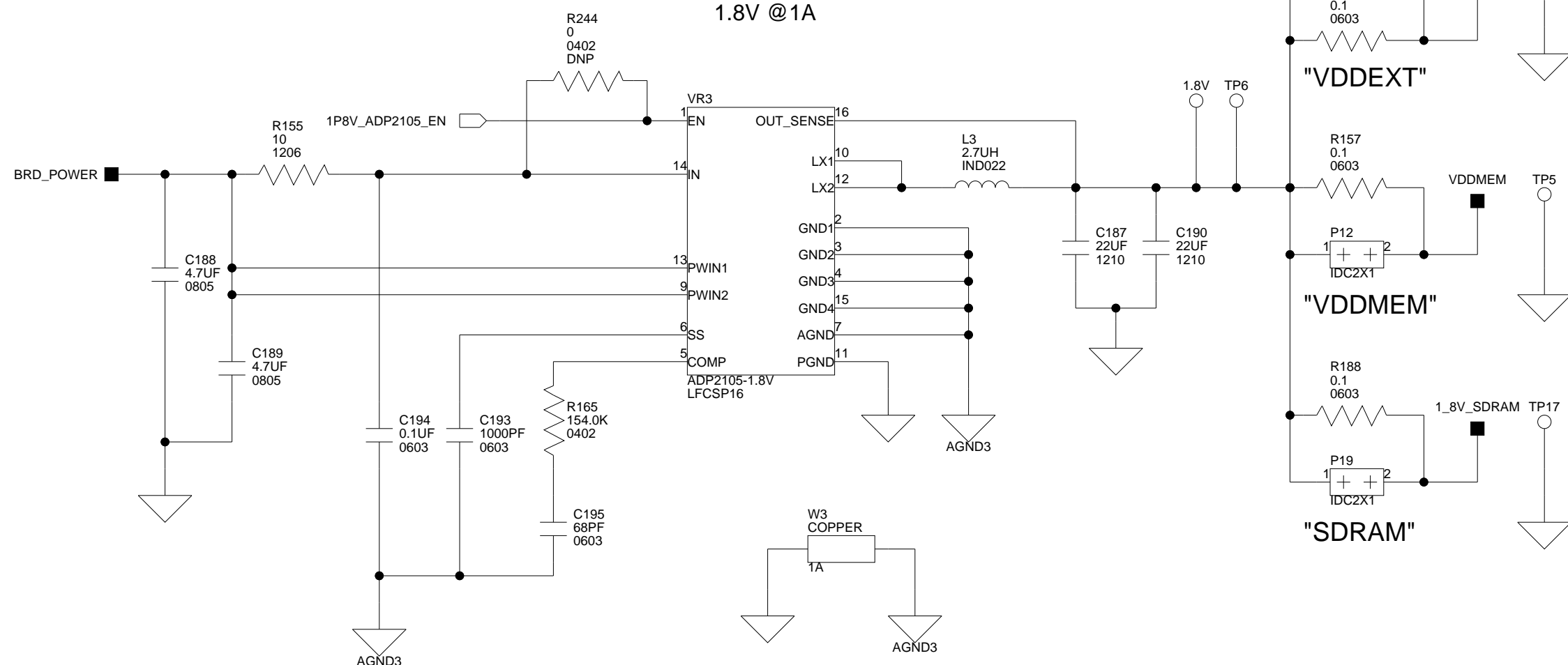
"5.0V"



3.3V @1A



1.8V @1A



"VDDEXT"

"VDDMEM"

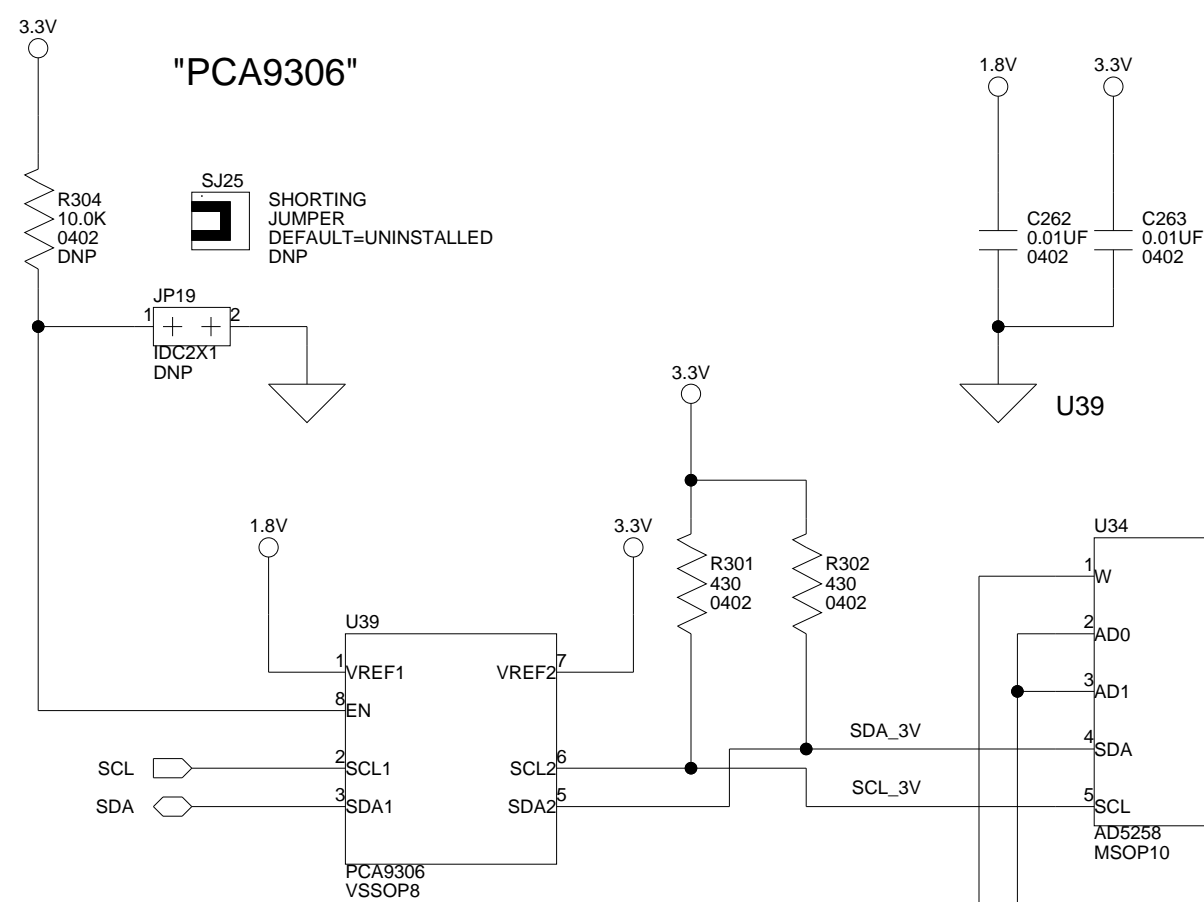
"SDRAM"

SJ11 SHORTING JUMPER DEFAULT=INSTALLED

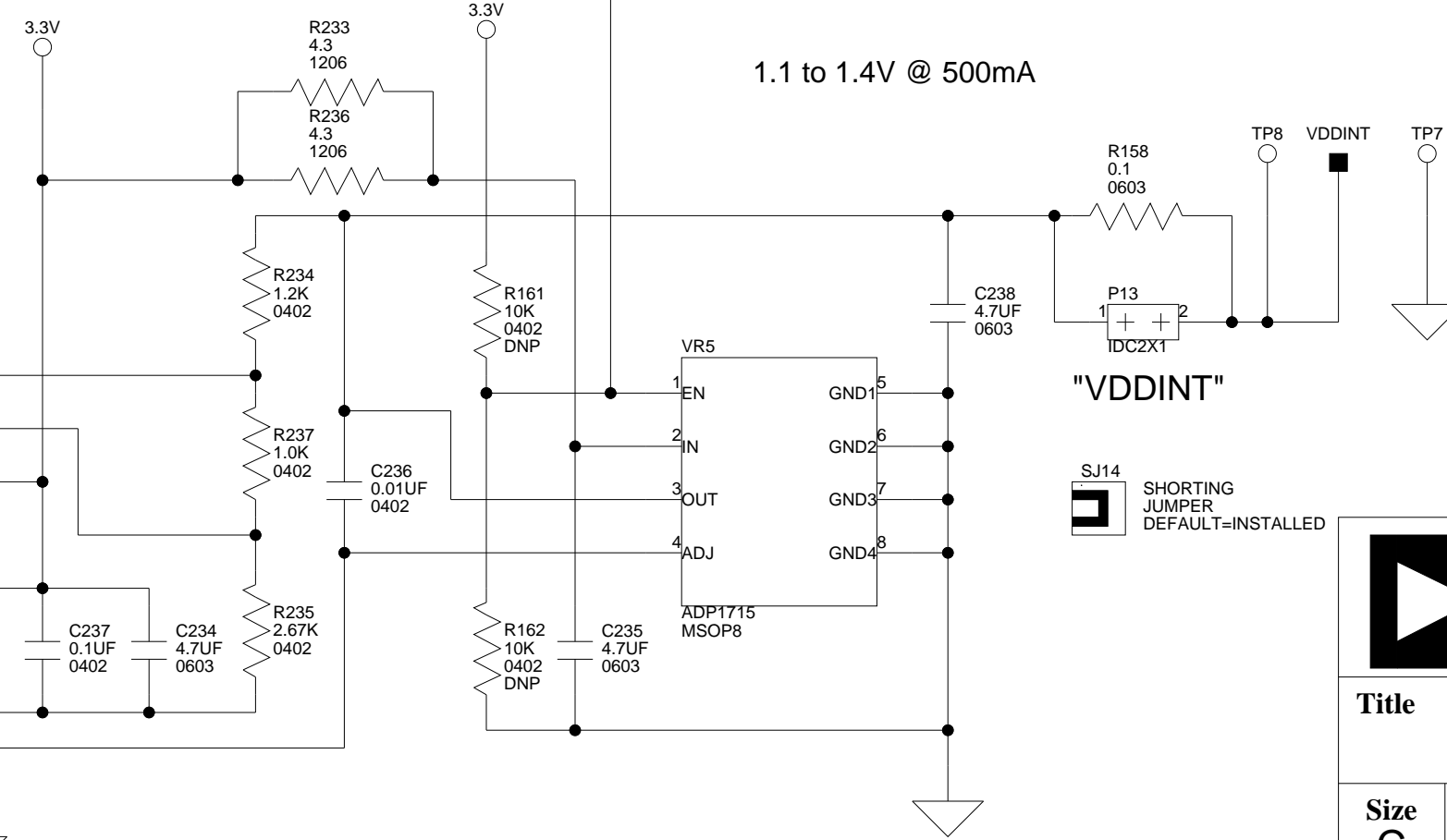
SJ12 SHORTING JUMPER DEFAULT=INSTALLED

SJ13 SHORTING JUMPER DEFAULT=INSTALLED

"PCA9306"



1.1 to 1.4V @ 500mA



"VDDINT"

SJ14 SHORTING JUMPER DEFAULT=INSTALLED

**ANALOG DEVICES** 20 Cotton Road  
Nashua, NH 03063  
PH: 1-800-ANALOGD

**Title** ADSP-526 EZ-BOARD  
POWER, VDDINT, VDDEXT, 3.3V

<b>Size C</b>	<b>Board No.</b> A0212-2007	<b>Rev</b> 0.2A
<b>Date</b> 8-28-2008_16:17	<b>Sheet</b> 14 of 14	



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