DENSITRON®
DISPLAYS

OLED DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**	
PRODUCT NUMBER	**DD-128128FC-6A**	
CUSTOMER APPROVAL		**Date**

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Bazile Peter	**Anthony Perkins**	**Rekha Mani**
Date: 17/03/10	Date: 17/03/10	Date: 17/03/10

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	05 August 09			First Issue	
B	04 Nov 09	10	3.3	PIN 17 and 18 corrected	
C	17 Mar 10	8 9 10	3.2 3.3 3.3	Note1 and 2 : VCC=13V R/W# : When serial mode is selected, this pin must be connected to VSS 17: BS0 18: BS1	

1 MAIN FEATURES

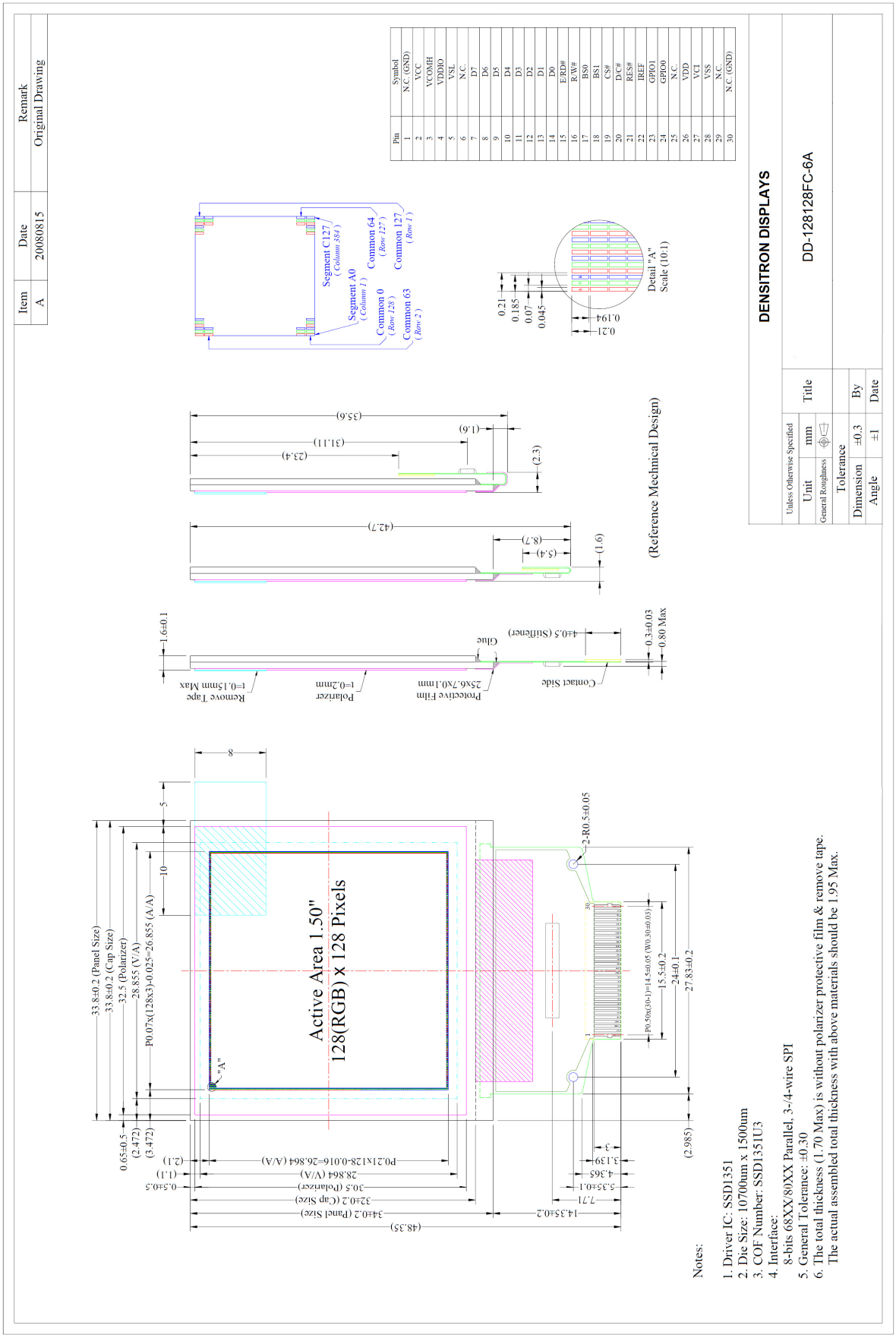
ITEM	CONTENTS
Display Format	128 (RGB) x 128 Dots
Overall Dimensions	33.8 x 34.00 x 1.60 mm
Colour	262,144 Colour
Active Area	26.855 x 26.864 mm
Viewing Area	28.855 x 28.864 mm
Display Mode	Passive Matrix (1.50”)
Driving Method	1/128 duty
Driver IC	SSD1351
Operating temperature	-30 ~ +70
Storage temperature	-40 ~ +80

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	128 (RGB) x 128	Dots
Overall Dimensions	33.8 x 34.00 x 1.60	mm
Viewing Area	28.855 x 28.864	mm
Active Area	26.855 x 26.864	mm
Dot Size	0.045 x RGB x 0.194	mm
Dot Pitch	0.07 x RGB x 0.21	mm
Weight	3.75	g
IC Controller/Driver	SSD1351 (COF)	

2.2 MECHANICAL DRAWING



3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Min	Max	Unit	Note
Supply Voltage for Operation	V_{CI}	-0.3	4	V	Note 1, 2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	
Supply Voltage for I/O Pins	V_{DDIO}	-0.5	V_{CI}	V	
Supply Voltage for Display	V_{CC}	-0.5	16	V	
Operating Current for V_{CC}	I_{CC}	-	41.8	mA	
Operating Temperature	Top	-30	70	°C	
Storage Temperature	Tstg	-40	80	°C	
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of "VSS=0V".

Note 2: When this module is used beyond above absolute maximum ratings, permanent damage to the module may occur. Also for normal operations it's desirable to use this module under the conditions according to Section 3.2 "Electrical Characteristics" and section 4 "optical characteristic. If this module is used beyond these conditions the module may malfunction and the reliability could deteriorate.

3.2 ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}	Ta = 25°C	2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}	Ta = 25°C	2.4	2.5	2.6	V
Supply Voltage for I/O pins	V_{DDIO}	Ta = 25°C	1.65	1.8	V_{CI}	V
Supply Voltage for Display	V_{CC}	Note 3	12.5	13	13.5	V
High Level Input	V_{IH}		0.8xV_{DDIO}	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	0.2xV_{DDIO}	V
High Level Output	V_{OH}	Iout=100µA,3.3MH	0.9xV_{DDIO}	-	V_{DDIO}	V
Low Level Output	V_{OL}	Iout=100µA,3.3MH	0	-	0.1xV_{DDIO}	V
Operating Current for V_{CI}	I_{CI}			240	300	µA
Operating Current for V_{CC}	I_{CC}	Note 1		23.2	29.0	mA
		Note 2		33.4	41.8	mA
Sleep Mode Current for V_{CI}	$I_{CI, SLEEP}$			1	5	µA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$			1	5	µA

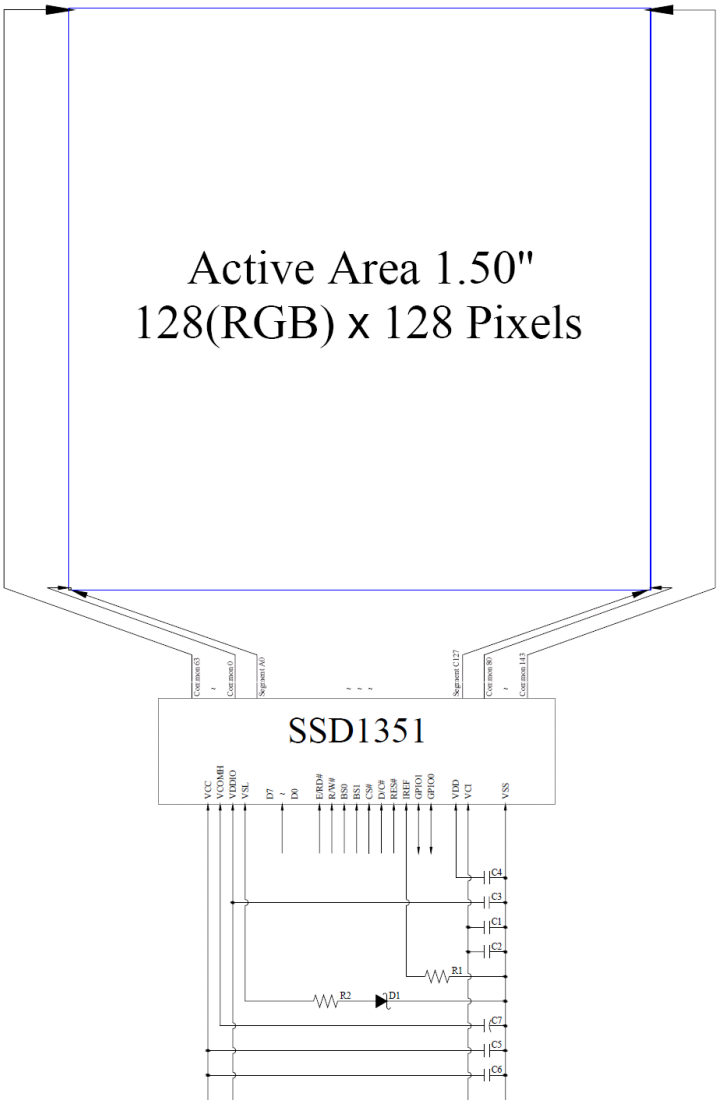
Note 1 V_{CI}= 2.8V, V_{CC} = 13V, 50% Display area turned on.
Note 2 V_{CI} = 2.8V, V_{CC} = 13V, 100% Display area turned on
Note 3 Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

3.3 INTERFACE PIN ASSIGNMENT

No.	Symbol	I/O	Function
1	N.C. (GND)	-	Reserved Pin (Supporting Pin) The supporting pin can reduce the influence from stress on the function pins. This pin must be connected to external ground.
2	VCC	P	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. It must be connected to external source.
3	VCOMH	P	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
4.	VDDIO	P	Power Supply for I/O Pin This pin is a power supply pin of I/O buffer. It should be connected to VCI or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) are pulled high, they should be connected to VDDIO.
5	VSL	P	Voltage Output Low Level for SEG Signal This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.
6	N.C.	-	Reserved Pin The N.C. pins between function pins are reserved for compatible and flexible design.
7~14	D7~D0	I/O	Host Data Input/output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2.
15	E/RD#	I	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.
16	R/W#	I	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>17
18</td><td>BS0
BS1</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>BS0</td><td>BS1</td></tr>
<tr><td>3-wire SPI</td><td>1</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td></tr>
<tr><td>68XX-parallel (8-/16-/18-bit)</td><td>1</td><td>1</td></tr>
<tr><td>80XX-parallel (8-/16-/18-bit)</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>19</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>20</td><td>D/C#</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data.
When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
When 3-wire serial mode is selected, this pin must be connected to VSS</td></tr>
<tr><td>21</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input.. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>22</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 12.5uA.</td></tr>
<tr><td>23</td><td>GPIO1</td><td rowspan="2">I/O</td><td rowspan="2">General Purpose Input/Output
These pins could be left open individually or have signal inputted/outputted. They are able to use as the external DC/DC converter circuit enabled/disabled control or other applications.</td></tr>
<tr><td>24</td><td>GPIO0</td></tr>
<tr><td>25</td><td>N.C.</td><td>-</td><td>Reserved Pin
The N.C. pins between function pins are reserved for compatible and flexible design.</td></tr>
<tr><td>26</td><td>VDD</td><td>P</td><td>Power Supply for Core Logic Circuit
This is a voltage supply pin which is regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.</td></tr>
<tr><td>27</td><td>VCI</td><td>P</td><td>Power Supply for Operation
This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.</td></tr>
<tr><td>28</td><td>VSS</td><td>P</td><td>Ground of OEL System
This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analogue circuits. It must be connected to external ground.</td></tr>
<tr><td>29</td><td>N.C.</td><td>-</td><td>Reserved Pin
The N.C. pins between function pins are reserved for compatible and flexible design.</td></tr>
<tr><td>30</td><td>N.C. (GND)</td><td>-</td><td>Reserved Pin (Supporting Pin)
The supporting pin can reduce the influence from stress on the function pins. This pin must be connected to external ground.</td></tr>
</table>

3.4 BLOCK DIAGRAM



MCU Interface Selection: BS0 and BS1
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, CS#, D/C#, and RES#

C1, C5: 0.1µF
C2: 4.7µF
C6: 10µF
C3, C4: 1µF
C7: 4.7uF / 25V Tantalum Capacitor
R1: 560kΩ, R1 = (Voltage at IREF – VSS) / IREF
R2: 50Ω, 1/4W
D1: <=1.4V, 0.5W

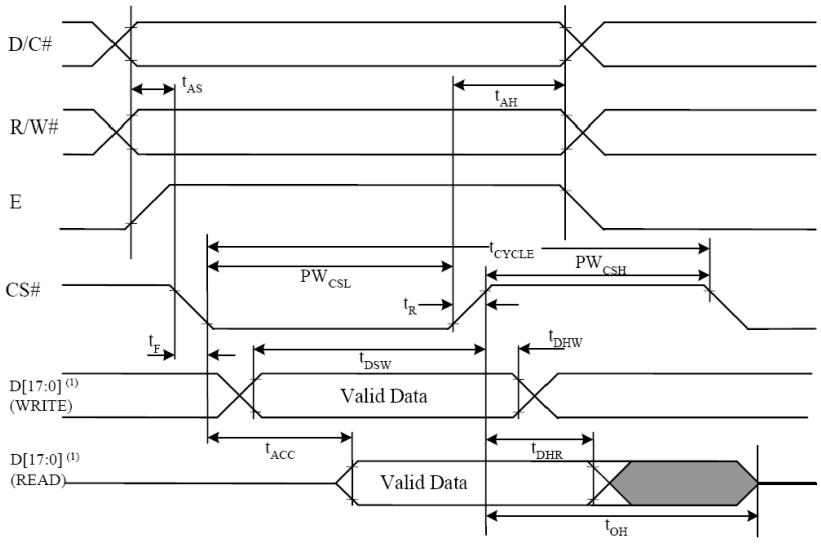
3.5 TIMING CHARACTERISTICS

3.5.1 AC CHARACTERISTICS

3.5.2 68XX-Series MPU Parallel Interface Timing Characteristics

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	300	-	ns
Address Setup Time	t_{AS}	10	-	ns
Address Hold Time	t_{AH}	0	-	ns
Write Data Setup Time	t_{DSW}	40	-	ns
Write Data Hold Time	t_{DHW}	7	-	ns
Read Data Hold Time	t_{DHR}	20	-	ns
Output Disable Time	t_{OH}	-	70	ns
Access Time	t_{ACC}	-	140	ns
Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	PW_{CSL}	120 60	-	ns
Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	PW_{CSH}	60 60	-	ns
Rise Time	t_R	-	15	ns
Fall Time	t_F	-	15	ns

(V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

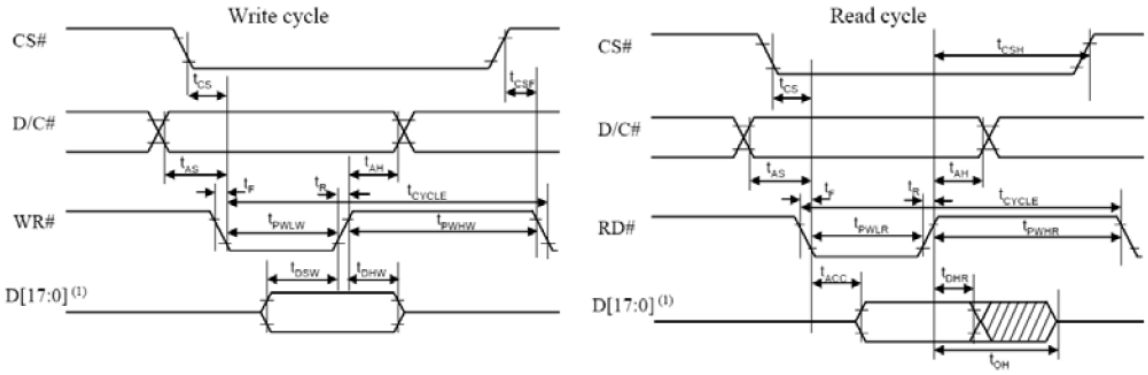


When 8-bit Used: D[7:0] Instead

3.5.3 8080-Series MPU Parallel Interface Timing Characteristics

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	300	-	ns
Address Setup Time	t_{AS}	10	-	ns
Address Hold Time	t_{AH}	0	-	ns
Write Data Setup Time	t_{DSW}	40	-	ns
Write Data Hold Time	t_{DHW}	7	-	ns
Read Data Hold Time	t_{DHR}	20	-	ns
Output Disable Time	t_{OH}	-	70	ns
Access Time	t_{ACC}	-	140	ns
Read Low Time	t_{PWLR}	150	-	ns
Write Low Time	t_{PWLW}	60	-	ns
Read High Time	t_{PWHR}	60	-	ns
Write High Time	t_{PWHW}	60	-	ns
Chip Select Setup Time	t_{CS}	0	-	ns
Chip Select Hold Time to Read Signal	t_{CSH}	0	-	ns
Chip Select Hold Time	t_{CSF}	20	-	ns
Rise Time	t_R	-	15	ns
Fall Time	t_F	-	15	ns

(V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

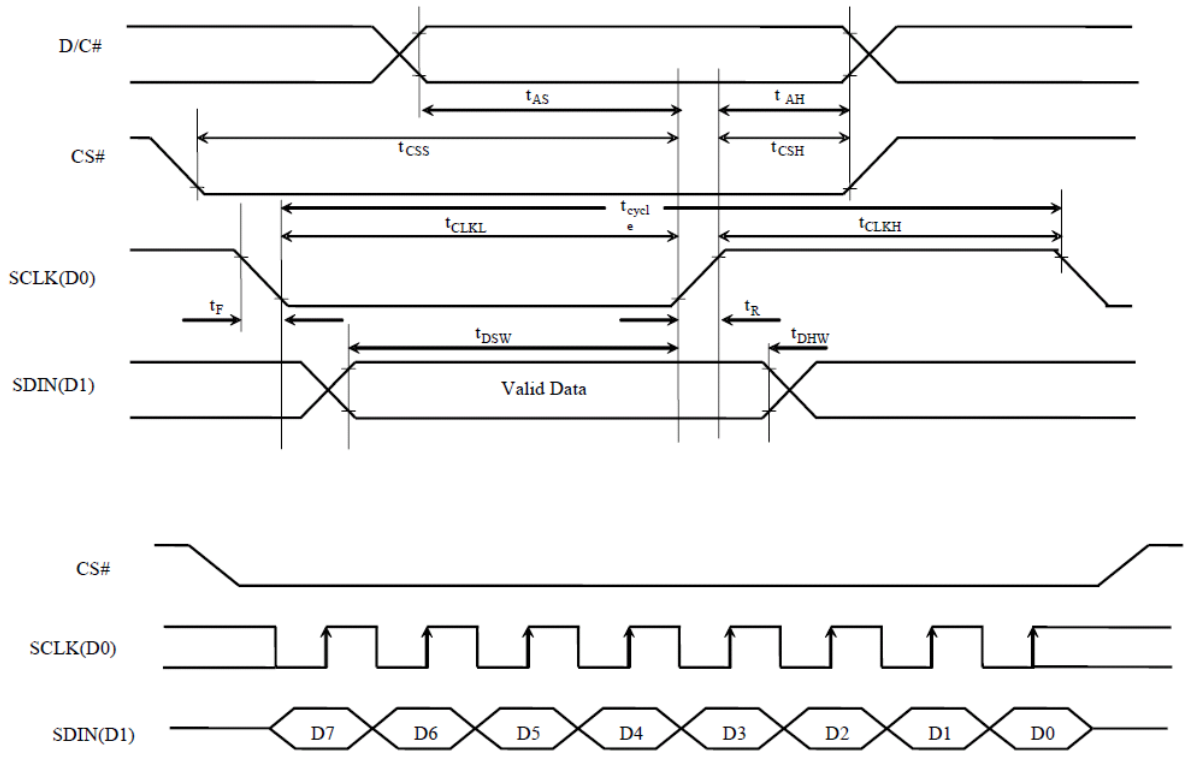


* When 8-bit Used: D[7:0] Instead

3.5.4 Serial Interface Timing Characteristics (4-wire SPI)

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	50	-	ns
Address Setup Time	t_{AS}	15	-	ns
Address Hold Time	t_{AH}	15	-	ns
Chip Select Setup Time	t_{CSS}	20	-	ns
Chip Select Hold Time	t_{CSH}	10	-	ns
Write Data Setup Time	t_{DSW}	15	-	ns
Write Data Hold Time	t_{DHW}	15	-	ns
Clock Low Time	t_{CLKL}	20	-	ns
Clock High Time	t_{CLKH}	20		ns
Rise Time	t_R	-	15	ns
Fall Time	t_F	-	15	ns

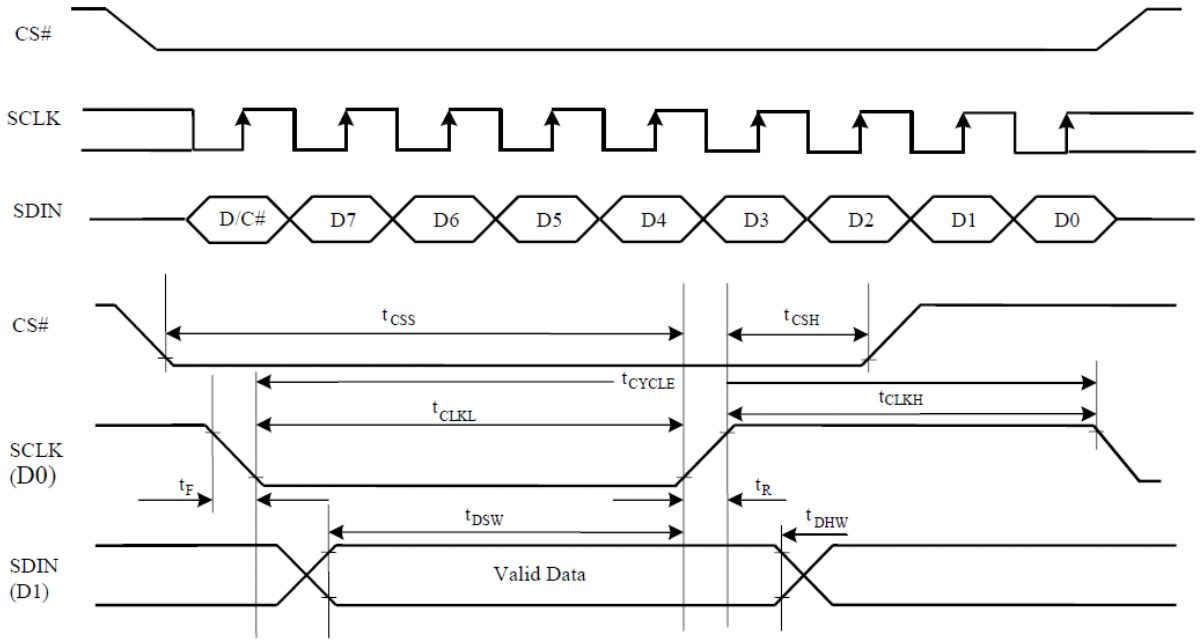
(VDD – VSS = 2.4V to 2.6V, VDDIO = 1.6V, VCI = 2.8V, Ta = 25°C)



3.5.5 Serial Interface Timing Characteristics (3-wire SPI)

Characteristics	Symbol	Min	Max	Unit
Clock Cycle Time	t_{cycle}	50	-	ns
Chip Select Setup Time	t_{CSS}	20	-	ns
Chip Select Hold Time	t_{CSH}	10	-	ns
Write Data Setup Time	t_{DSW}	15	-	ns
Write Data Hold Time	t_{DHW}	15	-	ns
Clock Low Time	t_{CLKL}	20	-	ns
Clock High Time	t_{CLKH}	20		ns
Rise Time	t_R	-	15	ns
Fall Time	t_F	-	15	ns

(VDD – VSS = 2.4V to 2.6V, VDDIO = 1.6V, VCI = 2.8V, Ta = 25°C)



4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness(White)	L_{br}	With Polarizer (Note 3)	70	90	-	cd/m^2
C.I.E.(White)	(X)	With Polarizer	0.26	0.30	0.34	-
	(Y)		0.29	0.33	0.37	
C.I.E.(Red)	(X)	With Polarizer	0.60	0.64	0.68	-
	(Y)		0.30	0.34	0.38	
C.I.E.(Green)	(X)	With Polarizer	0.27	0.31	0.35	-
	(Y)		0.58	0.62	0.66	
C.I.E.(Blue)	(X)	With Polarizer	0.10	0.14	0.18	-
	(Y)		0.12	0.16	0.20	
Dark Room Contrast	CR		-	>2000:1	-	-
Viewing Angle			>160	-	-	degree

Optical measurement taken at V_{CI} = 2.8V, V_{CC} = 13V
Software configuration follows Section 5.4 Initialization.

Note 3 Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

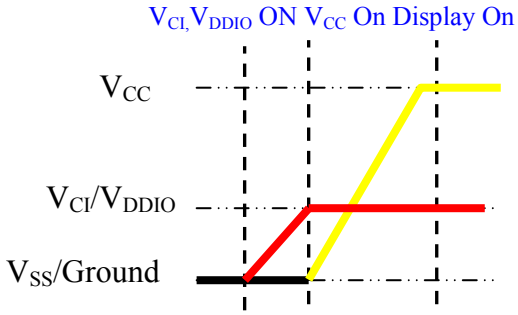
Please refer to the Technical Manual for the SSD1351

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

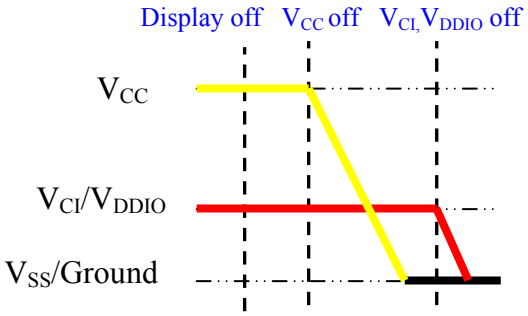
5.2.1 POWER UP SEQUENCE

1. Power up V_{CI} & V_{DDIO}
2. Send Display off command
3. Initialization 4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



5.2.2 POWER DOWN SEQUENCE

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{CI} & V_{DDIO}



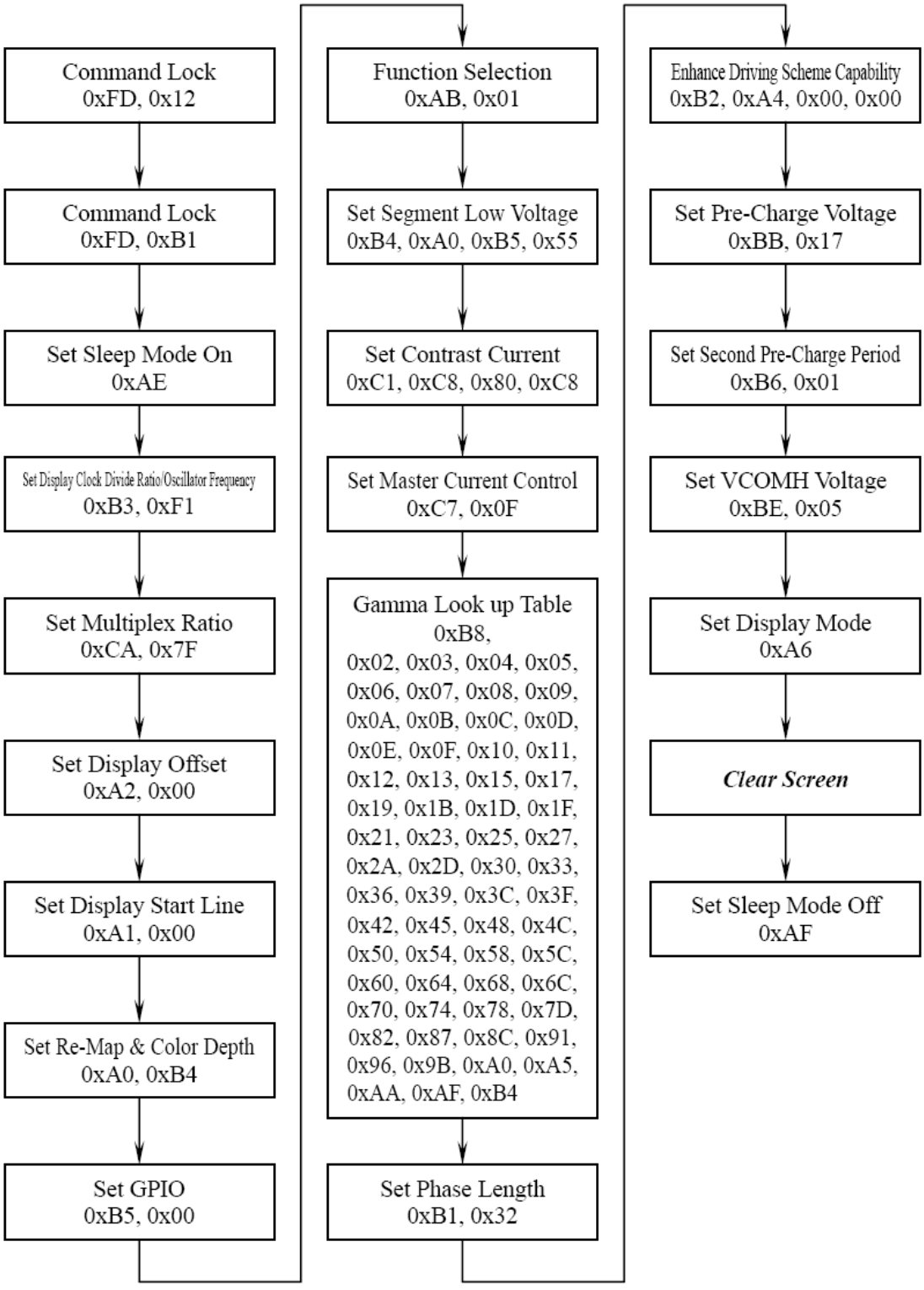
5.3 RESET CIRCUIT

When RES# input is low, the chip is initialized with the following status:

1. Display is off
2. 128(RGB)x128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Command A2h, B1h, B3h, BBh, BEh are locked by command FDh

5.4 ACTUAL APPLICATION EXAMPLE

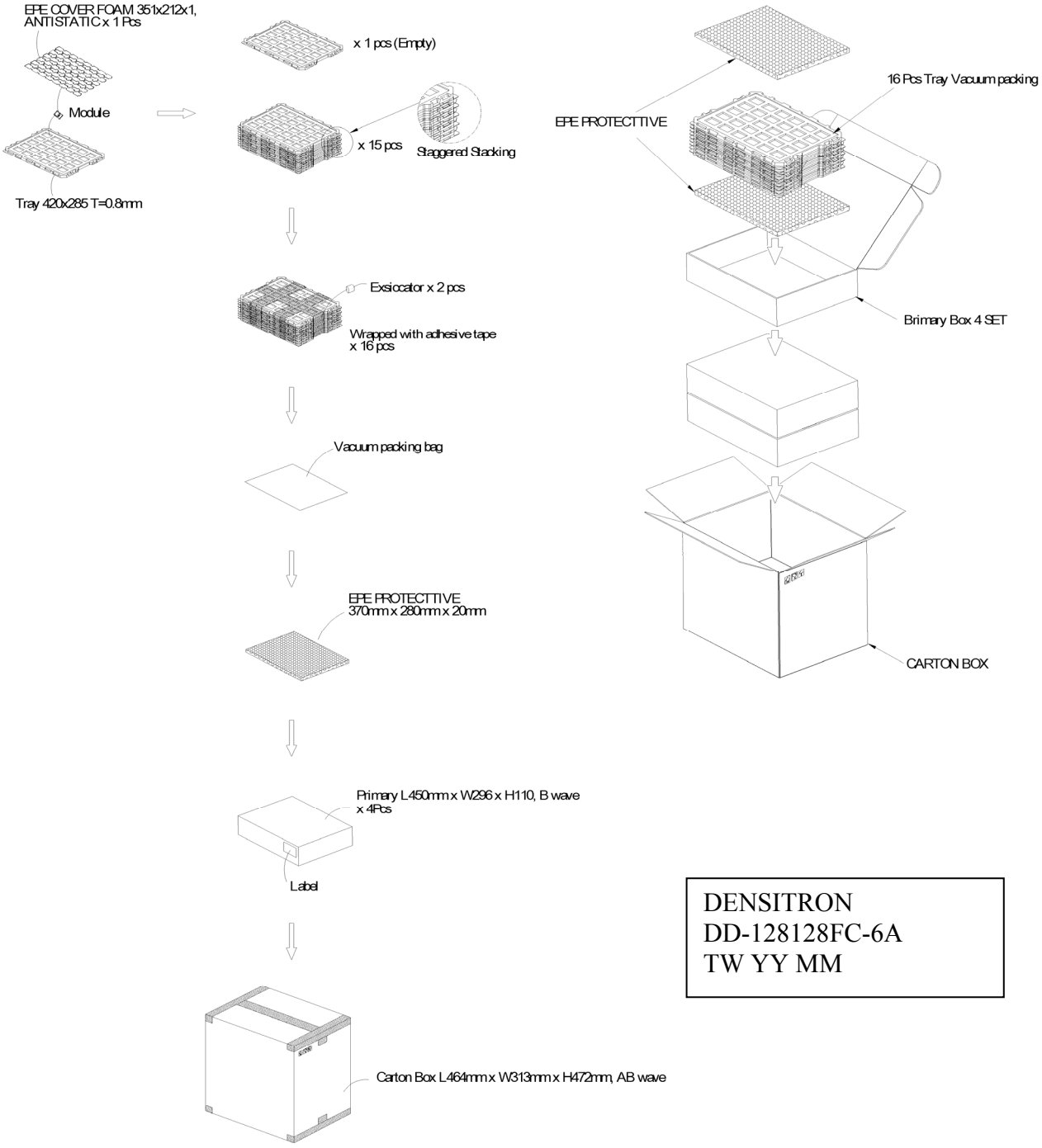
Command usage and explanation of an actual example



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

6 PACKAGING AND LABELLING SPECIFICATION

6.1 LABELLING & MARKING



7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

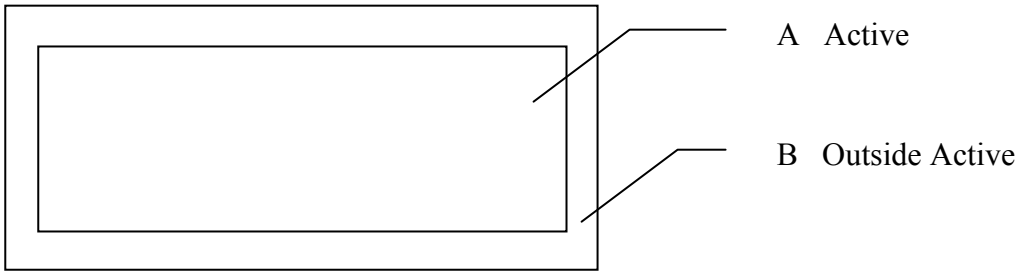
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assemblies standard

7.2.2 Zone definition



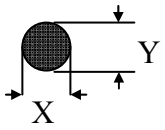
7.2.3 Visual inspection

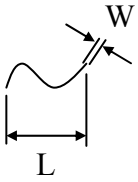
Test and measurement to be conducted under following conditions□

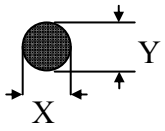
Temperature:	23±5℃
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≧30cm
Distance between the Panel & the lamp:	≧50cm

7.2.4 Standard of appearance inspection

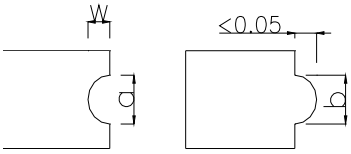
Units: mm

<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td rowspan="2">Packing & Label</td><td>Outside & inside package | Presence of product no., lot no., quantity</td></tr>
<tr><td>Critical</td><td>Product must not be mixed with others and quantity must not be different from that indicated on the label</td></tr>
<tr><td>Major</td><td>Dimension</td><td>Product dimensions must be according to specification and drawing</td></tr>
<tr><td>Major</td><td>Electrical</td><td>Product electrical characteristics must be according to specification</td></tr>
<tr><td>Critical</td><td>OLED Display</td><td>Missing lines, short circuits or wrong patterns on OLED display are not allowed</td></tr>
<tr><td>Minor</td><td>Black spot, white spot, dust</td><td>Round type: as per following drawing
∅ = (X+Y)/2
 

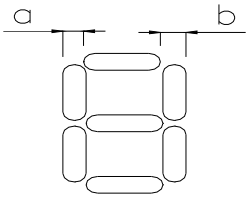
<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.1</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>0.1<∅<0.2</td><td>3</td></tr><tr><td>0.2<∅<0.25</td><td>1</td></tr><tr><td>0.25<∅</td><td>0</td></tr></table>
Line type: as per following drawing
 

<table><tr><th colspan="4">Acceptable quantity</th></tr><tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr><tr><td>- -</td><td>W≤0.05</td><td>Any number</td><td rowspan="3">Any number</td></tr><tr><td>L≤2.0</td><td>W≤0.1</td><td>3</td></tr><tr><td>L>2.0</td><td></td><td>0</td></tr></table>
Total acceptable quantity: 3</td></tr>
<tr><td>Minor</td><td>Polariser scratch</td><td>Scratch on protective film is permitted
Scratch on polariser: same as No. 1</td></tr>
<tr><td>Minor</td><td>Polariser bubble</td><td>∅ = (X+Y)/2
 

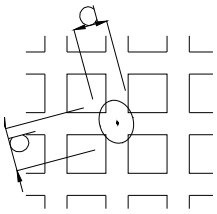
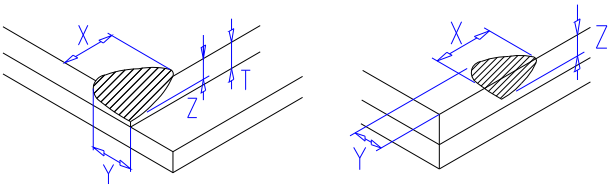
<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.5</td><td>Any number</td><td rowspan="2">Any number</td></tr><tr><td>∅>0.5</td><td>0</td></tr></table></td></tr>
</table>

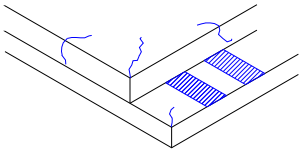
<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Segment deformation</td><td>
1b. Pin hole on dot matrix display


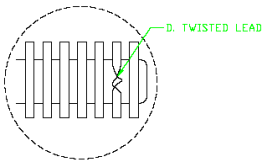
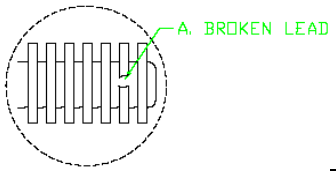
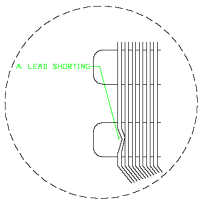
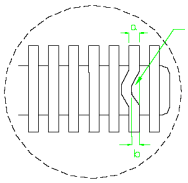
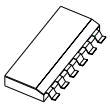
<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>a,b<0.1</td><td>Any number</td></tr>
<tr><td>(a+b)/2≤0.1</td><td>Any number</td></tr>
<tr><td>0.5<∅<1.0</td><td>3</td></tr>
</table>
Total acceptable quantity: 7

2. Segments / dots with different width


<table>
<tr><td colspan="2">Acceptable</td></tr>
<tr><td>a≥b</td><td>a/b≤4/3</td></tr>
<tr><td>a<b</td><td>a/b>4/3</td></tr>
</table>

3. Alignment layer defect
∅ = (a+b)/2

<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>∅≤0.4</td><td>Any number</td></tr>
<tr><td>0.4<∅≤1.0</td><td>5</td></tr>
<tr><td>1.0<∅≤1.5</td><td>3</td></tr>
<tr><td>1.5<∅≤2.0</td><td>2</td></tr>
</table>
Total acceptable quantity: 7
</td></tr>
<tr><td>Minor</td><td>Panel Chipping</td><td>
X ≤ 1/6 Panel length
Y ≤ 1
Z ≤ T


</td></tr>
<tr><td>Minor</td><td>Panel Cracking</td><td>
Cracks not allowed

</td></tr>
<tr><td>Minor</td><td>Cupper exposed (pin or film)</td><td>Not allowed if visible by eye inspection</td></tr>
<tr><td>Minor</td><td>Film or Trace Damage</td><td>Not allowed if affect electrical function</td></tr>
</table>

<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Contact
Lead Twist</td><td>Not allowed
 
</td></tr>
<tr><td>Minor</td><td>Contact
Lead
Broken</td><td>Not allowed
 
</td></tr>
<tr><td rowspan="2">Minor</td><td rowspan="2">Contact
Lead Bent</td><td>Not allowed if
bent lead causes
short circuit
 
</td></tr>
<tr><td>Not allowed if bent lead
extends horizontally
more than 50%
of its width
  </td></tr>
<tr><td>Minor</td><td>Colour
uniformity</td><td>Level of sample for approval set as limit sample</td></tr>
<tr><td>Major</td><td rowspan="4">PCB
  </td><td>No unmelted solder paste should be present on PCB</td></tr>
<tr><td>Critical</td><td>Cold solder joints, missing solder connections, or oxidation are not allowed</td></tr>
<tr><td>Minor</td><td>No residue or solder balls on PCB are allowed</td></tr>
<tr><td>Critical</td><td>Short circuits on components are not allowed</td></tr>
<tr><td>Minor</td><td>Tray
particles</td><td>
<table>
<tr><th></th><th>Size</th><th>Quantity</th></tr>
<tr><td rowspan="2">On tray</td><td>∅<0.2</td><td>Any number</td></tr>
<tr><td>∅>0.25</td><td>4</td></tr>
<tr><td rowspan="2">On display</td><td>∅≥0.25</td><td>2</td></tr>
<tr><td>L = 3</td><td>1</td></tr>
</table>
</td></tr>
</table>

7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70°C±2, 240 hours	No abnormalities in function and appearance
Low Temperature Operation	-30°C±2, 240 hours	No abnormalities in function and appearance
High Temperature Storage	80°C±2, 240 hours	No abnormalities in function and appearance
Low Temperature Storage	-40°C±2, 240 hours	No abnormalities in function and appearance
High Temperature & High Humidity Storage(Operation)	60°C±2, 90%RH, 120 hours	No abnormalities in function and appearance
Thermal Shock	24 cycle of -40°C 1 Hour, R.T. 5 min, 85°C 1 Hour	No abnormalities in function and appearance

- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 °C□55±15% RH

8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration more than 10,000 hours under ordinary operating conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight. Storage Life time is 20,000 hr under room temperature (25±10 °C), normal humidity (45±20% RH)
2	End of lifetime is specified as 50% of initial brightness.

8.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

9 PRECAUTIONS

9.1 Handling

Safety
If the panel breaks, be careful not to get the organic substance in your mouth or in your eyes.
If the organic substance touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design
Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.
Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during OLED cleaning
Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.
Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge
As the display uses C-MOS LSI drivers, connect any unused input terminal to V_{DD} or V_{SS}. Do not input any signals before power is turned on.
Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging
Displays use OLED elements, and must be treated as such. Avoid strong shock and drop from a height.
To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation
It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.

Other Precautions
When a display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored.
Also, there will be no problem in the reliability of the module.

Storage
Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH.
Store the display in a clean environment, free from dust, organic solvents and corrosive gases.
Do not crash, shake or jolt the display (including accessories).

9.2 STORAGE

When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Factory.)
At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

9.3 DESIGNING

The absolute maximum ratings are the ratings which cannot be exceeded for
OEL display module, and if these values are exceeded, panel damage may be happen.

To prevent occurrence of malfunctioning by noise: pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.

We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VCI). (Recommend value: 0.5A)

Pay sufficient attention to avoid occurrence of mutual noise interference with the neighbouring devices.

As for EMI, take necessary measures on the equipment side basically.

When fastening the OEL display module, fasten the external plastic housing section.

If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.

The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1351
* Connection (contact) to any other potential than the above may lead to rupture of the IC.

9.4 Disposing

Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

9.5 Other

When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
* Pins and electrodes
* Pattern layouts such as the COF

With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
* Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
* Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.

Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.