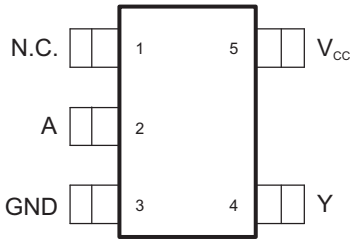
# LOW-POWER SINGLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

**Check for Samples: SN74AUP1G07**

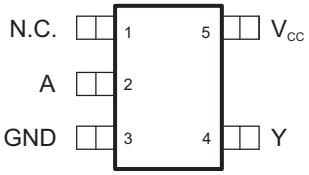
## FEATURES

- **Available in the Texas Instruments NanoStar™ Package**
- **Low Static-Power Consumption ($I_{CC}$ = 0.9 μA Maximum)**
- **Low Dynamic-Power Consumption ($C_{pd}$ = 1 pF Typical at 3.3 V)**
- **Low Input Capacitance ($C_i$ = 1.5 pF Typical)**
- **Low Noise – Overshoot and Undershoot <10% of $V_{CC}$**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input ($V_{hys}$ = 250 mV Typ at 3.3 V)**
- **Wide Operating $V_{CC}$ Range of 0.8 V to 3.6 V**
- **Optimized for 3.3-V Operation**
- **3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **$t_{pd}$ = 3.3 ns Maximum at 3.3 V**
- **Suitable for Point-to-Point Applications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

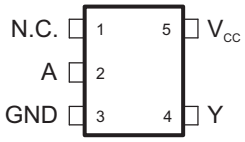
**DBV PACKAGE (TOP VIEW)**



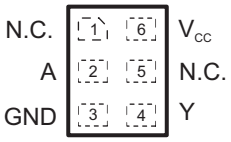

**DCK PACKAGE (TOP VIEW)**



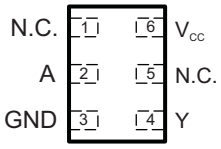

**DRL PACKAGE (TOP VIEW)**



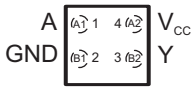

**DRY PACKAGE (TOP VIEW)**



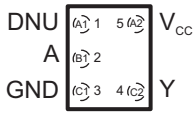

**DSF PACKAGE (TOP VIEW)**




**YFP PACKAGE (TOP VIEW)**




**YZP PACKAGE (TOP VIEW)**




N.C. – No internal connection.

DNU – Do not use

See mechanical drawings for dimensions.

## DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire $V_{CC}$ range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figure 1 and Figure 2).

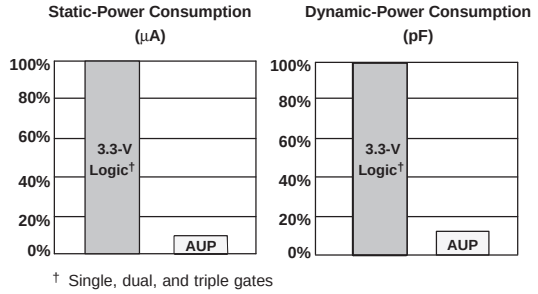



**Figure 1. AUP – The Lowest-Power Family**

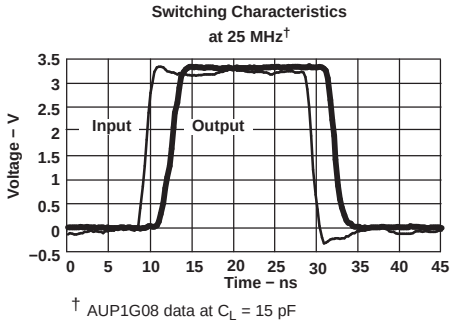



**Figure 2. Excellent Signal Integrity**

The output of this single buffer/driver is open drain, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION(1)

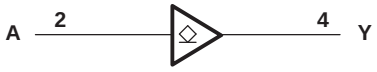
| $T_A$ | PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING(3) |
|---|---|---|---|---|
| –40°C to 85°C | NanoStar – WCSP (DSBGA) 0.23-mm large bump – YFP | Reel of 3000 | SN74AUP1G07YFPR | _ _ _ HV_ |
| | NanoStar – WCSP (DSBGA) 0.23-mm large bump – YZP (Pb-free) | Reel of 3000 | SN74AUP1G07YZPR | _ _ _ HV_ |
| | QFN – DRY | Reel of 5000 | SN74AUP1G07DRYR | HV |
| | uQFN – DSF | Reel of 5000 | SN74AUP1G07DSFR | HV |
| | SOT (SOT-23) – DBV | Reel of 3000 | SN74AUP1G07DBVR | H07_ |
| | SOT (SC-70) – DCK | Reel of 3000 | SN74AUP1G07DCKR | HV_ |
| | SOT (SOT-553) – DRL | Reel of 4000 | SN74AUP1G07DRLR | HV_ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

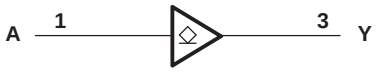
## FUNCTION TABLE

| INPUT A | OUTPUT Y |
|---|---|
| H | H |
| L | L |

## LOGIC DIAGRAM (POSITIVE LOGIC) (DBV, DCK, DRL, DRY, DRT, and YZP Packages)




## (YFP Package)



## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 4.6 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 4.6 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 4.6 | V |
| $V_O$ | Voltage range applied to any output in the high or low state(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±20 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $\theta_{JA}$ | Package thermal impedance(3) | DBV package | | 206 | °C/W |
| | | DCK package | | 252 | |
| | | DRL package | | 142 | |
| | | DSF package | | 300 | |
| | | DRY package | | 234 | |
| | | YFP/YZP package | | 132 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 0.8 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 0.8 V | $V_{CC}$ | | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | 0.65 × $V_{CC}$ | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.6 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 0.8 V | | 0 | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | | 0.35 × $V_{CC}$ | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.9 | |
| $V_I$ | Input voltage | | 0 | 3.6 | V |
| $V_O$ | Output voltage | | 0 | 3.6 | V |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 0.8 V | | 20 | μA |
| | | $V_{CC}$ = 1.1 V | | 1.1 | mA |
| | | $V_{CC}$ = 1.4 V | | 1.7 | |
| | | $V_{CC}$ = 1.65 V | | 1.9 | |
| | | $V_{CC}$ = 2.3 V | | 3.1 | |
| | | $V_{CC}$ = 3 V | | 4 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 0.8 V to 3.6 V | | 200 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $V_{OL}$ | | $I_{OL}$ = 20 μA | 0.8 V to 3.6 V | | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 1.1 mA | 1.1 V | | | 0.3 × $V_{CC}$ | | 0.3 × $V_{CC}$ | |
| | | $I_{OL}$ = 1.7 mA | 1.4 V | | | 0.31 | | 0.37 | |
| | | $I_{OL}$ = 1.9 mA | 1.65 V | | | 0.31 | | 0.35 | |
| | | $I_{OL}$ = 2.3 mA | 2.3 V | | | 0.31 | | 0.33 | |
| | | $I_{OL}$ = 3.1 mA | | | | 0.44 | | 0.45 | |
| | | $I_{OL}$ = 2.7 mA | 3 V | | | 0.31 | | 0.33 | |
| | | $I_{OL}$ = 4 mA | | | | 0.44 | | 0.45 | |
| $I_I$ | A input | $V_I$ = GND to 3.6 V | 0 V to 3.6 V | | | 0.1 | | 0.5 | μA |
| $I_{off}$ | | $V_I$ or $V_O$ = 0 V to 3.6 V | 0 V | | | 0.2 | | 0.6 | μA |
| $\Delta I_{off}$ | | $V_I$ or $V_O$ = 0 V to 3.6 V | 0 V to 0.2 V | | | 0.2 | | 0.6 | μA |
| $I_{CC}$ | | $V_I$ = GND or $V_{CC}$ to 3.6 V, $I_O$ = 0 | 0.8 V to 3.6 V | | | 0.5 | | 0.9 | μA |
| $\Delta I_{CC}$ | | $V_I$ = $V_{CC}$ – 0.6 V, $I_O$ = 0 | 3.3 V | | | 40 | | 50 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 0 V | | 1.5 | | | | pF |
| | | | 3.6 V | | 1.7 | | | | |
| $C_o$ | | $V_O$ = GND | 0 V | | 1.7 | | | | pF |

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L$ = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 0.8 V | | 12.2 | | | | ns |
| | | | 1.2 V ± 0.1 V | 3.4 | 5.1 | 7.5 | 1.5 | 14.7 | |
| | | | 1.5 V ± 0.1 V | 2.3 | 3.6 | 5.1 | 1.3 | 8.3 | |
| | | | 1.8 V ± 0.15 V | 2.4 | 3.1 | 4 | 1 | 6.3 | |
| | | | 2.5 V ± 0.2 V | 1.5 | 2.1 | 2.9 | 0.9 | 4.1 | |
| | | | 3.3 V ± 0.3 V | 1.8 | 2.2 | 2.8 | 1.1 | 3.3 | |

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L$ = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 0.8 V | | 15 | | | | ns |
| | | | 1.2 V ± 0.1 V | 4 | 6.2 | 9 | 2.4 | 16.2 | |
| | | | 1.5 V ± 0.1 V | 3.1 | 4.4 | 6.1 | 2 | 9.4 | |
| | | | 1.8 V ± 0.15 V | 3.3 | 3.9 | 4.8 | 1.6 | 7.1 | |
| | | | 2.5 V ± 0.2 V | 2.1 | 2.8 | 3.5 | 1.3 | 4.8 | |
| | | | 3.3 V ± 0.3 V | 2.3 | 3 | 4 | 1.4 | 4.5 | |

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L$ = 15 pF (unless otherwise noted) (see Figure 3 and 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 0.8 V | | 18.2 | | | | ns |
| | | | 1.2 V ± 0.1 V | 4.9 | 7.3 | 10.4 | 3.2 | 17.6 | |
| | | | 1.5 V ± 0.1 V | 3.8 | 5.2 | 6.8 | 2.6 | 10.2 | |
| | | | 1.8 V ± 0.15 V | 3.4 | 4.8 | 6.7 | 2.2 | 7.9 | |
| | | | 2.5 V ± 0.2 V | 2.4 | 3.4 | 4.5 | 1.9 | 5.3 | |
| | | | 3.3 V ± 0.3 V | 2.2 | 3.7 | 5.4 | 1.8 | 6.1 | |

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L$ = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

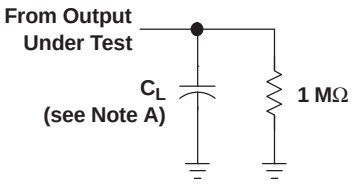
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 0.8 V | | 26.5 | | | | ns |
| | | | 1.2 V ± 0.1 V | 8.1 | 10.7 | 14.4 | 4.5 | 21.9 | |
| | | | 1.5 V ± 0.1 V | 6.5 | 7.7 | 9.4 | 3.8 | 13 | |
| | | | 1.8 V ± 0.15 V | 5.8 | 7.5 | 9.7 | 3.2 | 11 | |
| | | | 2.5 V ± 0.2 V | 4.5 | 5.4 | 6.7 | 3 | 7.1 | |
| | | | 3.3 V ± 0.3 V | 3.9 | 6.3 | 9.7 | 2.8 | 10.4 | |

## OPERATING CHARACTERISTICS

$T_A$ = 25°C

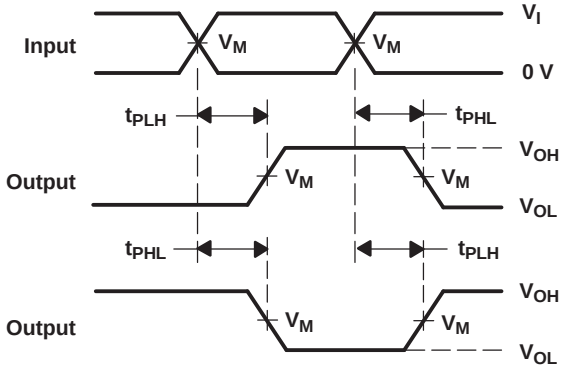
| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 0.8 V | 1 | pF |
| | | | 1.2 V ± 0.1 V | 1 | |
| | | | 1.5 V ± 0.1 V | 1 | |
| | | | 1.8 V ± 0.15 V | 1 | |
| | | | 2.5 V ± 0.2 V | 1 | |
| | | | 3.3 V ± 0.3 V | 1 | |

## PARAMETER MEASUREMENT INFORMATION
## (Propagation Delays, Setup and Hold Times, and Pulse Duration)

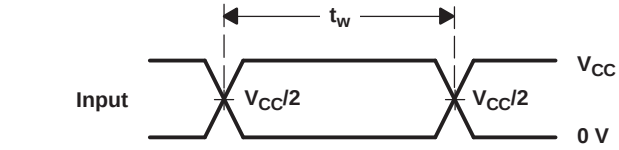



**LOAD CIRCUIT**

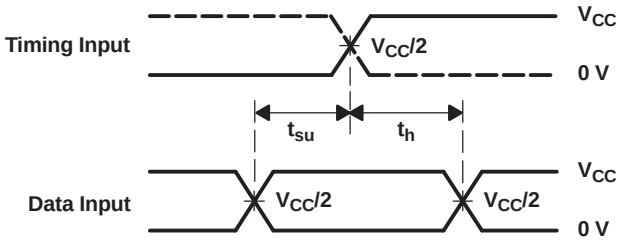
| | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V ± 0.1 V | $V_{CC}$ = 1.5 V ± 0.1 V | $V_{CC}$ = 1.8 V ± 0.15 V | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V |
|---|---|---|---|---|---|---|
| $C_L$ | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF |
| $V_M$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_I$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |




**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**




**VOLTAGE WAVEFORMS**
**PULSE DURATION**

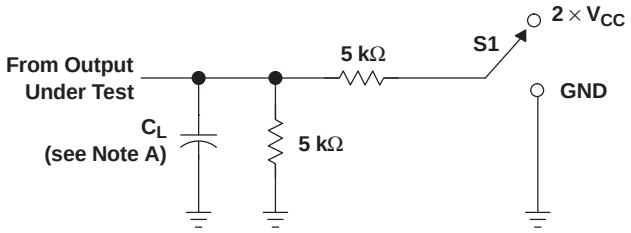



**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
E. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

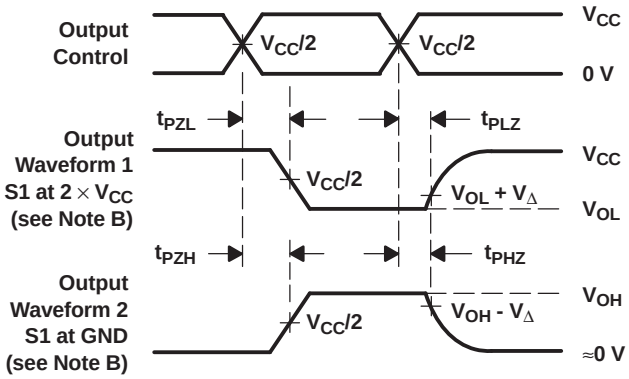
## PARAMETER MEASUREMENT INFORMATION
## (Enable and Disable Times)




LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | $2 \times V_{CC}$<br>GND |

| | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V ± 0.1 V | $V_{CC}$ = 1.5 V ± 0.1 V | $V_{CC}$ = 1.8 V ± 0.15 V | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V |
|---|---|---|---|---|---|---|
| $C_L$ | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF |
| $V_M$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_I$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| $V_\Delta$ | 0.1 V | 0.1 V | 0.1 V | 0.15 V | 0.15 V | 0.3 V |




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. All parameters and waveforms are not applicable to all devices.

**Figure 4. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1G07DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DBVTE4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DCKTE4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DRLR | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DRLRG4 | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07DSFR | ACTIVE | SON | DSF | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AUP1G07YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1G07YZPR | ACTIVE | DSBGA | YZP | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |

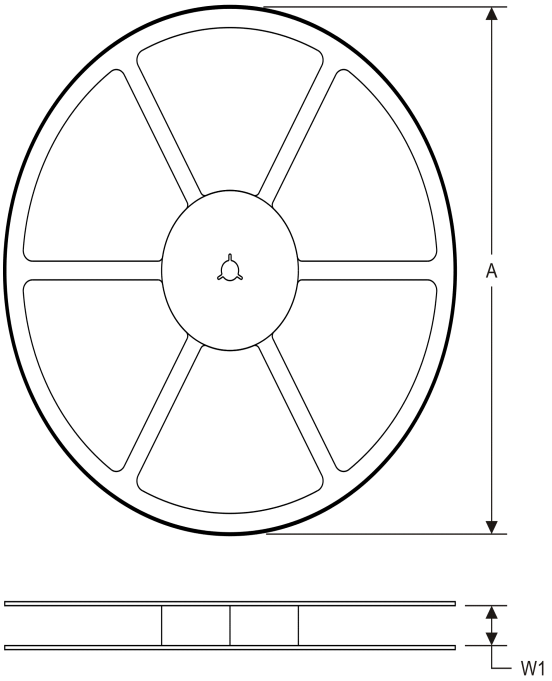
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

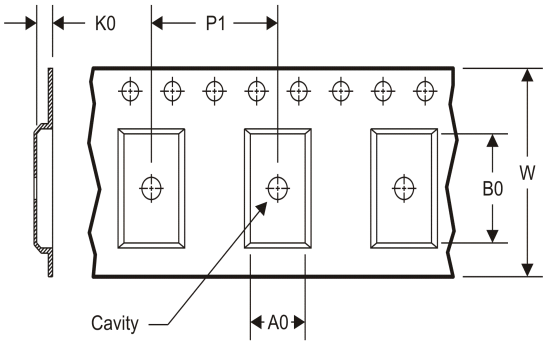
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



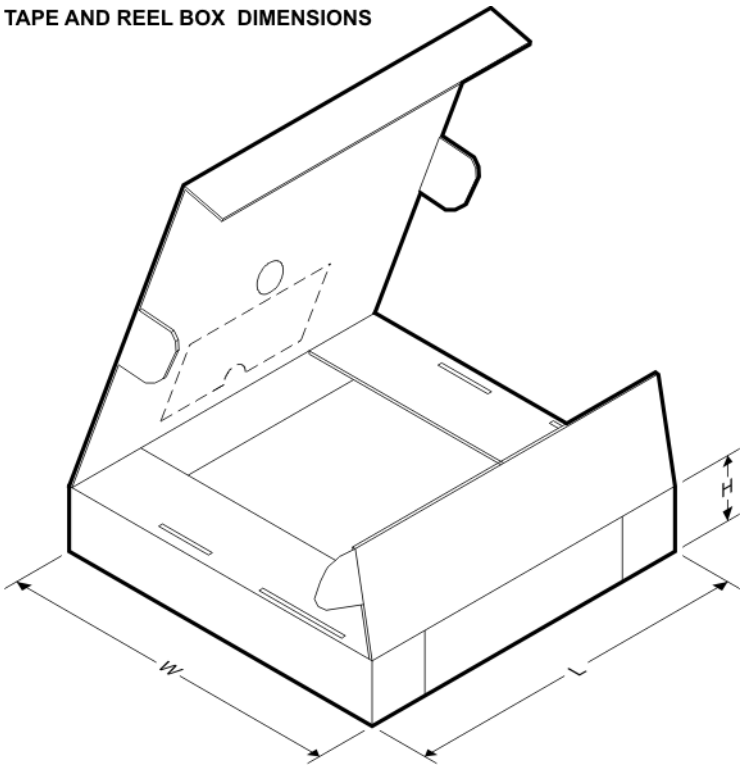

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1G07DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 9.2 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DRLR | SOT | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74AUP1G07DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74AUP1G07YFPR | DSBGA | YFP | 4 | 3000 | 178.0 | 9.2 | 0.89 | 0.89 | 0.58 | 4.0 | 8.0 | Q1 |
| SN74AUP1G07YZPR | DSBGA | YZP | 5 | 3000 | 180.0 | 8.4 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

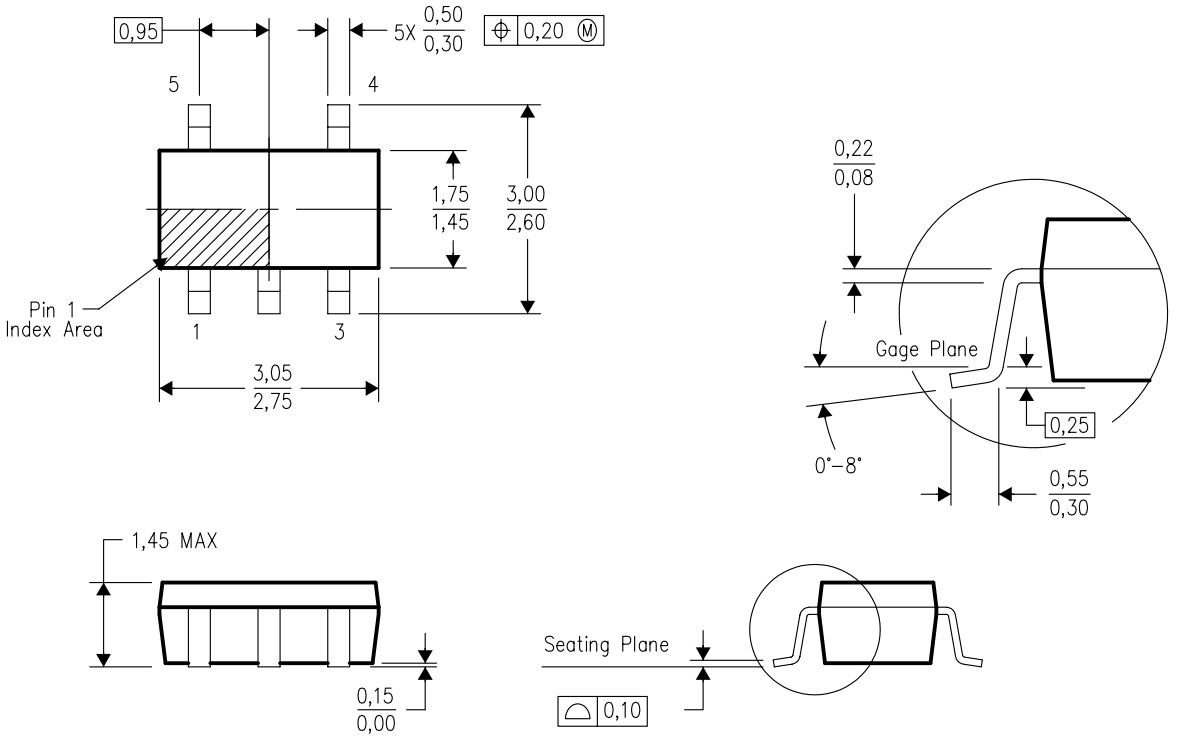
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AUP1G07DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUP1G07DBVT | SOT-23 | DBV | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G07DCKR | SC70 | DCK | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74AUP1G07DRLR | SOT | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G07DRYR | SON | DRY | 6 | 5000 | 180.0 | 180.0 | 30.0 |
| SN74AUP1G07DSFR | SON | DSF | 6 | 5000 | 180.0 | 180.0 | 30.0 |
| SN74AUP1G07YFPR | DSBGA | YFP | 4 | 3000 | 220.0 | 220.0 | 35.0 |
| SN74AUP1G07YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 34.0 |

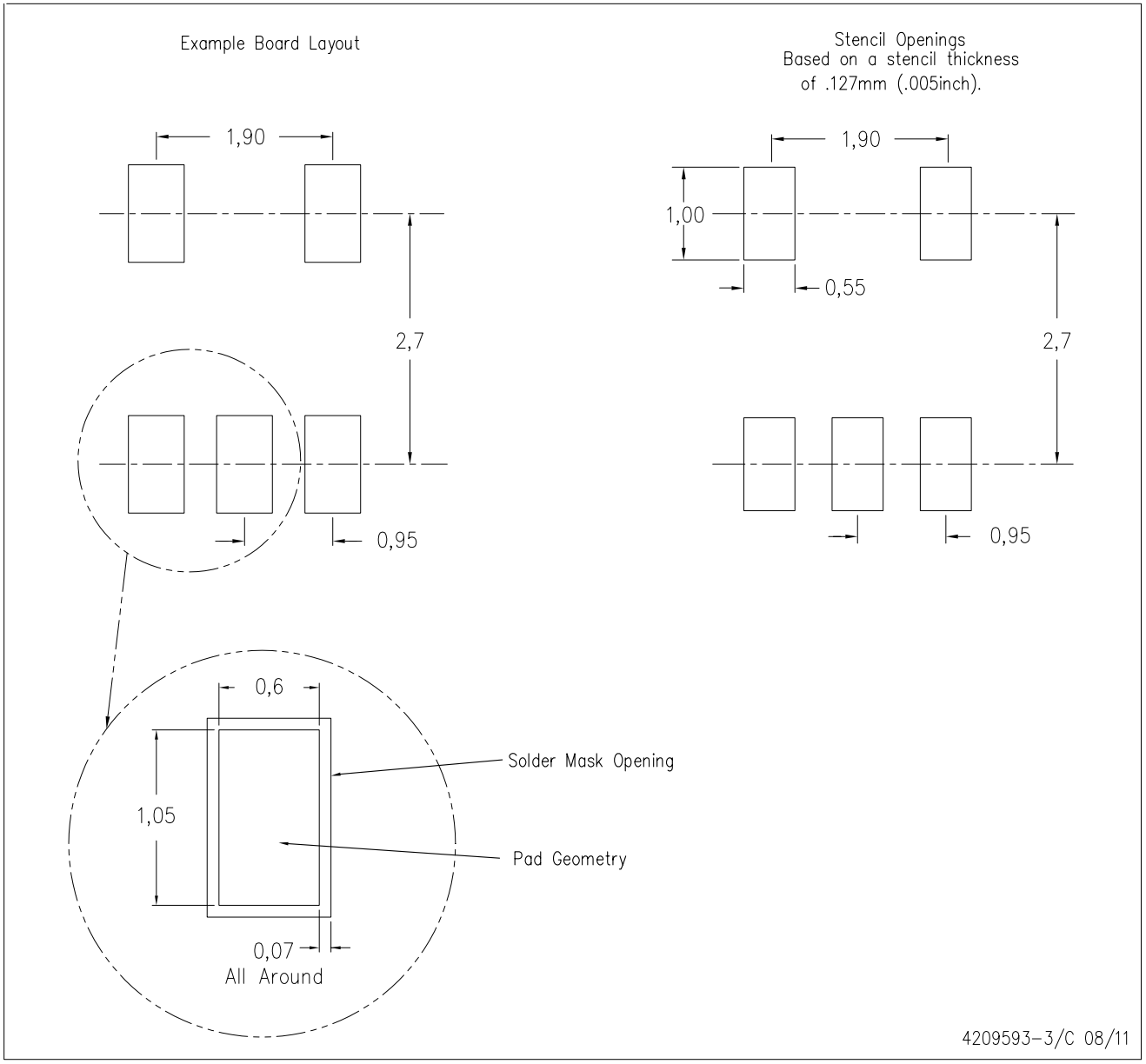
## DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/K 03/2006

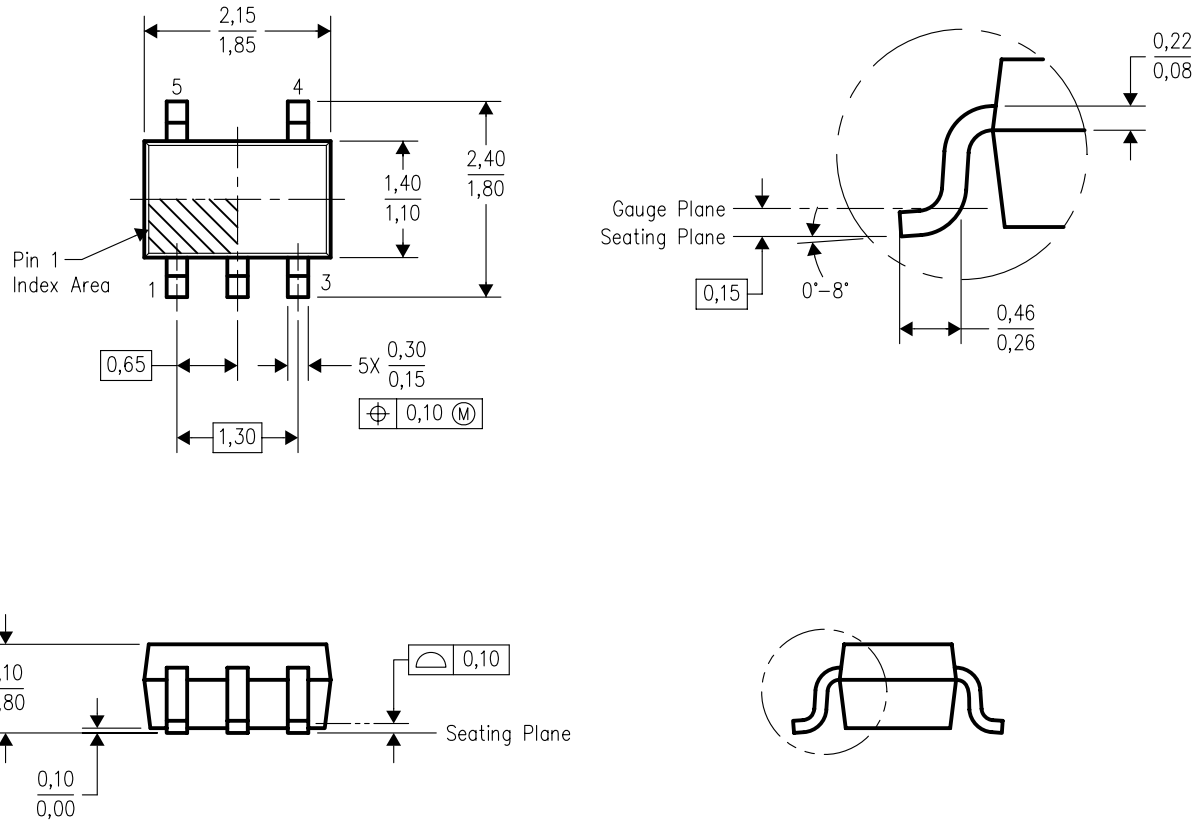
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

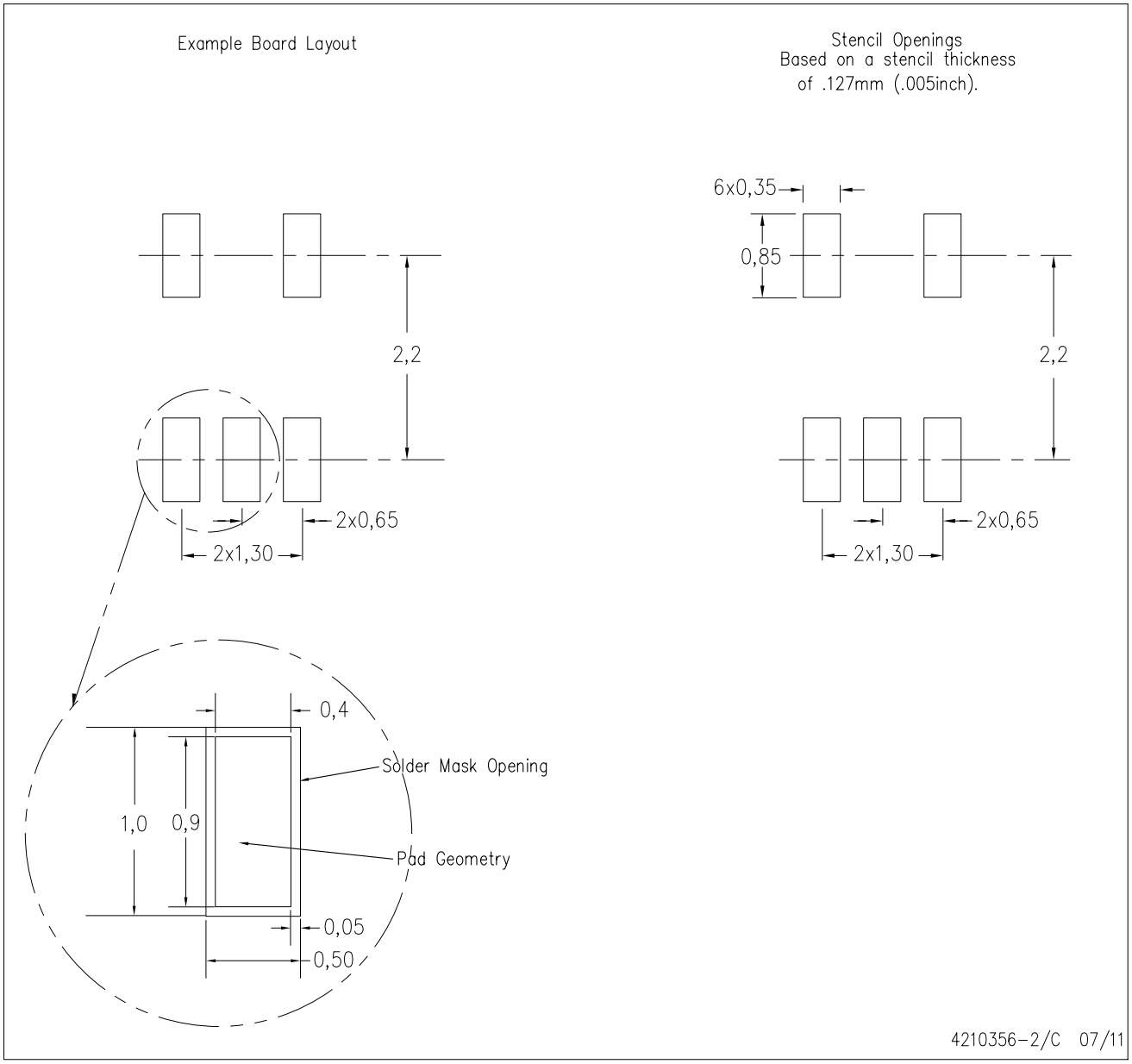
## DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



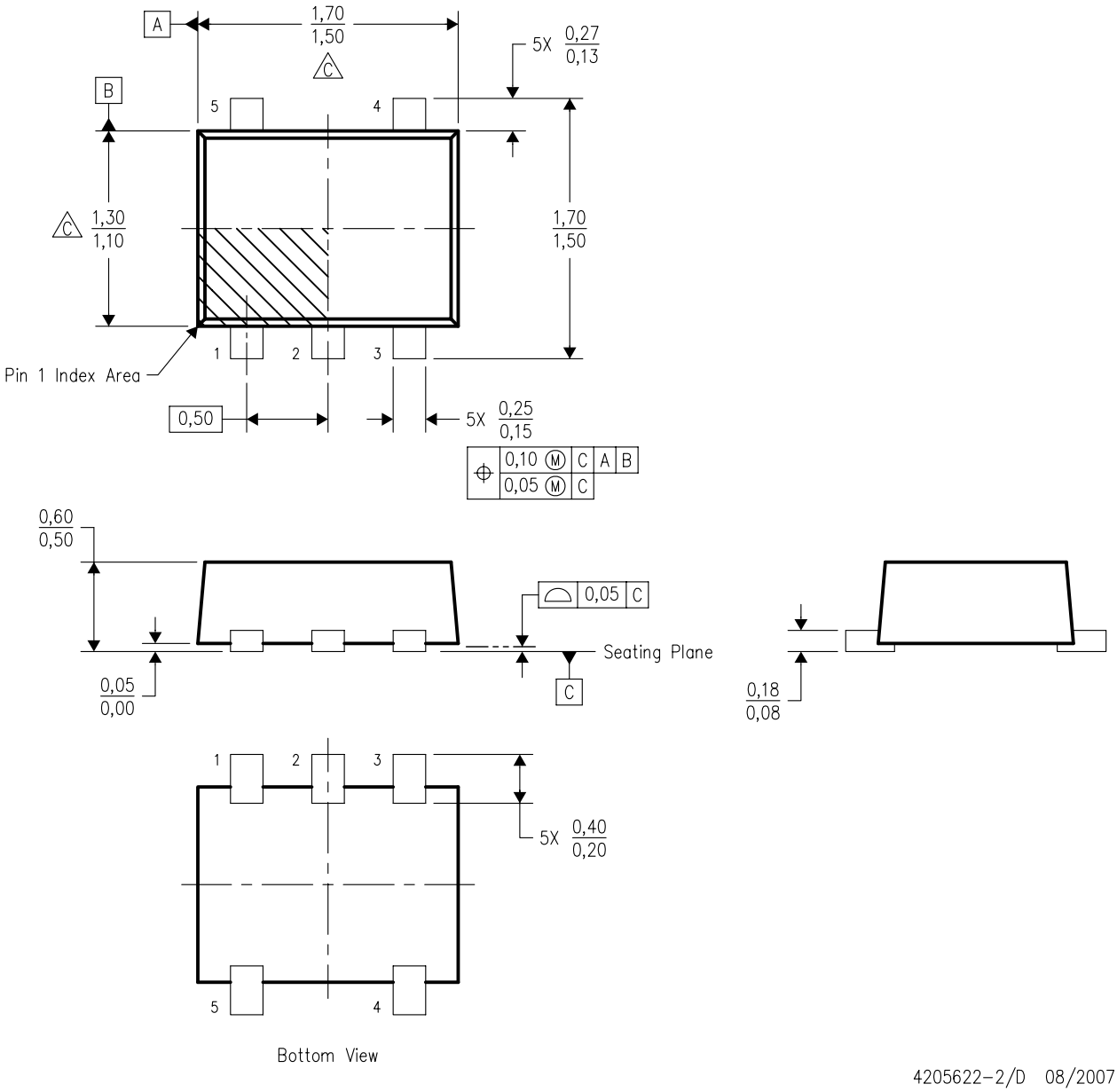

4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE

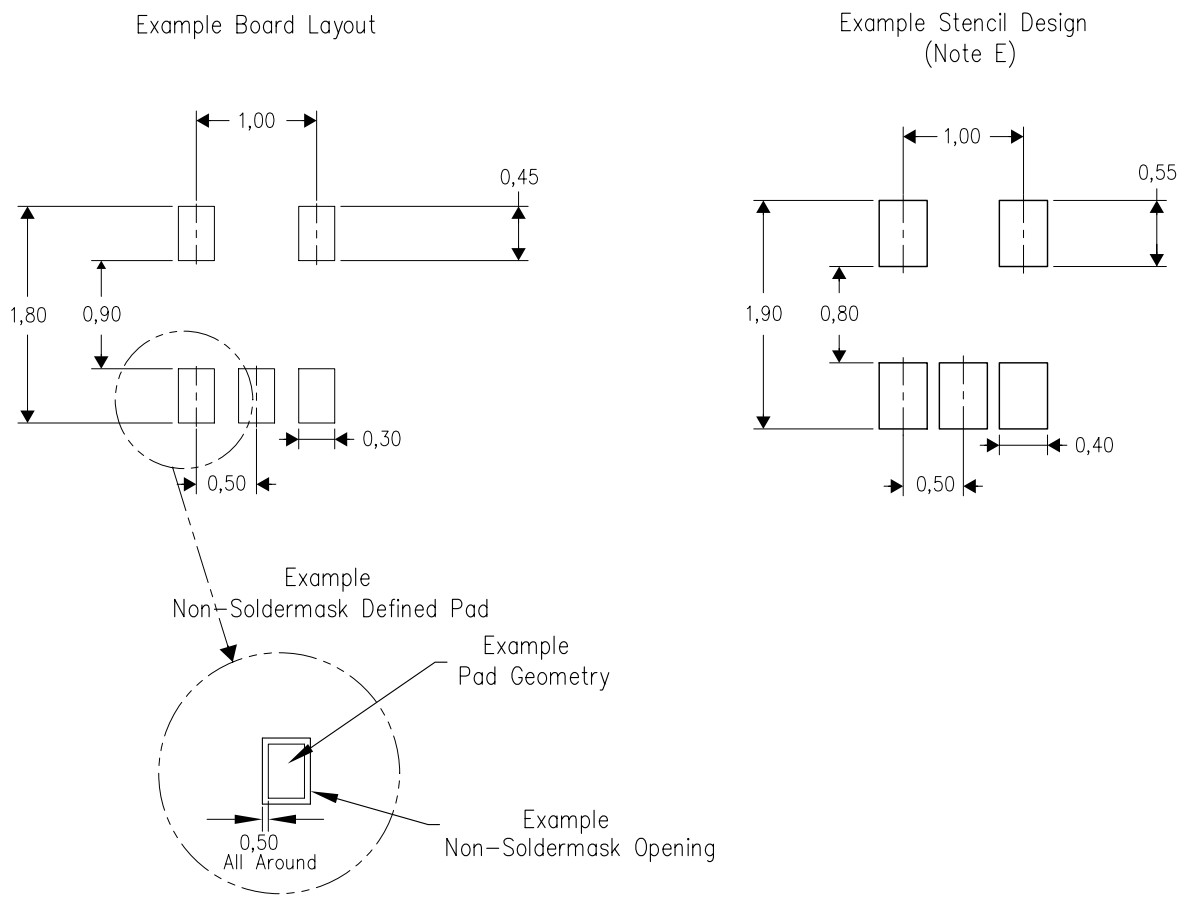



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

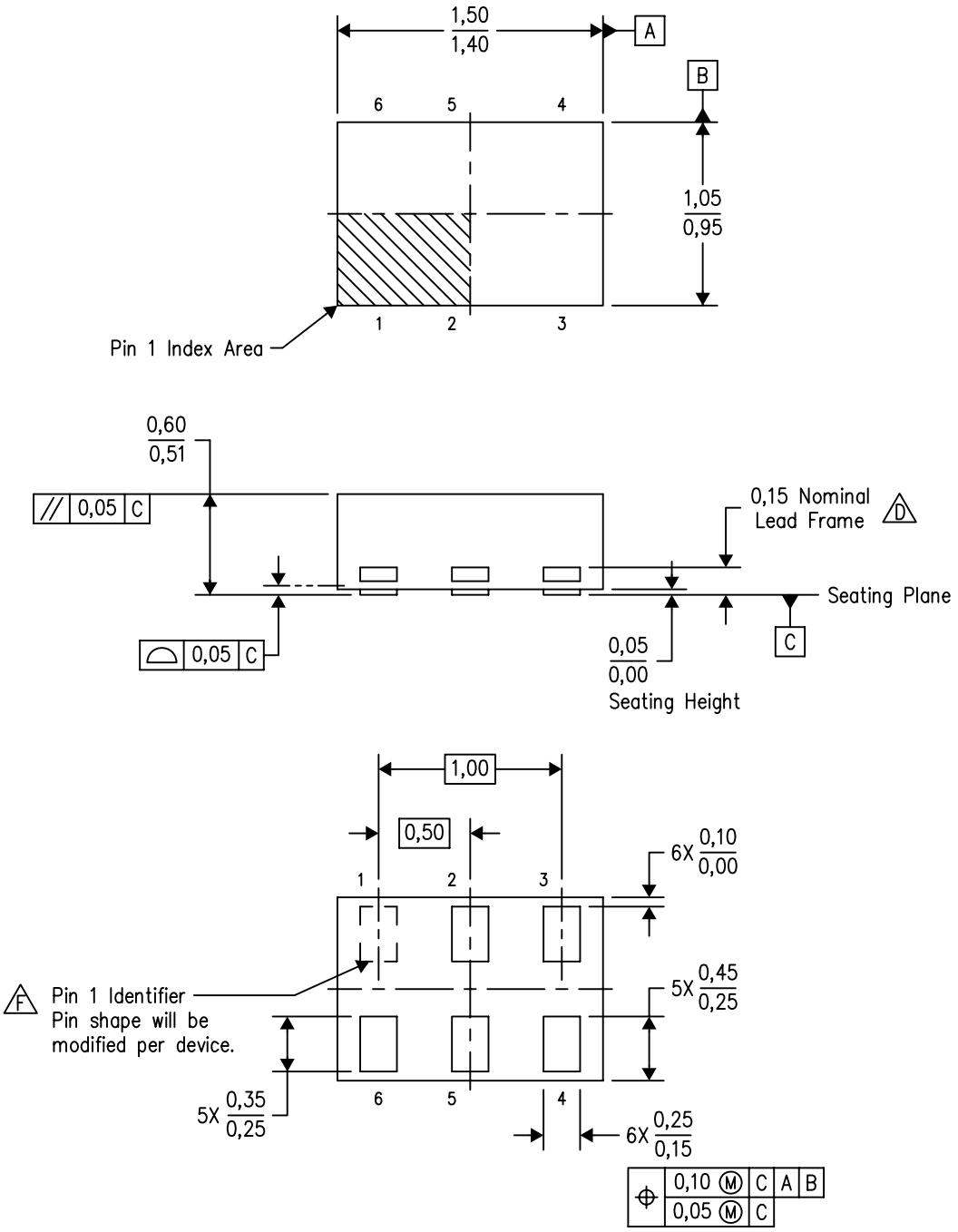
DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE




4208207–2/D 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

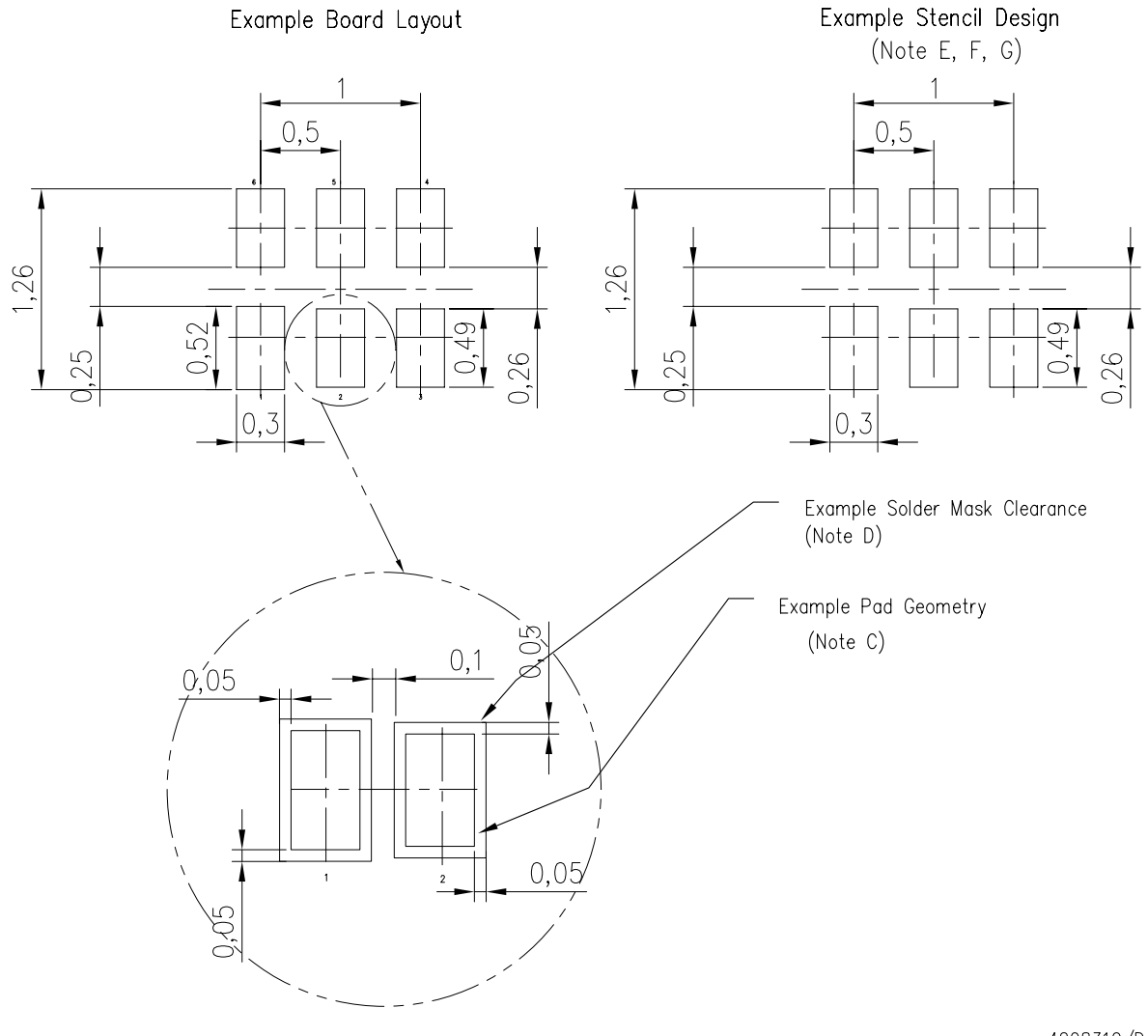
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4207181/F 12/11

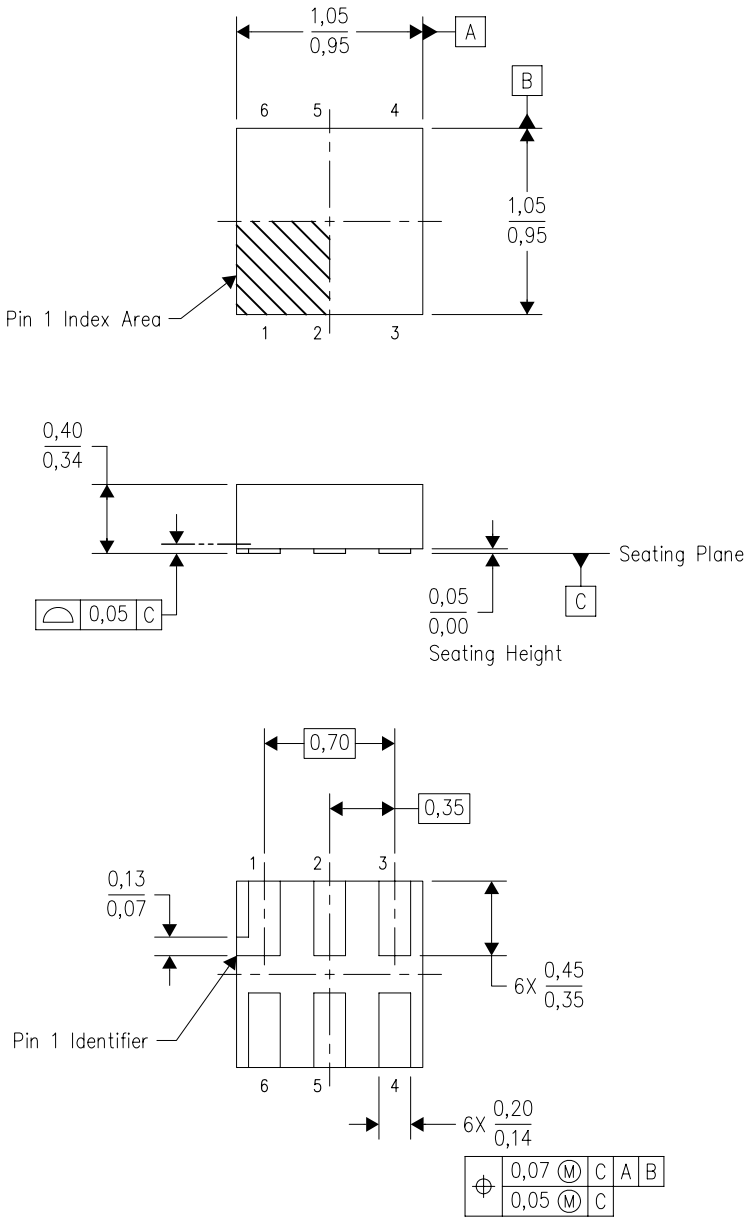
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (S–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

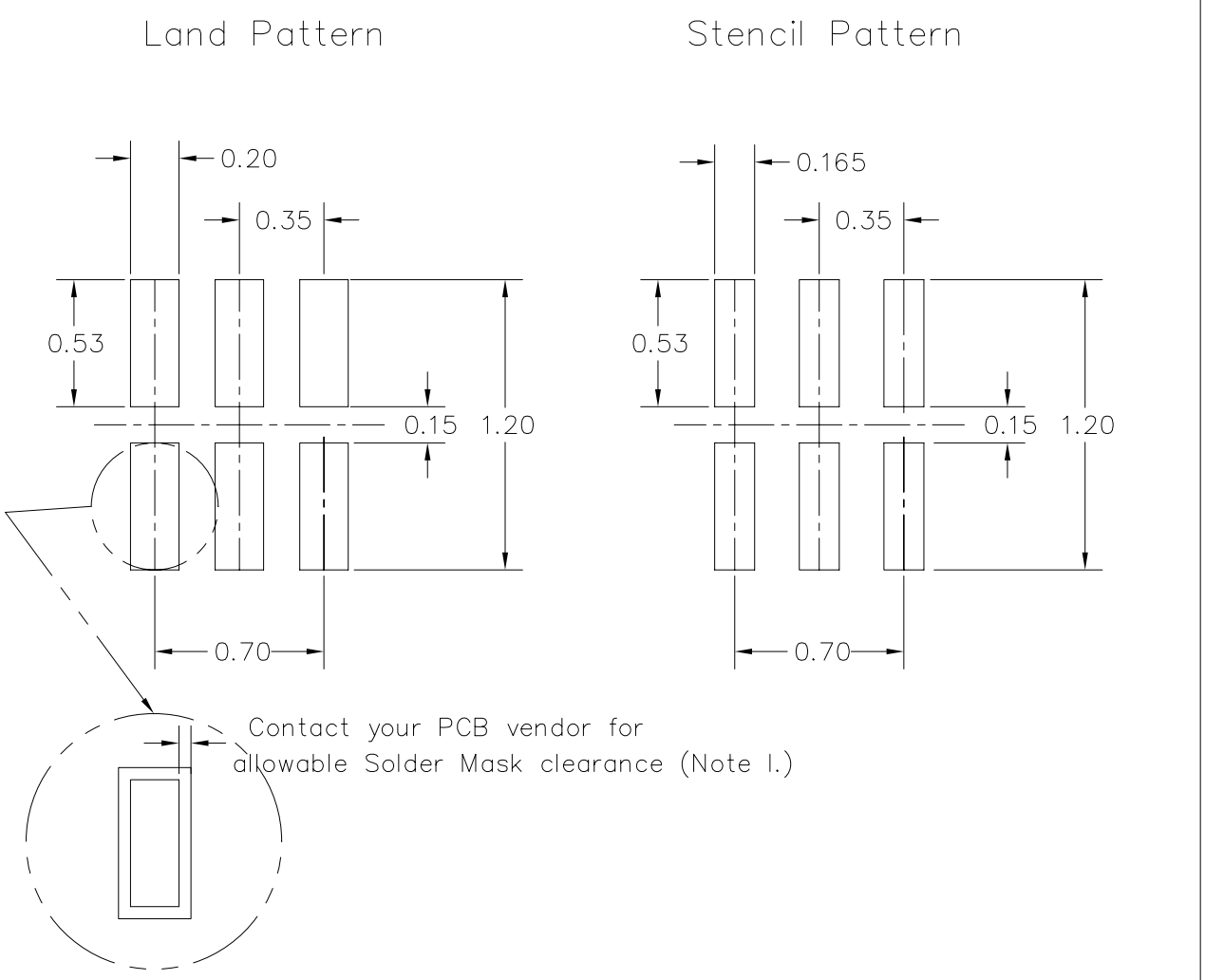
DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4208186/E 03/11

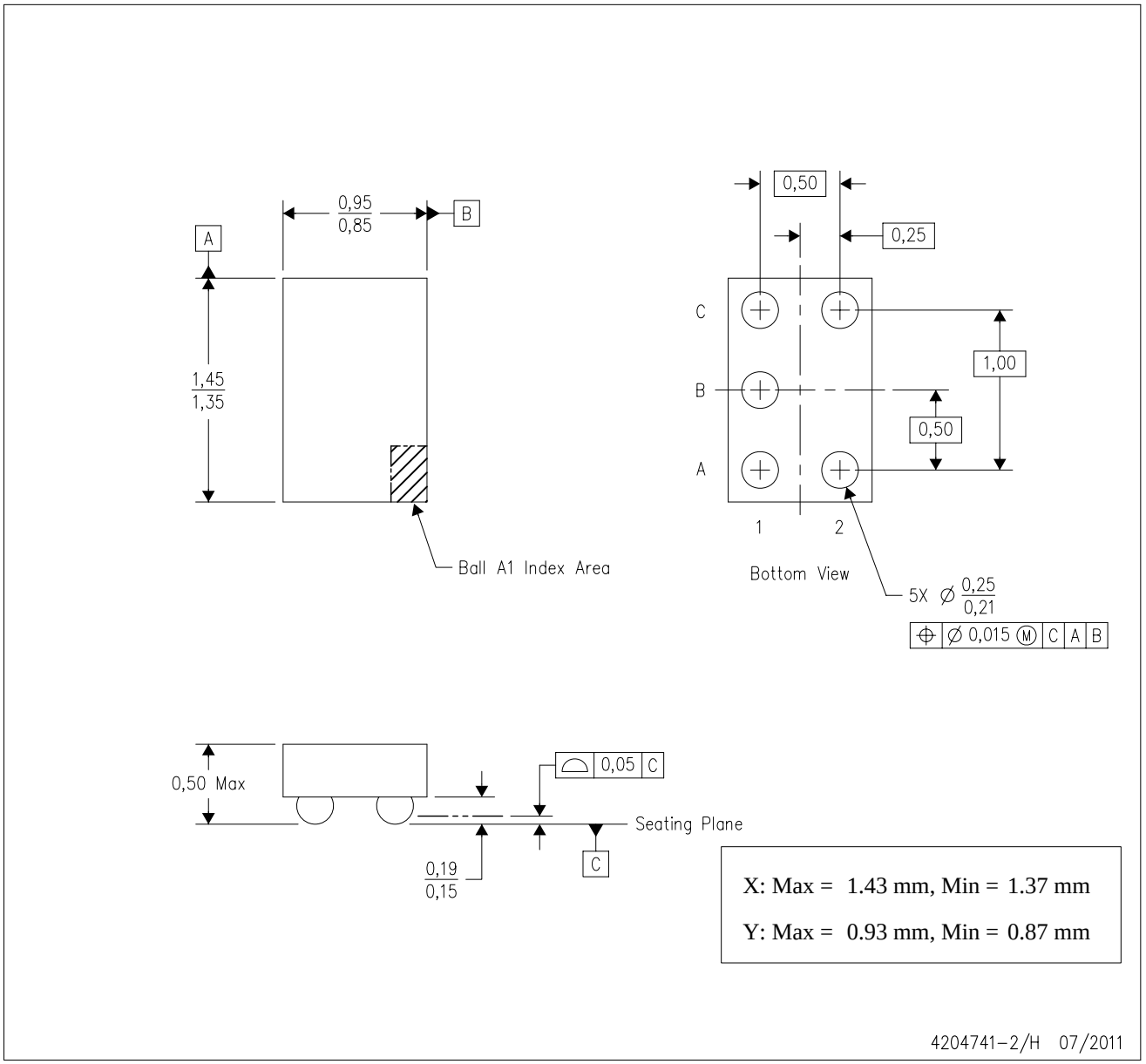
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. This package complies to JEDEC MO–287 variation X2AAF.

DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD



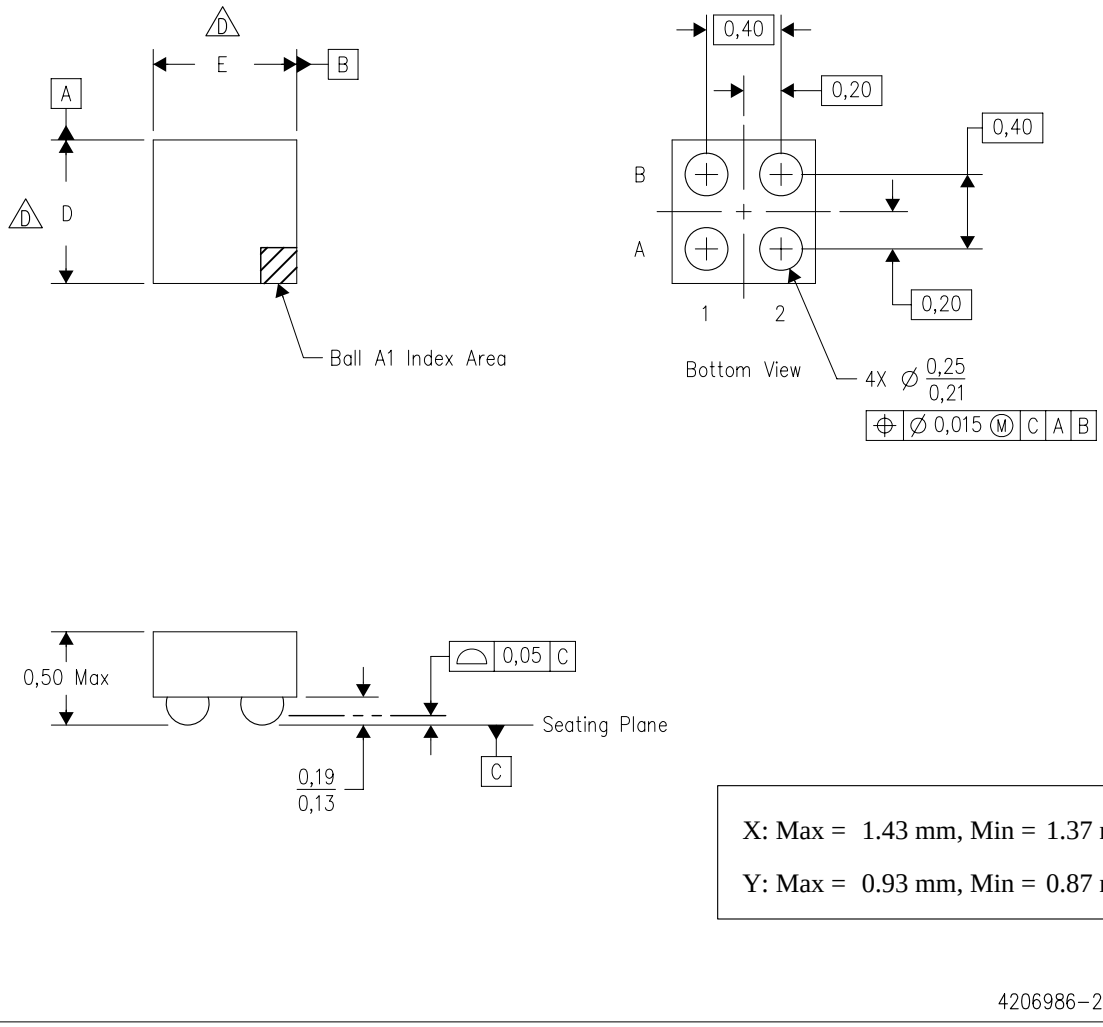

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Over–printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
I. Component placement force should be minimized to prevent excessive paste block deformation.

YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is a Pb–free solder ball design. Refer to the 5 YEP package (drawing 4204725) for tin–lead (SnPb).

YFP (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population.
2 x 2 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

**NanoFree is a trademark of Texas Instruments**

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| RFID | www.ti-rfid.com | | |
| OMAP Mobile Processors | www.ti.com/omap | | |
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