

# TVS Diode Arrays

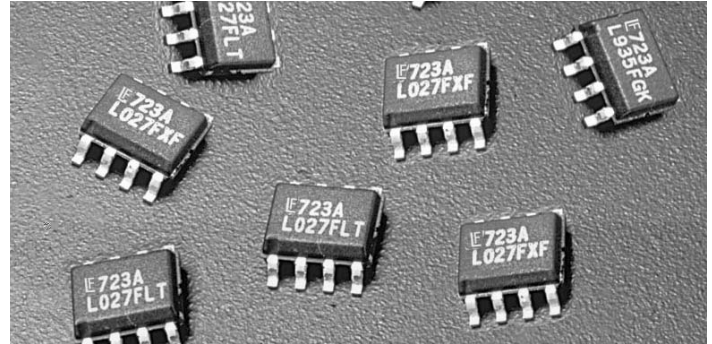
Electronic Protection Array for ESD and Overvoltage Protection

## RoHS GREEN SP723 Lead-Free/Green

The SP723 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection of sensitive input circuits. The SP723 has 2 protection SCR/Diode device structures per input. There are a total of 6 available inputs that can be used to protect up to 6 external signal or bus lines. Over-voltage protection is from the IN (Pins 1 - 3 and Pins 5 - 7) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one  $+V_{BE}$  diode threshold above V+ (Pin 8) or a  $-V_{BE}$  diode threshold below V- (Pin 4). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one  $V_{BE}$  above V+. A similar clamp to V- is activated if a negative pulse, one  $V_{BE}$  less than V-, is applied to an IN input.

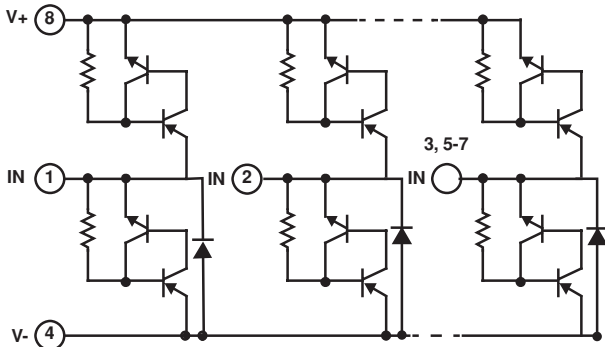
Refer to Fig 1 and Table 1 for further details. Refer to Application Note AN9304 and AN9612 for further detail.



### Ordering Information

PART NO.	TEMP. RANGE (°C)	PACKAGE	ENVIRONMENTAL INFORMATON	MARKING	Min. Order
SP723APP	-40 to 105	8 Ld PDIP	Lead-free	723APP	2000
SP723ABG	-40 to 105	8 Ld SOIC	Green	723AG	1960
SP723ABTG	-40 to 105	8 Ld SOIC Tape and Reel	Green	723AG	2500

### Functional Diagram



### Features

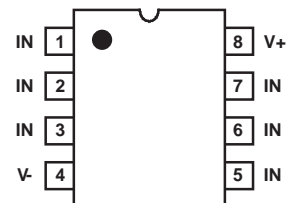
- ESD Interface per HBM Standards
  - IEC 61000-4-2, Direct Discharge ..... 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge ..... 15kV (Level 4)
  - MIL-STD-3015.7 ..... 25kV
- Peak Current Capability
  - IEC 61000-4-5 8/20µs Peak Pulse Current. .... ±7A
  - Single Transient Pulse, 100s Pulse Width. .... ±4A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to ..... +30V
  - Differential Voltage Range to ..... ±15V
- Fast Switching ..... 2ns Risetime
- Low Input Leakages ..... 2nA at 25°C Typical
- Low Input Capacitance ..... 5pF Typical
- An Array of 6 SCR/Diode Pairs
- Operating Temperature Range ..... -40°C to 105°C

### Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

### Pinout

SP723  
(PDIP, SOIC)  
TOP VIEW





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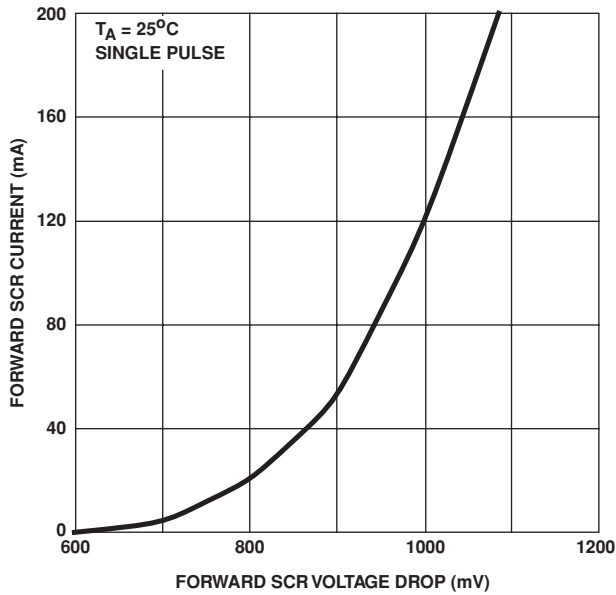


FIGURE 2. LOW CURRENT SCR FORWARD VOLTAGE DROP CURVE

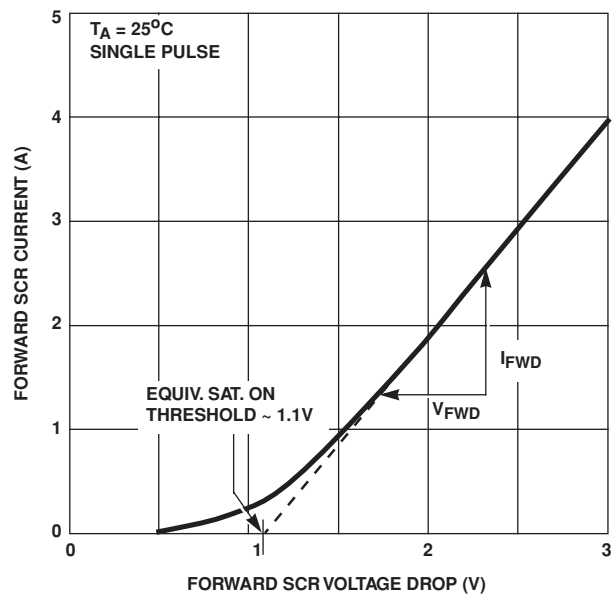


FIGURE 3. HIGH CURRENT SCR FORWARD VOLTAGE DROP CURVE

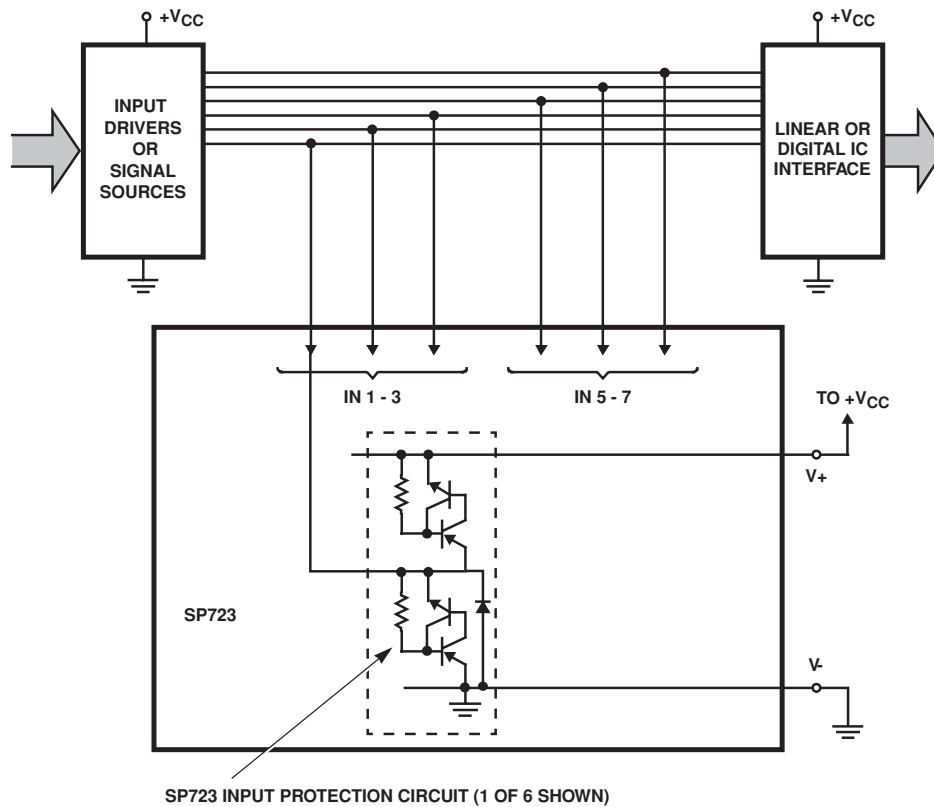


FIGURE 4. TYPICAL APPLICATION OF THE SP723 AS AN INPUT CLAMP FOR OVER-VOLTAGE, GREATER THAN  $1V_{BE}$  ABOVE  $V_+$  OR LESS THAN  $-1V_{BE}$  BELOW  $V_-$

**RoHS** **Pb** **GREEN** **SP723 Lead-Free/Green**

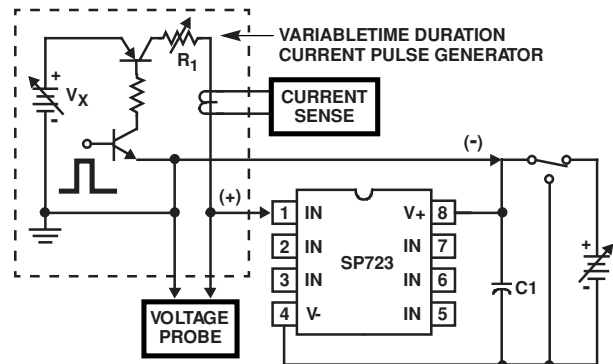
**Peak Transient Current Capability of the SP723**

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP723's ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 5.

The test circuit of Figure 5 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP723 'IN' input pin and the (+) current pulse input goes to the SP723 V- pin. The V+ to V- supply of the SP723 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 6 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

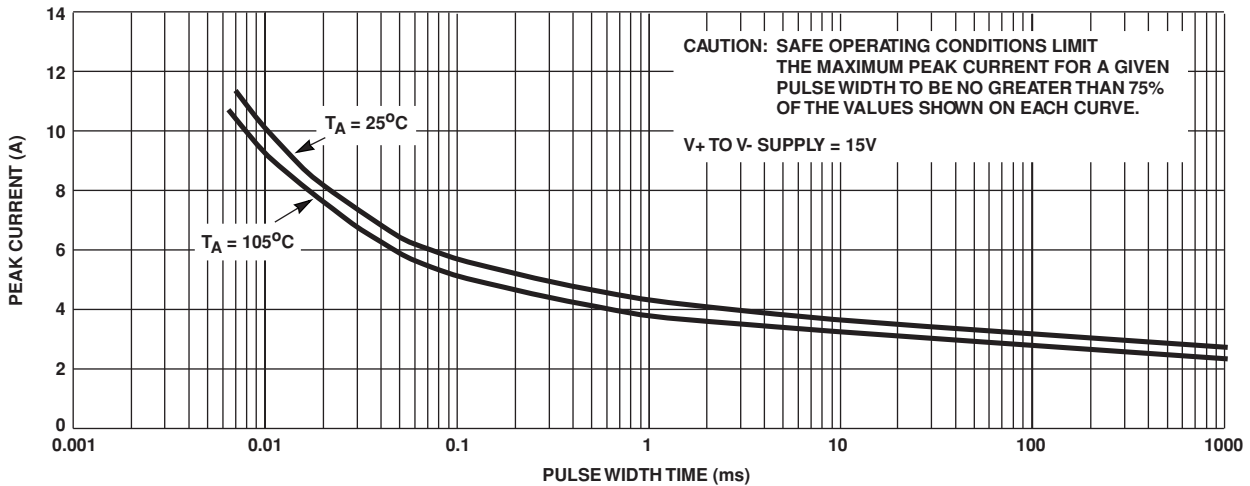
The maximum peak input current capability is dependent on the ambient temperature, improving as the temperature is reduced. Peak current curves are shown for ambient temperatures of 25°C and 105°C and a 15V power supply condition. The safe operating range of the transient peak current should be limited to no more than 75% of the measured over-stress level for any given pulse width as shown in the curves of Figure 6.

Note that adjacent input pins of the SP723 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.



$R_1 \sim 10\Omega$  TYPICAL  
 $V_X$  ADJ. 10V/A TYPICAL  
 $C_1 \sim 100\mu F$

**FIGURE 5. TYPICAL SP723 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT**



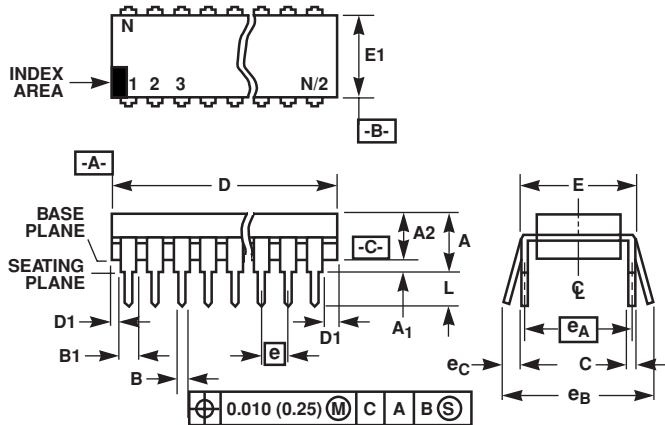
**FIGURE 6. SP723 TYPICAL SINGLE PULSE PEAK CURRENT CURVES SHOWING THE MEASURED POINT OF OVERSTRESS IN AMPERES vs PULSE WIDTH TIME IN MILLISECONDS**

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## Dual-In-Line Plastic Packages (PDIP)



**NOTES:**

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
7.  $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

## E8.3 (JEDEC MS-001-BA ISSUE D)

### 8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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