ULTRALOW-NOISE, HIGH PSRR, FAST RF 200-mA LOW-DROPOUT LINEAR REGULATORS IN NanoStar™ WAFER CHIP SCALE AND SOT23

FEATURES

- **200-mA RF Low-Dropout Regulator With Enable**
- **Available in 1.8-V, 2.5-V, 2.8-V, 2.85-V, 3-V, 3.3-V, 4.75-V, and Adjustable (1.22-V to 5.5-V)**
- **High PSRR (70 dB at 10 kHz)**
- **Ultralow-Noise (32 μV_{RMS}, TPS79328)**
- **Fast Start-Up Time (50 µs)**
- **Stable With a 2.2-µF Ceramic Capacitor**
- **Excellent Load/Line Transient Response**
- **Very Low Dropout Voltage (112 mV at Full Load, TPS79330)**
- **5- and 6-Pin SOT23 (DBV) and NanoStar Wafer Chip Scale (YEQ) Packages**

APPLICATIONS

- **RF: VCOs, Receivers, ADCs**
- **Audio**
- **Cellular and Cordless Telephones**
- **Bluetooth™, Wireless LAN**
- **Handheld Organizers, PDAs**

DESCRIPTION

The TPS793xx family of low-dropout (LDO) low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow-noise, fast start-up, and excellent line and load transient responses in NanoStar wafer chip scale and SOT23 packages. NanoStar packaging gives an ultrasmall footprint as well as an ultralow profile and package weight, making it ideal for portable applications such as handsets and PDAs. Each device in the family is stable, with a small 2.2-µF ceramic capacitor on the output. The TPS793xx family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (e.g., 112 mV at 200 mA, TPS79330). Each device achieves fast start-up times (approximately 50 µs with a 0.001-µF bypass capacitor) while consuming very low quiescent current (170 µA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 µA. The TPS79328 exhibits approximately 32 μV_{RMS} of output voltage noise at 2.8-V output with a 0.1-µF bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high PSRR and low-noise features as well as the fast response time.

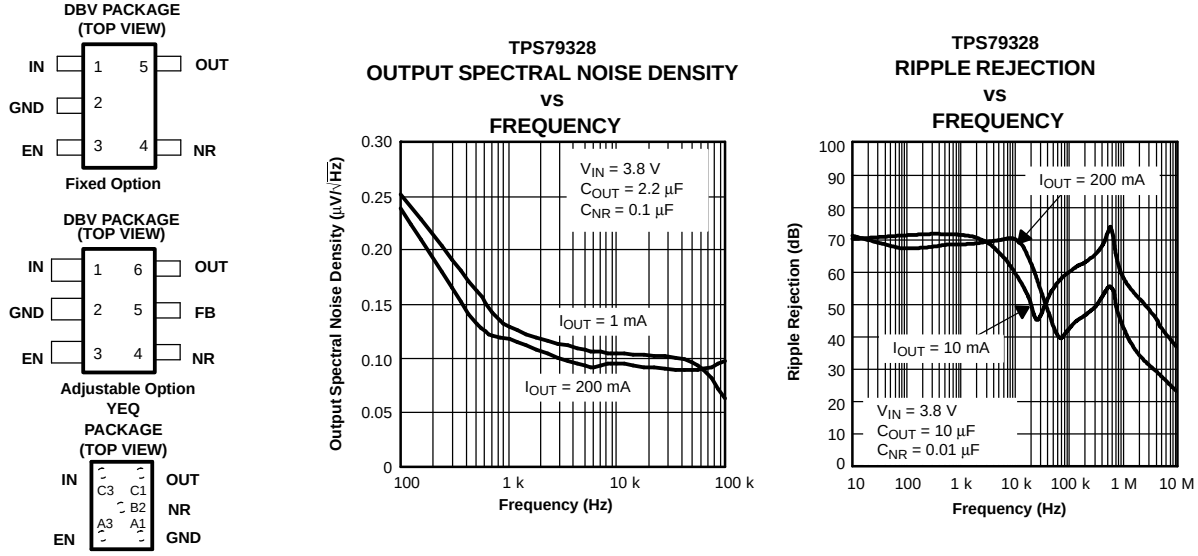


Figure 1.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS[1][2]

PRODUCT	VOLTAGE	PACKAGE	T_J	SYMBOL	PART NUMBER
TPS79301	1.22 V to 5.5 V	SOT23 (DBV)	-40°C to +125°C	PGVI	TPS79301DBVR
TPS79318	1.8 V	SOT23 (DBV)		PHHI	TPS79318DBVR
		CSP (YEQ)		E3	TPS79318YEQ
TPS79325	2.5 V	SOT23 (DBV)		PGWI	TPS79325DBVR
		CSP (YEQ)		E4	TPS79325YEQ
TPS79328	2.8 V	SOT23 (DBV)		PGXI	TPS79328DBVR
		CSP (YEQ)		E2	TPS79328YEQ
TPS793285	2.85 V	SOT23 (DBV)		PHII	TPS793285DBVR
		CSP (YEQ)		E5	TPS793285YEQ
TPS79330	3 V	SOT23 (DBV)		PGYI	TPS79330DBVR
		CSP (YEQ)		E6	TPS79330YEQ
TPS79333	3.3 V	SOT23 (DBV)		PHUI	TPS79333DBVR
TPS793475	4.75 V	SOT23 (DBV)		PHJI	TPS793475DBVR

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.
(2) DBV**R** indicates tape and reel of 3000 parts. YEQ**R** indicates tape and reel of 3000 parts. YEQ**T** indicates tape and reel of 250 parts.

ABSOLUTE MAXIMUM RATINGS

over operating temperature range (unless otherwise noted)[1]

	UNIT
V_{IN} range	-0.3 V to 6 V
V_{EN} range	-0.3 V to V_{IN} + 0.3 V
V_{OUT} range	-0.3 V to 6 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Ratings Table
Junction temperature range, DBV package	-40°C to 150°C
Junction temperature range, YEQ package	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS TABLE

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low-K(1)	DBV	65°C/W	255°C/W	3.9 mW/°C	390 mW	215 mW	155 mW
High-K(2)	DBV	65°C/W	180°C/W	5.6 mW/°C	560 mW	310 mW	225 mW
Low-K(1)	YEQ	27°C/W	255°C/W	3.9 mW/°C	390 mW	215 mW	155 mW
High-K(2)	YEQ	27°C/W	190°C/W	5.3 mW/°C	530 mW	296 mW	216 mW

(1) The JEDEC low-K (1s) board design used to derive this data was a 3-inch x 3-inch, two layer board with 2 ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

over recommended operating temperature range T_J = -40 to 125°C, $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V(1), I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (unless otherwise noted). Typical values are at 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} Input voltage(1)				2.7		5.5	V
I_{OUT} Continuous output current				0		200	mA
V_{FB} Internal reference (TPS79301)				1.201	1.225	1.250	V
Output voltage range (TPS79301)				V_{FB}		5.5 - V_{DO}	V
Output voltage	TPS79318	0 µA < I_{OUT} < 200 mA,	2.8 V < V_{IN} < 5.5 V	1.764	1.8	1.836	V
	TPS79325	0 µA < I_{OUT} < 200 mA,	3.5 V < V_{IN} < 5.5 V	2.45	2.5	2.55	V
	TPS79328	0 µA < I_{OUT} < 200 mA,	3.8 V < V_{IN} < 5.5 V	2.744	2.8	2.856	V
	TPS793285	0 µA < I_{OUT} < 200 mA,	3.85 V < V_{IN} < 5.5 V	2.793	2.85	2.907	V
	TPS79330	0 µA < I_{OUT} < 200 mA,	4 V < V_{IN} < 5.5 V	2.94	3	3.06	V
	TPS79333	0 µA ≤ I_{OUT} < 200 mA,	4.3 V < V_{IN} < 5.5 V	3.234	3.3	3.366	V
	TPS793475	0 µA < I_{OUT} < 200 mA,	5.25 V < V_{IN} < 5.5 V	4.655	4.75	4.845	V
Line regulation ($\Delta V_{OUT}\%/\Delta V_{IN}$) (1)		V_{OUT} + 1 V < V_{IN}≤ 5.5 V			0.05	0.12	%/V
Load regulation ($\Delta V_{OUT}\%/\Delta I_{OUT}$)		0 µA < I_{OUT} < 200 mA,	T_J = 25°C		5		mV
Dropout voltage(2) ($V_{IN} = V_{OUT(nom)}$ - 0.1V)	TPS79328	I_{OUT} = 200 mA			120	200	mV
	TPS793285	I_{OUT} = 200 mA			120	200	
	TPS79330	I_{OUT} = 200 mA			112	200	
	TPS79333	I_{OUT} = 200 mA			102	180	
	TPS793475	I_{OUT} = 200 mA			77	125	
Output current limit		V_{OUT} = 0 V		285		600	mA
GND pin current		0 µA < I_{OUT} < 200 mA			170	220	µA
Shutdown current(3)		V_{EN} = 0 V, 2.7 V < V_{IN} < 5.5 V			0.07	1	µA
FB pin current		V_{FB} = 1.8 V				1	µA
Power-supply ripple rejection	TPS79328	f = 100 Hz, T_J = 25°C,	I_{OUT} = 10 mA		70		dB
		f = 100 Hz, T_J = 25°C,	I_{OUT} = 200 mA		68		
		f = 10 kHz, T_J = 25°C,	I_{OUT} = 200 mA		70		
		f = 100 kHz, T_J = 25°C,	I_{OUT} = 200 mA		43		
Output noise voltage (TPS79328)		BW = 200 Hz to 100 kHz, I_{OUT} = 200 mA	C_{NR} = 0.001 µF		55		μV_{RMS}
			C_{NR} = 0.0047 µF		36		
			C_{NR} = 0.01 µF		33		
			C_{NR} = 0.1 µF		32		

(1) Minimum V_{IN} is 2.7 V or V_{OUT} + V_{DO}, whichever is greater.
(2) Dropout is not measured for the TPS79318 and TPS79325 since minimum V_{IN} = 2.7 V.
(3) For adjustable versions, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

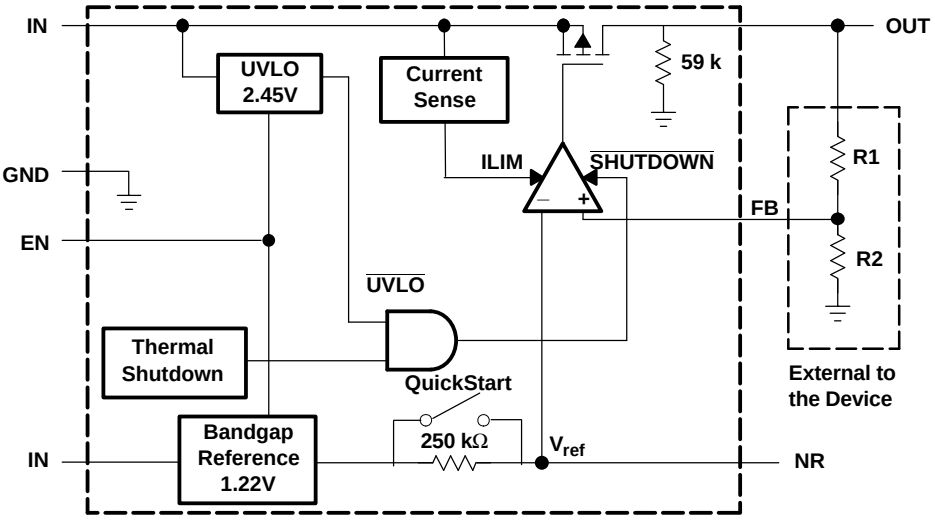
ELECTRICAL CHARACTERISTICS (continued)

over recommended operating temperature range T_J = -40 to 125°C, $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (unless otherwise noted). Typical values are at 25°C.

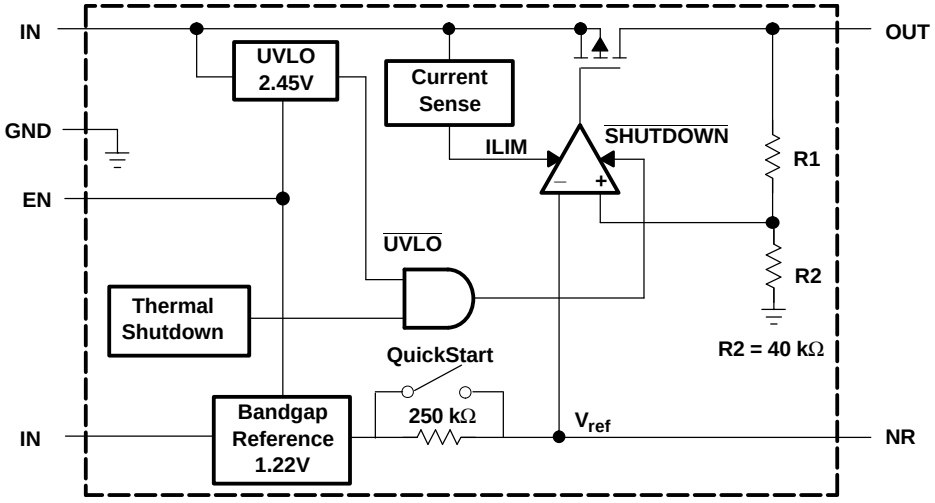
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Time, start-up (TPS79328)	R_L = 14 Ω, C_{OUT} = 1 µF	C_{NR} = 0.001 µF		50		µs
		C_{NR} = 0.0047 µF		70		
		C_{NR} = 0.01 µF		100		
High level enable input voltage	2.7 V < V_{IN} < 5.5 V		1.7		V_{IN}	V
Low level enable input voltage	2.7 V < V_{IN} < 5.5 V		0		0.7	V
EN pin current	V_{EN} = 0		-1		1	µA
UVLO threshold	V_{CC} rising		2.25		2.65	V
UVLO hysteresis				100		mV

FUNCTIONAL BLOCK DIAGRAMS

ADJUSTABLE VERSION



FIXED VERSION



Terminal Functions

TERMINAL				DESCRIPTION
NAME	SOT23 ADJ	SOT23 FIXED	WCSP FIXED	
NR	4	4	B2	Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This improves power-supply rejection and reduces output noise.
EN	3	3	A3	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	5	N/A	N/A	This terminal is the feedback input voltage for the adjustable device.
GND	2	2	A1	Regulator ground
IN	1	1	C3	Unregulated input to the device.
OUT	6	5	C1	Output of the regulator.

TYPICAL CHARACTERISTICS (SOT23 PACKAGE)

**TPS79328
OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

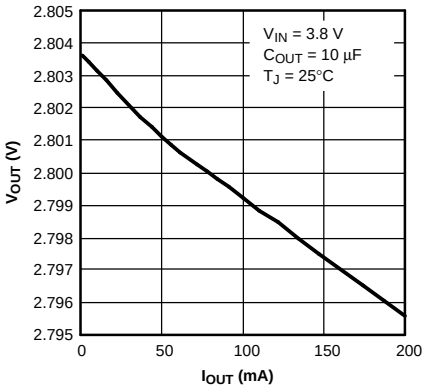


Figure 2.

**TPS79328
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE**

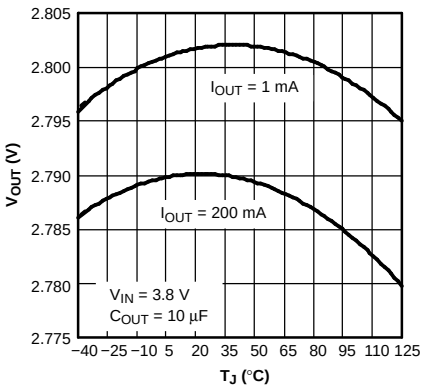


Figure 3.

**TPS79328
GROUND CURRENT
vs
JUNCTION TEMPERATURE**

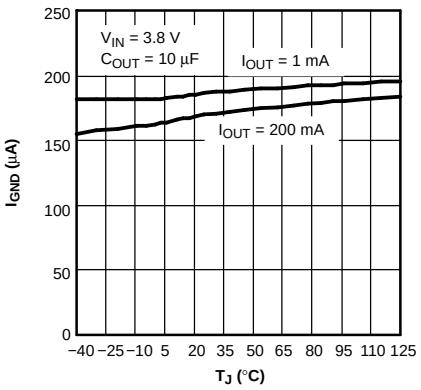


Figure 4.

**TPS79328 OUTPUT SPECTRAL
NOISE DENSITY
vs
FREQUENCY**

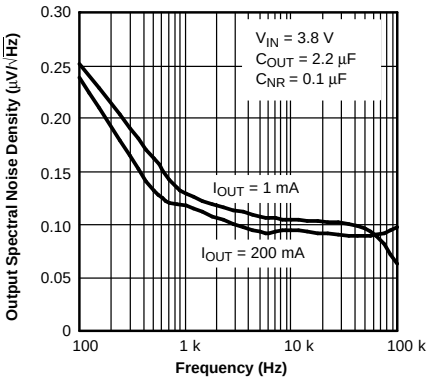


Figure 5.

**TPS79328 OUTPUT SPECTRAL
NOISE DENSITY
vs
FREQUENCY**

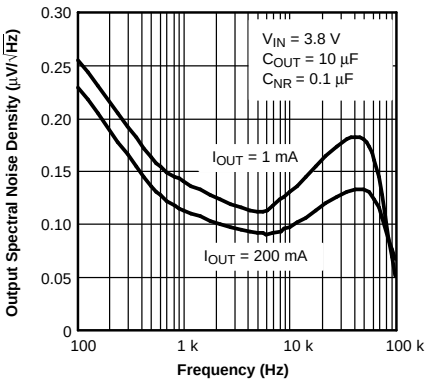


Figure 6.

**TPS79328 OUTPUT SPECTRAL
NOISE DENSITY
vs
FREQUENCY**

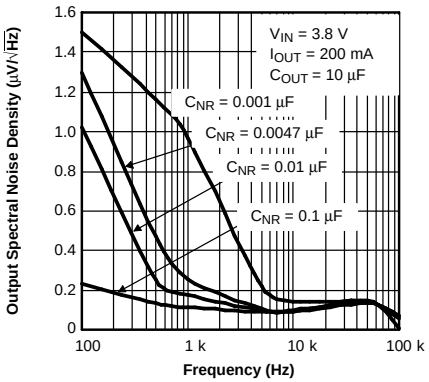


Figure 7.

**ROOT MEAN SQUARE OUTPUT
NOISE
vs
C_{NR}**

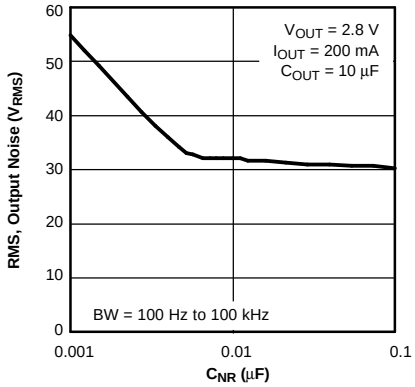


Figure 8.

**OUTPUT IMPEDANCE
vs
FREQUENCY**

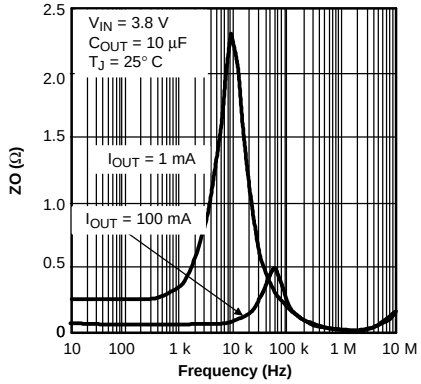


Figure 9.

**TPS79328
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE**

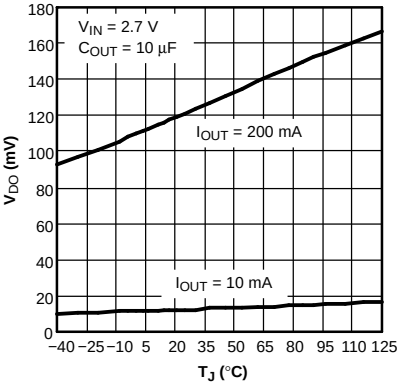


Figure 10.

TYPICAL CHARACTERISTICS (SOT23 PACKAGE) (continued)

TPS79328
RIPPLE REJECTION
vs
FREQUENCY

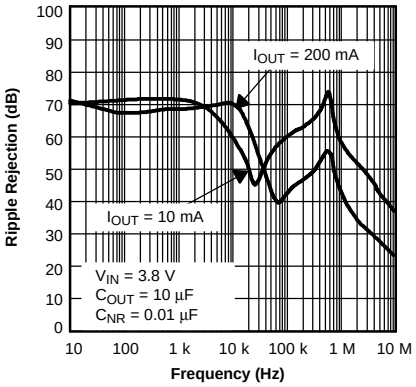


Figure 11.

TPS79328
RIPPLE REJECTION
vs
FREQUENCY

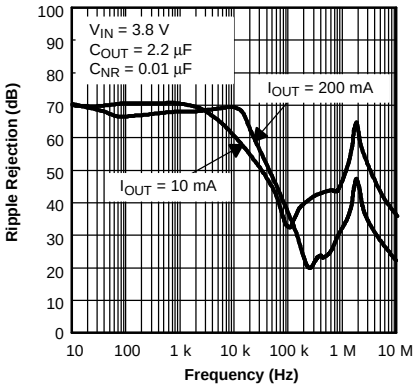


Figure 12.

TPS79328
RIPPLE REJECTION
vs
FREQUENCY

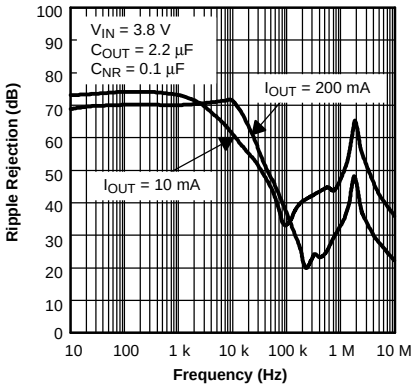


Figure 13.

TPS79328 OUTPUT VOLTAGE,
ENABLE VOLTAGE
vs
TIME (START-UP)

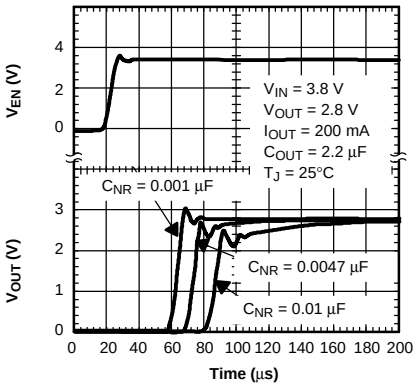


Figure 14.

TPS79328
LINE TRANSIENT RESPONSE

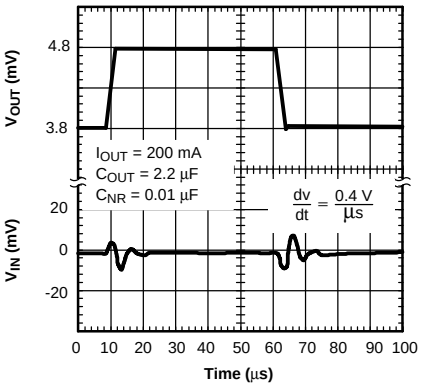


Figure 15.

TPS79328
LOAD TRANSIENT RESPONSE

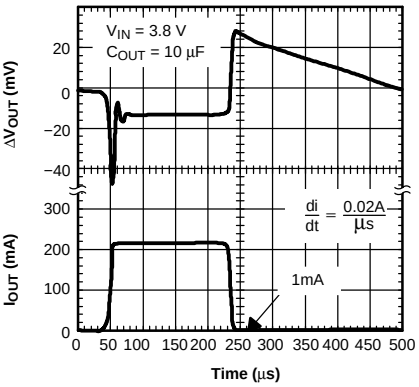


Figure 16.

POWER-UP / POWER-DOWN

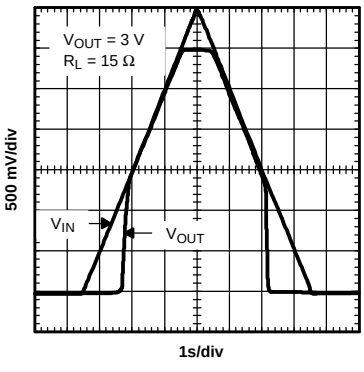


Figure 17.

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

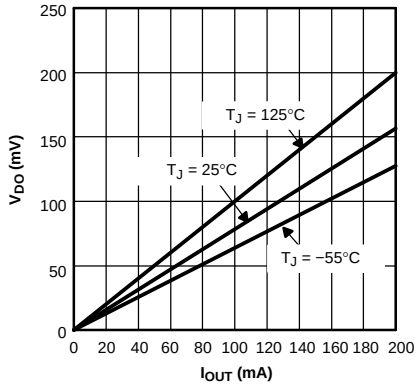


Figure 18.

TPS79301
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

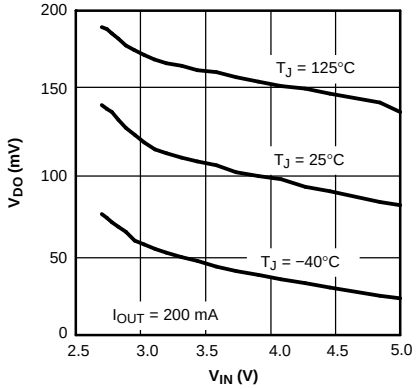


Figure 19.

TYPICAL CHARACTERISTICS (SOT23 PACKAGE) (continued)

TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

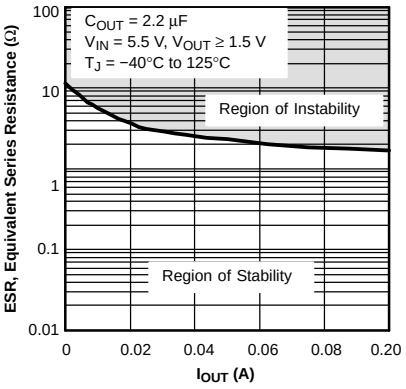


Figure 20.

TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

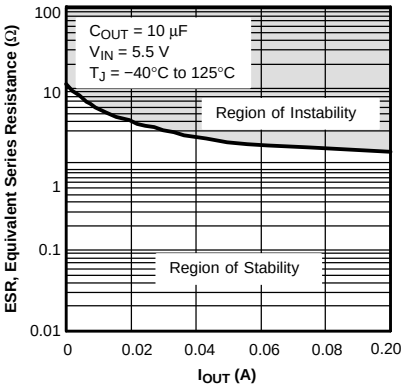


Figure 21.

APPLICATION INFORMATION

The TPS793xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 µA typically), and enable-input to reduce supply currents to less than 1 µA when the regulator is turned off.

A typical application circuit is shown in Figure 22.

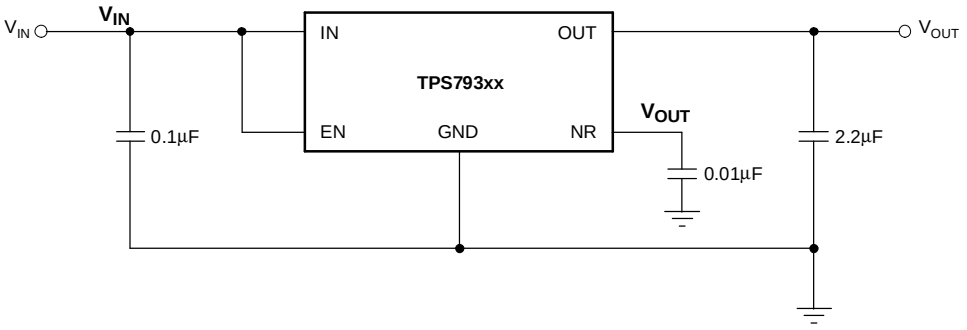


Figure 22. Typical Application Circuit

External Capacitor Requirements

A 0.1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS793xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated or the device is located several inches from the power source.

Like most low dropout regulators, the TPS793xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2 µF. Any 2.2-µF or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature. If load current is not expected to exceed 100 mA, a 1.0-µF ceramic capacitor can be used.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS793xx has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1-µF to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the Functional Block Diagrams

As an example, the TPS79328 exhibits only 32 μV_{RMS} of output voltage noise using a 0.1-µF ceramic bypass capacitor and a 2.2-µF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the NR pin that is created by the internal 250-kΩ resistor and external capacitor.

Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

APPLICATION INFORMATION (continued)

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using Equation 1:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\Theta JA}} \quad (1)$$

Where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the Dissipation Ratings Table).
- T_A is the ambient temperature.

The regulator dissipation is calculated using Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Programming the TPS79301 Adjustable LDO Regulator

The output voltage of the TPS79301 adjustable regulator is programmed using an external resistor divider as shown in Figure 23. The output voltage is calculated using Equation 3:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

Where:

- V_{REF} = 1.2246 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_{OUT}. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 µA, C1 = 15 pF for stability, and then calculate R1 using Equation 4:

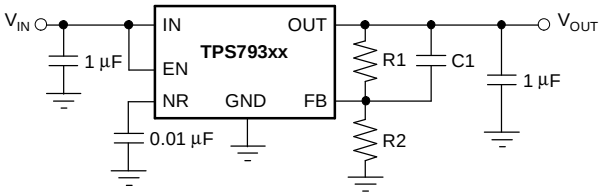
$$R_1 = \left(\frac{V_{OUT}}{V_{ref} - 1}\right) \times R_2 \quad (4)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. For voltages <1.8 V, the value of this capacitor should be 100 pF. For voltages >1.8 V, the approximate value of this capacitor can be calculated as shown in Equation 5:

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (5)$$

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage <1.8 V is chosen, then the minimum recommended output capacitor is 4.7 µF instead of 2.2 µF.

APPLICATION INFORMATION (continued)



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
1.22 V	short	open	0 pF
2.5 V	31.6 kΩ	30.1 kΩ	22 pF
3.3 V	51 kΩ	30.1 kΩ	15 pF
3.6 V	59 kΩ	30.1 kΩ	15 pF

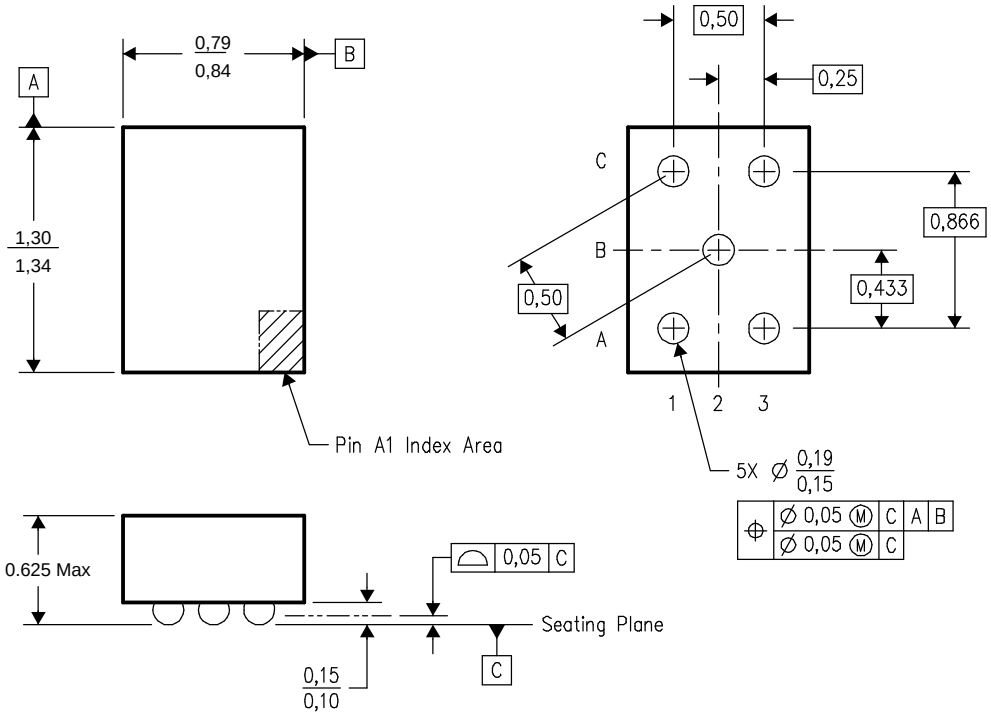
Figure 23. TPS79301 Adjustable LDO Regulator Programming

Regulator Protection

The TPS793xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS793xx features internal current limiting and thermal protection. During normal operation, the TPS793xx limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

TPS793xxYEQ NanoStar™ Wafer Chip Scale Information



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin-lead (SnPb); consult the factory for availability of lead-free material.

NanoStar is a trademark of Texas Instruments.

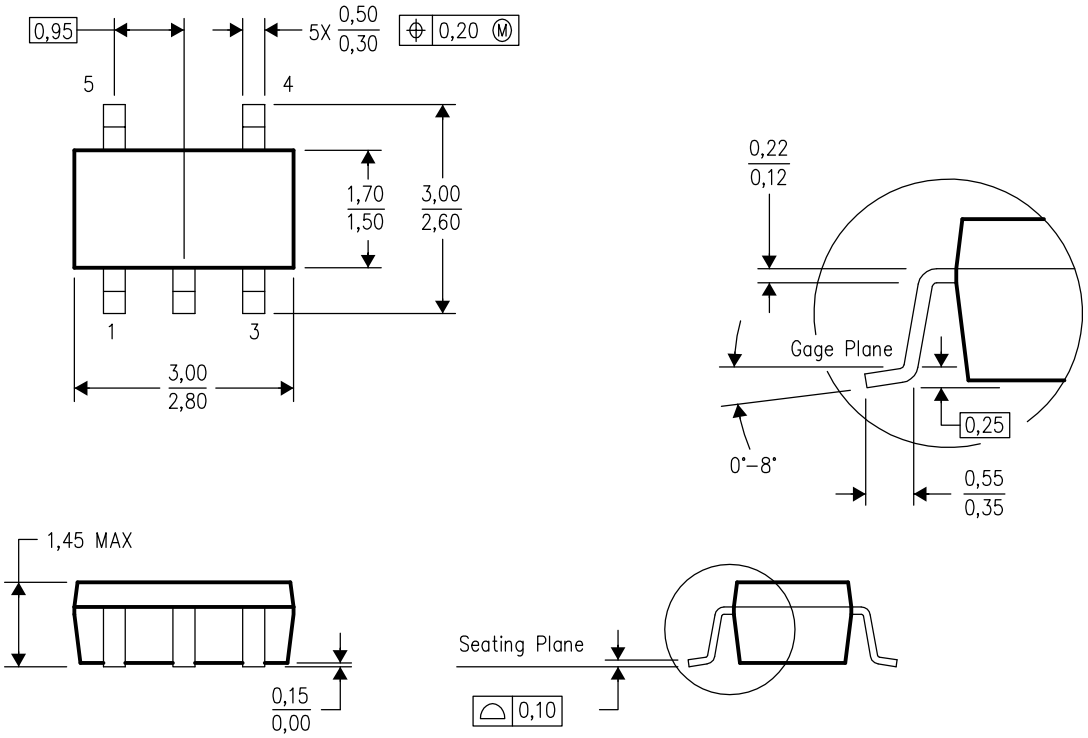
Figure 24. NanoStar™ Wafer Chip Scale Package

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
TPS79301DBVR	ACTIVE	SOP	DBV	6	3000
TPS79318DBVR	ACTIVE	SOP	DBV	5	3000
TPS79318DBVT	ACTIVE	SOP	DBV	5	250
TPS79318YEQR	ACTIVE	DSBGA	YEQ	5	3000
TPS79318YEQT	ACTIVE	DSBGA	YEQ	5	250
TPS79325DBVR	ACTIVE	SOP	DBV	5	3000
TPS79325YEQR	ACTIVE	DSBGA	YEQ	5	3000
TPS79325YEQT	ACTIVE	DSBGA	YEQ	5	250
TPS793285DBVR	ACTIVE	SOP	DBV	5	3000
TPS793285DBVT	ACTIVE	SOP	DBV	5	250
TPS793285YEQR	ACTIVE	DSBGA	YEQ	5	3000
TPS793285YEQT	ACTIVE	DSBGA	YEQ	5	250
TPS79328DBVR	ACTIVE	SOP	DBV	5	3000
TPS79328YEQR	ACTIVE	DSBGA	YEQ	5	3000
TPS79328YEQT	ACTIVE	DSBGA	YEQ	5	250
TPS79330DBVR	ACTIVE	SOP	DBV	5	3000
TPS79330YEQR	ACTIVE	DSBGA	YEQ	5	3000
TPS79330YEQT	ACTIVE	DSBGA	YEQ	5	250
TPS79333DBVR	ACTIVE	SOP	DBV	5	3000
TPS793475DBVR	ACTIVE	SOP	DBV	5	3000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

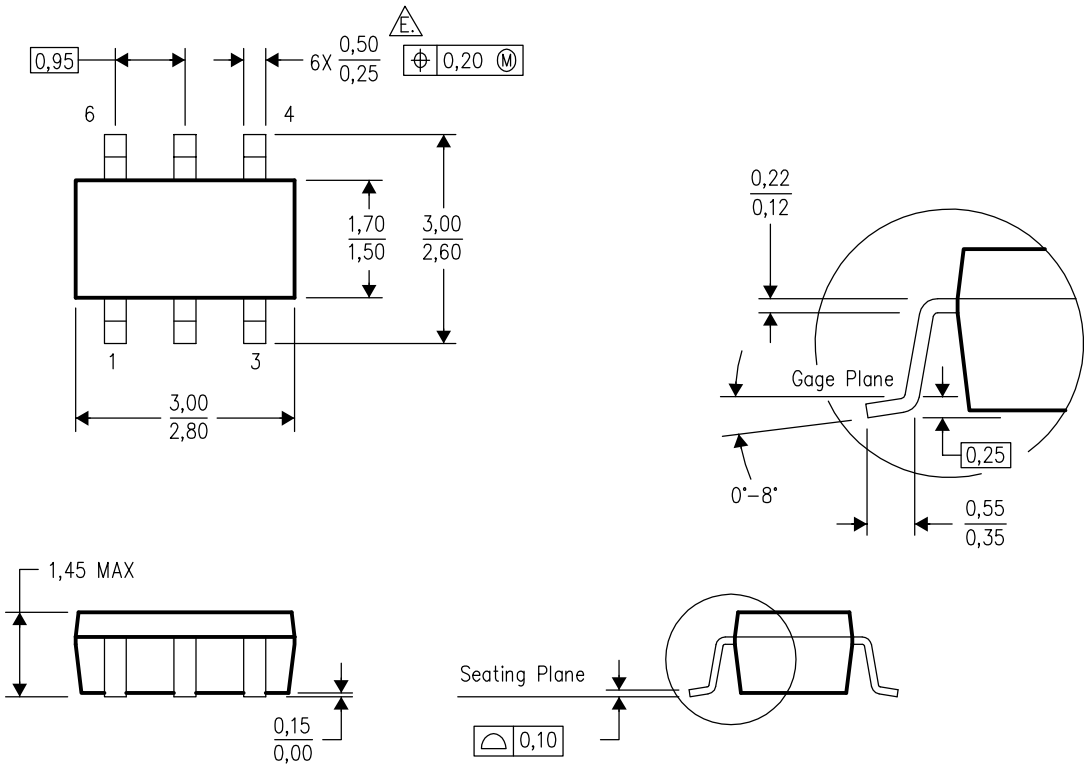
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/H 10/2003

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–178 Variation AA.

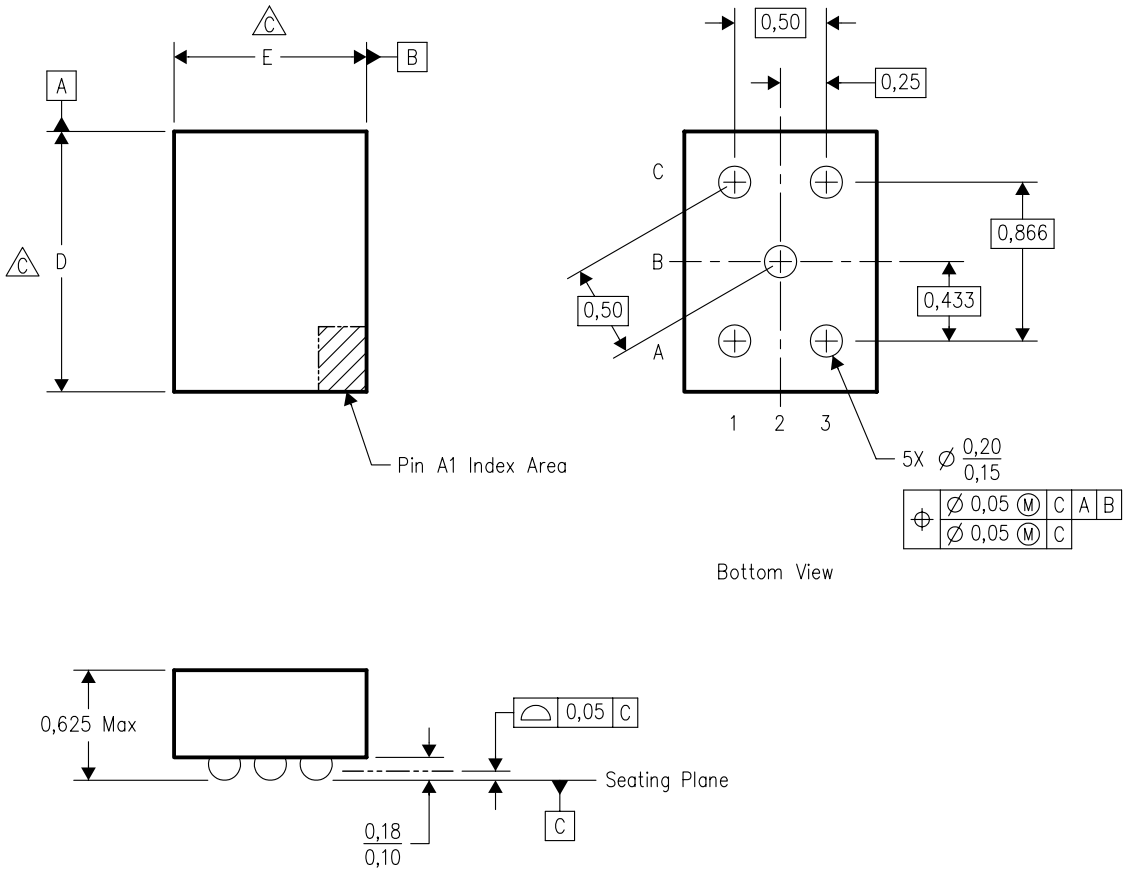
DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4073253–5/H 10/2003

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

YEQ (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



4205338/C 04/2004

Notes:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Devices in this YEQ package can have dimension D ranging from 1.17 to 1.67 and dimension E ranging from 0.80 to 1.30. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
D. NanoStar™ package configuration.
E. This package contains tin–lead (SnPb) balls. Refer to the 5 YZQ package (drawing 4205677) for lead–free balls.

NanoStar is a trademark of Texas Instruments.

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