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#### SLPS210B-AUGUST 2009-REVISED OCTOBER 2010

## P-Channel NexFET<sup>™</sup> Power MOSFET

Check for Samples: CSD25301W1015

### **FEATURES**

- Ultra Low Qg and Qgd
- Small Footprint
- Low Profile 0.62mm Height
- **Pb Free**
- **RoHS Compliant**
- **Halogen Free**
- CSP 1 × 1.5 mm Wafer Level Package

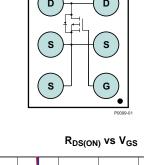
#### **APPLICATIONS**

- **Battery Management**
- Load Switch
- **Battery Protection**

### DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

### **Top View** D D s s S G •



#### 300 $R_{DS(on)}$ – On-State Resistance – m $\Omega$ $I_D = -1A$ 250 200 $T_C = 125^{\circ}C$ 150 100 50 $T_C = 25^{\circ}C$ 0 0 2 3 4 5 6 1 -V<sub>GS</sub> - Gate to Source Voltage - V G006

#### **PRODUCT SUMMARY**

V <sub>DS</sub>	Drain to Source Voltage	-20		V
Qg	Gate Charge Total (4.5V)	1.9		nC
Q <sub>gd</sub>	Gate Charge Gate to Drain	0.4		nC
		$V_{GS} = -1.5V$	175	mΩ
R <sub>DS(on)</sub>	Drain to Source On Resistance	$V_{GS} = -2.5V$	80	mΩ
		$V_{GS} = -4.5V$	62	mΩ
V <sub>GS(th)</sub>	Voltage Threshold	-0.75		V

#### **ORDERING INFORMATION**

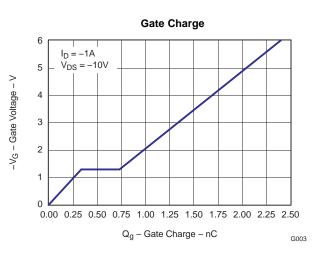
Device	Package	Media	Qty	Ship
CSD25301W1015	1 × 1.5 Wafer Level Package	7-inch reel	3000	Tape and Reel

#### **ABSOLUTE MAXIMUM RATINGS**

$T_A = 25^{\circ}C$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±8	V
I <sub>D</sub>	Continuous Drain Current, $T_C = 25^{\circ}C^{(1)}$	-2.2	А
I <sub>DM</sub>	Pulsed Drain Current, $T_A = 25^{\circ}C^{(2)}$	-8.8	А
PD	Power Dissipation <sup>(1)</sup>	1.5	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

(1)  $R_{\theta JA} = 85^{\circ}C/W$  on  $1in^2$  Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤300µs, duty cycle ≤2%



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

# ELECTRICAL CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static C	haracteristics		ŧ			
BV <sub>DSS</sub>	Drain to Source Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
I <sub>DSS</sub>	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = -16V$			-1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 8V$			-100	nA
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-0.4	-0.75	-1	V
		$V_{GS} = -1.5V, I_D = -1A$		175	220	mΩ
R <sub>DS(on)</sub>	Drain to Source On Resistance	$V_{GS} = -2.5V, I_D = -1A$		80	100	mΩ
		$V_{GS} = -4.5V, I_D = -1A$		62	75	mΩ
9 <sub>fs</sub>	Transconductance	$V_{DS} = -10V, I_D = -1A$		5.8		S
Dynamic	Characteristics					
C <sub>ISS</sub>	Input Capacitance			210	270	pF
C <sub>OSS</sub>	Output Capacitance	$V_{GS} = 0V, V_{DS} = -10V, f = 1MHz$		90	120	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			30	40	pF
Qg	Gate Charge Total (-4.5V)			1.9	2.5	nC
Q <sub>gd</sub>	Gate Charge Gate to Drain	V_DS = -10V. ID = -1A		0.4		nC
Q <sub>gs</sub>	Gate Charge Gate to Source	$v_{DS} = -10v, I_D = -1A$		0.35		nC
Qg(th)	Gate Charge at Vth			0.17		nC
Q <sub>OSS</sub>	Output Charge	$V_{DS} = -9.8V, V_{GS} = 0V$		1.7		nC
t <sub>d(on)</sub>	Turn On Delay Time			4		ns
t <sub>r</sub>	Rise Time	$V_{DS} = -10V, V_{GS} = -4.5V, I_{D} = -1A$		2		ns
t <sub>d(off)</sub>	Turn Off Delay Time	$R_{G} = 20\Omega$		29		ns
t <sub>f</sub>	Fall Time			12		ns
Diode C	haracteristics					
$V_{SD}$	Diode Forward Voltage	$I_{\rm S} = -1$ A, $V_{\rm GS} = 0$ V		-0.75	-1	V
Q <sub>rr</sub>	Reverse Recovery Charge	$V_{dd}$ = -9.8V, I <sub>F</sub> = -1A, di/dt = 200A/µs		0.9		nC
t <sub>rr</sub>	Reverse Recovery Time	$V_{dd}$ = -9.8V, I <sub>F</sub> = -1A, di/dt = 200A/µs		8.2	-	ns

### THERMAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

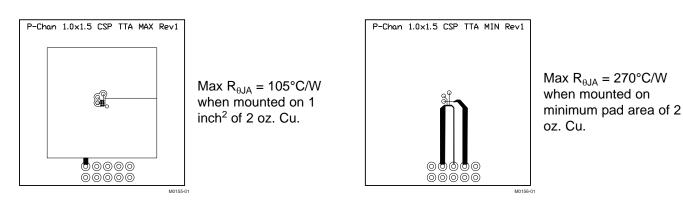
PARAMETER		MIN	TYP	MAX	UNIT
в	Thermal Resistance Junction to Ambient (Minimum Cu area)			270	°C/W
R <sub>θJA</sub>	Thermal Resistance Junction to Ambient (1 in <sup>2</sup> Cu area)			105	°C/W



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### **TYPICAL MOSFET CHARACTERISTICS**

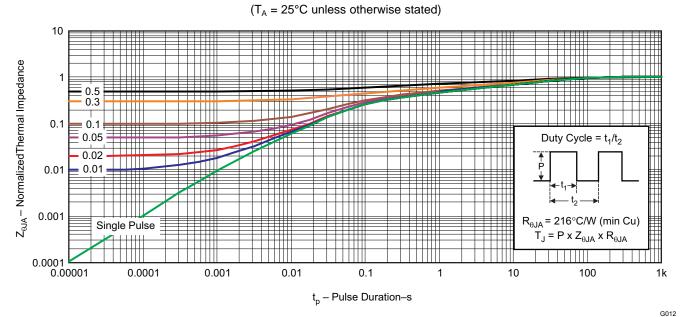


Figure 1. Transient Thermal Impedance

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ISTRUMENTS

**EXAS** 

#### **TYPICAL MOSFET CHARACTERISTICS (continued)**

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

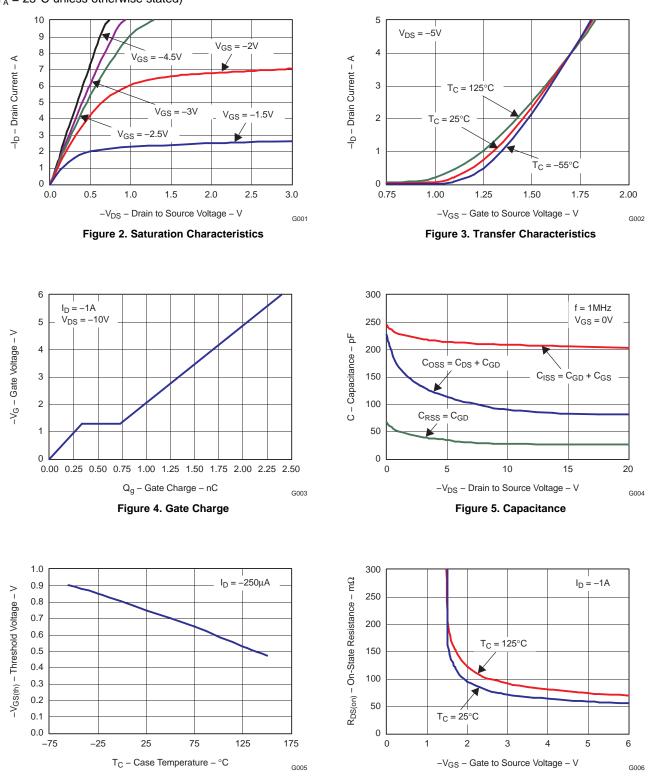


Figure 6. Threshold Voltage vs. Temperature

Figure 7. On Resistance vs. Gate Voltage



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**TYPICAL MOSFET CHARACTERISTICS (continued)** 

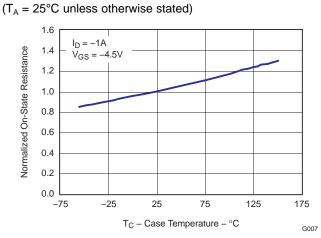


Figure 8. On Resistance vs. Temperature

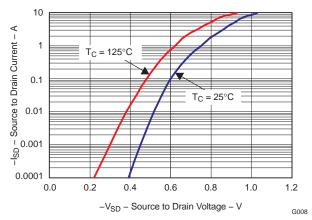
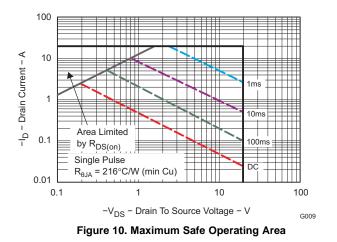
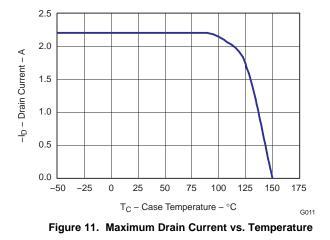


Figure 9. Typical Diode Forward Voltage

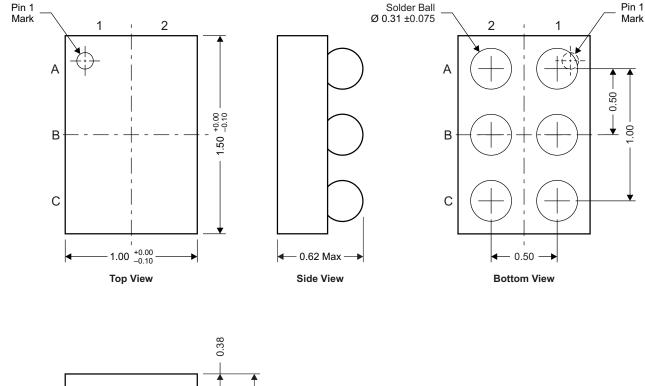




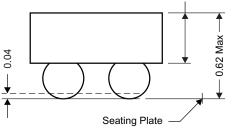
TEXAS INSTRUMENTS

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#### **MECHANICAL DATA**



### CSD25301W1015 Package Dimensions



**Front View** 

M0157-01

NOTE: All dimensions are in mm (unless otherwise specified)

Pinout				
POSITION	DESIGNATION			
C1, C2	Drain			
A1	Gate			
A2, B1, B2	Source			

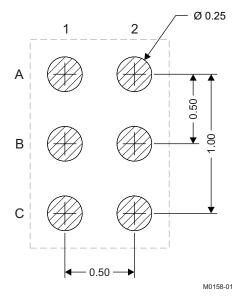
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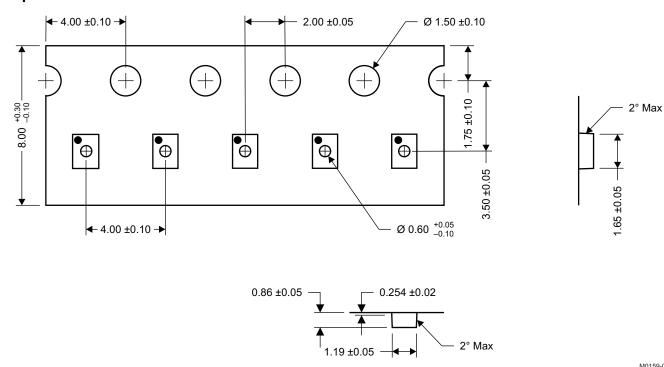


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#### Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)



#### **Tape and Reel Information**

NOTE: All dimensions are in mm (unless otherwise specified)



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### **REVISION HISTORY**

Changes from Original (August 2009) to Revision A	
• Replaced incorrect label: $R_{\theta JC}$ with $R_{\theta JA}$ in the THERMAL CHARACTERISTICS table.	2
Changes from Revision A (August 2010) to Revision B	Page
Deleted the Package Marking Information section	

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