

# TPIC6273 POWER LOGIC OCTAL D-TYPE LATCH

SLIS011A – APRIL 1992 – REVISED OCTOBER 1995

- Low  $r_{DS(on)}$  . . . 1.3  $\Omega$  Typ
- Avalanche Energy . . . 75 mJ
- Eight Power DMOS Transistor Outputs of 250-mA Continuous Current
- 1.5-A Pulsed Current Per Output
- Output Clamp Voltage up to 45 V
- Low Power Consumption

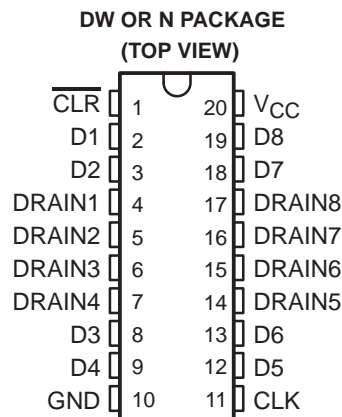
## description

The TPIC6273 is a monolithic high-voltage high-current power logic octal D-type latch with DMOS transistor outputs designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

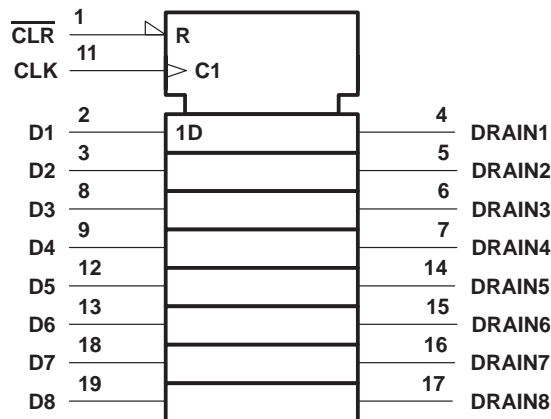
The TPIC6273 contains eight positive-edge-triggered D-type flip-flops with a direct clear input. Each flip-flop features an open-drain power DMOS transistor output.

When clear ( $\overline{CLR}$ ) is high, information at the D inputs meeting the setup time requirements is transferred to the DRAIN outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous  $\overline{CLR}$  is provided to turn all eight DMOS-transistor outputs off.

The TPIC6273 is characterized for operation over the operating case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .



## logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

**FUNCTION TABLE  
(each channel)**

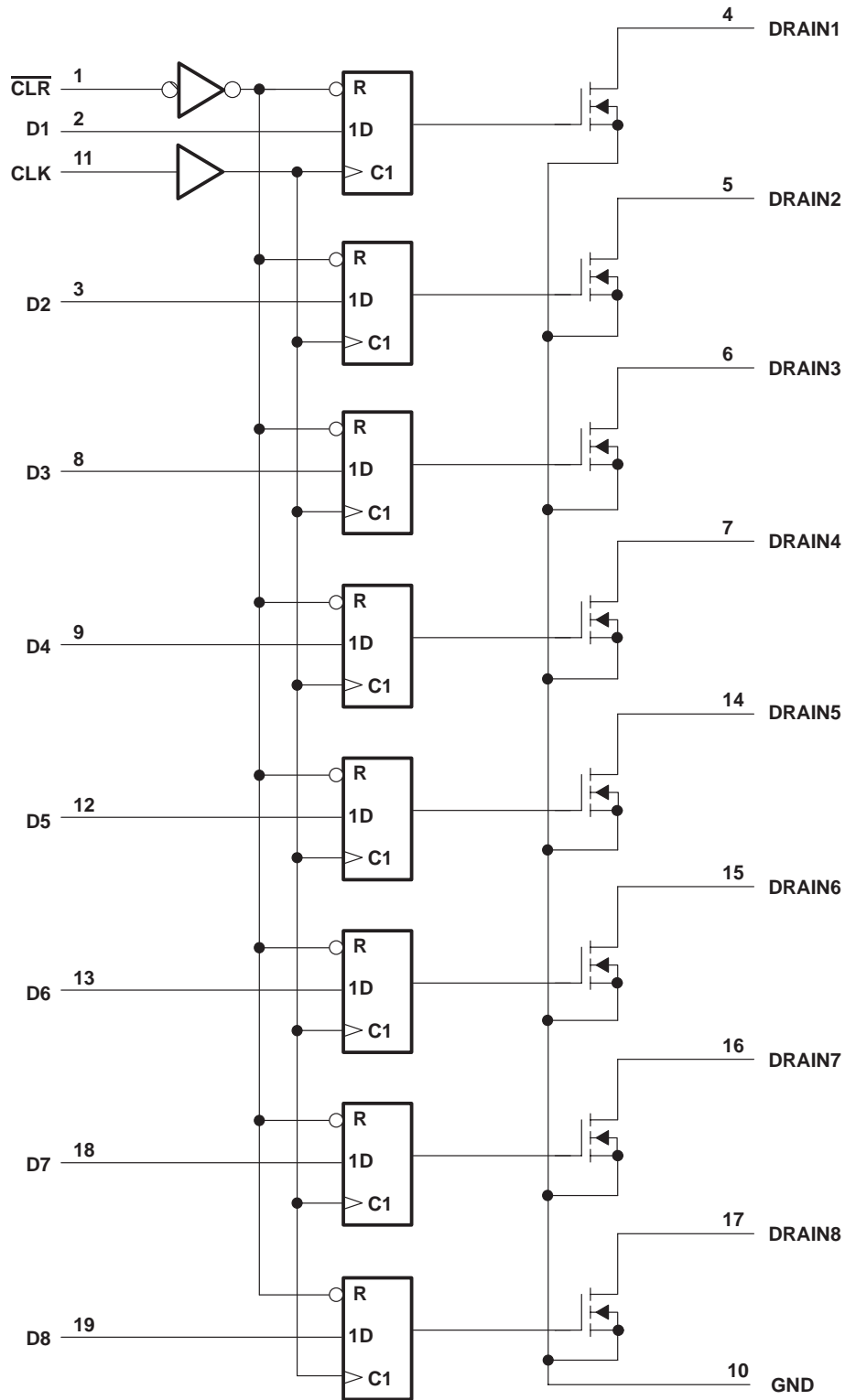
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	DRAIN
L	X	X	H
H	$\uparrow$	H	L
H	$\uparrow$	L	H
H	L	X	Latched

H = high level, L = low level, X = irrelevant

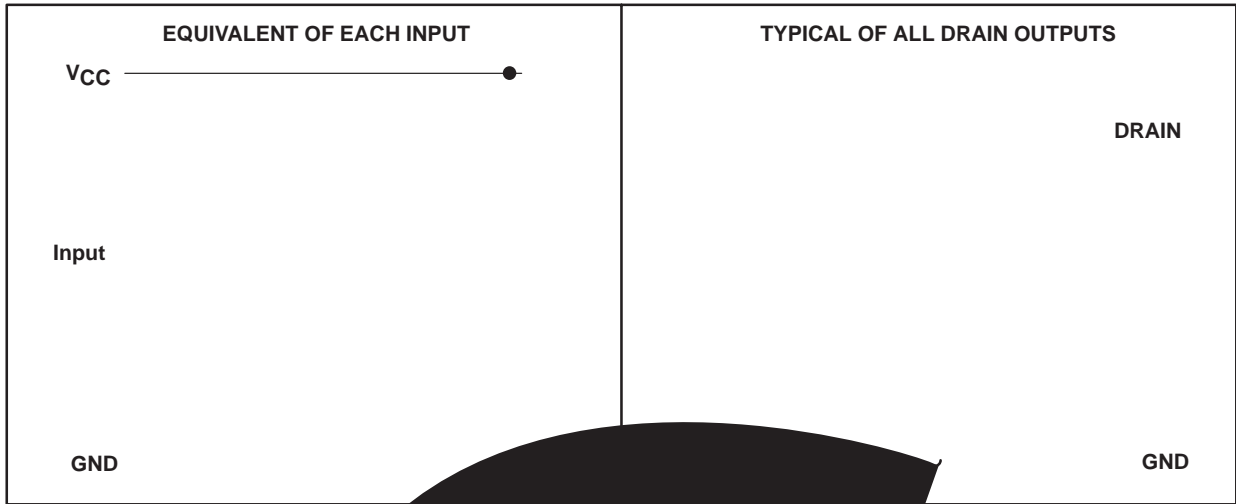
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## logic diagram (positive logic)



schematic of inputs and outputs





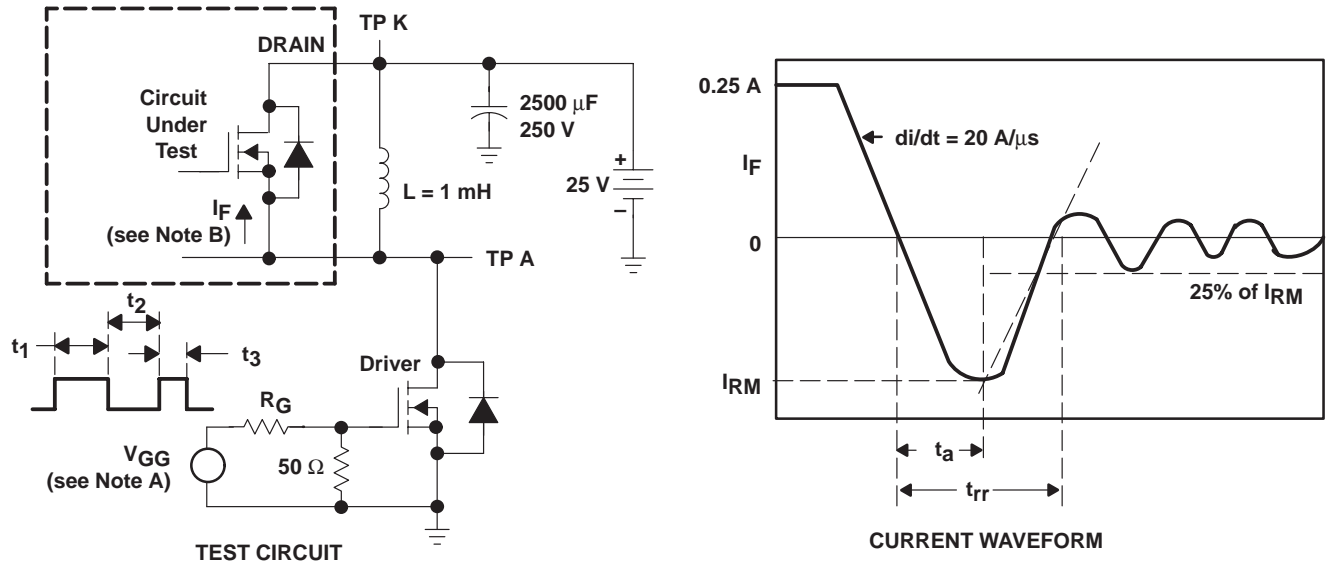
**INSTRUMENTS**



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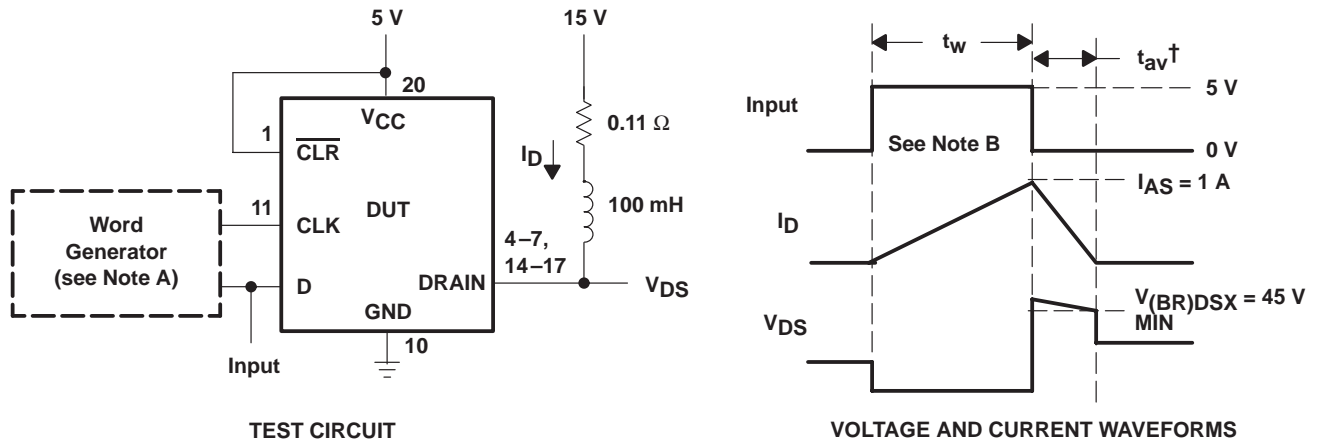
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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The  $V_{GG}$  amplitude and  $R_G$  are adjusted for  $di/dt = 20 \text{ A}/\mu\text{s}$ . A  $V_{GG}$  double-pulse train is used to set  $I_F = 0.25 \text{ A}$ , where  $t_1 = 10 \mu\text{s}$ ,  $t_2 = 7 \mu\text{s}$ , and  $t_3 = 3 \mu\text{s}$ .  
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode

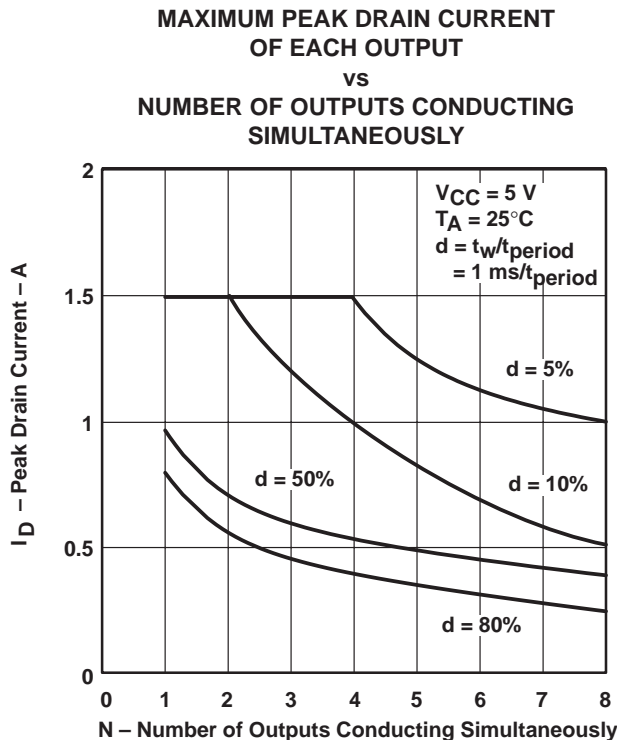
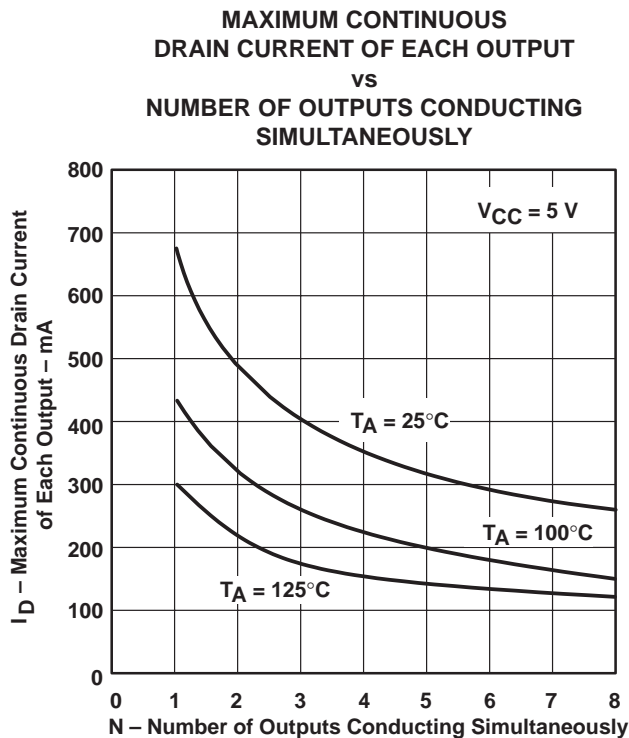
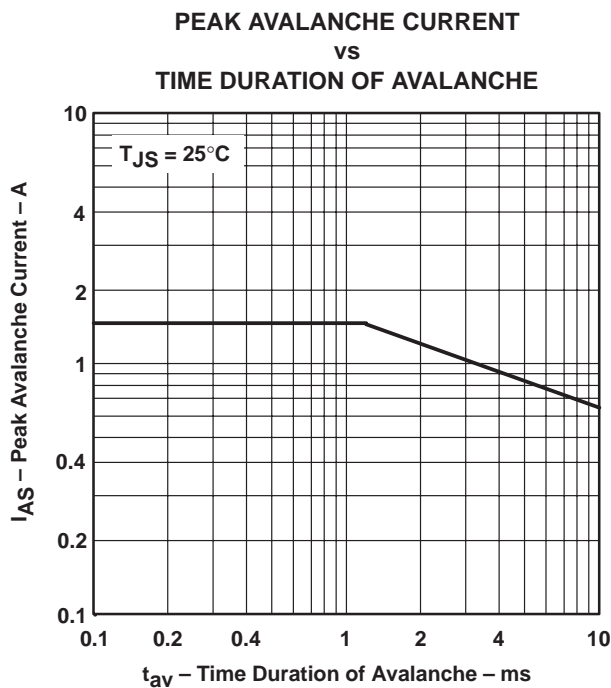


† Non-JEDEC symbol for avalanche ftime.

- NOTES: A. The word generator A has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
B. Input pulse duration,  $t_w$ , is increased until peak current  $I_{AS} = 1 \text{ A}$ .  
Energy test is defined as  $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 75 \text{ mJ}$ , where  $t_{av}$  = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

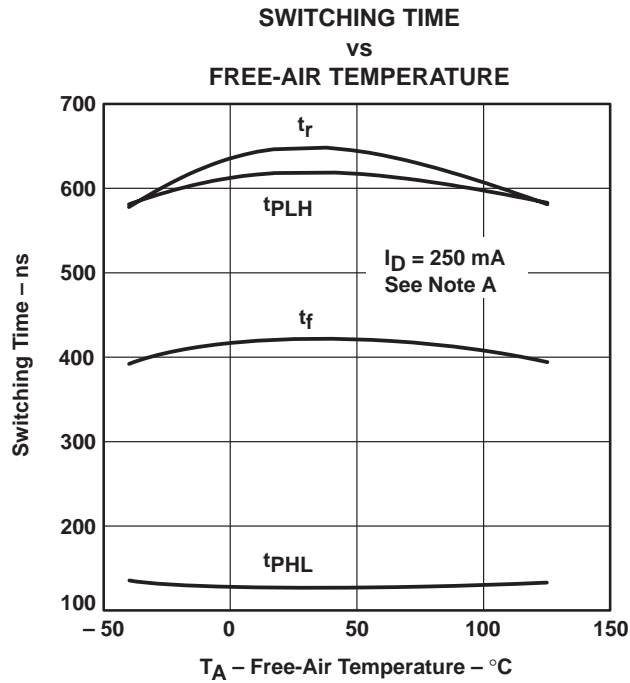
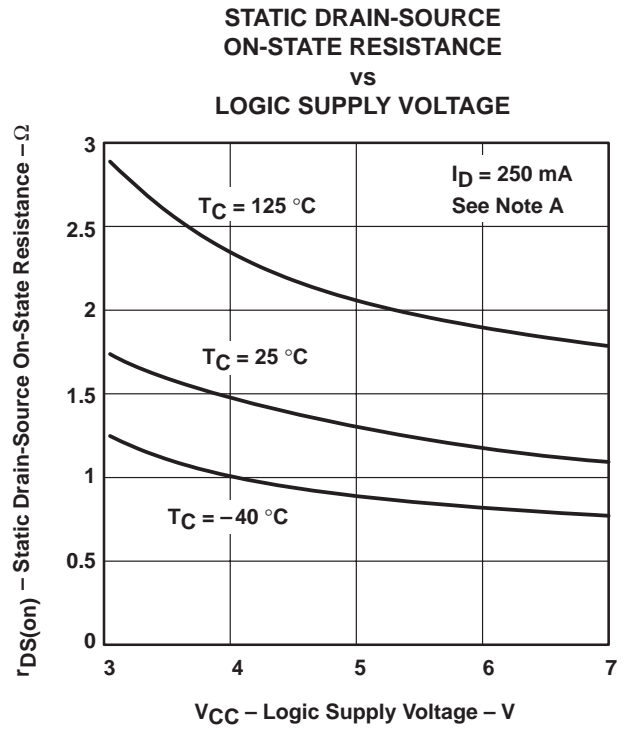
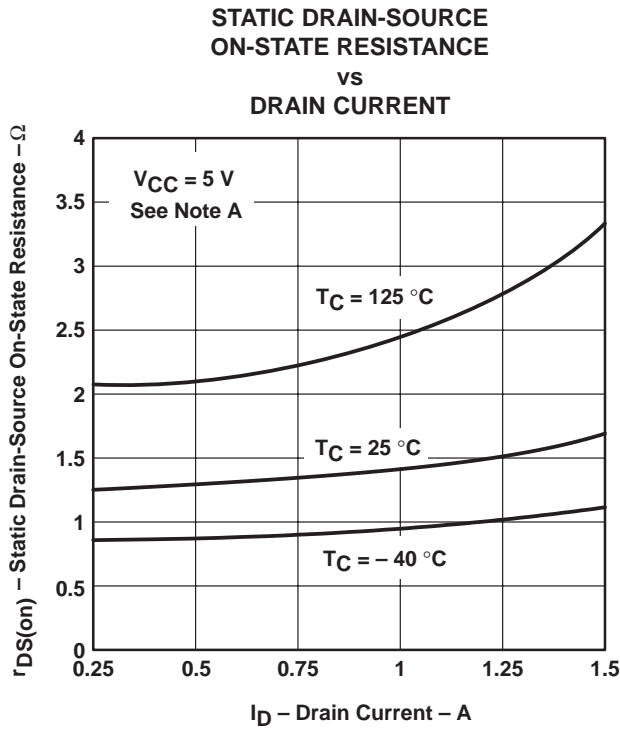
TYPICAL CHARACTERISTICS



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## TYPICAL CHARACTERISTICS



NOTE A: Technique should limit  $T_J - T_C$  to 10°C maximum.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPIC6273DW	ACTIVE	SOIC	DW	20	25	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPIC6273DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPIC6273DWR	ACTIVE	SOIC	DW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPIC6273DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPIC6273N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

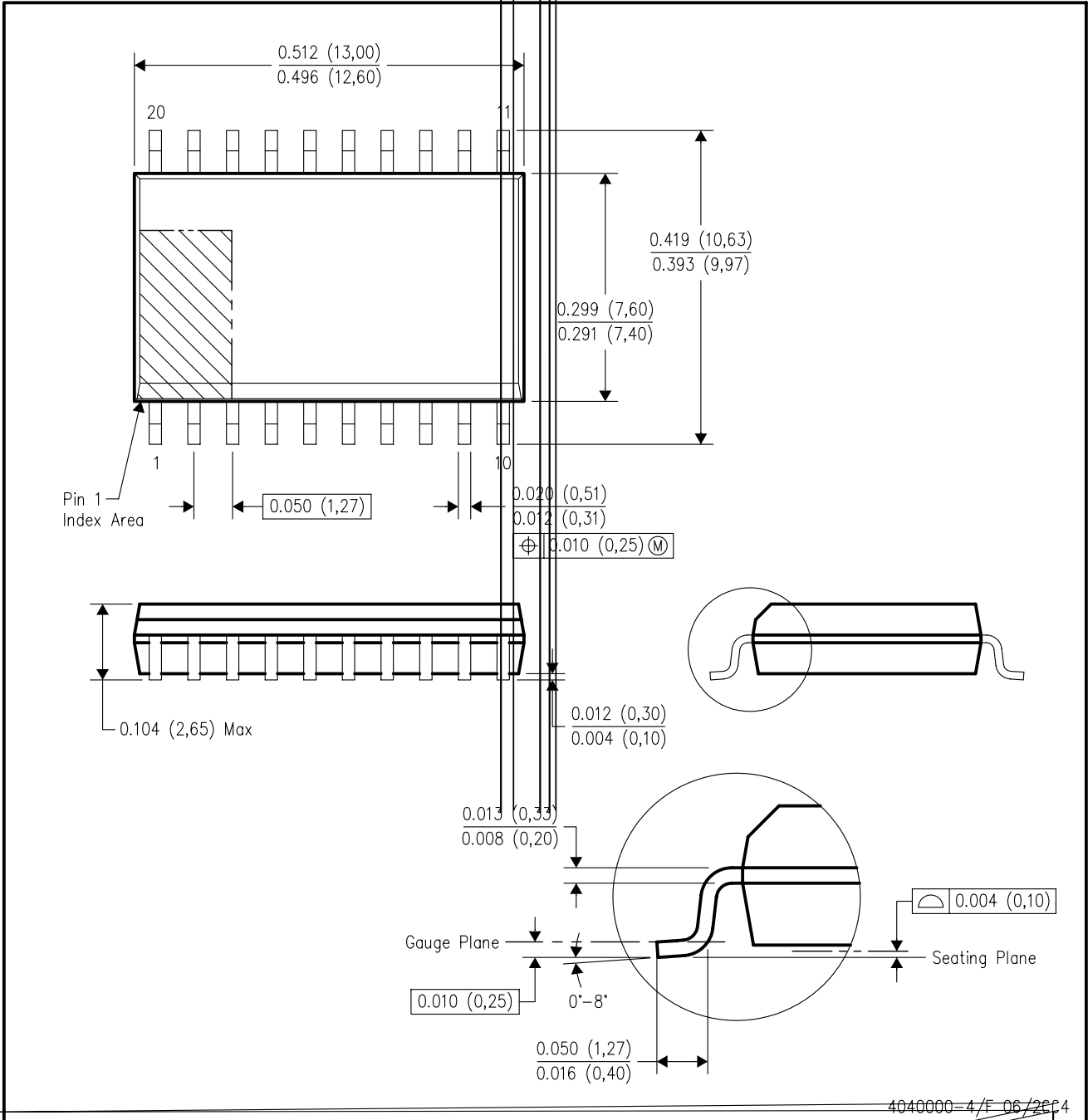
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-4/F 06/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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