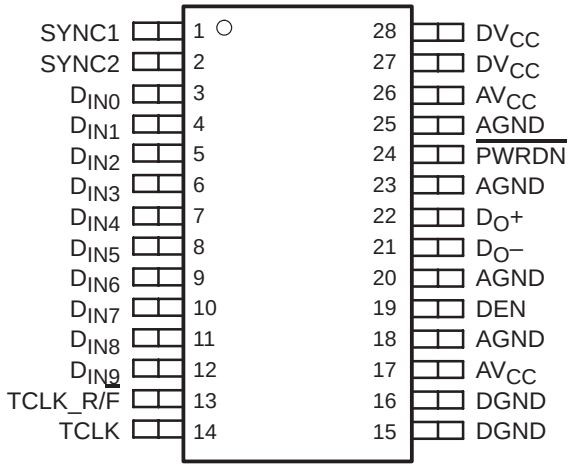
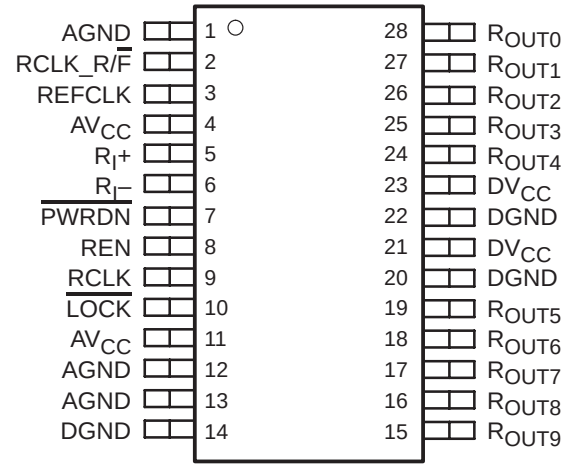
- **100-Mbps to 400-Mbps Serial LVDS Data Payload Bandwidth at 10-MHz to 40-MHz System Clock**
- **Pin-Compatible Superset of NSM DS92LV1021/DS92LV1212**
- **Chipset (Serializer/Deserializer) Power Consumption <350 mW (Typ) at 40 MHz**
- **Synchronization Mode for Faster Lock**
- **Lock Indicator**
- **No External Components Required for PLL**
- **Low-Cost 28-Pin SSOP Package**
- **Industrial Temperature Qualified, T_A = –40°C to 85°C**
- **Programmable Edge Trigger on Clock (Rising or Falling Edge)**
- **Flow-Through Pinout for Easy PCB Layout**

SN65LV1021
Serializer



SN65LV1212
Deserializer



description

The SN65LV1021 serializer and SN65LV1212 deserializer comprise a 10-bit serdes chipset designed to transmit and receive serial data over LVDS differential backplanes at equivalent parallel word rates from 10 MHz to 40 MHz. Including overhead, this translates into a serial data rate between 120-Mbps and 480-Mbps payload-encoded throughput.

Upon power up, the chipset link can be initialized via a synchronization mode with internally generated SYNC patterns, or the deserializer can be allowed to synchronize to random data. By using the synchronization mode, the deserializer establishes lock within specified, shorter time parameters.

The device can be entered into a power-down state when no data transfer is required. Alternatively, a mode is available to place the output pins in the high-impedance state without losing PLL lock.

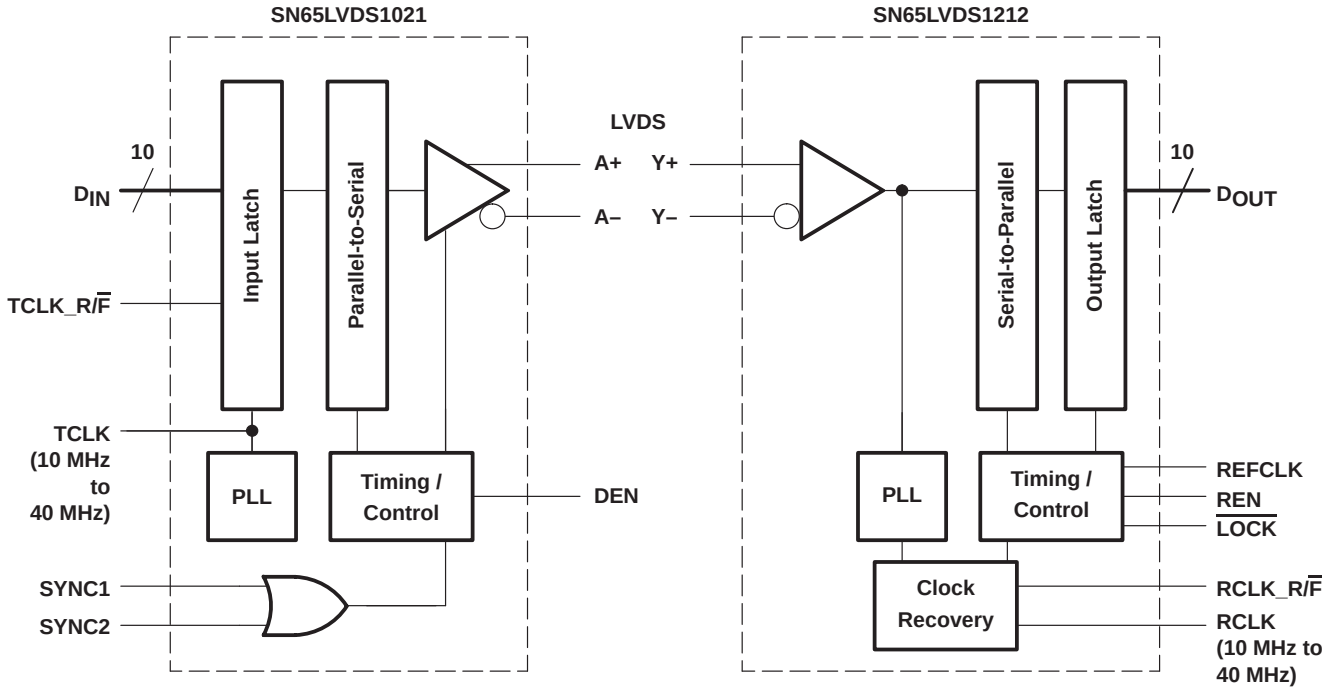
The SN65LV1021 and SN65LV1212 are characterized for operation over ambient air temperature of –40°C to 85°C.

ORDERING INFORMATION

DEVICE	PART NUMBER
Serializer	SN65LV1021DB
Deserializer	SN65LV1212DB

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

block diagrams



functional description

The SN65LV1021 and SN65LV1212 are a 10-bit serializer/deserializer chipset designed to transmit data over differential backplanes or unshielded twisted pair (UTP) at clock speeds from 10 MHz to 40 MHz. The chipset has five states of operation: initialization mode, synchronization mode, data transmission mode, power-down mode, and high-impedance mode. The following sections describe each state of operation.

initialization mode

Initialization of both devices must occur before data transmission can commence. Initialization refers to synchronization of the serializer and deserializer PLLs to local clocks.

When V_{CC} is applied to the serializer and/or deserializer, the respective outputs enter the high-impedance state, while on-chip power-on circuitry disables internal circuitry. When V_{CC} reaches 2.45 V, the PLL in each device begins locking to a local clock. For the serializer, the local clock is the transmit clock (TCLK) provided by an external source. For the deserializer, a local clock must be applied to the REFCLK pin. The serializer outputs remain in the high-impedance state, while the PLL locks to the TCLK.

functional description (continued)

synchronization mode

The deserializer PLL must synchronize to the serializer in order to receive valid data. Synchronization can be accomplished in one of two ways:

- **Rapid Synchronization:** The serializer has the capability to send specific SYNC patterns consisting of six ones and six zeros switching at the input clock rate. The transmission of SYNC patterns enables the deserializer to lock to the serializer signal within a deterministic time frame. This transmission of SYNC patterns is selected via the SYNC1 and SYNC2 inputs on the serializer. Upon receiving valid a SYNC1 or SYNC2 pulse (wider than 6 clock cycles), 1026 cycles of SYNC pattern are sent.

When the deserializer detects edge transitions at the LVDS input, it attempts to lock to the embedded clock information. The deserializer $\overline{\text{LOCK}}$ output remains high while its PLL locks to the incoming data or SYNC patterns present on the serial input. When the deserializer locks to the LVDS data, the $\overline{\text{LOCK}}$ output goes low. When $\overline{\text{LOCK}}$ is low, the deserializer outputs represent incoming LVDS data. One approach is to tie the deserializer $\overline{\text{LOCK}}$ output directly to SYNC1 or SYNC2.

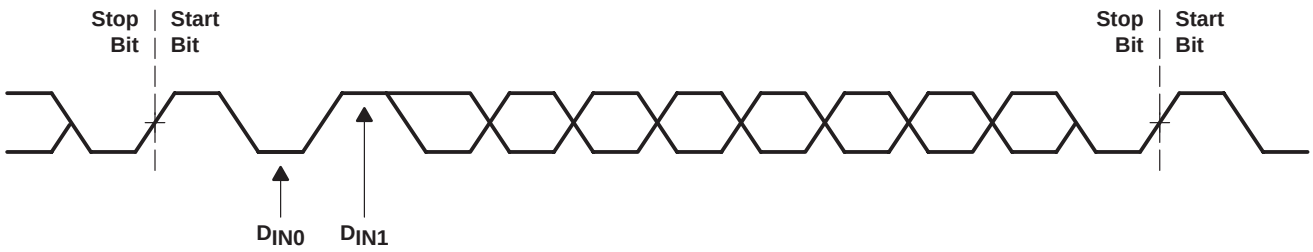
- **Random-Lock Synchronization:** The deserializer can attain lock to a data stream without requiring the serializer to send special SYNC patterns. This allows the SN65LV1212 to operate in open-loop applications. Equally important is the deserializer's ability to support hot insertion into a running backplane. In the open-loop or hot-insertion case, it is assumed the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, the exact lock time cannot be predicted. The primary constraint on the random lock time is the initial phase relation between the incoming data and the REFCLK when the deserializer powers up.

The data contained in the data stream can also affect lock time. If a specific pattern is repetitive, the deserializer could enter false lock—falsely recognizing the data pattern as the start/stop bits. This is referred to as repetitive multitransition (RMT); see Figure 1 for RMT examples. RMT occurs when more than one low-high transition takes place per clock cycle over multiple cycles. In the worst case, the deserializer could become locked to the data pattern rather than the clock. Circuitry within the deserializer can detect that the possibility of false lock exists. Upon detection, the circuitry prevents the $\overline{\text{LOCK}}$ output from becoming active until the potential false lock pattern changes. Notice that the RMT pattern only affects the deserializer lock time, and once the deserializer is in lock, the RMT pattern does not affect the deserializer state as long as the same data boundary happens each cycle. The deserializer does not go into lock unitil it finds a unique four consecutive cycles of data boundary (stop/start bits) at the same position.

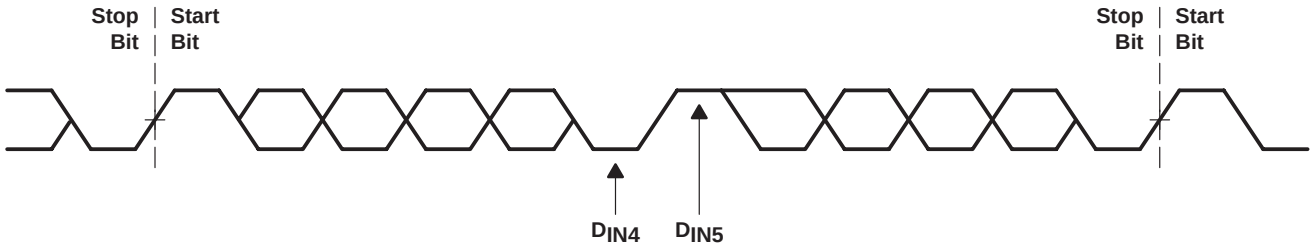
The deserializer stays in lock until it cannot detect the same data boundary (stop/start bits) for four consecutive cycles. Then the desiralizer goes out of lock and hunts for the new data boundary (stop/start bits). In the event of loss of synchronization, the $\overline{\text{LOCK}}$ pin output goes high and the outputs (including RCLK) enter a high-impedance state. The user's system should monitor the $\overline{\text{LOCK}}$ pin in order to detect a loss of synchronization. Upon detection of loss of lock, sending sync patterns for resynchronization is desirable if reestablishing lock within a specific time is critical. However, the deserializer can lock to random data as previously noted.

synchronization mode (continued)

D_{IN0} Held Low and D_{IN1} Held High



D_{IN4} Held Low and D_{IN5} Held High



D_{IN8} Held Low and D_{IN9} Held High

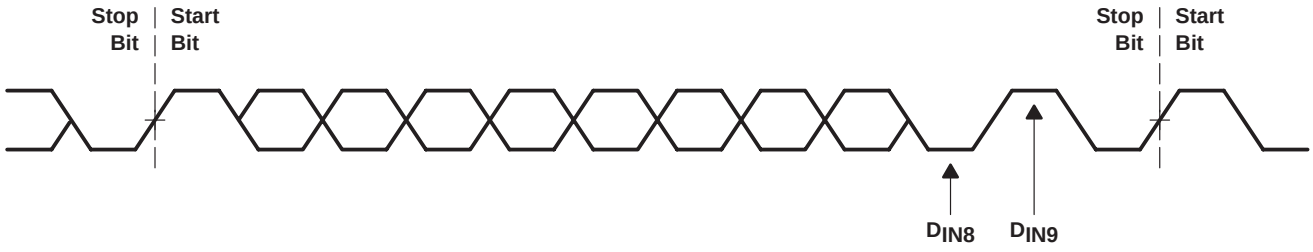


Figure 1. RMT Pattern Examples

data transmission mode

After initialization and synchronization, the serializer accepts parallel data from inputs D_{IN0}–D_{IN9}. The serializer uses the TCLK input to latch the incoming data. The TCLK_R/$\overline{F}$ pin selects which edge the serializer uses to strobe incoming data. If either of the SYNC inputs is high for 6 TCLK cycles, the data at D_{IN0}–D_{IN9} is ignored regardless of the clock edge selected and 1026 cycles of SYNC pattern are sent.

After determining which clock edge to use, a start and stop bit, appended internally, frames the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

The serializer transmits serialized data and appended clock bits (10+2 bits) from the serial data output (DO±) at 12 times the TCLK frequency. For example, if TCLK is 10 MHz, the serial rate is $10 \times 12 = 120$ Mbps. Because only 10 bits are input data, the useful data rate is 10 times the TCLK frequency. For instance, if TCLK = 12 MHz, the useful data rate is $10 \times 12 = 120$ Mbps. The data source, which provides TCLK, must be in the range of 10 MHz to 40 MHz.

functional description (continued)

The serializer outputs (DO±) can drive point-to-point connections or limited multipoint or multidrop backplanes. The outputs transmit data when the enable pin (DEN) is high, $\overline{\text{PWRDN}}$ is high, and SYNC1 and SYNC2 are low. When DEN is driven low, the serializer output pins enter the high-impedance state.

Once the deserializer has synchronized to the serializer, the $\overline{\text{LOCK}}$ pin transitions low. The deserializer locks to the embedded clock and uses it to recover the serialized data. R_{OUTx} data is valid when $\overline{\text{LOCK}}$ is low, otherwise $R_{OUT0}-R_{OUT9}$ is invalid. The $R_{OUT0}-R_{OUT9}$ data is strobed out by RCLK. The specific RCLK edge polarity to be used is selected by the RCLK_R/$\overline{\text{F}}$ input. The $R_{OUT0}-R_{OUT9}$, $\overline{\text{LOCK}}$ and RCLK outputs can drive a maximum of three CMOS input gates (15-pF load, total for all three) with a 40-MHz clock.

power down

When no data transfer is required, the power-down mode can be used. The serializer and deserializer use the power-down mode, a low-power sleep mode, to reduce power consumption. The deserializer enters power down when you drive $\overline{\text{PWRDN}}$ and REN low. The serializer enters power down when the $\overline{\text{PWRDN}}$ is driven low. In power down, the PLL stops and the outputs enter a high-impedance state, which disables load current and reduces supply current to the milliampere range. To exit power down, you must drive the $\overline{\text{PWRDN}}$ pin high.

Before valid data exchanges between the serializer and deserializer can resume, you must reinitialize and resynchronize the devices to each other. Initialization of the serializer takes 1026 TCLK cycles. The deserializer initializes and drives $\overline{\text{LOCK}}$ high until lock to the LVDS clock occurs.

high-impedance mode

The serializer enters the high-impedance mode when the DEN pin is driven low. This puts both driver output pins (DO+ and DO–) into a high-impedance state. When you drive DEN high, the serializer returns to its previous state, as long as all other control pins remain static (SYNC1, SYNC2, $\overline{\text{PWRDN}}$, TCLK_R/$\overline{\text{F}}$). When the REN pin is driven low, the deserializer enters high-impedance mode. Consequently, the receiver output pins ($R_{OUT0}-R_{OUT9}$) and RCLK are placed into the high-impedance state. The $\overline{\text{LOCK}}$ output remains active, reflecting the state of the PLL.

Deserializer Truth Table

INPUTS		OUTPUTS		
$\overline{\text{PWRDN}}$	REN	ROUT[0:9]	$\overline{\text{LOCK}}$	RCLK
H	H	Z	H	Z
H	H	Active	L	Active
L	X	Z	Z	Z
H	L	Z	Active	Z

NOTES: 1. $\overline{\text{LOCK}}$ output reflects the state of the deserializer with regard to the selected data stream.
2. RCLK active indicates the RCLK is running if the deserializer is locked. The timing of RCLK with respect to ROUT is determined by RCLK_R/$\overline{\text{F}}$.
3. ROUT and RCLK are 3-stated when $\overline{\text{LOCK}}$ is asserted high.

Terminal Functions

serializer

PIN	NAME	DESCRIPTION
1, 2	SYNC1, SYNC2	LVTTL logic inputs SYNC1 and SYNC2 are ORed together. When at least one of the two pins is asserted high for 6 cycles of TCLK, the serializer initiates transmission of a minimum 1026 SYNC patterns. If after completion of transmission of 1026 patterns SYNC continues to be asserted, then the transmission continues until SYNC is driven low and if the time SYNC holds > 6 cycles, another 1026 SYNC pattern transmission initiates.
3–12	D_{IN0}–D_{IN9}	Parallel LVTTL data inputs
13	TCLK_R/$\overline{F}$	LVTTL logic input. Low selects a TCLK falling-edge data strobe; high selects a TCLK rising-edge data strobe.
14	TCLK	LVTTL-level reference clock input. The SN65LV1021 accepts a 10-MHz to 40-MHz clock. TCLK strobes parallel data into the input latch and provides a reference frequency to the PLL.
15, 16	DGND	Digital circuit ground
18, 20, 23, 25	AGND	Analog circuit ground (PLL and analog circuits)
17, 26	AV_{CC}	Analog circuit power supply (PLL and analog circuits)
19	DEN	LVTTL logic input. Low puts the LVDS serial output into the high-impedance state. High enables serial data output.
21	D_O–	Inverting LVDS differential output
22	D_O+	Noninverting LVDS differential output
27, 28	DV_{CC}	Digital circuit power supply
24	$\overline{PWRDN}$	LVTTL logic input. Asserting this pin low turns off the PLL and places the outputs into the high-impedance state, putting the device into a low-power mode.

deserializer

PIN	NAME	DESCRIPTION
3	REFCLK	LVTTL logic input. Use this pin to supply a REFCLK signal for the internal PLL frequency.
15–19, 24–28	R_{OUT0}–R_{OUT9}	Parallel LVTTL data outputs
2	RCLK_R/$\overline{F}$	LVTTL logic input. Low selects an RCLK falling-edge data strobe; high selects an RCLK rising-edge data strobe.
9	RCLK	LVTTL-level output recovered clock. Use RCLK to strobe R_{OUTx}.
14, 20, 22	DGND	Digital circuit ground
1, 12, 13	AGND	Analog circuit ground (PLL and analog circuits)
4, 11	AV_{CC}	Analog circuit power supply (PLL and analog circuits)
8	REN	LVTTL logic input. Low places R_{OUT0}–R_{OUT9}, $\overline{LOCK}$, and RCLK in the high-impedance state.
5	R_I+	Serial data input. Noninverting LVDS differential input
6	R_I–	Serial data input. Inverting LVDS differential input
10	$\overline{LOCK}$	LVTTL-level output. $\overline{LOCK}$ goes low when the deserializer PLL locks onto the embedded clock edge.
21, 23	DV_{CC}	Digital circuit power supply
7	$\overline{PWRDN}$	LVTTL logic input. Asserting this pin low turns off the PLL and places outputs into a high-impedance state, putting the device into a low-power mode.

absolute maximum ratings (unless otherwise noted)†

V_{CC} to GND . . . . . –0.3 V to 4 V
LVTTL input voltage . . . . . –0.3 V to (V_{CC} + 0.3 V)
LVTTL output voltage . . . . . –0.3 V to (V_{CC} + 0.3 V)
LVDS receiver input voltage . . . . . –0.3 V to 3.9 V
LVDS driver output voltage . . . . . –0.3 V to 3.9 V
LVDS output short circuit duration . . . . . Continuous
Electrostatic discharge: HBM . . . . . up to 6 kV
MM . . . . . up to 200 V
Junction temperature . . . . . 150°C
Storage temperature . . . . . – 65°C to 150°C
Lead temperature (soldering, 4 seconds) . . . . . 260°C
Maximum package power dissipation, T_A = 25°C . . . . . 1.27 W
Package derating . . . . . 10.3 mW/°C above 25°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}‡	3	3.3	3.6	V
Receiver input voltage range	0		2.4	V
Receiver input common mode range, V_{CM}	$\frac{V_{ID}}{2}$		$2.4 - \left(\frac{V_{ID}}{2}\right)$	V
Supply noise voltage			100	mV_{P-P}
Operating free-air temperature, T_A	–40	25	85	°C

‡ By design, DVCC and AVCC are separated internally and does not matter what the difference is for $|DVCC–AVCC|$, as long as both are within 3 V to 3.6 V.

electrical characteristics over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SERIALIZER LVCMOS/LVTTL DC SPECIFICATIONS (see Note 4)							
V_{IH}	High-level input voltage			2		V_{CC}	V
V_{IL}	Low-level input voltage			GND		0.8	V
V_{CL}	Input clamp voltage	I_{CL} = –18 mA				–1.5	V
I_{IN}	Input current (see Note 5)	V_{IN} = 0 V or 3.6 V		–200	±100	200	µA
DESERIALIZER LVCMOS/LVTTL DC SPECIFICATIONS (see Note 6)							
V_{IH}	High-level input voltage			2		V_{CC}	V
V_{IL}	Low-level input voltage			GND		0.8	V
V_{CL}	Input clamp voltage	I_{CL} = –18 mA			–0.62	–1.5	V
I_{IN}	Input current	V_{IN} = 0 V or 3.6 V		–200		200	µA
V_{OH}	High-level output voltage	I_{OH} = –5 mA		2.2	3	V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 5 mA		GND	0.25	0.5	V
I_{OS}	Output short-circuit current	V_{OUT} = 0 V		–15	–47	–85	mA
I_{OZ}	High-impedance output current	$\overline{PWRDN}$ or REN = 0.8 V, V_{OUT} = 0 V or V_{CC}		–10	±1	10	µA
SERIALIZER LVDS DC SPECIFICATIONS (apply to pins DO+ and DO–)							
V_{OD}	Output differential voltage (DO+)–(DO–)	R_L = 27 Ω, See Figure 18		350	400		mV
ΔV_{OD}	Output differential voltage unbalance					35	mV
V_{OS}	Offset voltage			1.1	1.2	1.3	V
ΔV_{OS}	Offset voltage unbalance					35	mV
I_{OS}	Output short circuit current	D0 = 0 V, D_{INx} = high, $\overline{PWRDN}$ and DEN = 2.4 V			–10	–90	mA
I_{OZ}	High-impedance output current	$\overline{PWRDN}$ or DEN = 0.8 V, DO = 0 V or V_{CC}		–10	±1	10	µA
I_{OX}	Power-off output current	V_{CC} = 0 V, DO = 0 V or V_{CC}		–20	±1	20	µA
DESERIALIZER LVDS DC SPECIFICATIONS (apply to pins RI+ and RI–)							
V_{TH}	Differential threshold high voltage	V_{CM} = 1.1 V				50	mV
V_{TL}	Differential threshold low voltage			–50			mV
I_{IN}	Input current	V_{IN} = 2.4 V, V_{CC} = 3.6 V or 0 V		–10	±1	15	µA
		V_{IN} = 0 V, V_{CC} = 3.6 V or 0 V		–10	±0.05	10	
SERIALIZER SUPPLY CURRENT (applies to pins DVCC and AVCC)							
I_{CCD}	Serializer supply current, worst case	R_L = 27 Ω, See Figure 2	f = 40 MHz		40	50	mA
			f = 10 MHz		20	25	
I_{CCXD}	Serializer supply current, power down	$\overline{PWRDN}$ = 0.8 V			200	500	µA
DESERIALIZER SUPPLY CURRENT (applies to pins DVCC and AVCC)							
I_{CCR}	Deserializer supply current, worst case	C_L = 15 pF, See Figure 3	f = 40 MHz		63	75	mA
			f = 10 MHz		15	35	
I_{CCXR}	Deserializer supply current, power down	$\overline{PWRDN}$ = 0.8 V, REN = 0.8 V			0.36	1	mA

NOTES: 4. Apply to D_{IN0}–D_{IN9}, TCLK, $\overline{PWRDN}$, TCLK_R/$\overline{F}$, SYNC1, SYNC2, DEN
5. High I_{IN} values are due to pull-up and pull-down resistors on the inputs.
6. Apply to input pins $\overline{PWRDN}$, RCLK_R/$\overline{F}$, REN, REFCLK; apply to output pins R_{OUTx}, RCLK, $\overline{LOCK}$

serializer timing requirements for TCLK over recommended operating supply and temperature ranges (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TCP}	Transmit clock period		25	T	100	ns
t_{TCIH}	Transmit clock high time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit clock low time		0.4T	0.5T	0.6T	ns
$t_{t(CLK)}$	TCLK input transition time	See Figure 6		3	6	ns
t_{JIT}	TCLK input jitter				150	ps (RMS)

serializer switching characteristics over recommended operating supply and temperature ranges (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{TLH(L)}$	LVDS low-to-high transition time	R_L = 27 Ω, C_L = 10 pF to GND, See Figure 4		0.2	1	ns
$t_{THL(L)}$	LVDS high-to-low transition time			0.25	1	ns
$t_{su(DI)}$	D_{IN0}–D_{IN9} setup to TCLK	R_L = 27 Ω, C_L = 10 pF to GND, See Figure 7	1	0		ns
$t_{h(D)}$	D_{IN0}–D_{IN9} hold from TCLK		6.5	4.5		ns
$t_{d(HZ)}$	DO± high-to-high impedance state delay	R_L = 27 Ω, C_L = 10 pF to GND, See Figure 8		2.5	5	ns
$t_{d(LZ)}$	DO± low-to-high impedance state delay			2.5	5	ns
$t_{d(ZH)}$	DO± high-impedance state-to-high delay			2.5	10	ns
$t_{d(ZL)}$	DO± high-impedance state-to-low delay			2.7	10	ns
$t_{w(SP)}$	SYNC pulse duration	R_L = 27 Ω, See Figure 9 and Figure 10	$6 \times t_{TCP}$			ns
t_{PLD}	Serializer PLL lock time		$1026 \times t_{TCP}$			ns
$t_{d(S)}$	Serializer delay	R_L = 27 Ω, See Figure 11			$\frac{t_{TCP}}{2} + 3$	ns
$t_{(BIT)}$	Bus LVDS bit width	R_L = 27 Ω, C_L = 10 pF to GND		$t_{CLK}/12$		ns

deserializer timing requirements for REFCLK over recommended operating supply and temperature ranges (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RFCP}	REFCLK period		25	T	100	ns
t_{RFDC}	REFCLK duty cycle		40%	50%	60%	
$t_{t(RF)}$	REFCLK transition time			3	6	ns

deserializer switching characteristics over recommended operating supply and temperature ranges (unless otherwise specified)

PARAMETER		TEST CONDITIONS	PIN/FREQ	MIN	TYP	MAX	UNIT
t_{RCP}	Receiver out clock period	$t_{(RCP)} = t_{(TCP)}$ See Figure 11	RCLK	25		100	ns
$t_{TLH(C)}$	CMOS/TTL low-to-high transition time	C_L =15 pF, See Figure 5	R_{OUT0}–R_{OUT9}, $\overline{LOCK}$, RCLK		0.7	2.5	ns
$t_{THL(C)}$	CMOS/TTL high-to-low transition time				1.1	2.5	ns
$t_{d(D)}$	Deserializer delay, See Figure 12	Room temperature, 3.3 V	10 MHz	$2\times t_{RCP} + 9$		$2.833\times t_{RCP} + 14$	ns
			40 MHz	$2\times t_{RCP} + 6$		$2.833\times t_{RCP} + 10$	
$t_{su(ROS)}$	R_{OUT0}–R_{OUT9} setup data to RCLK	See Figure 13	RCLK	$0.4\times t_{RCP}$	$0.5\times t_{RCP}$		ns
$t_{(ROH)}$	R_{OUT0}–R_{OUT9} hold data to RCLK			$-0.4\times t_{RCP}$	$-0.5\times t_{RCP}$		
$t_{(RDC)}$	RCLK duty cycle			40%	50%	60%	
$t_{d(HZ)}$	High-to-high impedance state delay	See Figure 14	R_{OUT0}–R_{OUT9}, $\overline{LOCK}$		6.7	8	ns
$t_{d(LZ)}$	Low-to-high impedance state delay				4.6	8	ns
$t_{d(ZH)}$	High-impedance state-to-high delay				5.5	8	ns
$t_{d(ZL)}$	High-impedance state-to-low delay				4.8	8	ns
$t_{(DSR1)}$	$\overline{Deserializer}$ PLL lock time from $\overline{PWRDN}$ (with SYNCPAT)	See Figure 15, Figure 16, and Note 7	10 MHz			$(1024+26)t_{RFCP}$	µs
			40 MHz			$(1024+26)t_{RFCP}$	
$t_{(DSR2)}$	Deserializer PLL lock time from SYNCPAT		10 MHz			0.7	
			40 MHz			0.2	
$t_{d(ZHL)}$	High-impedance state-to-high delay (power up)		$\overline{LOCK}$			3	ns
$t_{(RNM)}$	Deserializer noise margin	See Figure 17 and Note 8	10 MHz		3680		ps
			40 MHz		1100		

NOTES: 7. $t_{(DSR1)}$ represents the time required for the deserializer to register that a lock has occurred upon power up or when leaving the power-down mode. $t_{(DSR2)}$ represents the time required to register that a lock has occurred for the powered up and enabled deserializer when the input (RI±) conditions change from not receiving data to receiving synchronization patterns (SYNCPATs). In order to specify deserializer PLL performance t_{DSR1} and t_{DSR2} are specified with REFCLK active and stable and specific conditions of SYNCPATs.

8. t_{RNM} represents the phase noise or jitter that the deserializer can withstand in the incoming data stream before bit errors occur.

timing diagrams and test circuits

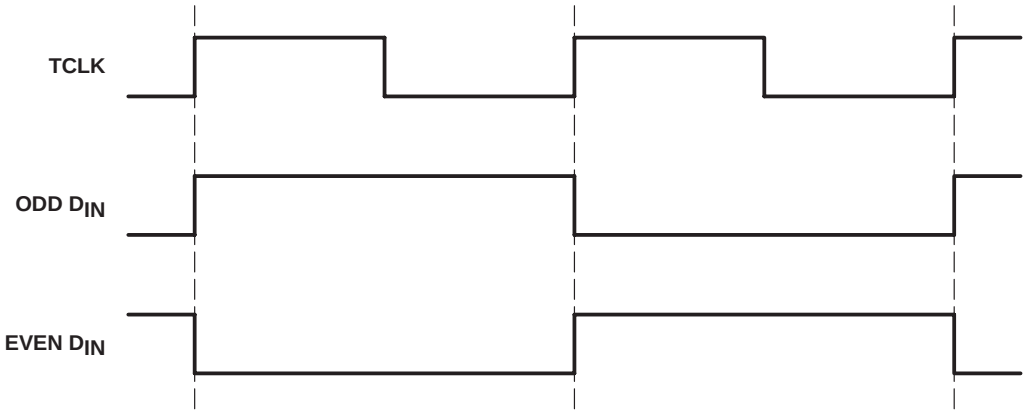


Figure 2. Worst-Case Serializer I_{CC} Test Pattern

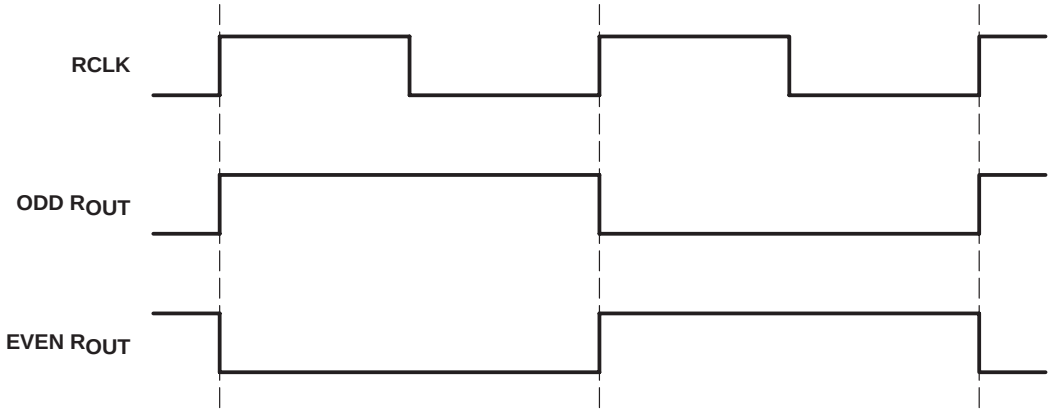


Figure 3. Worst-Case Deserializer I_{CC} Test Pattern

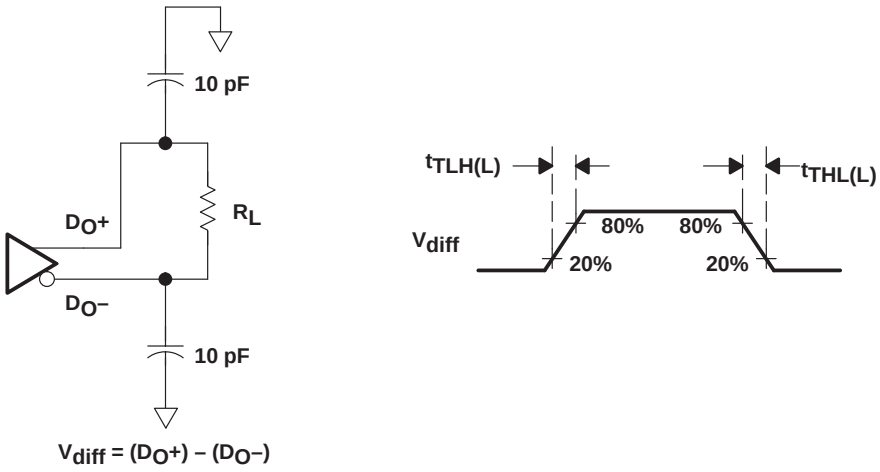


Figure 4. Serializer LVDS Output Load and Transition Times

timing diagrams and test circuits (continued)

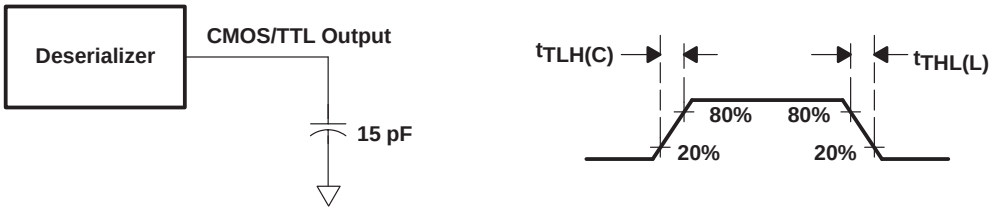


Figure 5. Deserializer CMOS/TTL Output Load and Transition Times

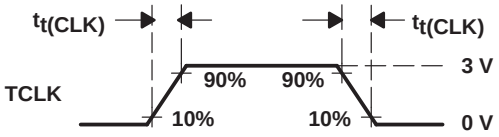


Figure 6. Serializer Input Clock Transition Time

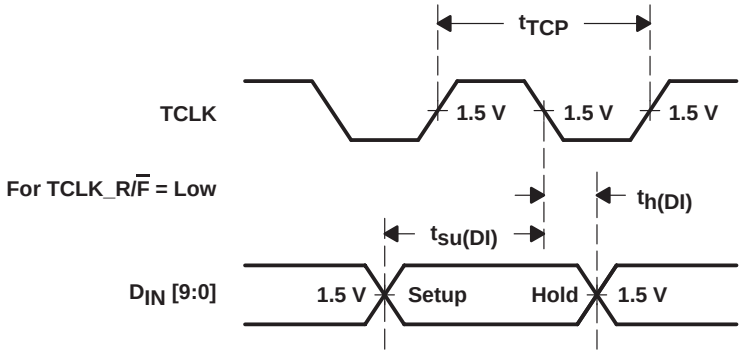


Figure 7. Serializer Setup/Hold Times

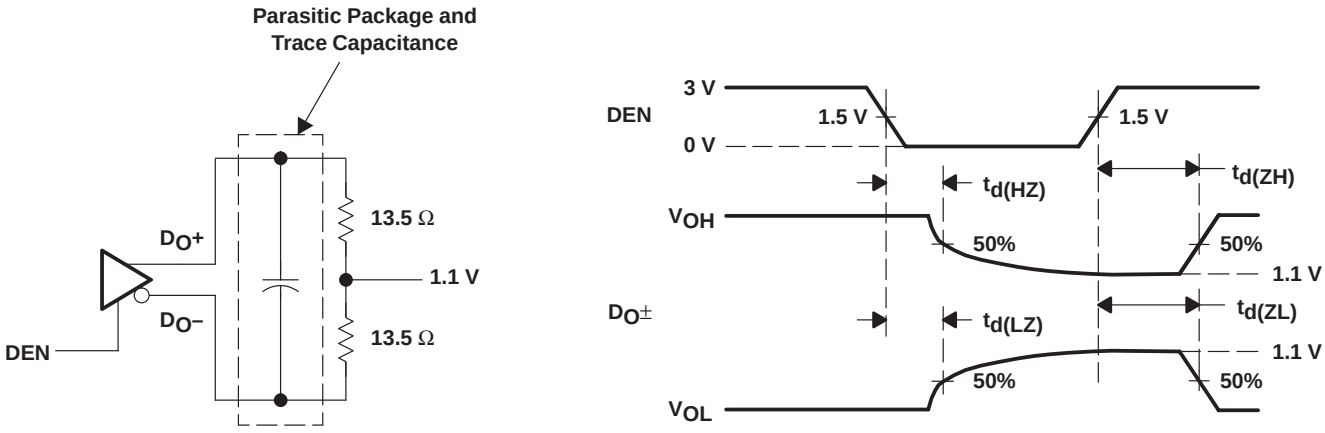


Figure 8. Serializer High-Impedance-State Test Circuit and Timing

timing diagrams and test circuits (continued)

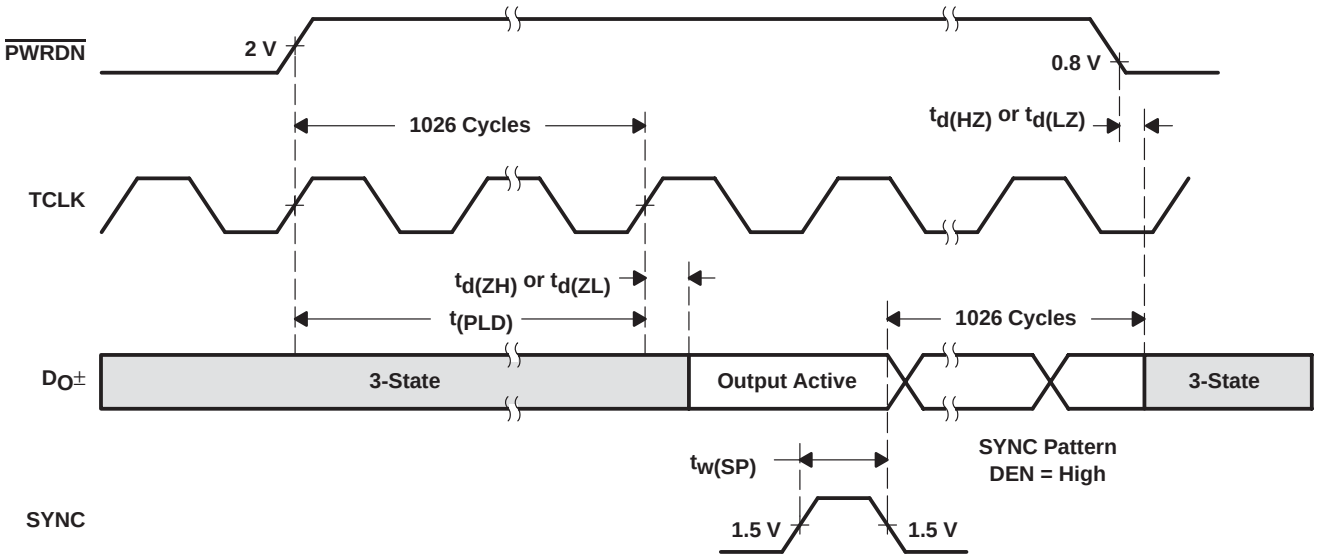


Figure 9. Serializer PLL Lock Time and $\overline{\text{PWRDN}}$ High-Impedance-State Delays

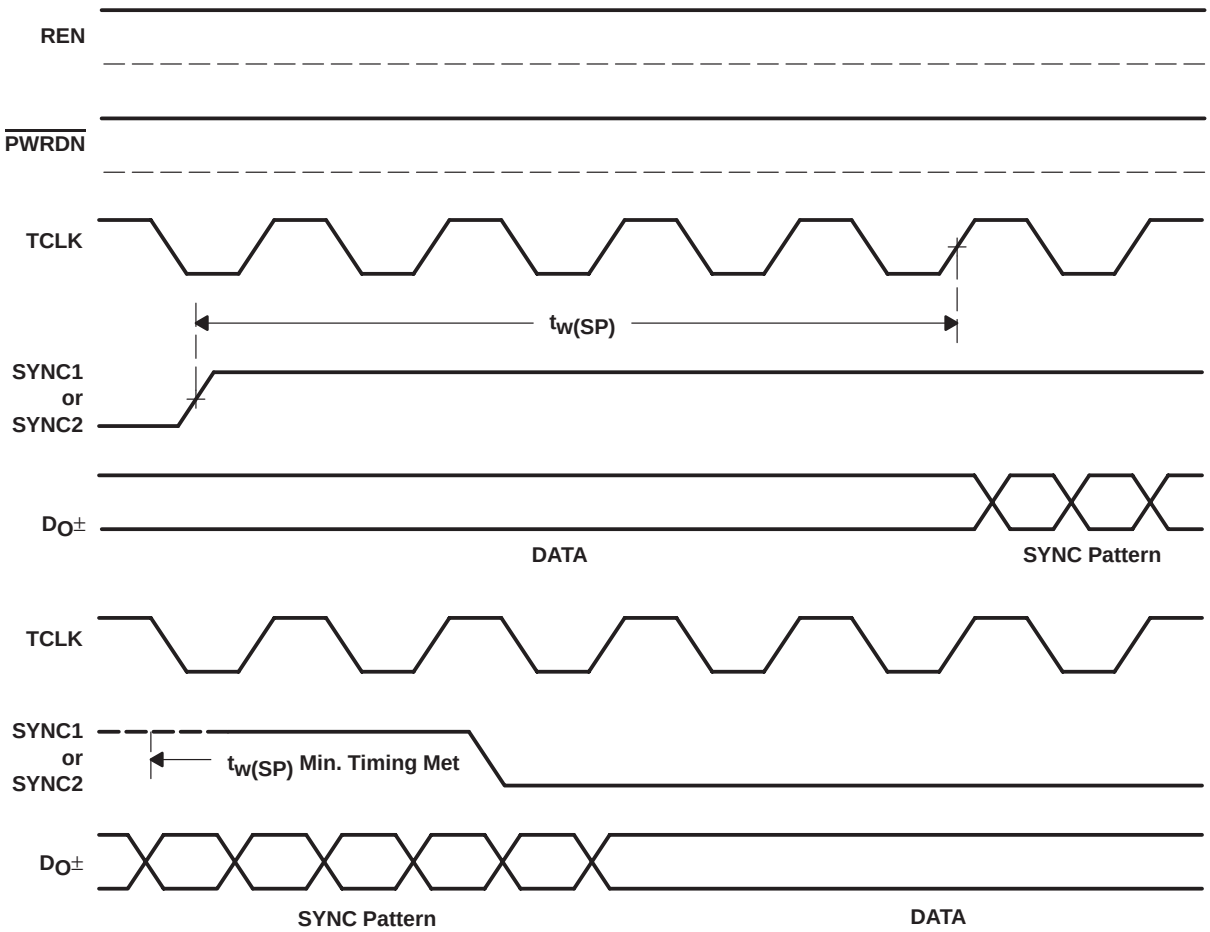


Figure 10. SYNC Timing Delays

timing diagrams and test circuits (continued)

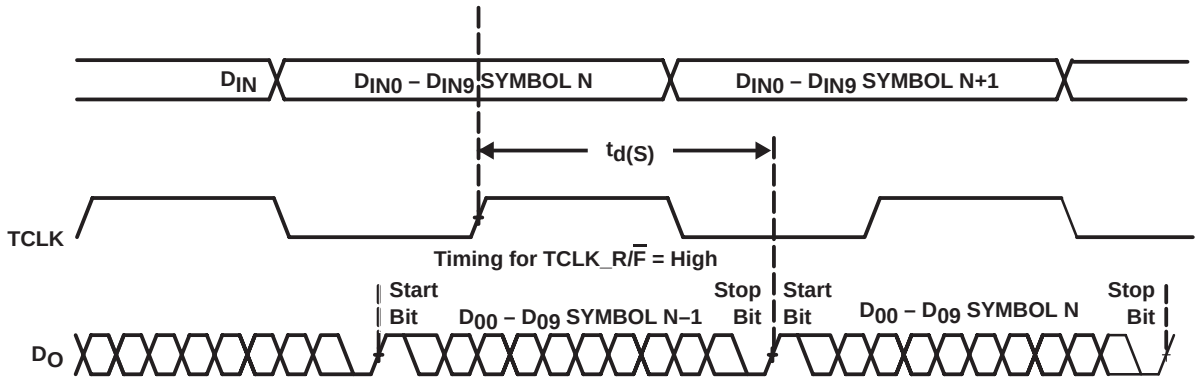


Figure 11. Serializer Delay

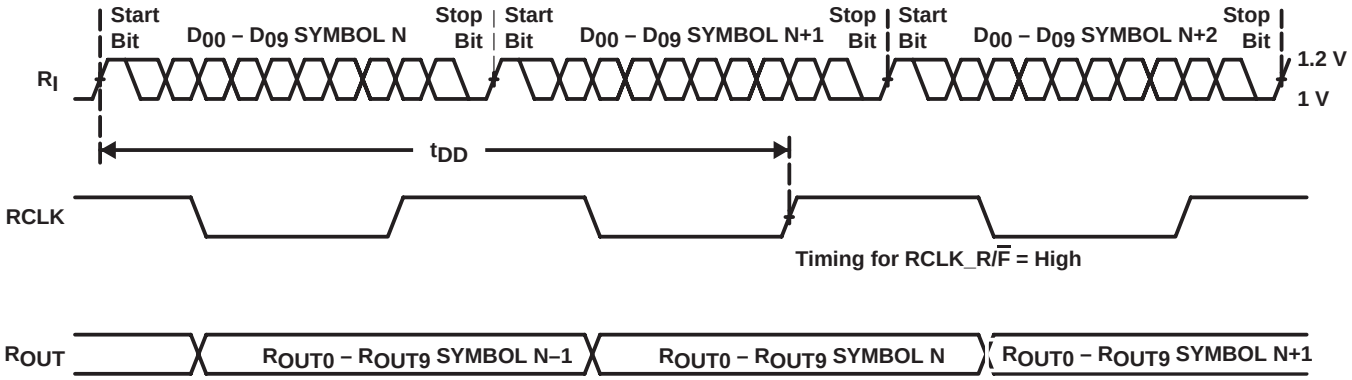


Figure 12. Deserializer Delay

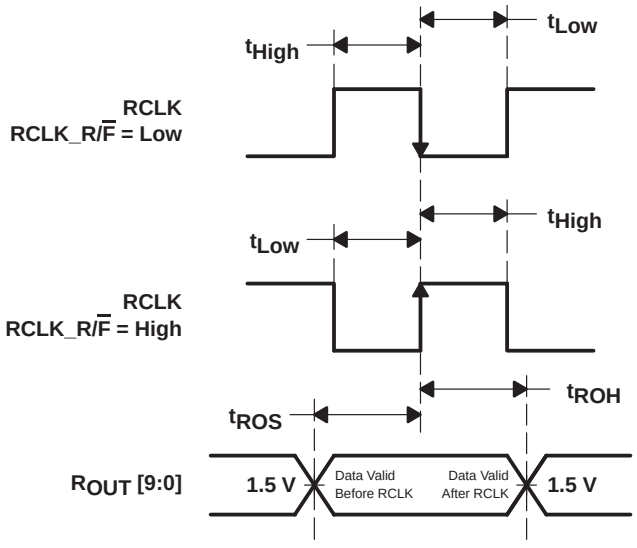


Figure 13. Deserializer Setup and Hold Times

timing diagrams and test circuits (continued)

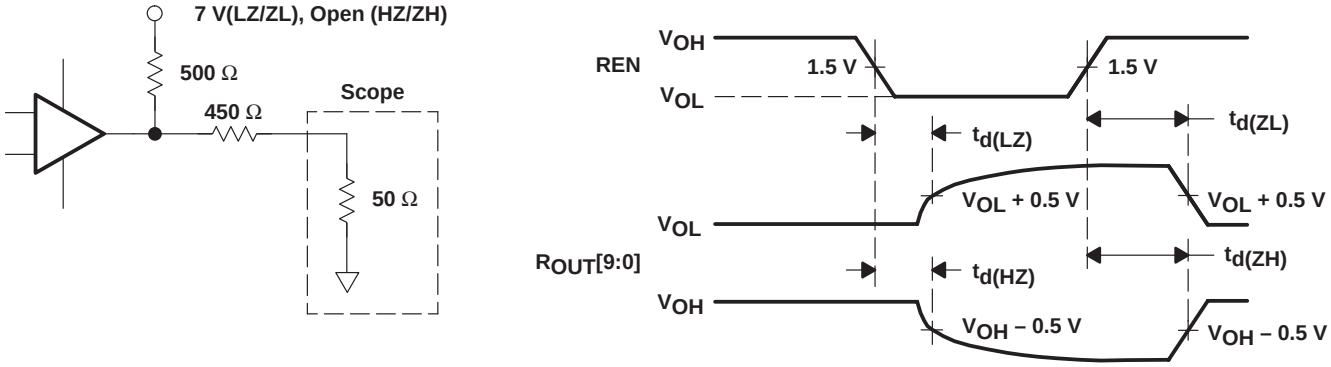


Figure 14. Deserializer High-Impedance-State Test Circuit and Timing

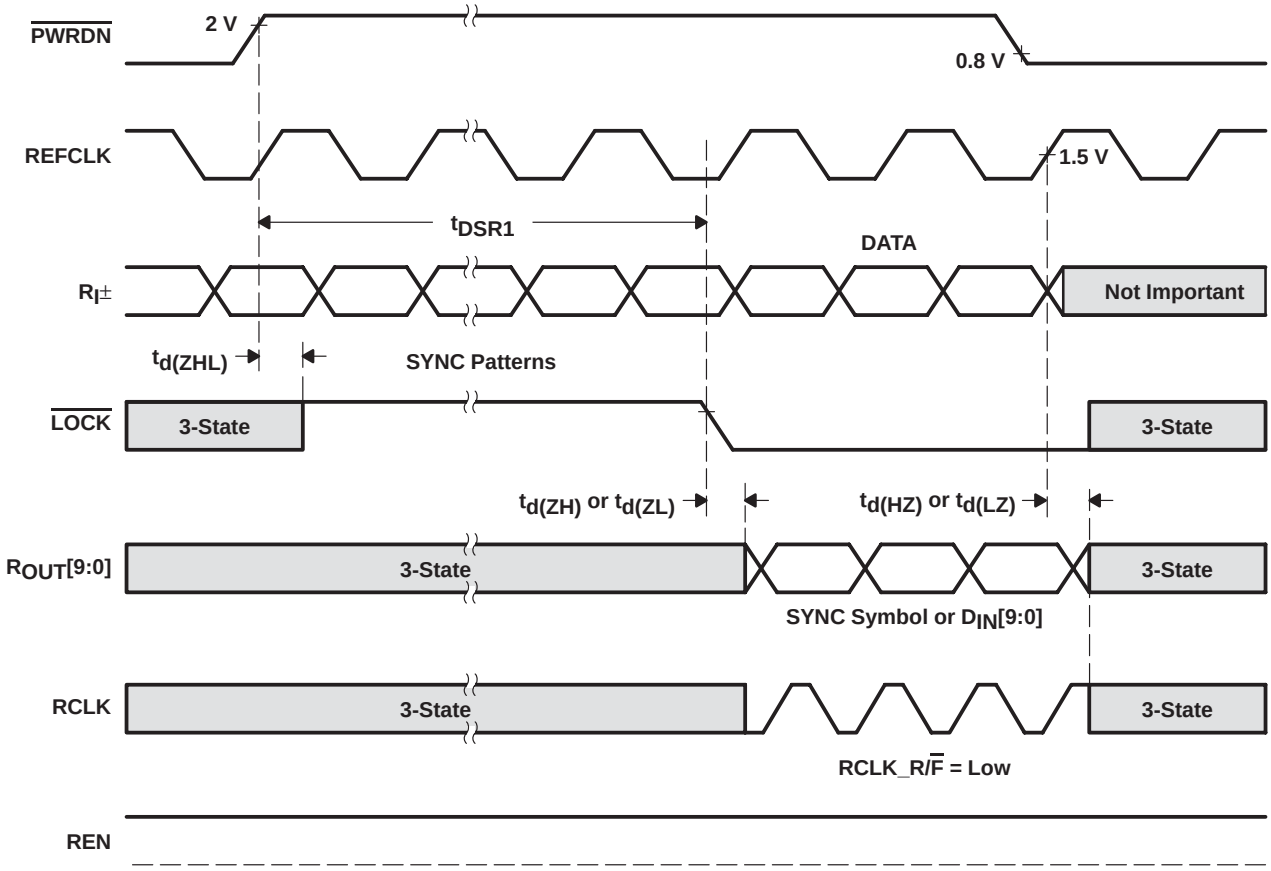


Figure 15. Receiver LVDS Input Skew Margin

timing diagrams and test circuits (continued)

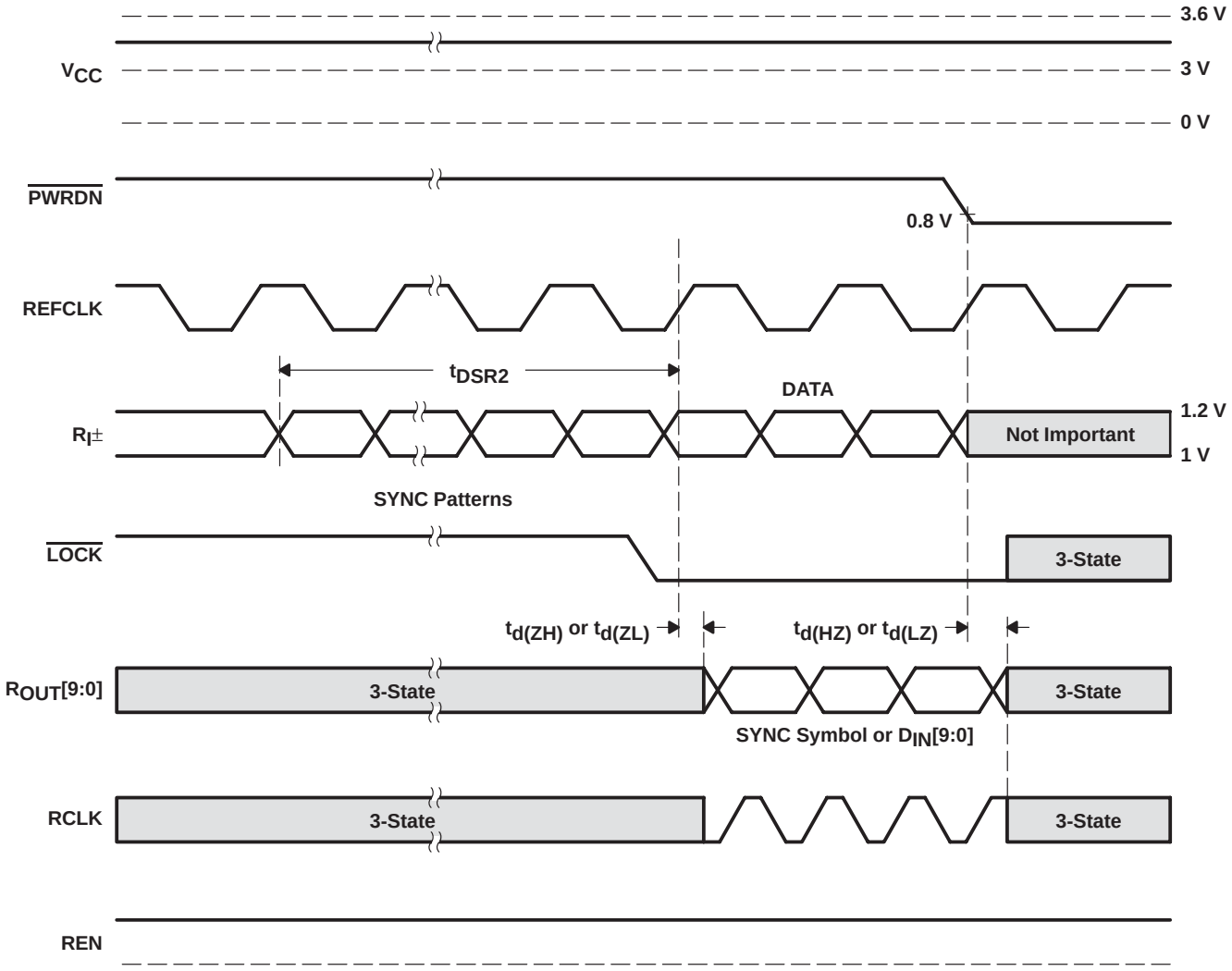
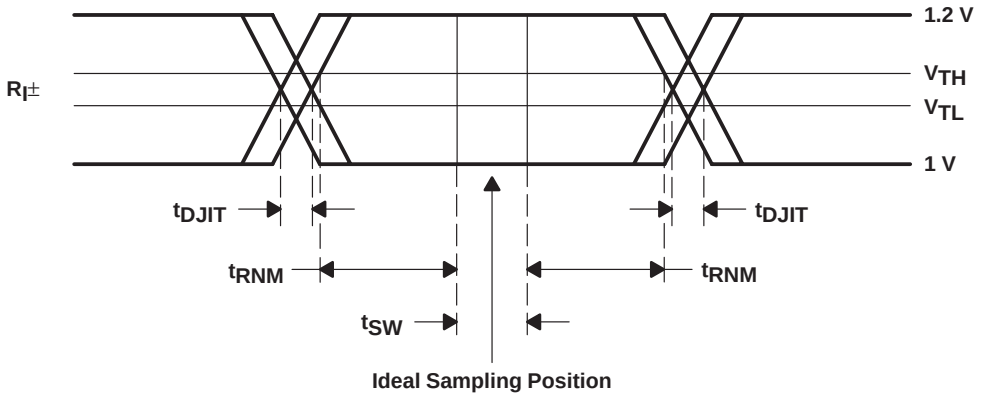


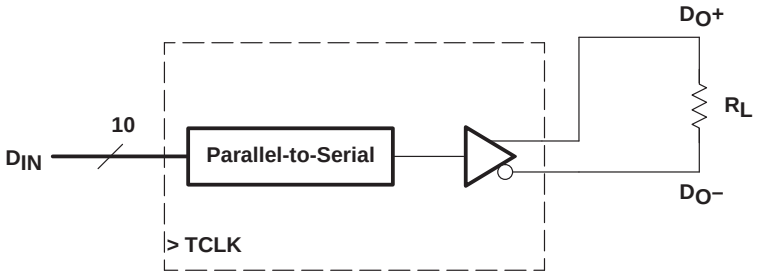
Figure 16. Deserilaizer PLL Lock Time From SyncPAT

timing diagrams and test circuits (continued)



t_{SW}: Setup and Hold Time (Internal Data Sampling Window)
t_{DJIT}: Serializer Output Bit Position Jitter That Results From Jitter on TCLK
t_{RNM}: Receiver Noise Margin Time

Figure 17. Receiver LVDS Input Skew Margin



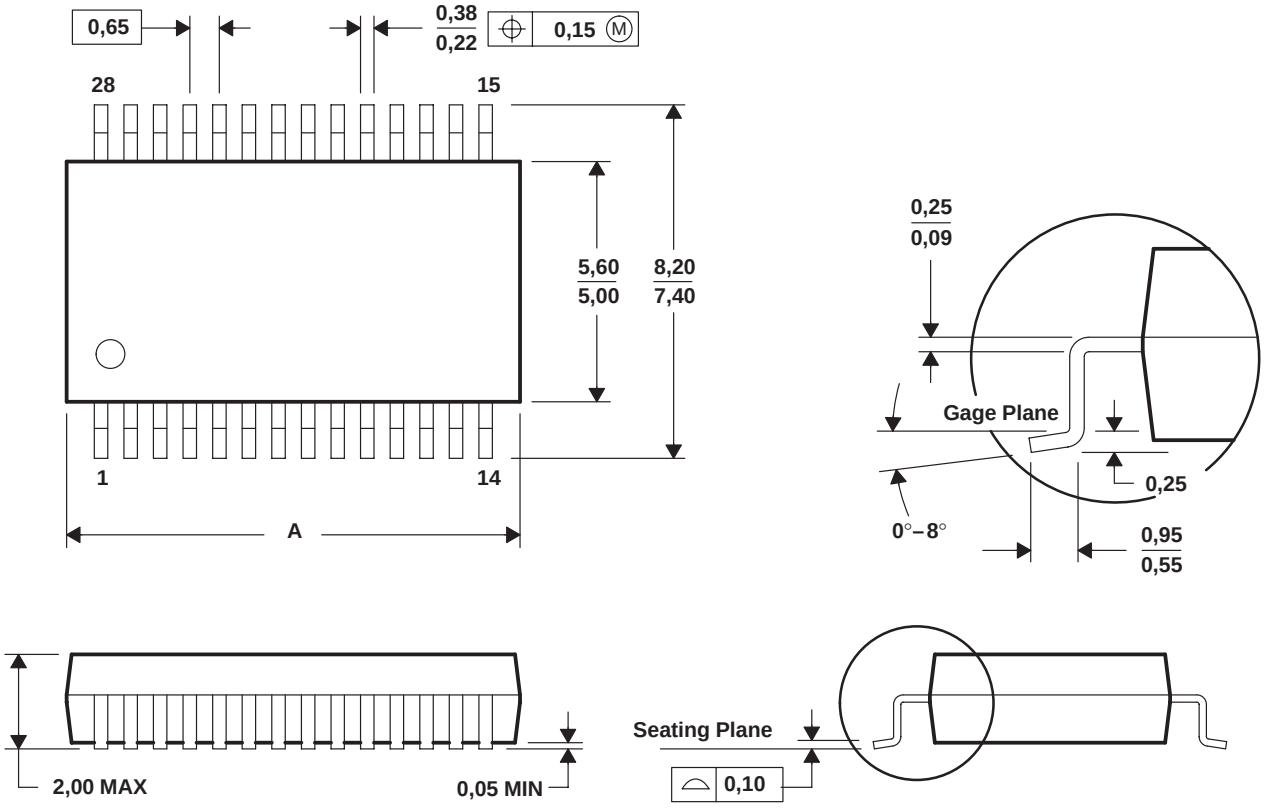
$V_{OD} = (D_O+) - (D_O-)$
Differential Output Signal Is Shown as $(D_O+) - (D_O-)$

Figure 18. V_{OD} Diagram

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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