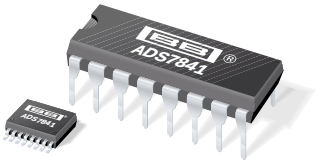
ADS7841



SBAS084B – JULY 2001

12-Bit, 4-Channel Serial Output Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- SINGLE SUPPLY: 2.7V to 5V
- 4-CHANNEL SINGLE-ENDED OR 2-CHANNEL DIFFERENTIAL INPUT
- UP TO 200kHz CONVERSION RATE
- ±1LSB MAX INL AND DNL
- NO MISSING CODES
- 72dB SINAD
- SERIAL INTERFACE
- DIP-16 OR SSOP-16 PACKAGE
- ALTERNATE SOURCE FOR MAX1247
- ADS7841ES: +125°C Version

APPLICATIONS

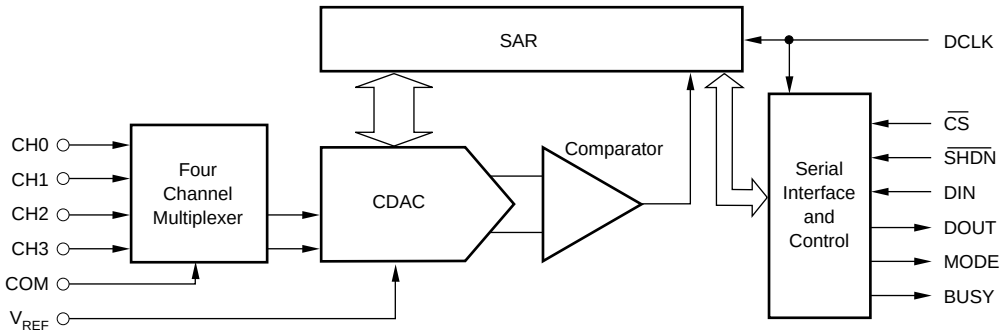
- DATA ACQUISITION
- TEST AND MEASUREMENT
- INDUSTRIAL PROCESS CONTROL
- PERSONAL DIGITAL ASSISTANTS
- BATTERY-POWERED SYSTEMS

DESCRIPTION

The ADS7841 is a 4-channel, 12-bit sampling Analog-to-Digital Converter (ADC) with a synchronous serial interface. The resolution is programmable to either 8 bits or 12 bits. Typical power dissipation is 2mW at a 200kHz throughput rate and a +5V supply. The reference voltage (V_{REF}) can be varied between 100mV and V_{CC}, providing a corresponding input voltage range of 0V to V_{REF}. The device includes a shutdown mode which reduces power dissipation to under 15µW. The ADS7841 is tested down to 2.7V operation.

Low power, high speed, and on-board multiplexer make the ADS7841 ideal for battery-operated systems such as personal digital assistants, portable multi-channel data loggers, and measurement equipment. The serial interface also provides low-cost isolation for remote data acquisition. The ADS7841 is available in a DIP-16 or a SSOP-16 package and is specified over the –40°C to +125°C(1) temperature range.

NOTE: (1) ES grade only.



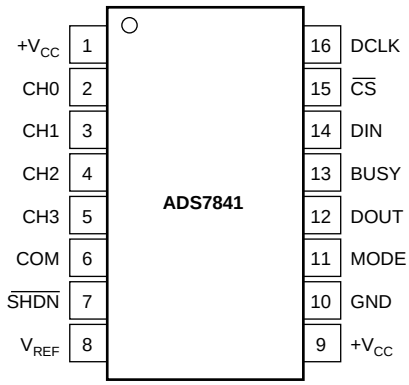
PACKAGE/ORDERING INFORMATION

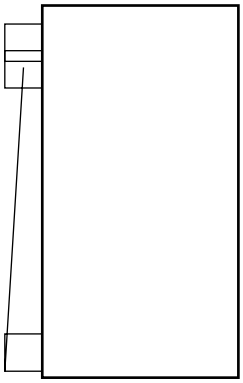
PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	MAXIMUM GAIN ERROR (LSB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DESIGNATOR	PACKAGE DRAWING NUMBER	ORDERING NUMBER(1)	TRANSPORT MEDIA
ADS7841E	±2	±4	–40°C to +85°C	SSOP-16	DBQ	322	ADS7841E	Rails
"	"	"	"	"	"	"	ADS7841E/2K5	Tape and Reel
ADS7841P	±2	"	–40°C to +85°C	DIP-16	N	180	ADS7841P	Rails
ADS7841EB	±1	±3	–40°C to +85°C	SSOP-16	DBQ	322	ADS7841EB	Rails
"	"	"	"	"	"	"	ADS7841EB/2K5	Tape and Reel
ADS7841PB	±1	"	–40°C to +85°C	DIP-16	N	180	ADS7841PB	Rails
ADS7841ES	±2	±4	–40°C to +125°C	SSOP-16	DBQ	322	ADS7841ES/2K5	Tape and Reel

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of “ADS7841E/2K5” will get a single 2500-piece Tape and Reel.

PIN CONFIGURATIONS

Top View





ELECTRICAL CHARACTERISTICS: +5V

At $T_A = T_{MIN}$ to T_{MAX}, $+V_{CC} = +5V$, $V_{REF} = +5V$, $f_{SAMPLE} = 200kHz$, and $f_{CLK} = 16 \bullet f_{SAMPLE} = 3.2MHz$, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7841E, P			ADS7841EB, PB			ADS7841ES			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT											
Full-Scale Input Span	Positive Input - Negative Input	0		V_{REF}	*		*	*		*	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ +0.2	*		*	*		*	V
	Negative Input	–0.2		+1.25	*		*	*		*	V
Capacitance			25			*			*		pF
Leakage Current				200			200			200	nA
SYSTEM PERFORMANCE											
Resolution			12			*			*		Bits
No Missing Codes		12			12			11			Bits
Integral Linearity Error				±2			±1			2	LSB[1]
Differential Linearity Error			±0.8			±0.5	±1		±0.8		LSB
Offset Error				±3			*			*	LSB
Offset Error Match			0.15	1.0		*	*		*	*	LSB
Gain Error				±4			±3			±4	LSB
Gain Error Match			0.1	1.0		*	*		*	*	LSB
Noise			30			*			*		µVrms
Power-Supply Rejection			70			*			*		dB
SAMPLING DYNAMICS											
Conversion Time				12			*			*	Clk Cycles
Acquisition Time		3			*			*			Clk Cycles
Throughput Rate				200			*			*	kHz
Multiplexer Settling Time			500			*			*		ns
Aperture Delay			30			*			*		ns
Aperture Jitter			100			*			*		ps
DYNAMIC CHARACTERISTICS											
Total Harmonic Distortion[2]	V_{IN} = 5Vp-p at 10kHz		–78	–72		–80	–76		–78	–72	dB
Signal-to-(Noise + Distortion)	V_{IN} = 5Vp-p at 10kHz	68	71		70	72		68	71		dB
Spurious-Free Dynamic Range	V_{IN} = 5Vp-p at 10kHz	72	79		76	81		72	79		dB
Channel-to-Channel Isolation	V_{IN} = 5Vp-p at 50kHz		120			*			120		dB
REFERENCE INPUT											
Range		0.1		$+V_{CC}$	*		*	*		*	V
Resistance	DCLK Static		5			*			*		GΩ
Input Current			40	100		*	*		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*			*		µA
	DCLK Static		0.001	3		*	*		*	*	µA
DIGITAL INPUT/OUTPUT											
Logic Family			CMOS			*			*		
Logic Levels											
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	3.0		5.5	*		*	*		*	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	–0.3		+0.8	*		*	*		*	V
V_{OH}	$I_{OH} = -250\mu A$	3.5			*			*			V
V_{OL}	$I_{OL} = 250\mu A$			0.4			*			*	V
Data Format			Straight Binary			*			*		
PWR SUPPLY REQUIREMENTS											
$+V_{CC}$	Specified Performance	4.75		5.25	*		*	*		*	V
Quiescent Current			550	900			*			*	µA
	f_{SAMPLE} = 12.5kHz		300			*			*		µA
	Power-Down Mode[3], $\overline{CS} = +V_{CC}$			3			*			*	µA
Power Dissipation				4.5			*			*	mW
TEMPERATURE RANGE											
Specified Performance		–40		+85	*		*	*		+125	°C

* Same specifications as ADS7841E, P.

NOTE: (1) LSB means Least Significant Bit. With V_{REF} equal to +5.0V, one LSB is 1.22mV. (2) First five harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND.

ELECTRICAL CHARACTERISTICS: +2.7V

At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7841E, P			ADS7841EB, PB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Full-Scale Input Span	Positive Input - Negative Input	0		V_{REF}	*		*	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ +0.2	*		*	V
	Negative Input	–0.2		+0.2	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
Resolution			12			*		Bits
No Missing Codes		12			12			Bits
Integral Linearity Error				±2			±1	LSB[1]
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error				±3			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				±4			±3	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		µVrms
Power-Supply Rejection			70			*		dB
SAMPLING DYNAMICS								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				125			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[2]	V_{IN} = 2.5Vp-p at 10kHz		–77	–72		–79	–76	dB
Signal-to-(Noise + Distortion)	V_{IN} = 2.5Vp-p at 10kHz	68	71		70	72		dB
Spurious-Free Dynamic Range	V_{IN} = 2.5Vp-p at 10kHz	72	78		76	80		dB
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100			*		dB
REFERENCE INPUT								
Range		0.1		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			13	40		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	$+V_{CC}$ • 0.7		5.5	*		*	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	$+V_{CC}$ • 0.8			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	2.7		3.6	*		*	V
Quiescent Current			280	650		*	*	µA
	f_{SAMPLE} = 12.5kHz		220			*		µA
	Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation				1.8			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

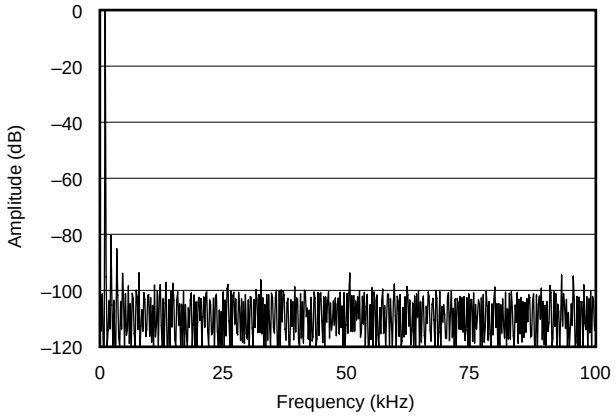
* Same specifications as ADS7841E, P.

NOTE: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, one LSB is 610mV. (2) First five harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND.

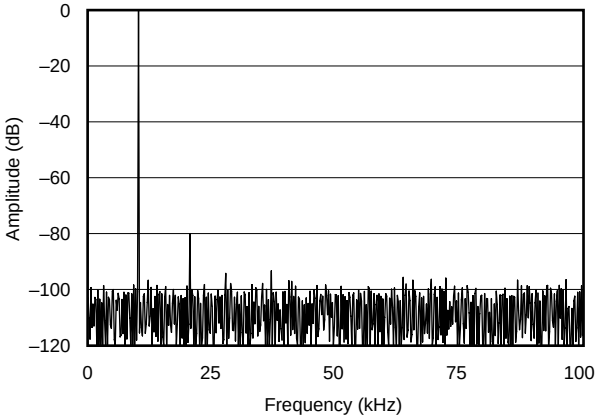
TYPICAL CHARACTERISTICS: +5V

At T_A = +25°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE} = 3.2MHz, unless otherwise noted.

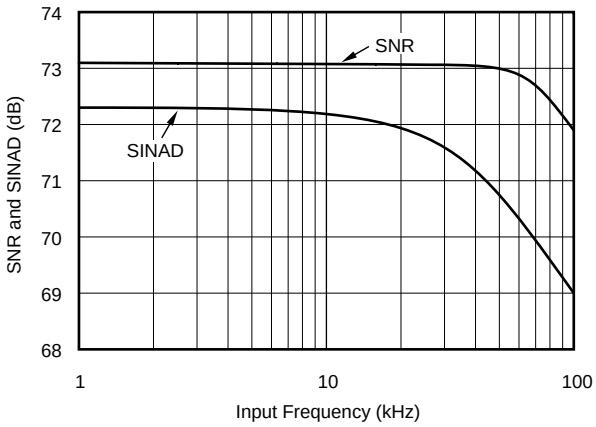
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,123Hz, –0.2dB)



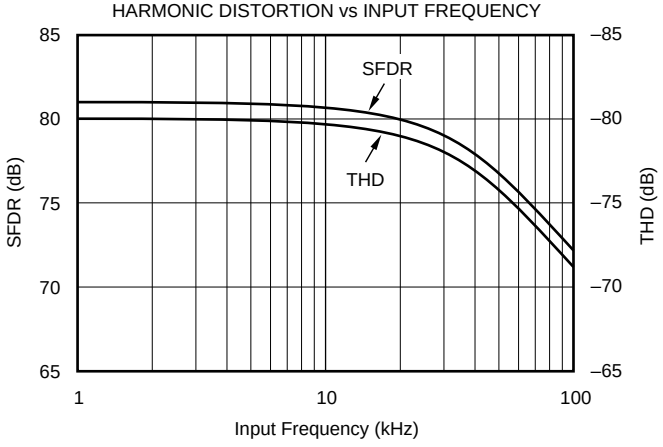
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.3kHz, –0.2dB)



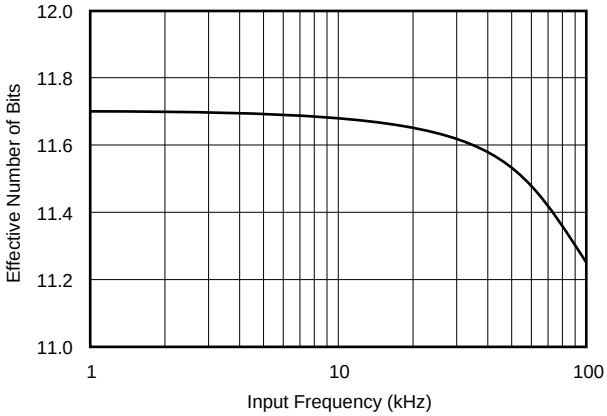
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY



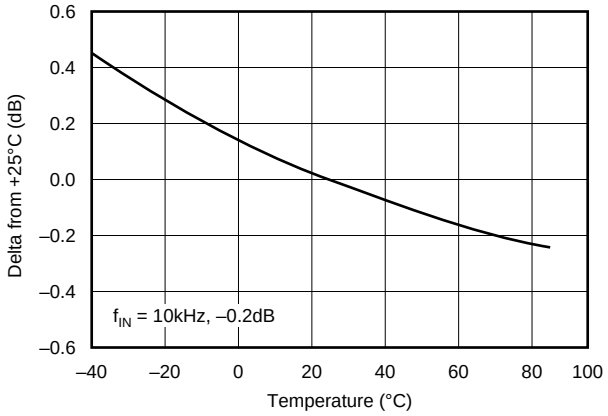
SPURIOUS-FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



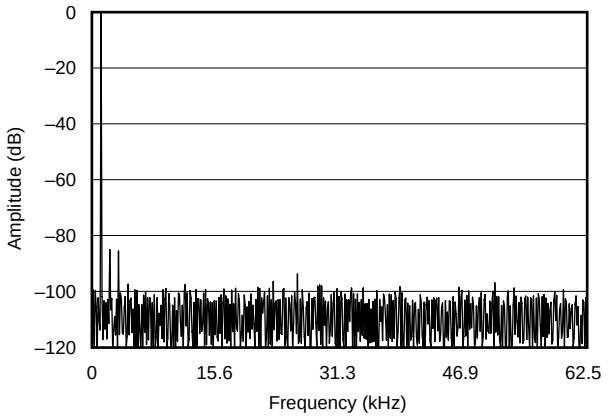
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



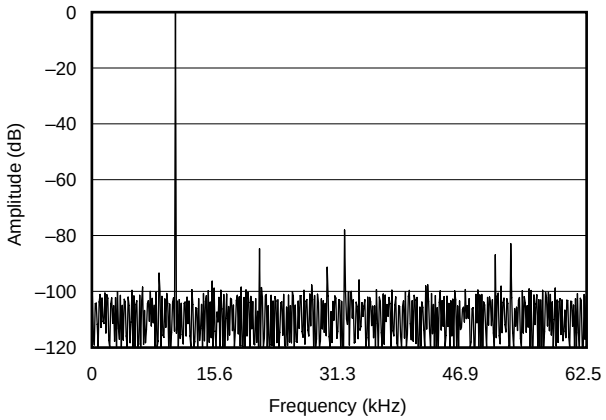
TYPICAL CHARACTERISTICS: +2.7V

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

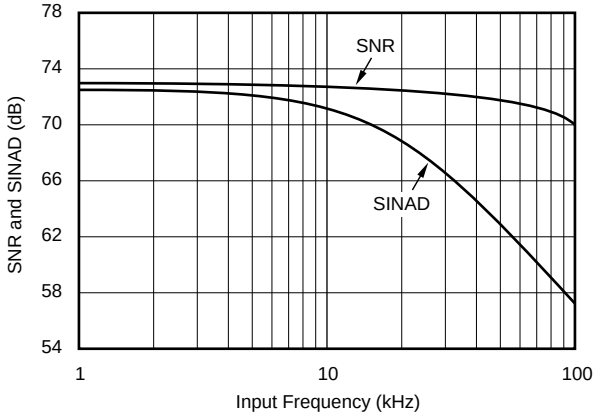
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,129Hz, –0.2dB)



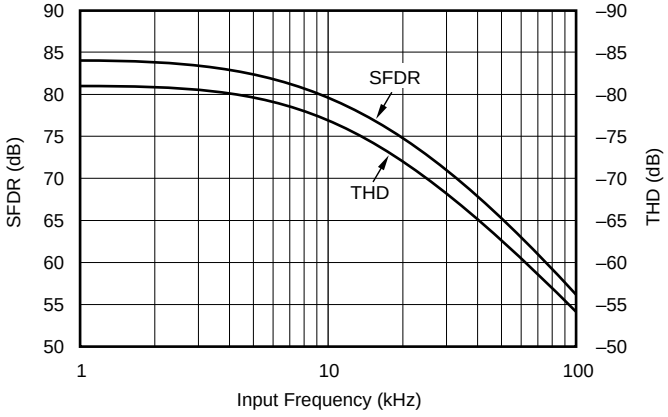
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.6kHz, –0.2dB)



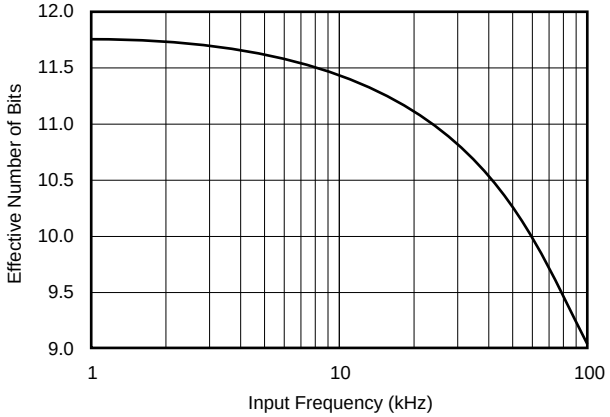
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-(NOISE+DISTORTION) vs INPUT FREQUENCY



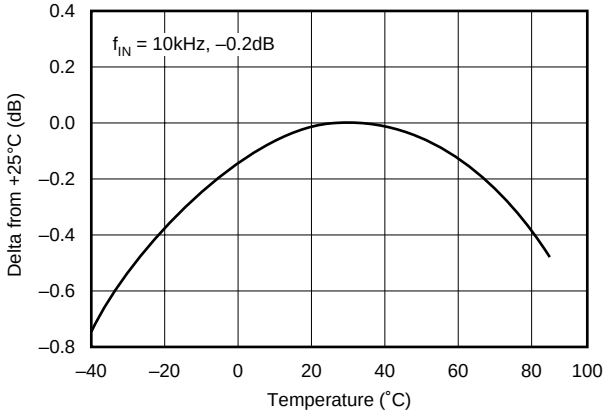
SPURIOUS-FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY



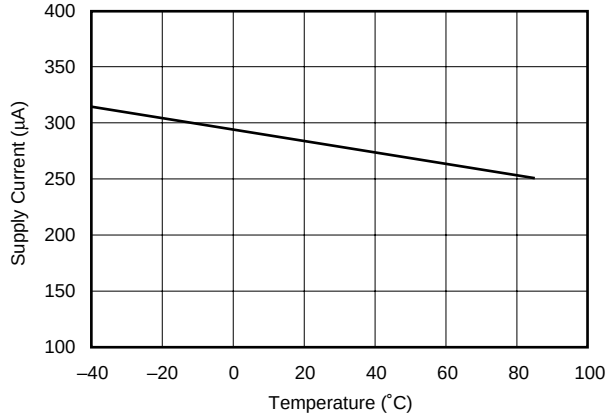
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION) vs TEMPERATURE



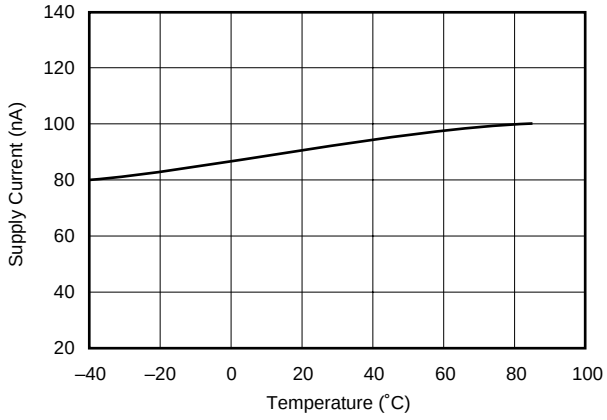
TYPICAL CHARACTERISTICS: +2.7V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

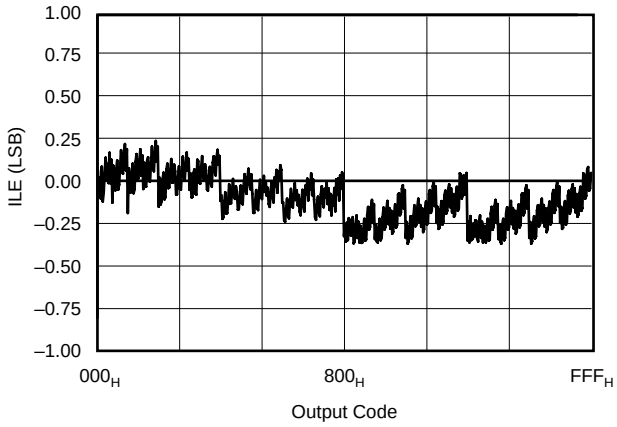
SUPPLY CURRENT vs TEMPERATURE



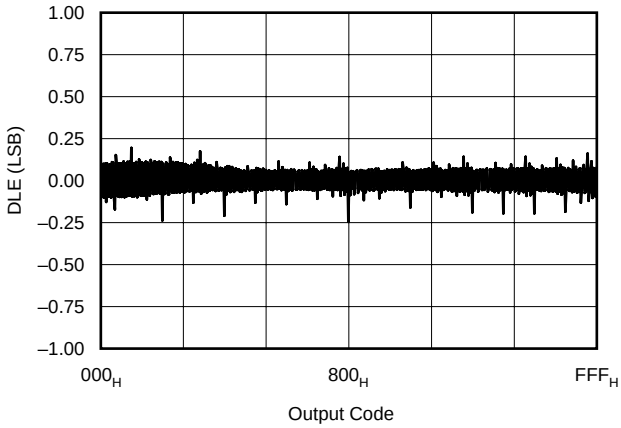
POWER DOWN SUPPLY CURRENT vs TEMPERATURE



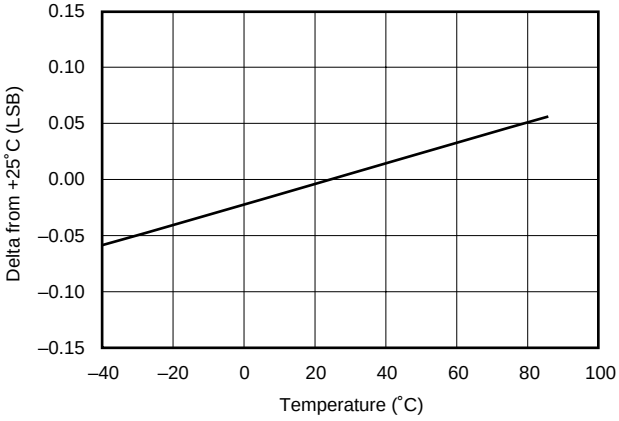
INTEGRAL LINEARITY ERROR vs CODE



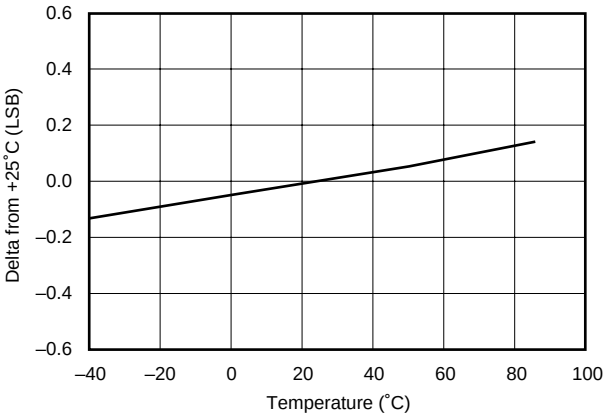
DIFFERENTIAL LINEARITY ERROR vs CODE



CHANGE IN GAIN vs TEMPERATURE



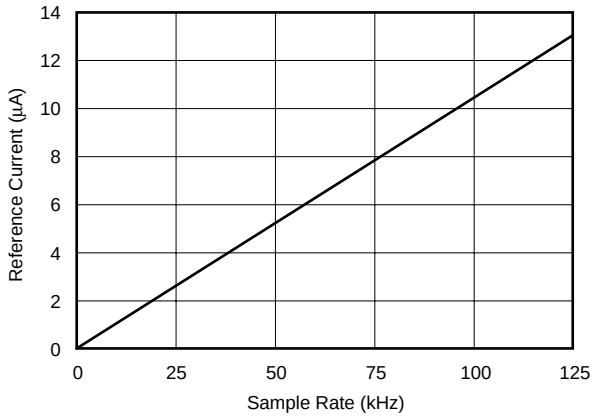
CHANGE IN OFFSET vs TEMPERATURE



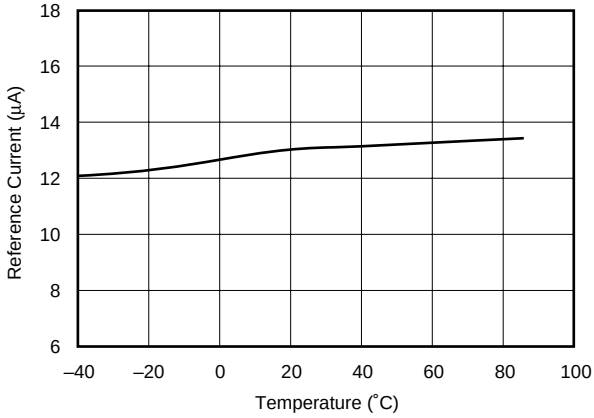
TYPICAL CHARACTERISTICS: +2.7V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

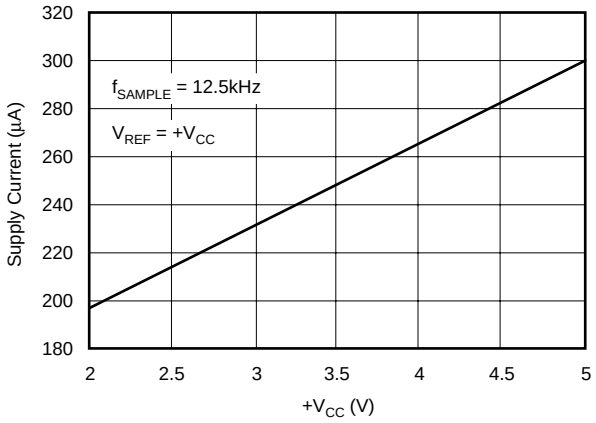
REFERENCE CURRENT vs SAMPLE RATE



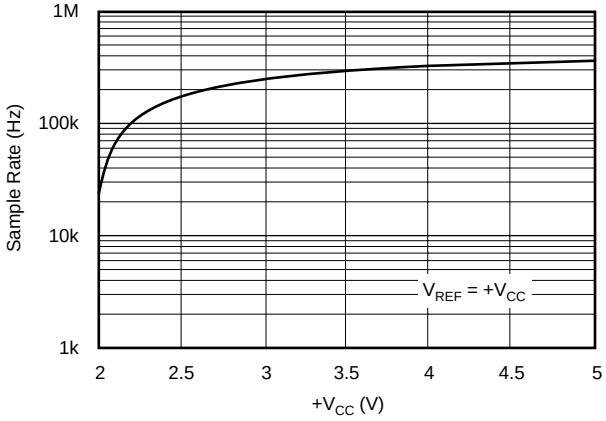
REFERENCE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs $+V_{CC}$



MAXIMUM SAMPLE RATE vs $+V_{CC}$



THEORY OF OPERATION

The ADS7841 is a classic Successive Approximation Register (SAR) ADC. The architecture is based on capacitive redistribution that inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µs CMOS process.

The basic operation of the ADS7841 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 100mV and $+V_{CC}$. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS7841.

The analog input to the converter is differential and is provided via a four-channel multiplexer. The input can be provided in reference to a voltage on the COM pin (which is generally ground) or differentially by using two of the four input channels (CH0 - CH3). The particular configuration is selectable via the digital interface.

ANALOG INPUT

Figure 2 shows a block diagram of the input multiplexer on the ADS7841. The differential input of the converter is derived from one of the four inputs in reference to the COM pin or two of the four inputs. Table I and Table II show the relationship between the A2, A1, A0, and SGL/$\overline{\text{DIF}}$ control bits and the configuration of the analog multiplexer. The control bits are provided serially via the DIN pin, see the Digital Interface section of this data sheet for more details.

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs (as shown in Figure 2) is captured on the internal capacitor array. The voltage on the –IN input is limited between –0.2V and 1.25V, allowing the input to reject small signals that are common to both the +IN and –IN input. The +IN input has a range of –0.2V to $+V_{CC}$ + 0.2V.

The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	1	+IN				–IN
1	0	1		+IN			–IN
0	1	0			+IN		–IN
1	1	0				+IN	–IN

TABLE I. Single-Ended Channel Selection (SGL/$\overline{\text{DIF}}$ HIGH).

A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	1	+IN	–IN			
1	0	1	–IN	+IN			
0	1	0			+IN	–IN	
1	1	0			–IN	+IN	

TABLE II. Differential Channel Control (SGL/$\overline{\text{DIF}}$ LOW).

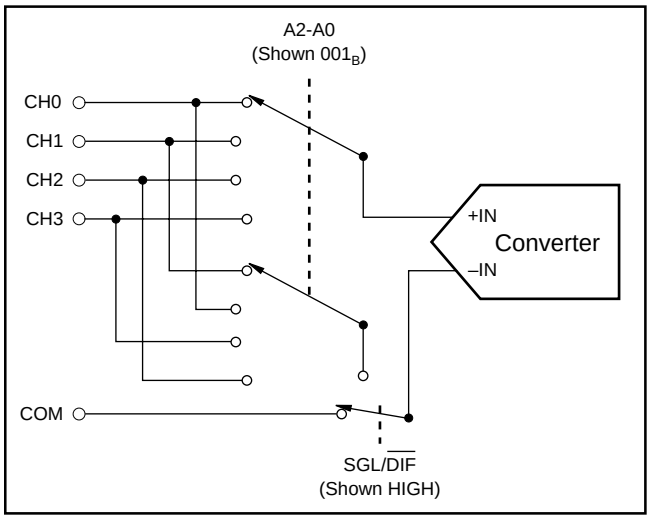


FIGURE 2. Simplified Diagram of the Analog Input.

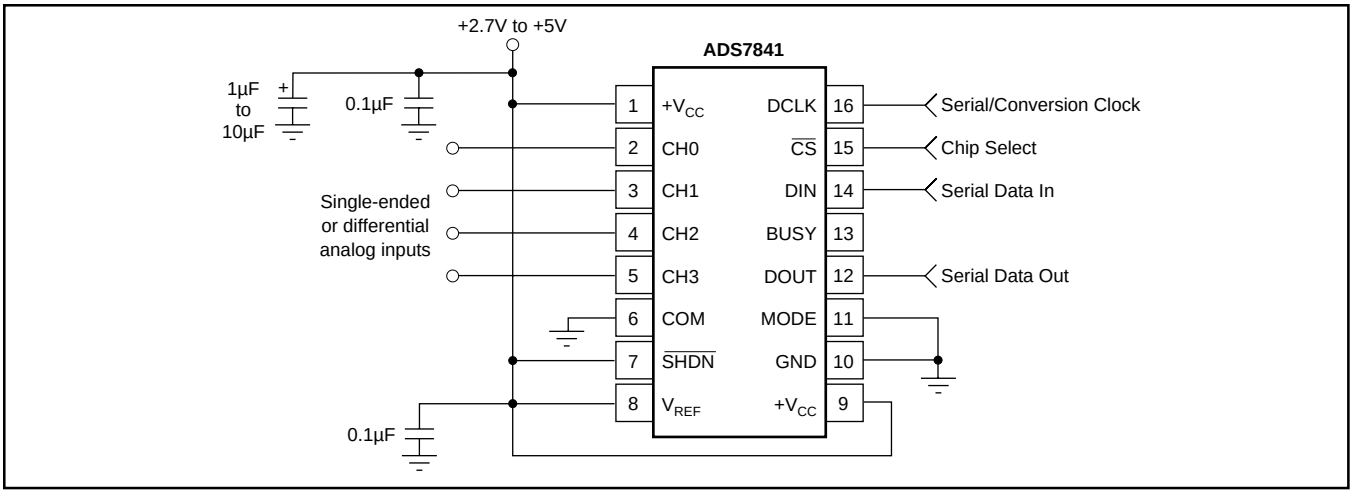


FIGURE 1. Basic Operation of the ADS7841.

REFERENCE INPUT

The external reference sets the analog input range. The ADS7841 will operate with a reference in the range of 100mV to $+V_{CC}$. Keep in mind that the analog input is the difference between the +IN input and the –IN input, see Figure 2. For example, in the single-ended mode, a 1.25V reference, and with the COM pin grounded, the selected input channel (CH0 - CH3) will properly digitize a signal in the range of 0V to 1.25V. If the COM pin is connected to 0.5V, the input range on the selected channel is 0.5V to 1.75V.

There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the ADC will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2LSBs with a 2.5V reference, then it will typically be 10LSBs with a 0.5V reference. In each case, the actual offset of the device is the same, 1.22mV.

Likewise, the noise or uncertainty of the digitized output will increase with lower LSB size. With a reference voltage of 100mV, the LSB size is 24μV. This level is below the internal noise of the device. As a result, the digital output code will not be stable and vary around a mean value by a number of LSBs. The distribution of output codes will be gaussian and the noise can be reduced by simply averaging consecutive conversion results or applying a digital filter.

With a lower reference voltage, care should be taken to provide a clean layout including adequate bypassing, a clean (low-noise, low-ripple) power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to nearby digital signals and electromagnetic interference.

The voltage into the V_{REF} input is not buffered and directly drives the Capacitor Digital-to-Analog Converter (CDAC) portion of the ADS7841. Typically, the input current is 13μA with a 2.5V reference. This value will vary by microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

DIGITAL INTERFACE

Figure 3 shows the typical operation of the ADS7841's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface (note that the digital inputs are over-voltage tolerant up to 5.5V, regardless of $+V_{CC}$). Each communication between the processor and the converter consists of eight clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer appropriately, it enters the acquisition (sample) mode. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the hold mode. The next twelve clock cycles accomplish the actual Analog-to-Digital conversion. A thirteenth clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be LOW). These will be ignored by the converter.

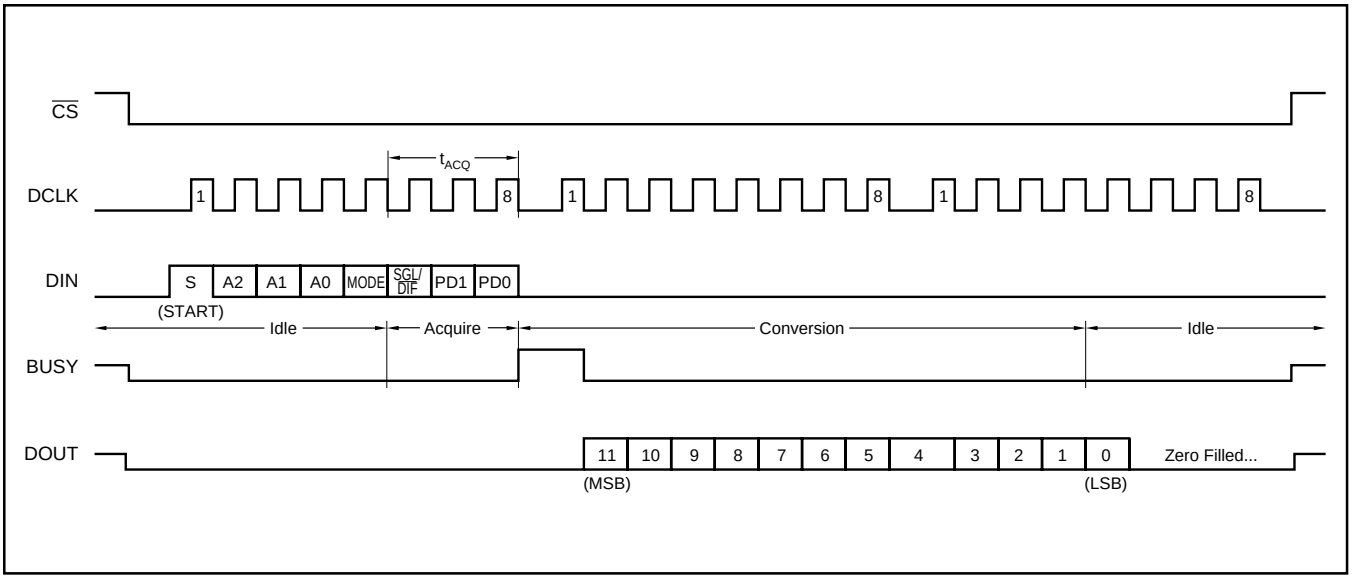


FIGURE 3. Conversion Timing, 24-Clocks per Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

Control Byte

Also shown in Figure 3 is the placement and order of the control bits within the control byte. Tables III and IV give detailed information about these bits. The first bit, the 'S' bit, must always be HIGH and indicates the start of the control byte. The ADS7841 will ignore inputs on the DIN pin until the start bit is detected. The next three bits (A2 - A0) select the active input channel or channels of the input multiplexer (see Tables I and II and Figure 2).

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	MODE	SGL/$\overline{\text{DIF}}$	PD1	PD0

TABLE III. Order of the Control Bits in the Control Byte.

BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first HIGH bit on DIN. A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode.
6 - 4	A2 - A0	Channel Select Bits. Along with the SGL/$\overline{\text{DIF}}$ bit, these bits control the setting of the multiplexer input, see Tables I and II.
3	MODE	12-Bit/8-Bit Conversion Select Bit. If the MODE pin is HIGH, this bit controls the number of bits for the next conversion: 12-bits (LOW) or 8-bits (HIGH). If the MODE pin is LOW, this bit has no function and the conversion is always 12 bits.
2	SGL/$\overline{\text{DIF}}$	Single-Ended/Differential Select Bit. Along with bits A2 - A0, this bit controls the setting of the multiplexer input, see Tables I and II.
1 - 0	PD1 - PD0	Power-Down Mode Select Bits. See Table V for details.

TABLE IV. Descriptions of the Control Bits within the Control Byte.

The MODE bit and the MODE pin work together to determine the number of bits for a given conversion. If the MODE pin is LOW, the converter always performs a 12-bit conversion regardless of the state of the MODE bit. If the MODE pin is HIGH, then the MODE bit determines the number of bits for each conversion, either 12 bits (LOW) or 8 bits (HIGH).

The SGL/$\overline{\text{DIF}}$ bit controls the multiplexer input mode: either single-ended (HIGH) or differential (LOW). In single-ended mode, the selected input channel is referenced to the COM pin. In differential mode, the two selected inputs provide a differential input. See Tables I and II and Figure 2 for more information. The last two bits (PD1 - PD0) select the power-down mode, as shown in Table V. If both inputs are HIGH, the device is always powered up. If both inputs are LOW, the device enters a power-down mode between conversions. When a new conversion is initiated, the device will resume normal operation instantly—no delay is needed to allow the device to power up and the very first conversion will be valid.

16-Clocks per Conversion

The control bits for conversion n+1 can be overlapped with conversion 'n' to allow for a conversion every 16 clock cycles, as shown in Figure 4. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer between the processor and the converter. This is possible provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that has been captured on the input sample-and-hold may droop enough to affect the conversion result. In addition, the ADS7841 is fully powered while other serial communications are taking place.

PD1	PD0	Description
0	0	Power-down between conversions. When each conversion is finished, the converter enters a low power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid.
0	1	Reserved for Future Use
1	0	Reserved for Future Use
1	1	No power-down between conversions, device always powered.

TABLE V. Power-Down Selection.

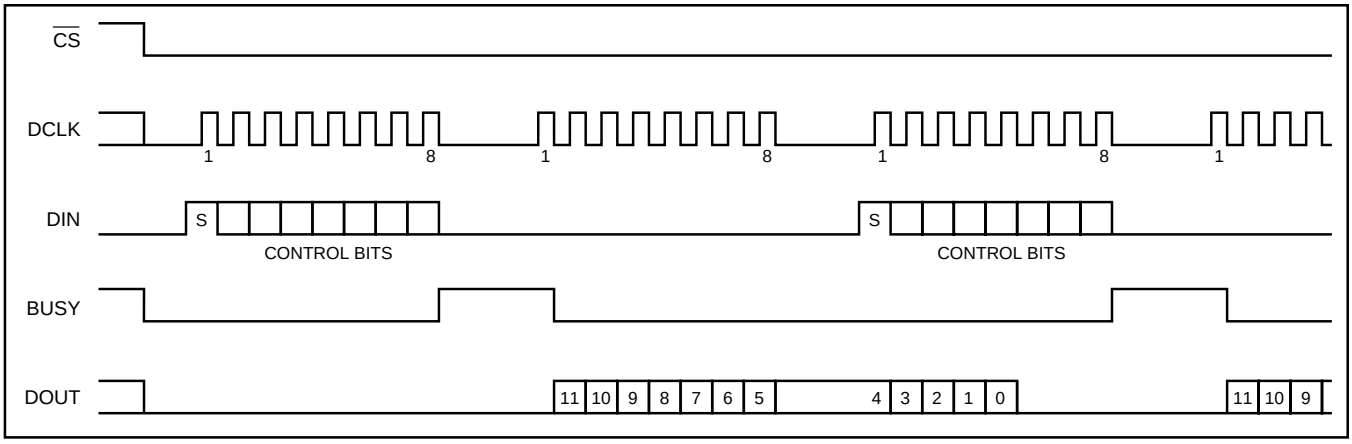


FIGURE 4. Conversion Timing, 16-Clocks per Conversion, 8-bit Bus Interface. No DCLK delay required with dedicated serial port.

Digital Timing

Figure 5 and Tables VI and VII provide detailed timing for the digital interface of the ADS7841.

15-Clocks per Conversion

Figure 6 provides the fastest way to clock the ADS7841. This method will not work with the serial interface of most

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	1.5			µs
t_{DS}	DIN Valid Prior to DCLK Rising	100			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			200	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			200	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			200	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	100			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	200			ns
t_{CL}	DCLK LOW	200			ns
t_{BD}	DCLK Falling to BUSY Rising			200	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			200	ns

TABLE VI. Timing Specifications ($+V_{CC}$ = +2.7V to 3.6V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	900			ns
t_{DS}	DIN Valid Prior to DCLK Rising	50			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			100	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			70	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			70	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	50			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	150			ns
t_{CL}	DCLK LOW	150			ns
t_{BD}	DCLK Falling to BUSY Rising			100	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			70	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			70	ns

TABLE VII. Timing Specifications ($+V_{CC}$ = +4.75V to +5.25V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

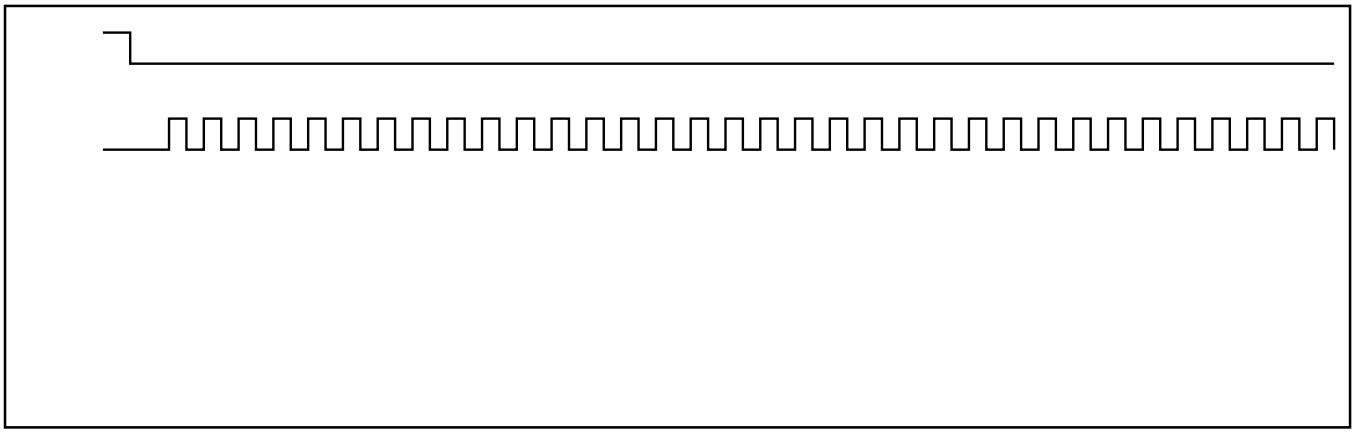
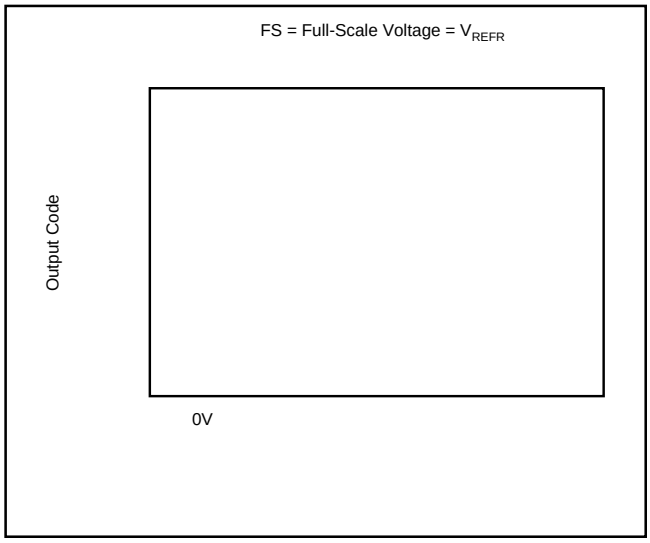


FIGURE 6. Maximum Conversion Rate, 15-Clocks per Conversion.

Data Format

The ADS7841 output data is in straight binary format, as shown in Figure 7. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS7841E	ACTIVE	SSOP/ QSOP	DBQ	16	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7841E/2K5	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7841E/2K5G4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7841EB	ACTIVE	SSOP/ QSOP	DBQ	16	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7841EB/2K5	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7841EB/2K5G4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7841EBG4	ACTIVE	SSOP/ QSOP	DBQ	16	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7841EG4	ACTIVE	SSOP/ QSOP	DBQ	16	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7841ES	ACTIVE	SSOP/ QSOP	DBQ	16	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7841ES/2K5	ACTIVE	SSOP/ QSOP	DBQ	16		TBD	Call TI	Call TI
ADS7841ES/2K5G4	ACTIVE	SSOP/ QSOP	DBQ	16		TBD	Call TI	Call TI
ADS7841ESG4	ACTIVE	SSOP/ QSOP	DBQ	16	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7841P	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
ADS7841PB	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
ADS7841PBG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
ADS7841PG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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TBD: The Pb-Free/Green conversion plan has not been defined.
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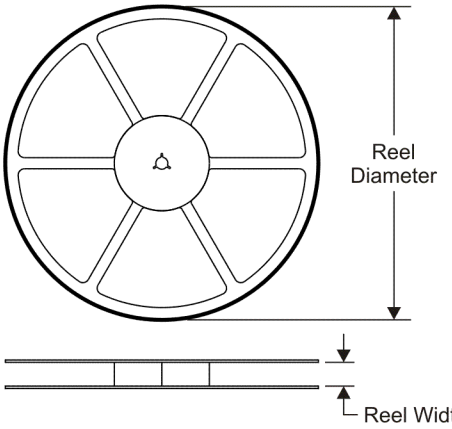
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

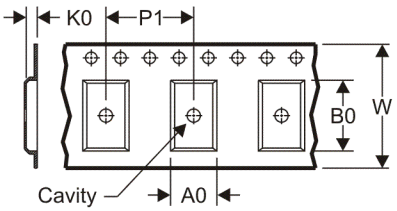
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

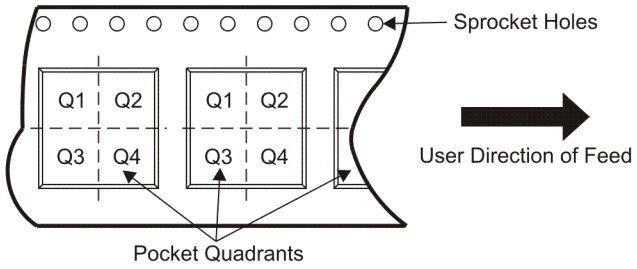


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

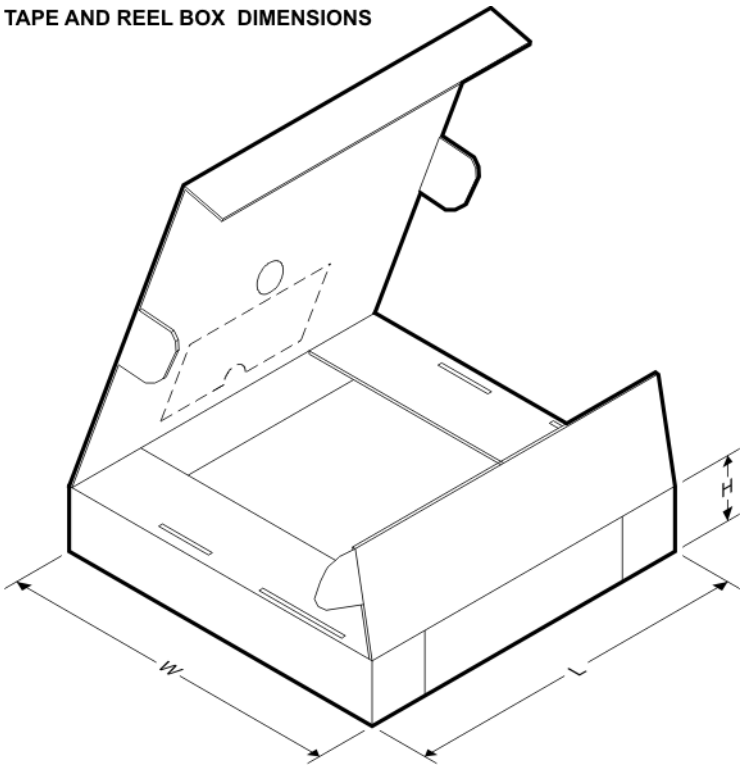
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7841E/2K5	SSOP/ QSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ADS7841EB/2K5	SSOP/ QSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7841E/2K5	SSOP/QSOP	DBQ	16	2500	346.0	346.0	29.0
ADS7841EB/2K5	SSOP/QSOP	DBQ	16	2500	346.0	346.0	29.0

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