19-2164; Rev 7; 7/08

High-Output-Drive, 10MHz, 10V/µs, Rail-to-Rail I/O Op Amps with Shutdown in SC70

General Description

The MAX4230–MAX4234 single/dual/quad, high-output-drive CMOS op amps feature 200mA of peak output current, rail-to-rail input, and output capability from a single 2.7V to 5.5V supply. These amplifiers exhibit a high slew rate of 10V/µs and a gain-bandwidth product (GBWP) of 10MHz. The MAX4230–MAX4234 can drive typical headset levels (32Ω), as well as bias an RF power amplifier (PA) in wireless handset applications.

The MAX4230 comes in a tiny 5-pin SC70 package and the MAX4231, single with shutdown, is offered in the 6-pin SC70 package and a 1.5mm x 1.0mm x 0.5mm ultra-thin µDFN package. The dual op-amp MAX4233 is offered in the space-saving 10-bump chip-scale package (UCSP™), providing the smallest footprint area for a dual op amp with shutdown.

These op amps are designed to be part of the PA control circuitry, biasing RF PAs in wireless headsets. The MAX4231/MAX4233 offer a $\overline{\text{SHDN}}$ feature that drives the output low. This ensures that the RF PA is fully disabled when needed, preventing unconverted signals to the RF antenna.

The MAX4230 family offers low offsets, wide bandwidth, and high-output drive in a tiny 2.1mm x 2.0mm space-saving SC70 package. These parts are offered over the automotive temperature range (-40°C to +125°C).

Applications

RF PA Biasing Controls in Handset Applications

Portable/Battery-Powered Audio Applications

Portable Headphone Speaker Drivers (32Ω)

Audio Hands-Free Car Phones (Kits)

Laptop/Notebook Computers/TFT Panels

Sound Ports/Cards

Set-Top Boxes

Digital-to-Analog Converter Buffers

Transformer/Line Drivers

Motor Drivers

Selector Guide appears at end of data sheet.
Pin Configurations appear at end of data sheet.

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- ♦ **30mA Output Drive Capability**
- ♦ **Rail-to-Rail Input and Output**
- ♦ **1.1mA Supply Current per Amplifier**
- ♦ **2.7V to 5.5V Single-Supply Operation**
- ♦ **10MHz Gain-Bandwidth Product**
- ♦ **High Slew Rate: 10V/µs**
- ♦ **100dB Voltage Gain (R_L = 100kΩ)**
- ♦ **85dB Power-Supply Rejection Ratio**
- ♦ **No Phase Reversal for Overdriven Inputs**
- ♦ **Unity-Gain Stable for Capacitive Loads to 780pF**
- ♦ **Low-Power Shutdown Mode Reduces Supply Current to < 1µA**
- ♦ **Available in 5-Pin SC70 Package (MAX4230) and 6-Pin Thin µDFN Package (MAX4231)**
- ♦ **Available in 10-Bump UCSP Package (MAX4233)**

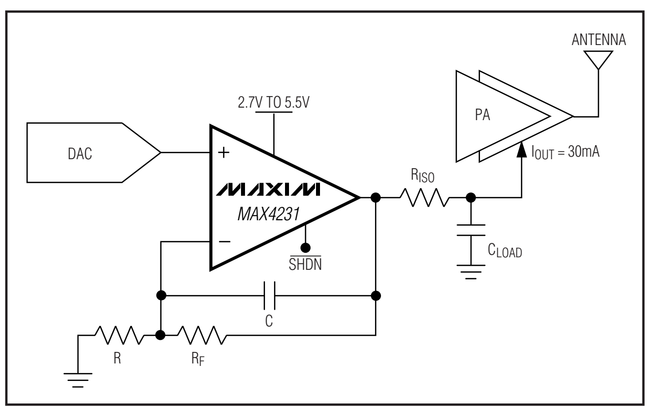
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4230AXK-T	-40°C to +125°C	5 SC70	ACS
MAX4230AUK-T	-40°C to +125°C	5 SOT23	ABZZ
MAX4231AXT-T	-40°C to +125°C	6 SC70	ABA
MAX4231AUT-T	-40°C to +125°C	6 SOT23	AAUV
MAX4231AYT+TG65	-40°C to +125°C	6 µDFN	+AI

Ordering Information continued at end of data sheet.

+Denotes a lead-free/RoHS-compliant package.
T = Tape and reel.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

High-Output-Drive, 10MHz, 10V/µs, Rail-to-Rail I/O Op Amps with Shutdown in SC70

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to V_{SS})..6V
All Other Pins....................................(V_{SS} - 0.3V) + (V_{DD} + 0.3V)
Output Short-Circuit Duration to V_{DD} or V_{SS} (Note 1)................10s
Continuous Power Dissipation (T_A = +70°C)
5-Pin SC70 (derate 3.1mW/°C above +70°C)..............247mW
5-Pin SOT23 (derate 7.1mW/°C above +70°C)............571mW
6-Pin SC70 (derate 3.1mW/°C above +70°C)..............245mW
6-Pin SOT23 (derate 8.7mW/°C above +70°C)...........696mW
6-Pin µDFN (derate 2.1mW/°C above +70°C).........170.2mW
8-Pin SOT23 (derate 8.9mW/°C above +70°C)...........714mW
8-Pin µMAX® (derate 4.5mW/°C above +70°C)..........362mW
10-Pin µMAX (derate 5.6mW/°C above +70°C)..........444mW
10-Bump UCSP (derate 6.1mW/°C above +70°C).....484mW
10-Pin TDFN (derate 24.4mW°C above +70°C)........1951mW
14-Pin SO (derate 8.3mW/°C above +70°C)...............667mW
Operating Temperature Range.........................-40°C to +125°C
Junction Temperature..+150°C
Storage Temperature Range.............................-65°C to +150°C
Lead Temperature (soldering, 10s).................................+300°C

Note 1: Package power dissipation should also be observed.

µMAX is a registered trademark of Maxim Integrated Products, Inc.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = (V_{DD}/2), R_L = ∞ connected to (V_{DD}/2), $V_{\overline{SHDN}}$ = V_{DD}, **T_A = +25°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{DD}	Inferred from PSRR test			2.7		5.5	V
Input Offset Voltage	V_{OS}					0.85	±6	mV
Input Bias Current	I_B	V_{CM} = V_{SS} to V_{DD}				50		pA
Input Offset Current	I_{OS}	V_{CM} = V_{SS} to V_{DD}				50		pA
Input Resistance	R_{IN}					1000		MΩ
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test			V_{SS}		V_{DD}	V
Common-Mode Rejection Ratio	CMRR	V_{SS} < V_{CM} < V_{DD}			52	70		dB
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.7V to 5.5V			73	85		dB
Shutdown Output Impedance	R_{OUT}	$V_{\overline{SHDN}}$ = 0V (Note 3)				10		Ω
Output Voltage in Shutdown	$V_{OUT(\overline{SHDN})}$	$V_{\overline{SHDN}}$ = 0V, R_L = 200Ω (Note 3)				68	120	mV
Large-Signal Voltage Gain	A_{VOL}	V_{SS} + 0.20V < V_{OUT} < V_{DD} - 0.20V	R_L = 100kΩ			100		dB
			R_L = 2kΩ		85	98		
			R_L = 200Ω		74	80		
Output Voltage Swing	V_{OUT}	R_L = 32Ω	V_{DD} - V_{OH}			400	500	mV
			V_{OL} - V_{SS}			360	500	
		R_L = 200Ω	V_{DD} - V_{OH}			80	120	
			V_{OL} - V_{SS}			70	120	
		R_L = 2kΩ	V_{DD} - V_{OH}			8	14	
			V_{OL} - V_{SS}			7	14	
Output Source/Sink Current	I_{OUT}	V_{DD} = 2.7V, V_{IN} = ±100mV				70		mA
		V_{DD} = 5V, V_{IN} = ±100mV				200		
Output Voltage		I_L = 10mA	V_{DD} = 2.7V	V_{DD} - V_{OH}		128	200	mV
				V_{OL} - V_{SS}		112	175	
		I_L = 30mA	V_{DD} = 5V	V_{DD} - V_{OH}		240	320	
				V_{OL} - V_{SS}		224	300	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = (V_{DD}/2), R_L = ∞ connected to (V_{DD}/2), $V_{\overline{SHDN}}$ = V_{DD}, **T_A = +25°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Supply Current (per Amplifier)	I_{DD}	V_{DD} = 5.5V, V_{CM} = V_{DD} / 2			1.2	2.3	mA
		V_{DD} = 2.7V, V_{CM} = V_{DD} / 2			1.1	2.0	
Shutdown Supply Current (per Amplifier) (Note 3)	$I_{DD(\overline{SHDN})}$	$V_{\overline{SHDN}}$ = 0V, R_L = ∞	V_{DD} = 5.5V		0.5	1	µA
			V_{DD} = 2.7V		0.1	1	
$\overline{SHDN}$ Logic Threshold (Note 3)		Shutdown mode			V_{SS} + 0.3		V
		Normal mode			V_{DD} - 0.3		
$\overline{SHDN}$ Input Bias Current		V_{SS} < $V_{\overline{SHDN}}$ < V_{DD} (Note 3)			50		pA

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = (V_{DD}/2), R_L = ∞ connected to (V_{DD}/2), $V_{\overline{SHDN}}$ = V_{DD}, **T_A = -40 to +125°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{DD}	Inferred from PSRR test			2.7		5.5	V
Input Offset Voltage	V_{OS}						±8	mV
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$					±3		µV/°C
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test			V_{SS}		V_{DD}	V
Common-Mode Rejection Ratio	CMRR	V_{SS} < V_{CM} < V_{DD}			46			dB
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.7V to 5.5V			70			dB
Output Voltage in Shutdown	$V_{OUT(\overline{SHDN})}$	$V_{\overline{SHDN}}$ < 0V, R_L = 200Ω (Note 3)					150	mV
Large-Signal Voltage Gain	A_{VOL}	V_{SS} + 0.2V < V_{DD} - 0.2V		R_L = 2kΩ	76			dB
				R_L = 200Ω	67			
Output Voltage Swing	V_{OUT}	R_L = 32Ω, T_A = +85°C		V_{DD} - V_{OH}			650	mV
				V_{OL} - V_{SS}			650	
		R_L = 200Ω		V_{DD} - V_{OH}			150	
				V_{OL} - V_{SS}			150	
		R_L = 2kΩ		V_{DD} - V_{OH}			20	
				V_{OL} - V_{SS}			20	
Output Voltage		I_L = 10mA	V_{DD} = 2.7V	V_{DD} - V_{OH}			250	mV
				V_{OL} - V_{SS}			230	
		I_L = 30mA, T_A = -40°C to +85°C	V_{DD} = 5V	V_{DD} - V_{OH}			400	
				V_{OL} - V_{SS}			370	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = (V_{DD}/2), R_L = ∞ connected to (V_{DD}/2), $V_{\overline{SHDN}}$ = V_{DD}, **T_A = -40 to +125°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Supply Current (per Amplifier)	I_{DD}	V_{DD} = 5.5V, V_{CM} = V_{DD}/2				2.8	mA
		V_{DD} = 2.7V, V_{CM} = V_{DD}/2				2.5	
Shutdown Supply Current (per Amplifier) (Note 3)	$I_{DD(SHDN)}$	$V_{\overline{SHDN}}$ < 0V, R_L = ∞	V_{DD} = 5.5V			2.0	µA
			V_{DD} = 2.7V			2.0	

AC ELECTRICAL CHARACTERISTICS

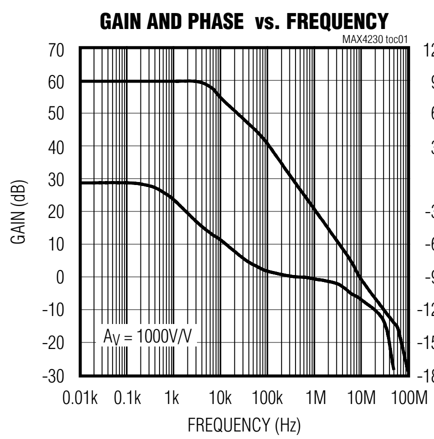
(V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = (V_{DD}/2), R_L = ∞ connected to (V_{DD}/2), $V_{\overline{SHDN}}$ = V_{DD}, **T_A = +25°C**, unless otherwise noted.) (Note 2)

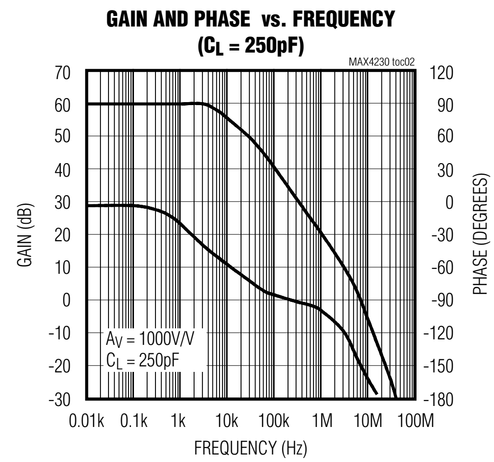
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBWP	V_{CM} = V_{DD}/2		10		MHz
Full-Power Bandwidth	FPBW	V_{OUT} = 2V_{P-P}, V_{DD} = 5V		0.8		MHz
Slew Rate	SR			10		V/µs
Phase Margin	PM			70		Degrees
Gain Margin	GM			15		dB
Total Harmonic Distortion Plus Noise	THD+N	f = 10kHz, V_{OUT} = 2V_{P-P}, A_{VCL} = 1V/V		0.0005		%
Input Capacitance	C_{IN}			8		pF
Voltage-Noise Density	e_n	f = 1kHz		15		nV/√Hz
		f = 10kHz		12		
Channel-to-Channel Isolation		f = 1kHz, R_L = 100kΩ		125		dB
Capacitive-Load Stability		A_{VCL} = 1V/V, no sustained oscillations		780		pF
Shutdown Time	$t_{\overline{SHDN}}$	(Note 3)		1		µs
Enable Time from Shutdown	t_{ENABLE}	(Note 3)		1		µs
Power-Up Time	t_{ON}			5		µs

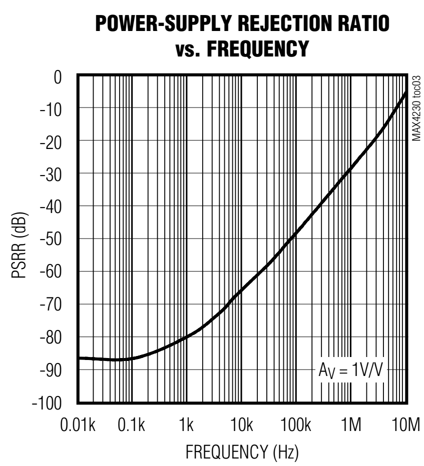
Note 2: All units 100% tested at +25°C. All temperature limits are guaranteed by design.
Note 3: $\overline{\text{SHDN}}$ logic parameters are for the MAX4231/MAX4233 only.

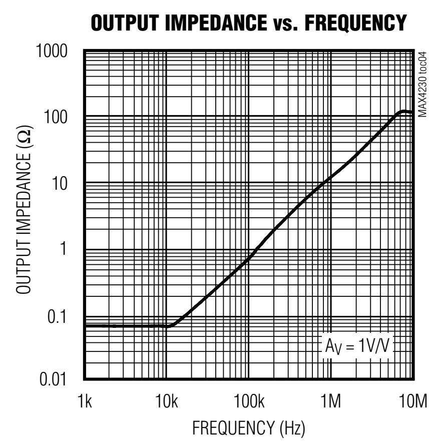
Typical Operating Characteristics

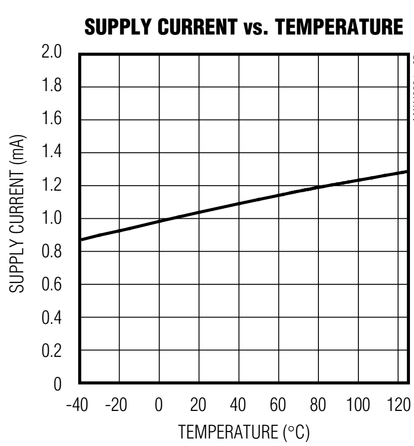
(V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, R_L = ∞, connected to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = +25°C, unless otherwise noted.)

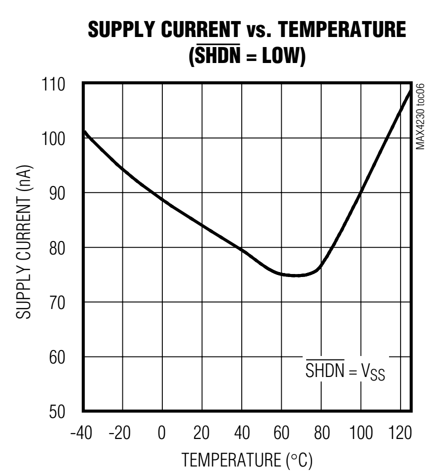








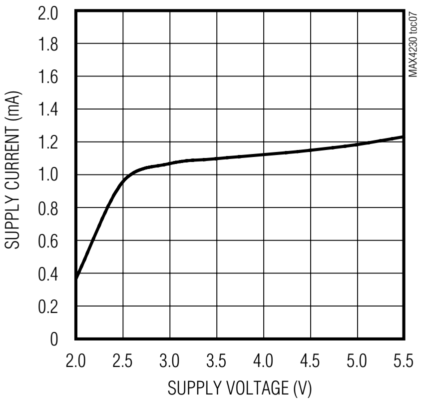




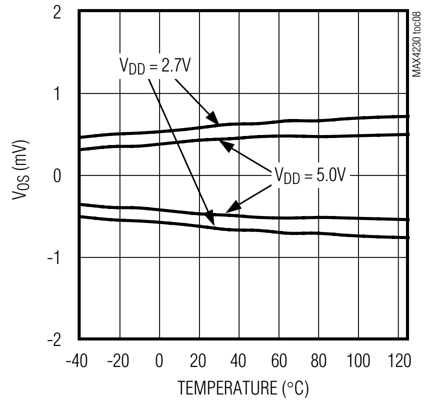
Typical Operating Characteristics (continued)

(V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, R_L = ∞, connected to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = +25°C, unless otherwise noted.)

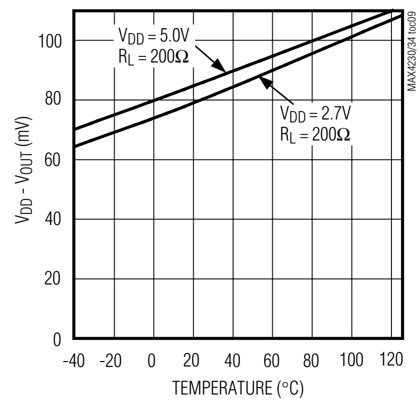
SUPPLY CURRENT PER AMPLIFIER vs. SUPPLY VOLTAGE



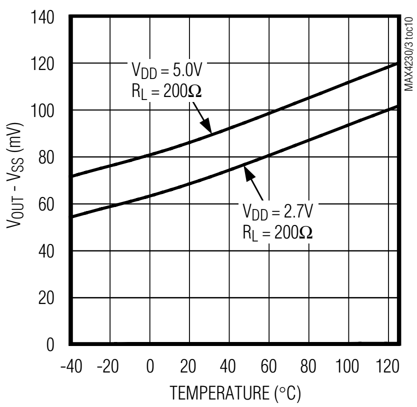
INPUT OFFSET VOLTAGE vs. TEMPERATURE



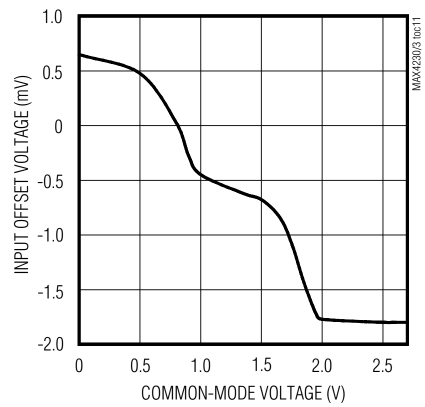
OUTPUT SWING HIGH vs. TEMPERATURE



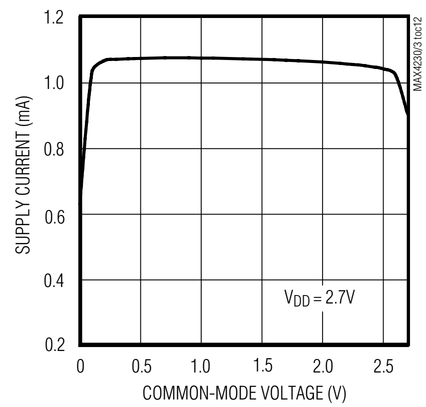
OUTPUT SWING LOW vs. TEMPERATURE



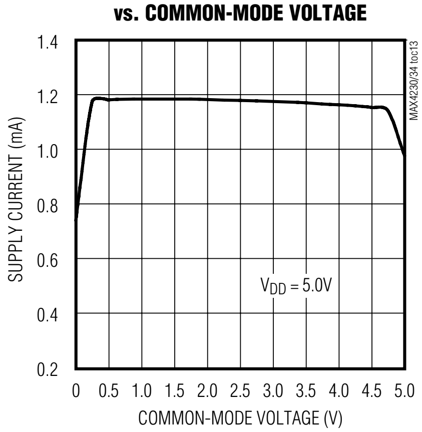
INPUT OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



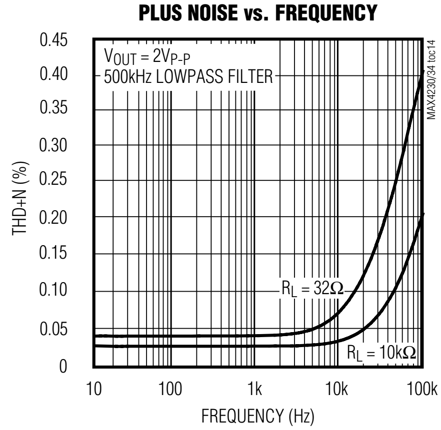
SUPPLY CURRENT PER AMPLIFIER vs. COMMON-MODE VOLTAGE



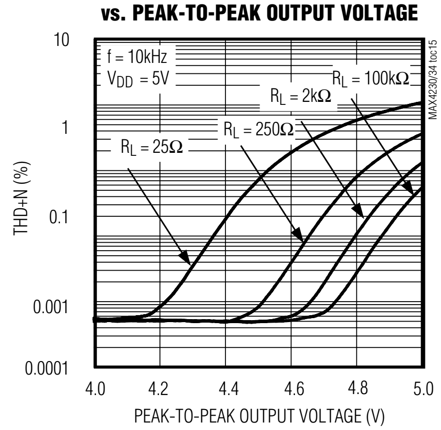
SUPPLY CURRENT PER AMPLIFIER vs. COMMON-MODE VOLTAGE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



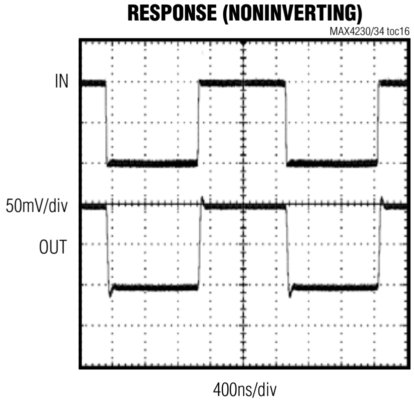
TOTAL HARMONIC DISTORTION PLUS NOISE vs. PEAK-TO-PEAK OUTPUT VOLTAGE



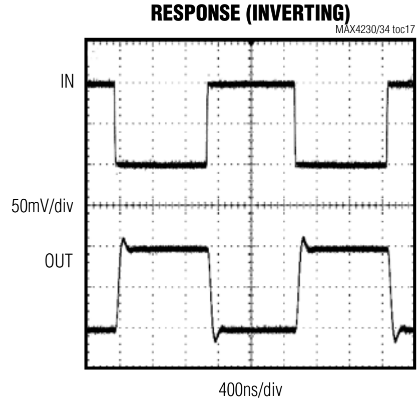
Typical Operating Characteristics (continued)

(V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = $V_{DD}/2$, V_{OUT} = $V_{DD}/2$, R_L = ∞, connected to $V_{DD}/2$, $V_{\overline{SHDN}}$ = V_{DD}, T_A = +25°C, unless otherwise noted.)

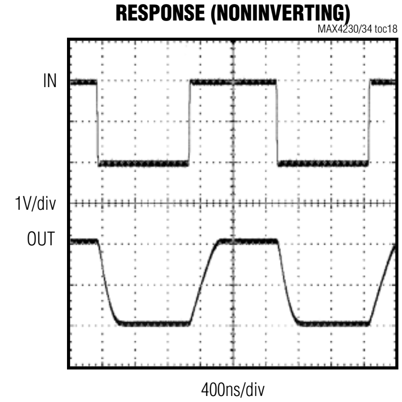
SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



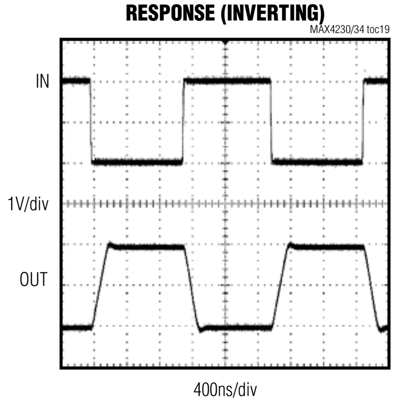
SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)



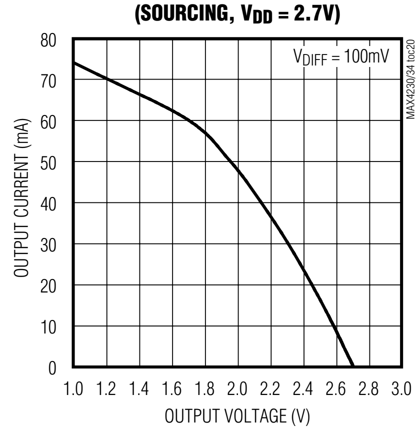
LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



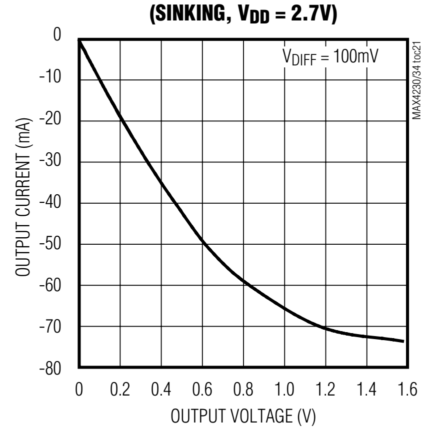
LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



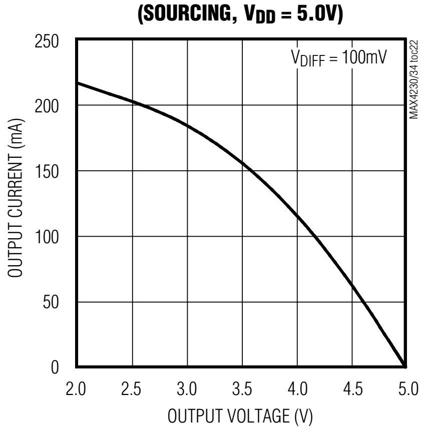
OUTPUT CURRENT vs. OUTPUT VOLTAGE (SOURCING, V_{DD} = 2.7V)



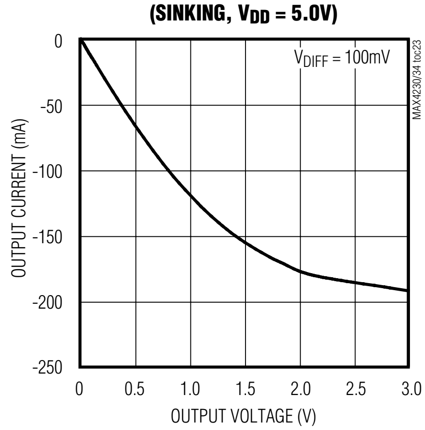
OUTPUT CURRENT vs. OUTPUT VOLTAGE (SINKING, V_{DD} = 2.7V)



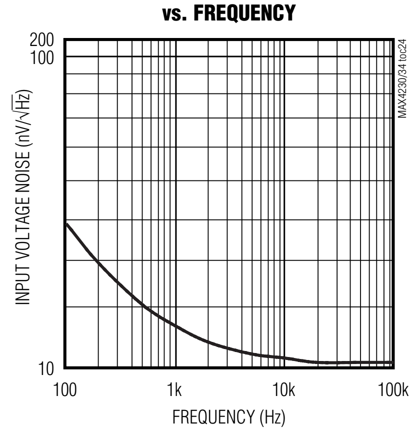
OUTPUT CURRENT vs. OUTPUT VOLTAGE (SOURCING, V_{DD} = 5.0V)



OUTPUT CURRENT vs. OUTPUT VOLTAGE (SINKING, V_{DD} = 5.0V)



INPUT VOLTAGE NOISE vs. FREQUENCY



Pin Description

PIN						NAME	FUNCTION
MAX4230 SOT23/ SC70	MAX4231 SOT23/ SC70/µDFN	MAX4232 SOT23/ µMAX	MAX4233 µMAX/ TDFN	MAX4233 UCSP	MAX4234T SSOP/ SO		
1	1	—	—	—	—	IN+	Noninverting Input
2	2	4	4	B4	11	V_{SS}	Negative Supply Input. Connect to ground for single-supply operation.
3	3	—	—	—	—	IN-	Inverting Input
4	4	—	—	—	—	OUT	Amplifier Output
5	6	8	10	B1	4	V_{DD}	Positive Supply Input
—	5	—	5, 6	C4, A4	—	$\overline{SHDN}$, $\overline{SHDN1}$, $\overline{SHDN2}$	Shutdown Control. Tie to high for normal operation.
—	—	3	3	C3	3	IN1+	Noninverting Input to Amplifier 1
—	—	2	2	C2	2	IN1-	Inverting Input to Amplifier 1
—	—	1	1	C1	1	OUT1	Amplifier 1 Output
—	—	5	7	A3	5	IN2+	Noninverting Input to Amplifier 2
—	—	6	8	A2	6	IN2-	Inverting Input to Amplifier 2
—	—	7	9	A1	7	OUT2	Amplifier 2 Output
—	—	—	—	—	10, 12	IN3+, IN4+	Noninverting Input to Amplifiers 3 and 4
—	—	—	—	—	9, 13	IN3-, IN4-	Inverting Input to Amplifiers 3 and 4
—	—	—	—	—	8, 14	OUT3, OUT4	Amplifiers 3 and 4 Outputs

Detailed Description

Rail-to-Rail Input Stage

The MAX4230–MAX4234 CMOS operational amplifiers have parallel-connected n- and p-channel differential input stages that combine to accept a common-mode range extending to both supply rails. The n-channel stage is active for common-mode input voltages typically greater than (V_{SS} + 1.2V), and the p-channel stage is active for common-mode input voltages typically less than (V_{DD} - 1.2V).

Applications Information

Package Power Dissipation

Warning: Due to the high output current drive, this op amp can exceed the absolute maximum power-dissipation rating. As a general rule, as long as the peak current is less than or equal to 40mA, the maximum package power dissipation is not exceeded for any of the package types offered. There are some exceptions to this rule, however. The absolute maximum power-dissipation rating of each package should always be verified using the following equations. The equation below gives an approximation of the package power dissipation:

$$P_{IC(DISS)} \cong V_{RMS}\, I_{RMS} \cos\theta$$

where:

V_{RMS} = RMS voltage from V_{DD} to V_{OUT} when sourcing current and RMS voltage from V_{OUT} to V_{SS} when sinking current.

I_{RMS} = RMS current flowing out of or into the op amp and the load.

θ = phase difference between the voltage and the current. For resistive loads, COS θ = 1.

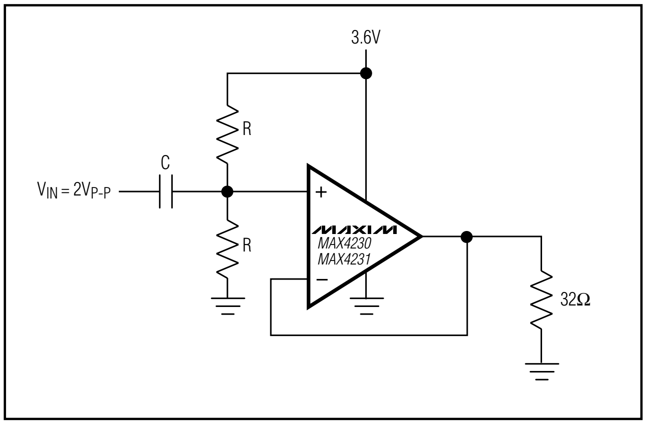


Figure 1. MAX4230/MAX4231 Used in Single-Supply Operation Circuit Example

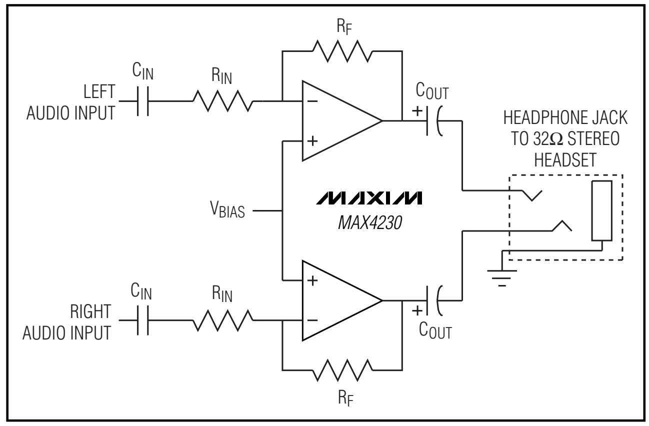


Figure 2. Circuit Example: Adding a Coupling Capacitor Greatly Reduces Power Dissipation of its Package

For example, the circuit in Figure 1 has a package power dissipation of 196mW:

$$\mathrm{RMS} \cong (V_{DD} - V_{DC}) + \frac{V_{PEAK}}{\sqrt{2}}$$

$$= 3.6V - 1.8V + \frac{1.0V}{\sqrt{2}} = 2.507V_{RMS}$$

$$I_{RMS} \cong I_{DC} + \frac{I_{PEAK}}{\sqrt{2}} = \frac{1.8V}{32\Omega} + \frac{1.0V/32\Omega}{\sqrt{2}}$$

$$= 78.4mA_{RMS}$$

where:

V_{DC} = the DC component of the output voltage.

I_{DC} = the DC component of the output current.

V_{PEAK} = the highest positive excursion of the AC component of the output voltage.

I_{PEAK} = the highest positive excursion of the AC component of the output current.

Therefore:

$$P_{IC(DISS)} = V_{RMS}\, I_{RMS} \cos\theta$$

$$= 196mW$$

Adding a coupling capacitor improves the package power dissipation because there is no DC current to the load, as shown in Figure 2:

$$V_{RMS} \cong \frac{V_{PEAK}}{\sqrt{2}}$$

$$= \frac{1.0V}{\sqrt{2}} = 0.707V_{RMS}$$

$$I_{RMS} \cong I_{DC} + \frac{I_{PEAK}}{\sqrt{2}} = 0A + \frac{1.0V/32\Omega}{\sqrt{2}}$$

$$= 22.1mA_{RMS}$$

Therefore:

$$P_{IC(DISS)} = V_{RMS}\, I_{RMS} \cos\theta$$

$$= 15.6mW$$

If the configuration in Figure 1 were used with all four of the MAX4234 amplifiers, the absolute maximum power-dissipation rating of this package would be exceeded (see the *Absolute Maximum Ratings* section).

60mW Single-Supply Stereo Headphone Driver

Two MAX4230/MAX4231s can be used as a single-supply, stereo headphone driver. The circuit shown in Figure 2 can deliver 60mW per channel with 1% distortion from a single 5V supply.

The input capacitor (C_{IN}), in conjunction with R_{IN}, forms a highpass filter that removes the DC bias from the incoming signal. The -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

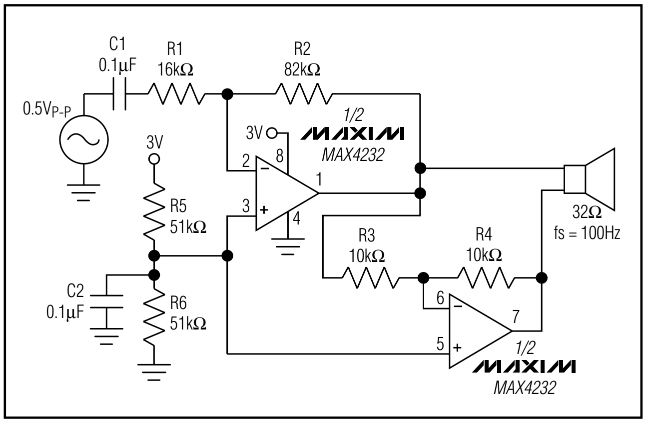


Figure 3. Dual MAX4230/MAX4231 Bridge Amplifier for 200mW at 3V

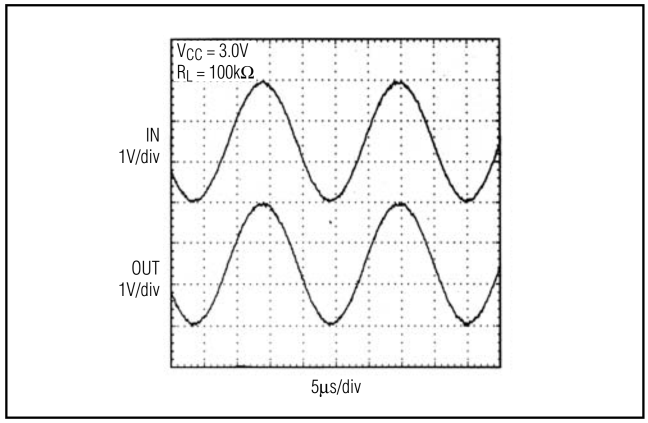


Figure 4. Rail-to-Rail Input/Output Range

Choose gain-setting resistors R_{IN} and R_F according to the amount of desired gain, keeping in mind the maximum output amplitude. The output coupling capacitor, C_{OUT}, blocks the DC component of the amplifier output, preventing DC current flowing to the load. The output capacitor and the load impedance form a highpass filer with the -3dB point determined by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

For a 32Ω load, a 100µF aluminum electrolytic capacitor gives a low-frequency pole at 50Hz.

Bridge Amplifier

The circuit shown in Figure 3 uses a dual MAX4230 to implement a 3V, 200mW amplifier suitable for use in size-constrained applications. This configuration eliminates the need for the large coupling capacitor required by the single op-amp speaker driver when single-supply operation is necessary. Voltage gain is set to 10V/V; however, it can be changed by adjusting the 82kΩ resistor value.

Rail-to-Rail Input Stage

The MAX4230–MAX4234 CMOS op amps have parallel-connected n- and p-channel differential input stages that combine to accept a common-mode range extending to both supply rails. The n-channel stage is active for common-mode input voltages typically greater than (V_{SS} + 1.2V), and the p-channel stage is active for common-mode input voltages typically less than (V_{DD} - 1.2V).

Rail-to-Rail Output Stage

The minimum output is within millivolts of ground for single-supply operation, where the load is referenced to ground (V_{SS}). Figure 4 shows the input voltage range and the output voltage swing of a MAX4230 connected as a voltage follower. The maximum output voltage swing is load dependent; however, it is guaranteed to be within 500mV of the positive rail (V_{DD} = 2.7V) even with maximum load (32Ω to ground).

Observe the *Absolute Maximum Ratings* for power dissipation and output short-circuit duration (10s, max) because the output current can exceed 200mA (see the *Typical Operating Characteristics*.)

Input Capacitance

One consequence of the parallel-connected differential input stages for rail-to-rail operation is a relatively large input capacitance C_{IN} (5pF typ). This introduces a pole at frequency $(2\pi R' C_{IN})^{-1}$, where R′ is the parallel combination of the gain-setting resistors for the inverting or noninverting amplifier configuration (Figure 5). If the pole frequency is less than or comparable to the unity-gain bandwidth (10MHz), the phase margin is reduced, and the amplifier exhibits degraded AC performance through either ringing in the step response or sustained oscillations. The pole frequency is 10MHz when R′ = 2kΩ. To maximize stability, R′ << 2kΩ is recommended.

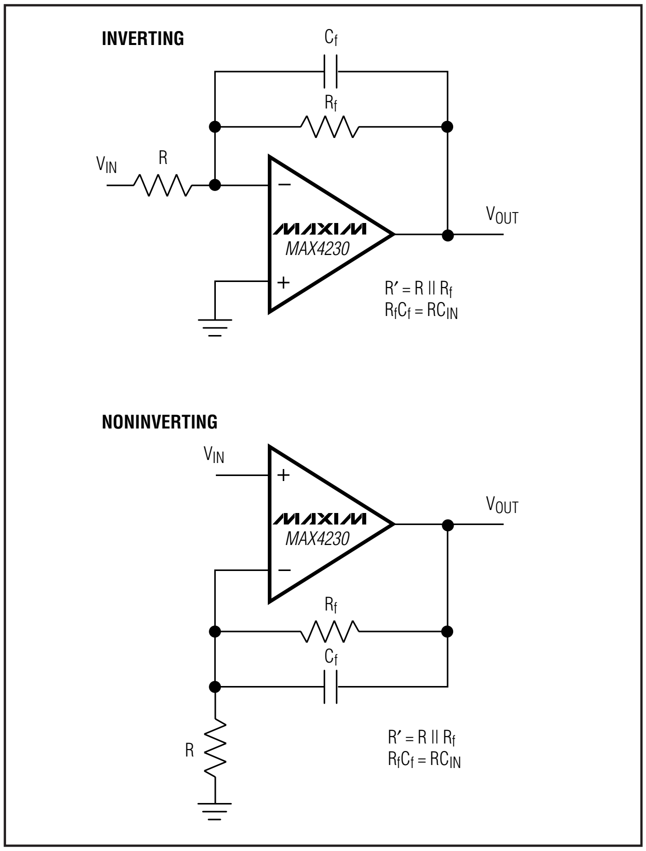


Figure 5. Inverting and Noninverting Amplifiers with Feedback Compensation

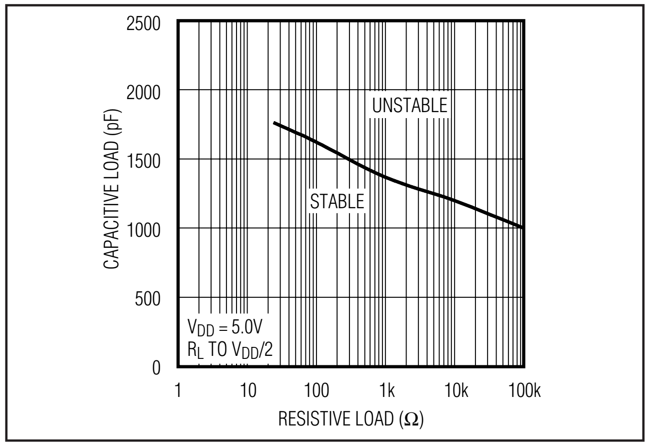


Figure 6. Capacitive-Load Stability

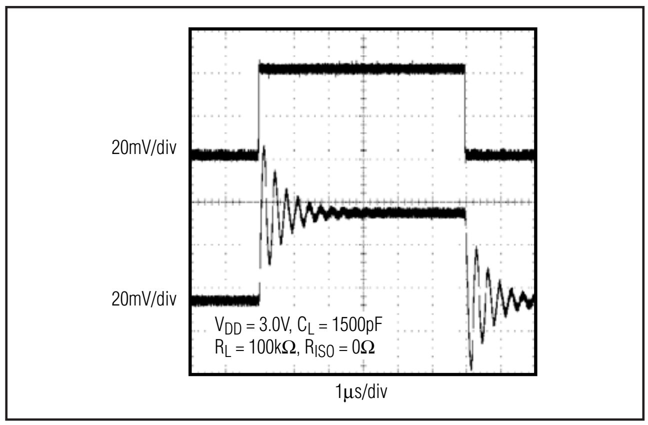


Figure 7. Small-Signal Transient Response with Excessive Capacitive Load

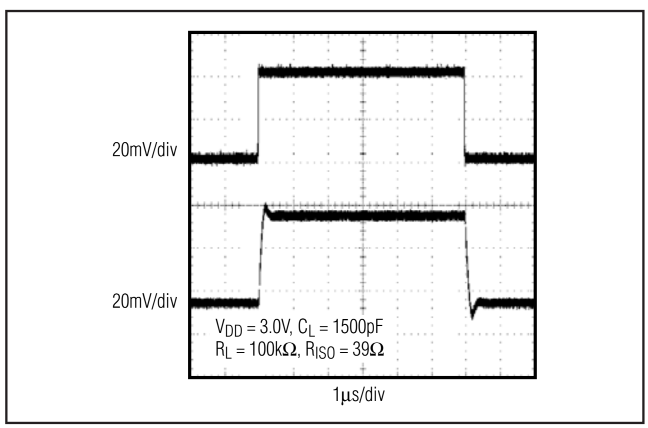


Figure 8. Small-Signal Transient Response with Excessive Capacitive Load with Isolation Resistor

To improve step response when $R' > 2k\Omega$, connect small capacitor C_f between the inverting input and output. Choose C_f as follows:

$$C_f = 8(R / R_f)\ [pf]$$

where R_f is the feedback resistor and R is the gain-setting resistor (Figure 5).

Driving Capacitive Loads

The MAX4230–MAX4234 have a high tolerance for capacitive loads. They are stable with capacitive loads up to 780pF. Figure 6 is a graph of the stable operating region for various capacitive loads vs. resistive loads. Figures 7 and 8 show the transient response with excessive capacitive loads (1500pF), with and without the addition of an isolation resistor in series with the output. Figure 9 shows a typical noninverting capacitive-load-driving circuit in the unity-gain configuration.

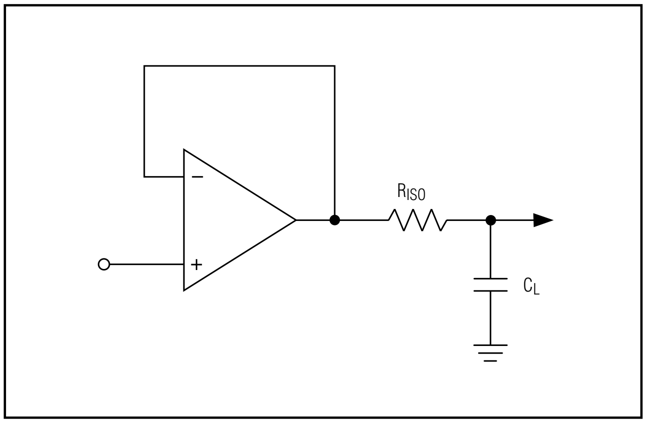


Figure 9. Capacitive-Load-Driving Circuit

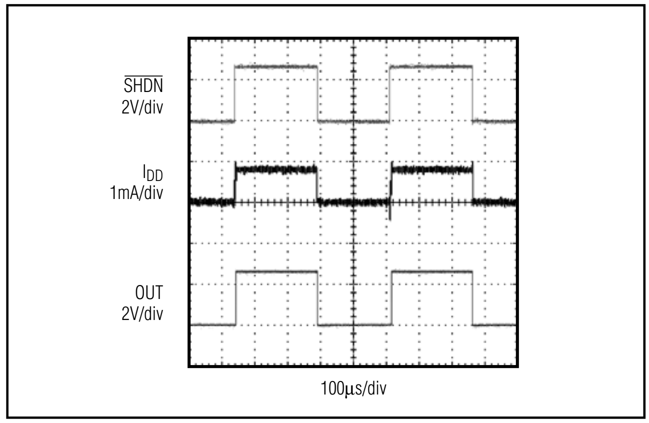


Figure 11. Shutdown Enable/Disable Supply Current

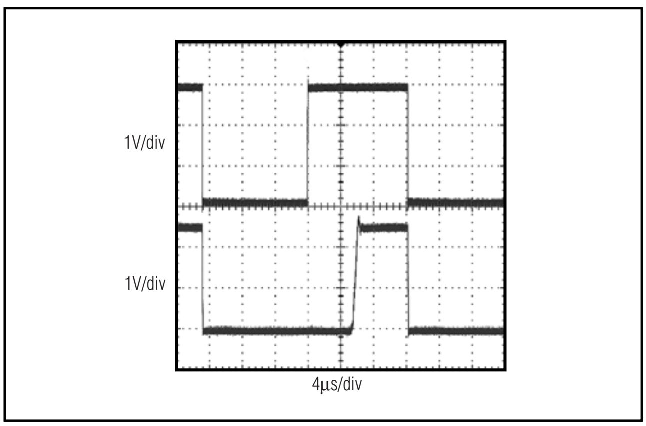


Figure 10. Shutdown Output Voltage Enable/Disable

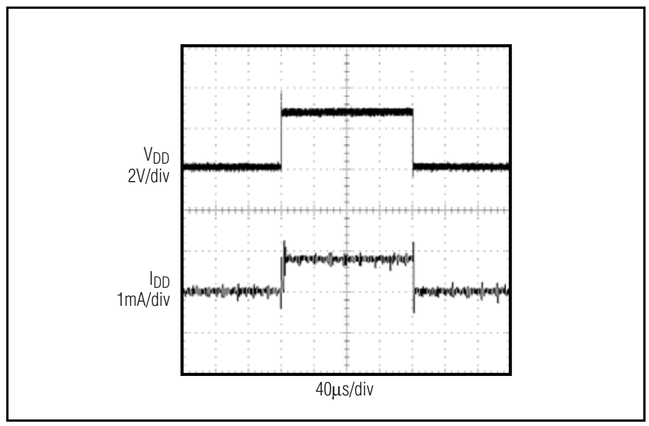


Figure 12. Power-Up/Down Supply Current

The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

Power-Up and Shutdown Modes

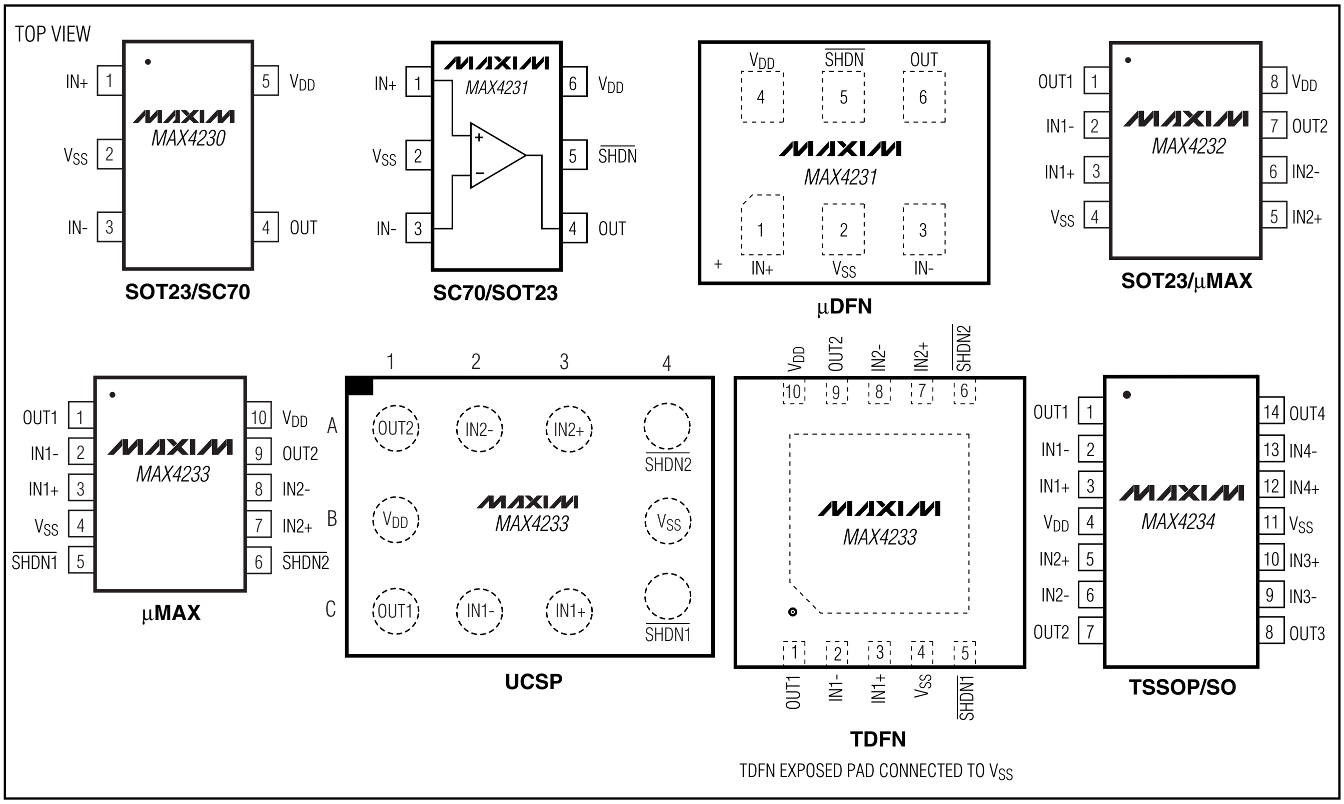
The MAX4231/MAX4233 have a shutdown option. When the shutdown pin ($\overline{SHDN}$) is pulled low, supply current drops to 0.5μA per amplifier (V_{DD} = 2.7V), the amplifiers are disabled, and their outputs are driven to V_{SS}. Since the outputs are actively driven to V_{SS} in shutdown, any pullup resistor on the output causes a current drain from the supply. Pulling $\overline{SHDN}$ high enables the amplifier. In the dual MAX4233, the two amplifiers shut down independently. Figure 10 shows the MAX4231's output voltage to a shutdown pulse. The MAX4231–MAX4234 typically settle within 5μs after power-up. Figures 11 and 12 show I_{DD} to a shutdown plus and voltage power-up cycle.

Selector Guide

PART	AMPS PER PACKAGE	SHUTDOWN MODE
MAX4230	Single	—
MAX4231	Single	Yes
MAX4232	Dual	—
MAX4233	Dual	Yes
MAX4234	Quad	—

When exiting shutdown, there is a 6μs delay before the amplifier's output becomes active (Figure 10).

Pin Configurations



Power Supplies and Layout

The MAX4230–MAX4234 can operate from a single 2.7V to 5.5V supply, or from dual ±1.35V to ±2.5V supplies. For single-supply operation, bypass the power supply with a 0.1µF ceramic capacitor. For dual-supply operation, bypass each supply to ground. Good layout improves performance by decreasing the amount of stray capacitance at the op amps' inputs and outputs. Decrease stray capacitance by placing external components close to the op amps' pins, minimizing trace and lead lengths.

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4232AKA+T	-40°C to +125°C	8 SOT23-8	AAKW
MAX4232AUA+T	-40°C to +125°C	8 µMAX-8	—
MAX4233AUB+T	-40°C to +125°C	10 µMAX-10	—
MAX4233ABC+T	-40°C to +125°C	10 UCSP-10	ABE
MAX4233ATB+T	-40°C to +125°C	10 TDFN-EP*	+AQH
MAX4234AUD	-40°C to +125°C	14 TSSOP	—
MAX4234ASD	-40°C to +125°C	14 SO	—

+Denotes a lead-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Chip Information

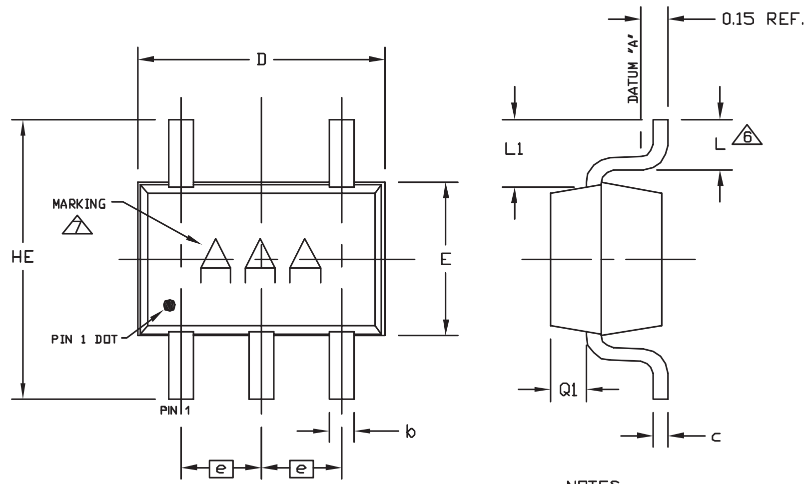
MAX4230 TRANSISTOR COUNT: 230
MAX4231 TRANSISTOR COUNT: 230
MAX4232 TRANSISTOR COUNT: 462
MAX4233 TRANSISTOR COUNT: 462
MAX4234 TRANSISTOR COUNT: 924

High-Output-Drive, 10MHz, 10V/µs, Rail-to-Rail I/O Op Amps with Shutdown in SC70

Package Information

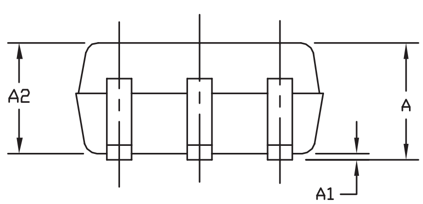
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SC70, 5L.EPS



COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.80	2.00	2.20
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.20	2.40
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODE	X5-1		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COMPLY TO JEITA SC-88A EXCEPT FOR DIMENSION "L". ALL DIMENSIONS COMPLY TO JEDEC MO-203.
5. COPLANARITY 4 MILS. MAX.
6. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.



-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

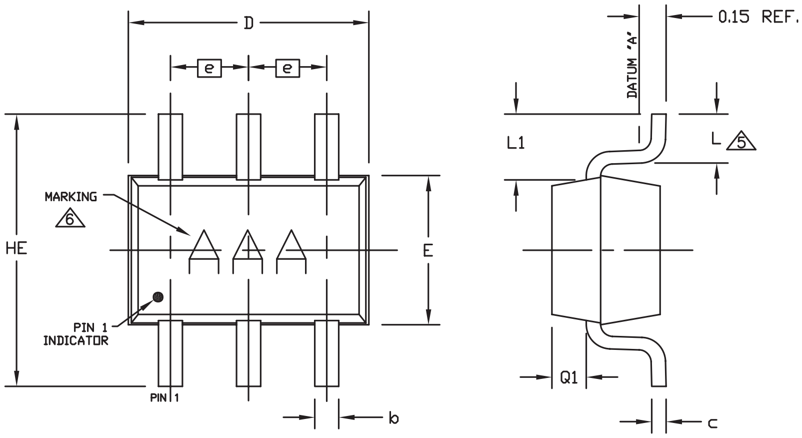
TITLE: PACKAGE OUTLINE, 5L SC70

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0076	E	1/1

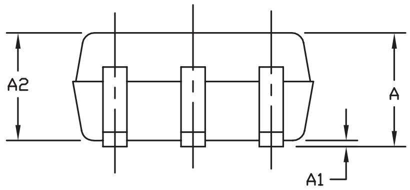
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SC70, 6L.EPS



COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.80	2.00	2.20
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.20	2.40
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODES	X6SN-1		



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM 'A' AND LEAD SURFACE.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
8. ALL DIMENSIONS COMPLY TO JEDEC MO-203.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

MAXIM

TITLE: PACKAGE OUTLINE, 6L SC70

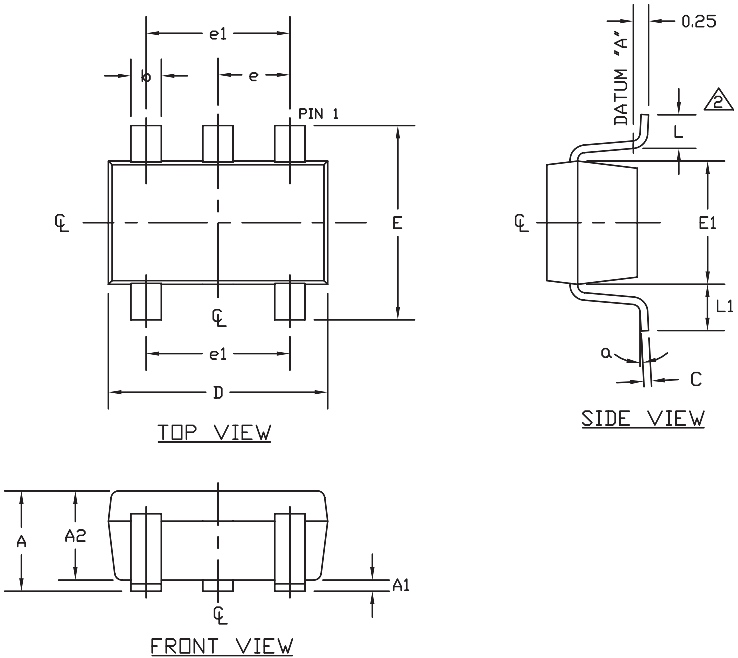
APPROVAL | DOCUMENT CONTROL NO. 21-0077 | REV. G | 1/1

-DRAWING NOT TO SCALE-

High-Output-Drive, 10MHz, 10V/µs, Rail-to-Rail I/O Op Amps with Shutdown in SC70

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1	0.60 REF		
e	0.95 BSC.		
e1	1.90 BSC.		
α	0°	2.5°	8°
PKG CODES: U5-1, U5-2			

SOT-23 5L .EPS

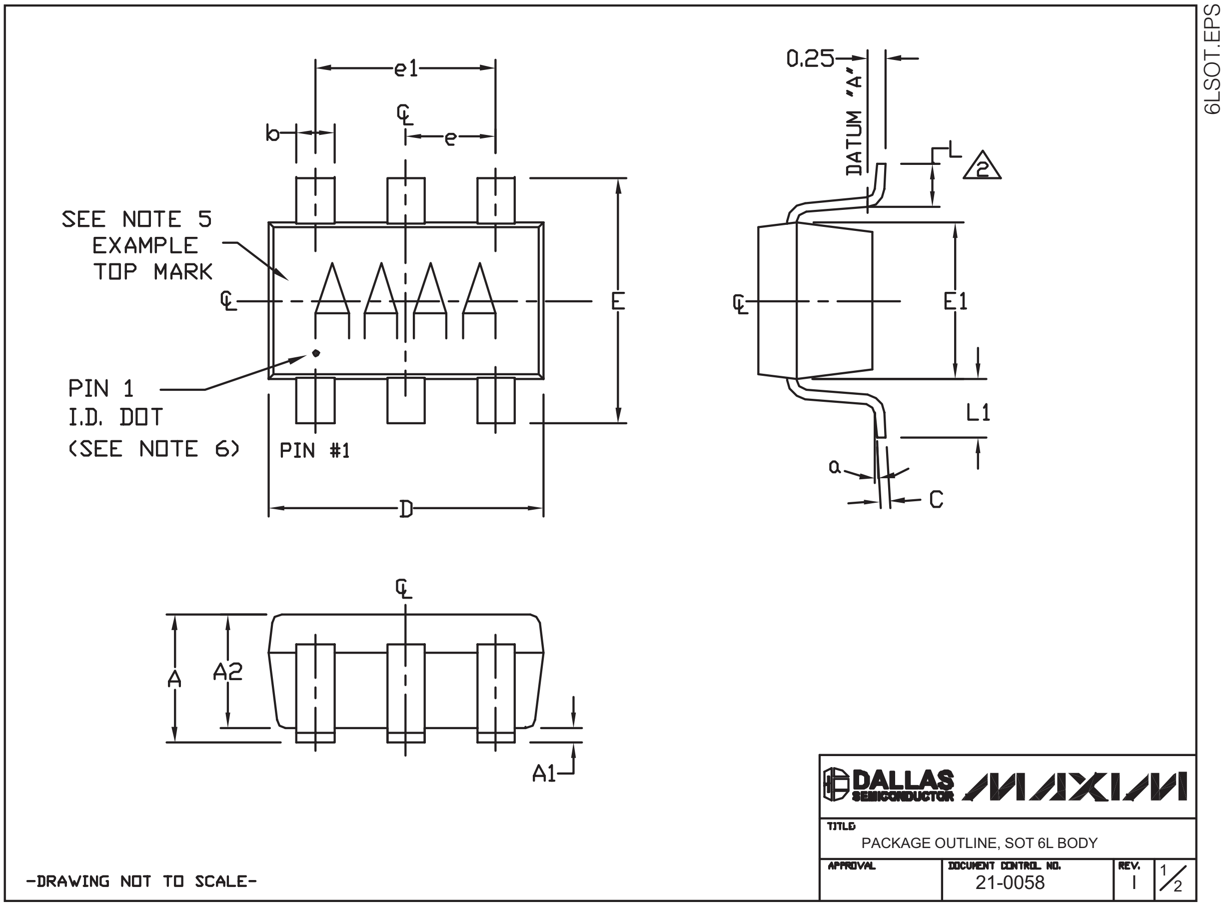
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. MEETS JEDEC MO178, VARIATION AA.
6. LEADS TO BE COPLANAR WITHIN 0.10 mm.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SOT-23, 5L

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0057	F	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25mm.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3mm ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1mm.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

SYMBOL	MIN	NOMINAL	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1		0.60 REF.	
e1		1.90 BSC.	
e		0.95 BSC.	
α	0°	2.5°	10°

PKG CODES:
U6-1, U6-2, U6-4, U6C-8, U6SN-1, U6CN-2, U6S-3, U6F-5, U6F-6, U6FH-5, U6FH-6

-DRAWING NOT TO SCALE-

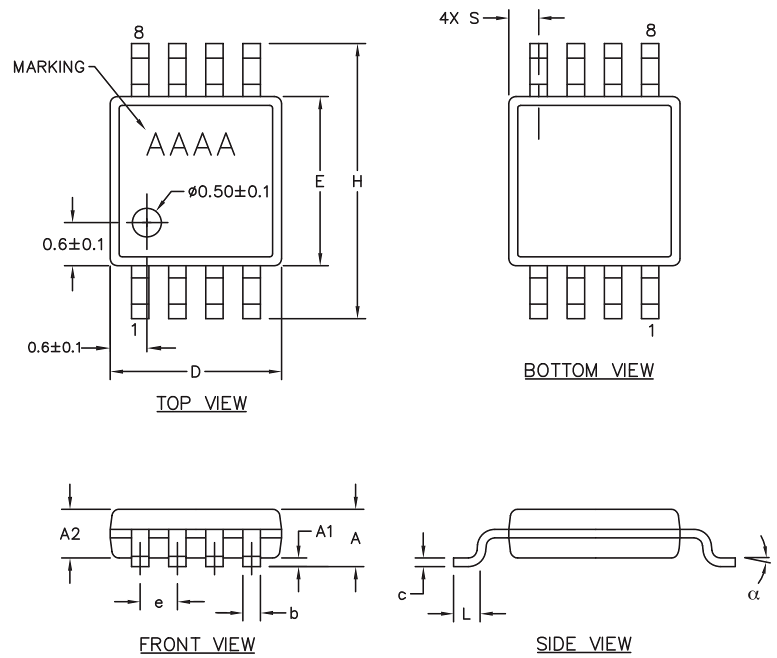
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, SOT 6L BODY

APPROVAL | DOCUMENT CONTROL NO. 21-0058 | REV. I | 2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



8LUMAXD.EPS

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	

PKG. CODES:
U8–1; U8–3; U8C–3; U8CN–1

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO–187, LATEST REVISION, VARIATION AA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

MAXIM

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

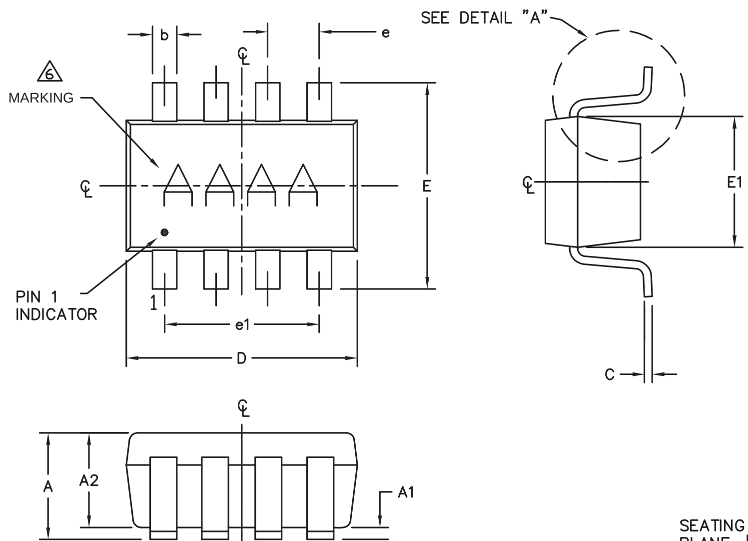
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21–0036	K	1/1

High-Output-Drive, 10MHz, 10V/µs, Rail-to-Rail I/O Op Amps with Shutdown in SC70

Package Information (continued)

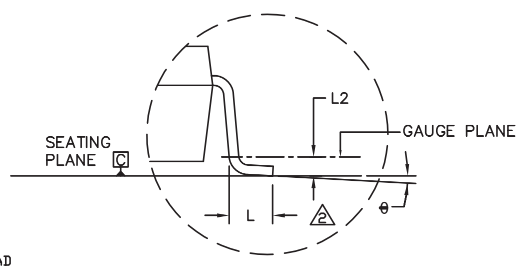
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOT23, 8L.EPS



SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.06	0.15
A2	0.90	1.10	1.30
b	0.22	0.30	0.38
C	0.08	0.15	0.22
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.30	0.45	0.60
L2	0.25 BSC.		
e	0.65 BSC.		
e1	1.95 REF.		
θ	0°	3°	8°

PKG CODES:
K8-1, K8-2, K8F-4, K8FH-4, K8-5,
K8C-6; K8SN-1



DETAIL "A"

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

MAXIM

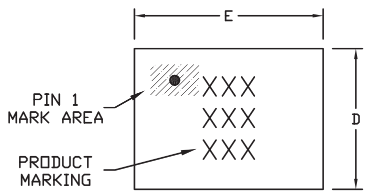
TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0078	H	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

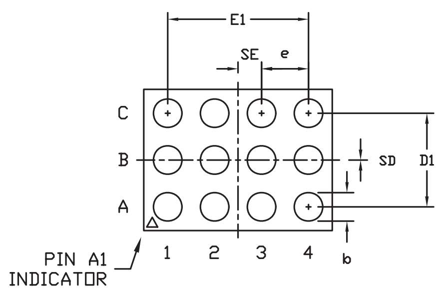
12L, UCSP 4x3.EPS



TOP VIEW

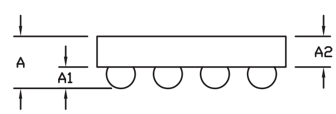
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B12-1	1.54±0.05	2.02±0.05	NONE
B12-2	1.54±0.05	2.02±0.05	B3
B12-3	1.54±0.05	2.12±0.05	NONE
B12-4	1.54±0.05	2.02±0.05	B2, B3
B12-5	1.64±0.05	2.12±0.05	B2
B12-6	1.64±0.05	2.12±0.05	B3
B12-7	1.54±0.05	2.02±0.05	B1, B3
B12-8	1.54±0.05	2.02±0.05	B2
B12-9	1.54±0.05	2.12±0.05	B2, B3
B12-10	1.54±0.05	2.02±0.05	B1, B2, B3, B4
B12-11	1.54±0.05	2.02±0.05	A2, C3



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

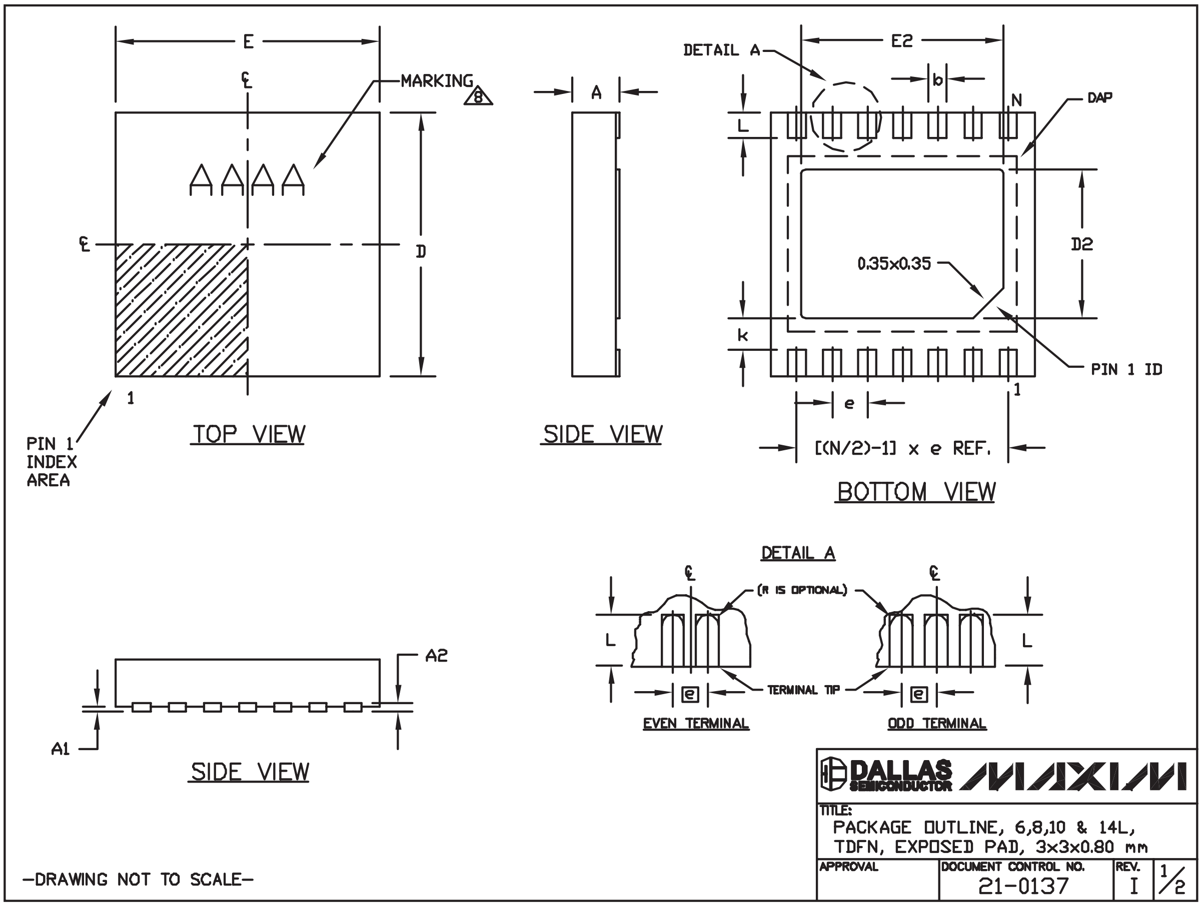
TITLE: PACKAGE OUTLINE, 4x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0104	F	1/1

High-Output-Drive, 10MHz, 10V/µs, Rail-to-Rail I/O Op Amps with Shutdown in SC70

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



6, 8, &10L, DFN THIN.EPS

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

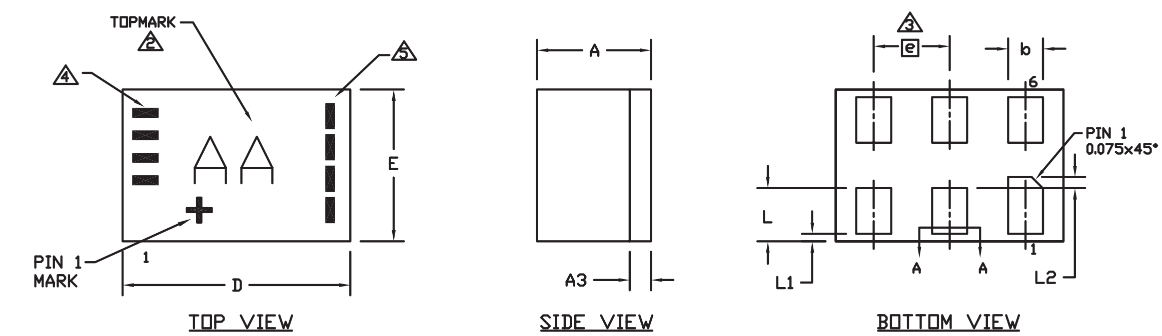
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	I	2/2

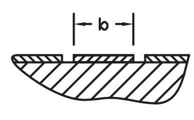
-DRAWING NOT TO SCALE-

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6L ULTRA THINLGA.EPS





SECTION A-A

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.
A	0.45	0.50	0.55
A3	0.15 REF		
D	1.45	1.50	1.55
E	0.95	1.00	1.05
L	0.30	0.35	0.40
L1	0.00	--	0.08
L2	0.05	--	0.10
b	0.15	0.20	0.25
e	0.50 BSC.		
Pkg. Code	Y61A1-1		

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY. PACKAGE USES 2 CHARACTER PRODUCT CODE.
3. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
4. CALENDAR YEAR BINARY DATE CODE (REFER TO PG. 2 TABLE 1 FOR TRANSLATION).
5. 6 WEEKLY DATE BINARY CODE (REFER TO PG. 2 TABLE 2 FOR TRANSLATION).
6. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC# 10-0131.
7. MEETS JEDEC MO-252 VARIATION WAAD.
8. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

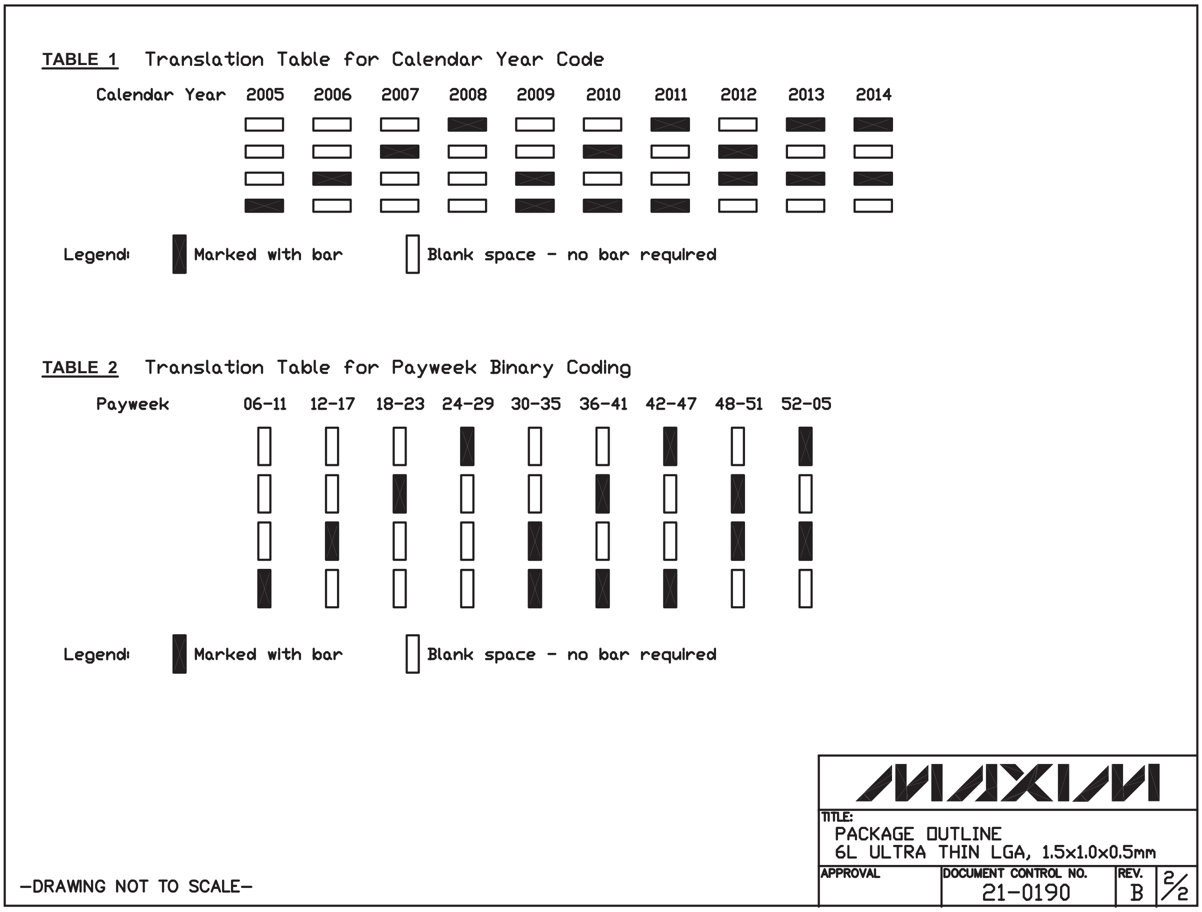
MAXIM

TITLE: PACKAGE OUTLINE
6L ULTRA THIN LGA, 1.5x1.0x0.5mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0190	B	1/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



High-Output-Drive, 10MHz, 10V/µs, Rail-to-Rail I/O Op Amps with Shutdown in SC70

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
7	7/08	Added 6-pin µDFN package for the MAX4231	1, 2, 8, 13

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