Reducing Ringing Through PCB Layout Techniques

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ABSTRACT

Designers must consider several topics when designing a printed-circuit board (PCB) layout for a dc-to-dc converter. In particular, the layout of the Power Stage components within a nonisolated synchronous buck converter requires special attention in order to optimize the overall performance of the switching function. The Power Stage in this application report is defined to include the input capacitors, power MOSFETs, driver IC, and output inductor (see Figure 1).

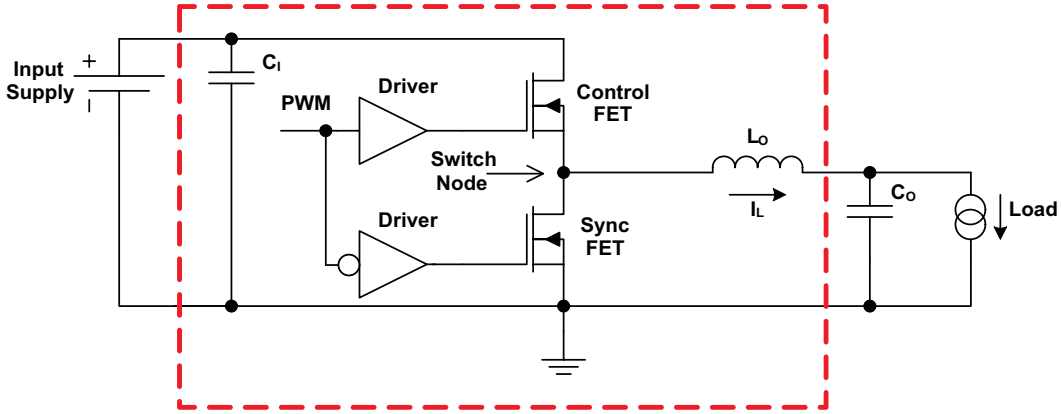

Figure 1. Definition of Power Stage Components

This document discusses the topic of *voltage ringing* commonly found to be superimposed on the *rising edge* of the switch node (V_{SW}) waveform. It also describes how to optimize the PCB layout design to minimize the magnitude of the ringing.

Background

The two major industry concerns toward the ringing commonly found to be superimposed on the switch node waveform are:

1. Voltage Margin
   - This is a percentage ratio which takes the magnitude of the first peak within the ringing waveform and compares it to the breakdown voltage of the power MOSFET (BV_{DSS}).
2. EMI/EMC
   - This the amount of conducted or radiated noise produced by the ringing waveform.

This application report only addresses the topic of voltage margin and does not focus on the topic of EMI/EMC. The topic of EMI/EMC can be somewhat subjective and greatly depends on the overall system/chassis design. However, the enhancements outlined in this document can improve the overall EMI/EMC performance of the system.

In terms of voltage margin, designers occasionally impose an 80% margin rule. This means that the maximum voltage measured across the drain to source of any MOSFET must not exceed 80% of the MOSFET's BV_{DSS}. For example, a MOSFET with a BV_{DSS} = 25 V requires only 20 V applied across the device at any given time. As such, power supply designers need to have a solution to address a situation that yields ringing that may exceed their voltage margin requirements.

Optimized Placement of Power Stage Components

The Control FET has the ability to switch voltages at rates greater than 10 kV/µs. Special care must be taken with the PCB layout design and placement of the Power Stage components in order to minimize voltage ringing at the switch node of this topology. Of particular importance is the placement of the input capacitors relative to the power MOSFETs. It is important to minimize the node lengths between these components.

1. Minimize the node length between the positive terminal of the input capacitors and the Drain pin of the Control FET.
2. Minimize the node length between the negative terminal of the input capacitors and the Source pin of the Sync FET.

A traditional placement of the Power Stage components is shown in Figure 2. Typically, one of these two node lengths is compromised. This results in a higher parasitic inductance between the power MOSFETs and the input capacitors which may yield higher than expected voltage ringing on the switch node. An optimized placement of the Power Stage components is shown in Figure 3. Both node lengths have been minimized which in turn minimizes the parasitic inductances.

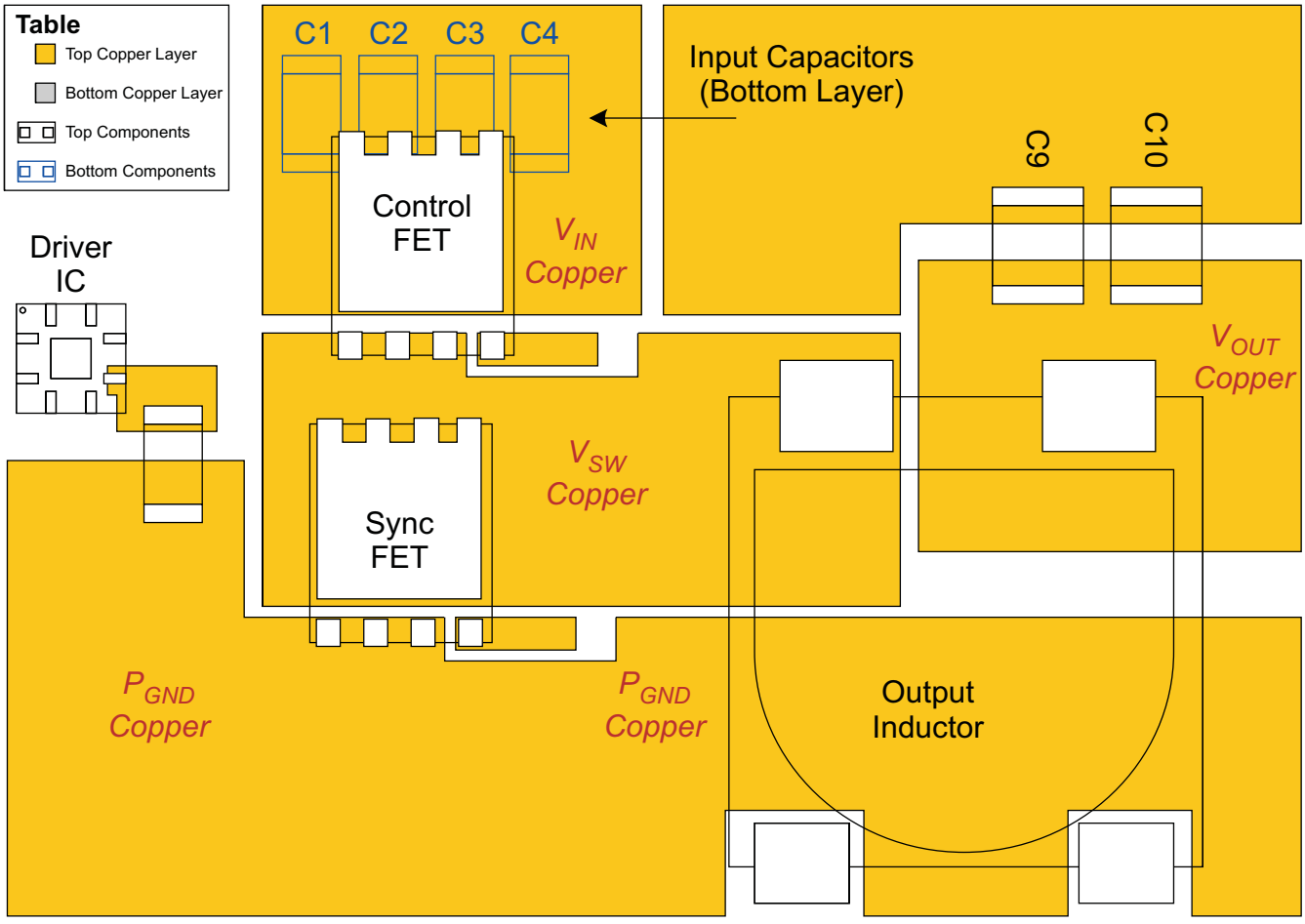

Figure 2. Typical Placement and PCB Layout of the Power Stage Components

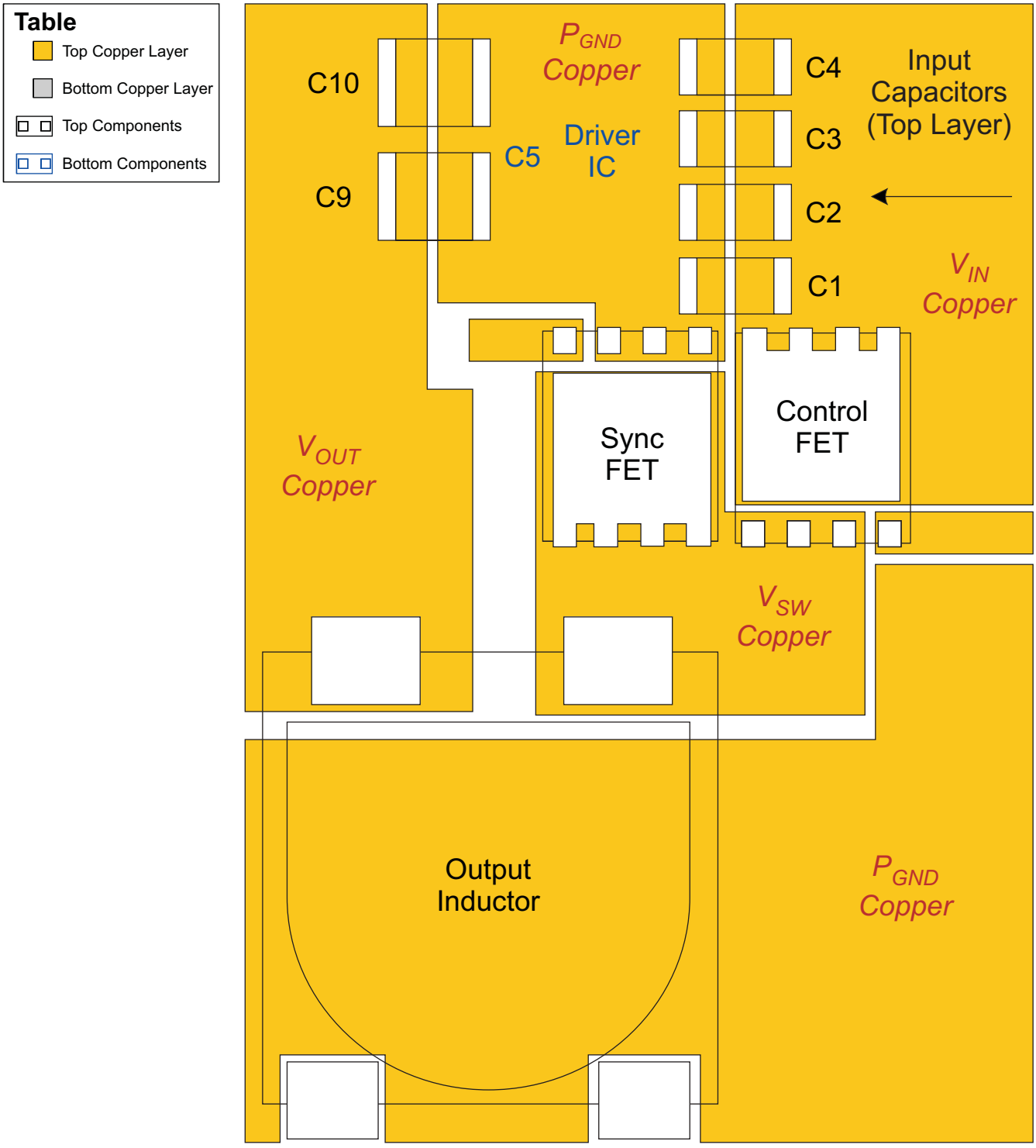

Figure 3. Optimized Placement and PCB Layout of Power Stage Components

The most important difference between Figure 2 and Figure 3 is the distance between the input capacitors and the power MOSFETs. In Figure 3, the Sync FET has been rotated 180° and placed to the left of the Control FET. The input capacitors have been moved to the top layer and placed next to the Drain pins of

the Control FET and the Source pins of the Sync FET. In both examples, ceramic input capacitors were used due to the inherently low equivalent series inductance (ESL) of these types of capacitors (10 µF, 16 V, 1206, X5R, TDK C3216X5R1A106M). In addition, the optimized layout allows the placement of the driver IC to be put directly below the power MOSFETs on the bottom layer. This minimizes the distance of gate drive traces.

Testing of Layouts

Figure 4 shows the ringing found on the switch node of the PCB layout example depicted in Figure 2. In this example, the amplitude of the ringing reaches 25 V. If the power MOSFETs used in this example were rated for 25 V (BV_{DSS}), then the amplitude of the voltage ringing yields no design margin as outlined in item 1 in the Background section of this document. Figure 5 shows the ringing found on the switch node of the PCB layout example depicted in Figure 3. In this example, the amplitude of the ringing reaches 20 V. By simply optimizing the placement of the power MOSFETs and input capacitors, the voltage ringing amplitude can be reduced by 5 V. If this design used 25-V rated power MOSFETs, the amplitude of the voltage ringing waveform meets the typical margin requirements.

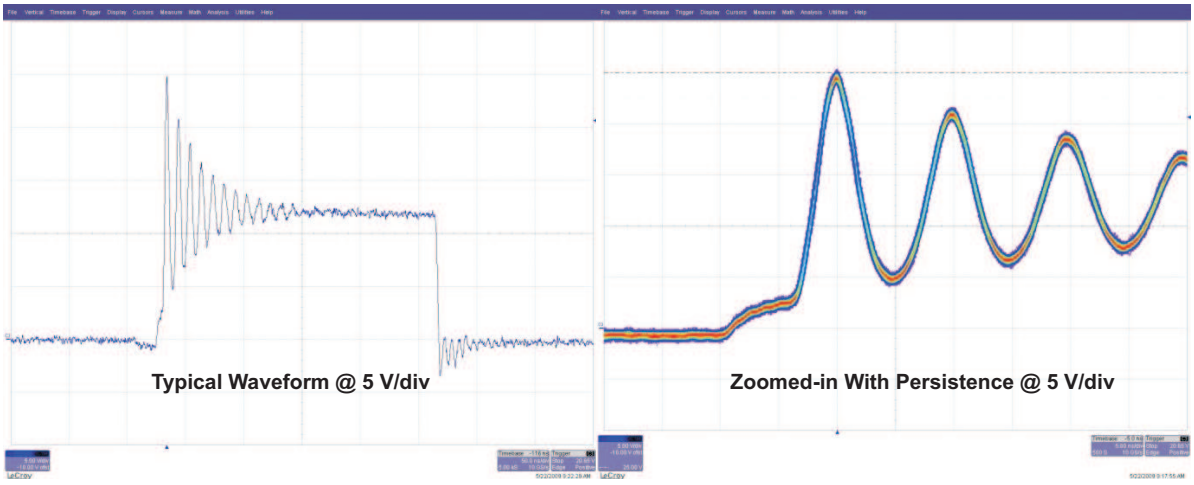

Figure 4. Switch Node (VSW) Voltage Ringing on Typical Layout

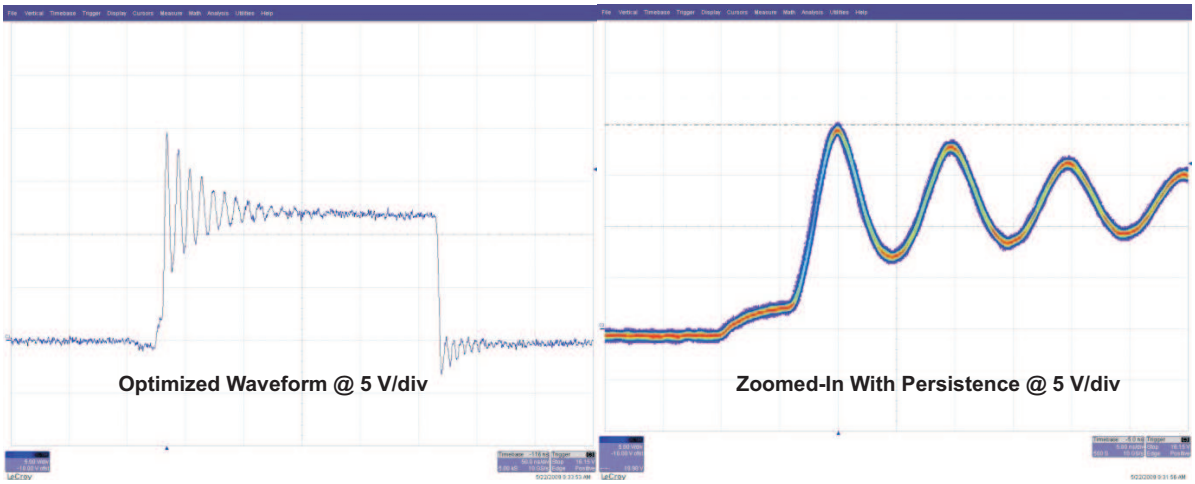

Figure 5. Switch Node (VSW) Voltage Ringing on Optimized Layout

Measurement Techniques

It is important to accurately measure the voltage applied across any power MOSFET in an application. The voltage measurement across the synchronous MOSFET's Drain and Source terminals (the switch node) is particularly important because the high rate of change in voltage imposed by the switching MOSFET induces a certain level of voltage ringing. The peak values of this voltage ringing may be misinterpreted if not properly measured. The following measurement tips can help minimize the overall measurement error.

1. The ground lead length of an oscilloscope probe is the most important item in properly capturing the peak values of the switch node voltage ringing. Do not use the standard 3-inch long ground wire supplied with the oscilloscope probe. The long wire loop will act as an antenna by picking up any radiated noised emitted by the system board and will yield a higher value of switch node voltage ringing than what is actually seen by the device (see Figure 6 and Figure 7). Instead, use a small-length ground wire that attaches to the oscilloscope probe tip end (see Figure 8).
2. Placement of the oscilloscope tip and ground must be right on the MOSFET leads. Placement anywhere else introduces higher voltage ringing induced by the PCB parasitic inductance.

A combination of these measurement tips can yield a proper measurement of the actual voltage ringing seen by the synchronous MOSFET.

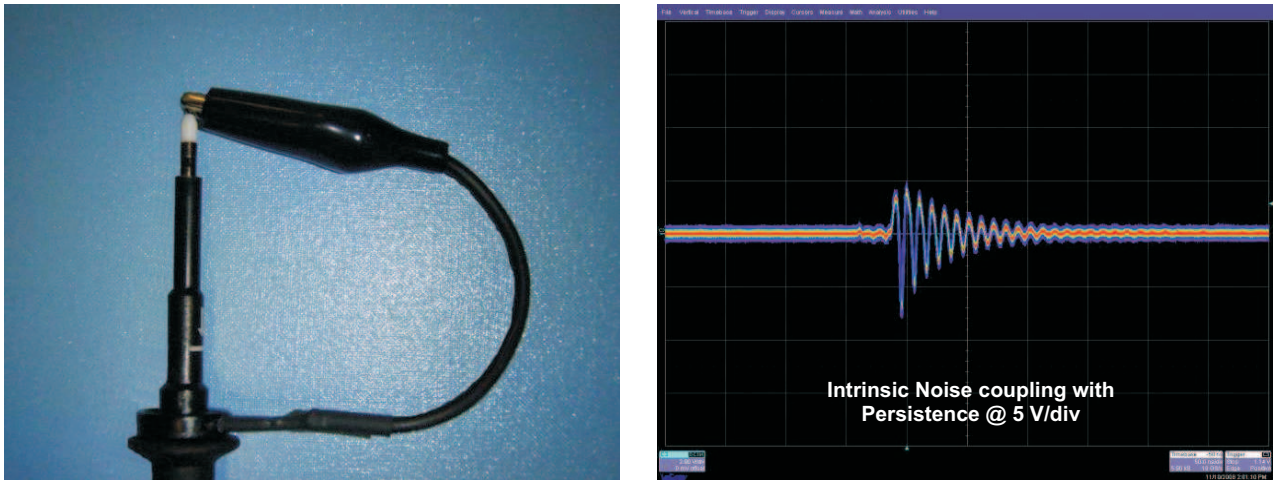

Figure 6. Ringing Voltage Pick-up by 3-Inch Ground Wire

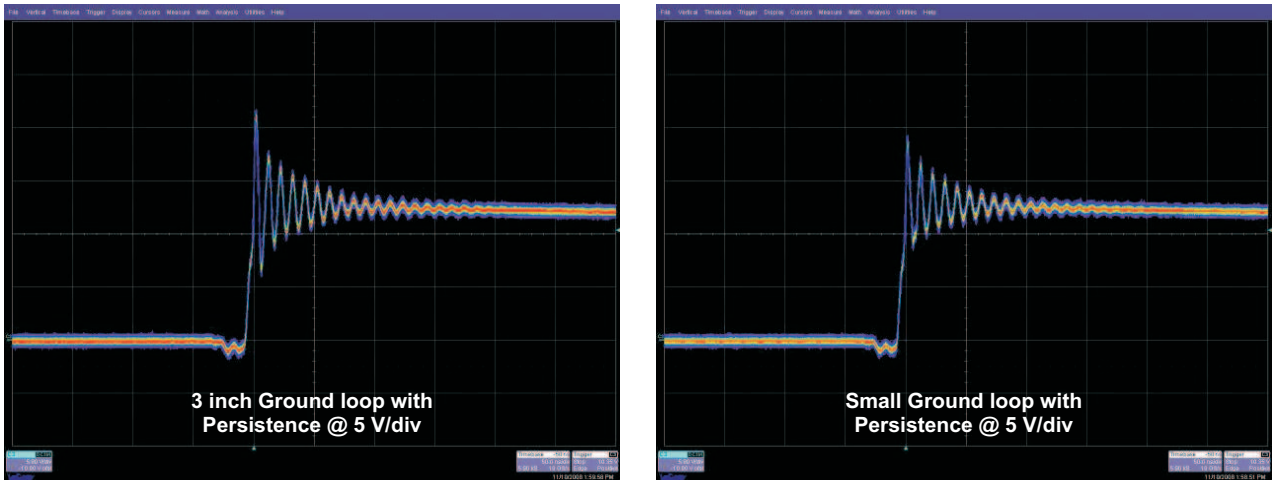

Figure 7. Switch Node Voltage Ringing Measurements: Typical 3-Inch Wire (Left) Versus Small Length Wire (Right)

Figure 8. Oscilloscope Probe Comparison: Typical 3-Inch Wire (Left) Versus Small Length Wire (Right)

Conclusion/Summary

The layout and placement of the Power Stage components in a nonisolated synchronous buck converter requires special attention in order to optimize the overall performance of the switching function. In particular, voltage ringing commonly found to be superimposed on the switching node can be reduced by up to 20% by simply optimizing the placement and PCB layout of the power MOSFETs and input capacitors.

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