

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS Quad 8-bit digital-to-analog converter, with output buffer amplifiers and interface logic. Separate on-chip latches are provided for each of the four D/A converters.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification is as follows:

| Device | Part Number ¹ |
|--------|--------------------------|
| - 1 | AD7226T(X)/883B |

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

| (X) | Package | Description |
|-----|---------|----------------|
| Q | Q-20 | 20-Pin Cerdip |
| E | E-20A | 20-Contact LCC |

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| | |
|------------------------------------|---------------------------------------------|
| V_{DD} to AGND | -0.3V, +17V |
| V_{DD} to DGND | -0.3V, +17V |
| V_{SS} to AGND | -7V, V_{DD} |
| V_{SS} to DGND | -7V, V_{DD} |
| V_{DD} to V_{SS} | -0.3V, +24V |
| AGND to DGND | -0.3V, V_{DD} |
| Digital Input Voltage to DGND | -0.3V, V_{DD} |
| V_{REF} to AGND | -0.3V, V_{DD} |
| V_{OUT} to AGND | V_{SS} , V_{DD} |
| Power Dissipation | |
| Up to $+75^\circ\text{C}$ | 500mW |
| Derates above $+75^\circ\text{C}$ | 2mW/ $^\circ\text{C}$ |
| Operating Temperature Range | -55°C to $+125^\circ\text{C}$ |
| Storage Temperature | -65°C to $+150^\circ\text{C}$ |
| Lead Temperature (Soldering 10sec) | $+300^\circ\text{C}$ |

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-20 and E-20A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-20 and E-20A

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Table 1.

| Test | Symbol | Device | Design Limit $T_{min}-T_{max}$ | Sub Group 1 | Sub Group 2, 3 | Test Condition ¹ | Units |
|-------------------------------------------|---------------|--------|-----------------------------------|-------------|----------------|------------------------------------------------------------------------------------------------------|----------|
| Resolution | RES | - 1 | 8 | | | | Bits |
| Relative Accuracy | RA | - 1 | ± 1 | ± 1 | ± 1 | $V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$ | LSB max |
| Total Unadjusted Error | E_T | - 1 | ± 2 | ± 2 | ± 2 | $V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$ | LSB max |
| Differential Nonlinearity | DNL | - 1 | ± 1 | ± 1 | ± 1 | $V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$ Guaranteed Monotonic to 8-Bits | LSB max |
| Full-Scale Error | A_E | - 1 | ± 3/2 | ± 3/2 | ± 3/2 | $V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$ | LSB max |
| Zero Code Error | A_{ZCE} | - 1 | ± 30 | ± 30 | ± 30 | $V_{DD} = 16.5V, 11.4V$ and $14V; V_{SS} = -5V; V_{REF} = V_{DD} - 4$ | mV max |
| Voltage Output Settling Time ² | t_{SI} | - 1 | 5 | | | Positive Full-Scale Change | µs max |
| | | | 7 | | | Negative Full-Scale Change | |
| Voltage Output Slew Rate | t_{SR} | - 1 | 2.5 | | | | V/µs min |
| Minimum Load Resistance | $R_{L_{MIN}}$ | - 1 | 2 | 2 | 2 | $V_{OUT} = +10V; V_{DD} = +14V$ | kΩ min |
| Reference Input Resistance | R_I | - 1 | 2 | 2 | 2 | $V_{DD} = 14V$ | kΩ min |
| Reference Input Capacitance | C_I | - 1 | 65 | | | Occurs when DAC is loaded with all 0's | pF min |
| | | | 300 | | | Occurs when DAC is loaded with all 1's | pF max |
| Digital Input High Voltage | V_{IH} | - 1 | 2.4 | 2.4 | 2.4 | $V_{DD} = 11.4V; V_{REF} = V_{DD} - 4$ | V min |
| Digital Input Low Voltage | V_{IL} | - 1 | 0.8 | 0.8 | 0.8 | $V_{DD} = 11.4V; V_{REF} = V_{DD} - 4$ | V max |
| Digital Input Leakage Current | I_{IN} | - 1 | 1 | 1 | 1 | $V_{IN} = 0V$ or $V_{DD}; V_{DD} = 16.5V$ | ± µA max |
| Digital Input Capacitance | C_{IN} | - 1 | 8 | | | | pF max |
| Address to Write Setup Time | t_{AS} | - 1 | 0 | | | | ns min |
| Address to Write Hold Time | t_{AH} | - 1 | 10 | | | | ns min |
| Data Valid to Write Setup Time | t_{DS} | - 1 | 100 | | | | ns min |
| Data Valid to Write Hold Time | t_{DH} | - 1 | 10 | | | | ns min |
| Write Pulse Width | t_{WR} | - 1 | 200 | | | | ns min |
| Power Supply Voltage Range | V_{DD} | - 1 | 11.4 | | | For Specified Performance | + V min |
| | | | 16.5 | | | | + V max |
| | V_S | - 1 | - 4.5 | | | | - V min |
| | | | - 5.5 | | | | - V max |
| Power Supply Current | I_{DD} | - 1 | 13 | 13 | 13 | Outputs Unloaded: $V_{IN} = V_{IL}$ or V_{IH} $V_{DD} = 16.5V; V_{SS} = -5.5V; V_{REF} = 12.5V$ | mA max |
| | I_{SS} | - 1 | 11 | 11 | 11 | | |

NOTES

¹ $V_{DD} = +11.4V$ to $16.5V; V_{SS} = -5V \pm 10\%$; AGND = DGND = 0V; $V_{REF} = +2V$ to $(V_{DD} - 4V)$ unless otherwise stated.

² $V_{REF} = +10V$; Settling Time to ± 1/2LSB.

Table 2.

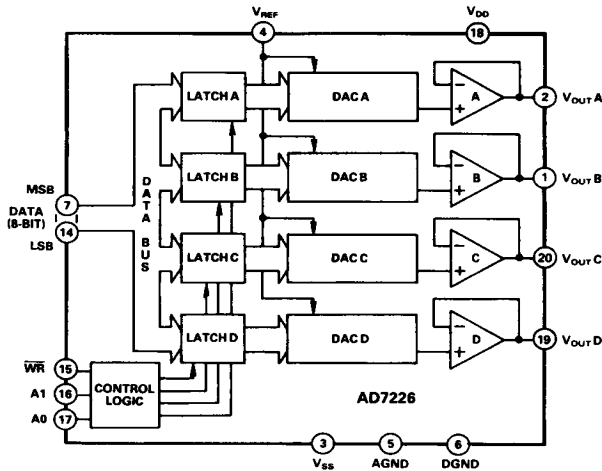
| Test | Symbol | Device | Design Limit $T_{min}-T_{max}$ | Sub Group 1 | Sub Group 2, 3 | Test Condition ¹ | Units |
|-------------------------------------------|------------|--------|-----------------------------------|----------------|-------------------|----------------------------------------------------------------------|-------------------|
| Resolution | RES | -1 | 8 | | | | Bits |
| Total Unadjusted Error | E_T | -1 | 2 | 2 | 2 | $V_{DD} = +14V$ | \pm LSB max |
| Differential Nonlinearity | DNL | -1 | 1 | 1 | 1 | $V_{DD} = +14V$ Guaranteed Monotonic to 8-Bits | \pm LSB max |
| Voltage Output Settling Time ² | t_{SL} | -1 | 5 | | | Positive Full-Scale Change | μ s max |
| | | | 20 | | | Negative Full-Scale Change | |
| Voltage Output Slew Rate | t_{SR} | -1 | 2 | | | | V/ μ s min |
| Minimum Load Resistance | RL_{MIN} | -1 | 2 | 2 | 2 | $V_{OUT} = +10V$; $V_{DD} = +15V$ | k Ω min |
| Reference Input Resistance | V_{REF} | -1 | 2 | | | $V_{DD} = 14.25V$ | k Ω min |
| Reference Input Capacitance | C_I | -1 | 65 | | | Occurs when DAC is loaded with all 0's | pF min |
| | | | 300 | | | Occurs when DAC is loaded with all 1's | pF max |
| Digital Input High Voltage | V_{IH} | -1 | 2.4 | 2.4 | 2.4 | $V_{DD} = +14.25V$ | V min |
| Digital Input Low Voltage | V_{IL} | -1 | 0.8 | 0.8 | 0.8 | $V_{DD} = +14.25V$ | V max |
| Digital Input Leakage Current | I_{IN} | -1 | 1 | | | $V_{IN} = 0V$ or V_{DD} ; $V_{DD} = +14.25V$ | \pm μ A max |
| Digital Input Capacitance | C_I | -1 | 8 | | | | pF max |
| Address to Write Setup Time | t_{AS} | -1 | 0 | | | | ns min |
| Address to Write Hold Time | t_{AH} | -1 | 10 | | | | ns min |
| Data Valid to Write Setup Time | t_{DS} | -1 | 100 | | | | ns min |
| Data Valid to Write Hold Time | t_{DH} | -1 | 10 | | | | ns min |
| Write Pulse Width | t_{WR} | -1 | 200 | | | | ns min |
| Power Supply Voltage Range | V_{DD} | -1 | 14.25 | | | For Specified Performance | + V min |
| | | | 15.75 | | | | + V max |
| Power Supply Current | I_{DD} | -1 | 13 | | | Outputs Unloaded; $V_{IN} = V_{IL}$ or V_{IH} $V_{DD} = 15.75V$ | mA max |

NOTES

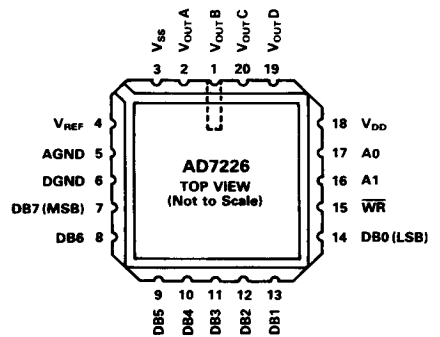
¹ $V_{DD} = +15V \pm 5\%$; $V_{SS} = AGND = DGND = 0V$; $V_{REF} = +10V$ unless otherwise stated.²Settling Time to $\pm 1/2$ LSB.

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3.2.1 Functional Block Diagram and Terminal Assignments.



E Package (LCC)

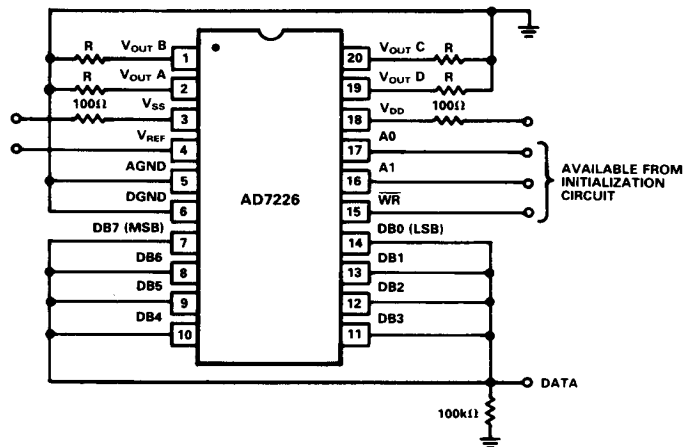


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883, Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



V_{DD} = +15V
 V_{SS} = -5V
 V_{REF} = +5V
 DATA = V_{DD}
 R = 10k Ω
 I_{DD} = 8.5mA
 I_{SS} = -5.0mA
 I_{REF} = 0.5mA

INITIALIZATION PROCEDURE: (SEE SHEET 3)
 V_{DD} IS TURNED ON FIRST, THEN V_{SS} , FOLLOWED BY V_{REF} .
 THE V_{CC} OF THE INITIALIZATION CIRCUIT IS TURNED ON.
 THE START LINE IS TAKEN FROM "LOW" TO "HIGH". WHERE-
 UPON WR GOES LOW FOR 140 μ S. DURING THIS TIME A0
 AND A1 GO THROUGH THE FOLLOWING STATES:

| | | |
|----------|----------|---------------|
| A1 | A0 | DAC ADDRESSED |
| GND | V_{CC} | DAC B |
| GND | GND | DAC A |
| V_{CC} | GND | DACC |
| V_{CC} | V_{CC} | DACD |

 THUS, ALL FOUR DAC'S ARE LOADED WITH ALL 1'S.

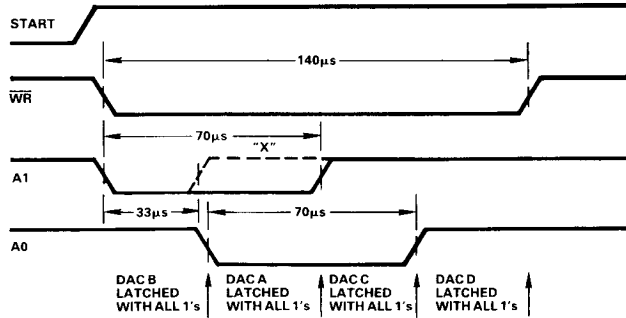


Figure 1. Initialization Timing Diagram

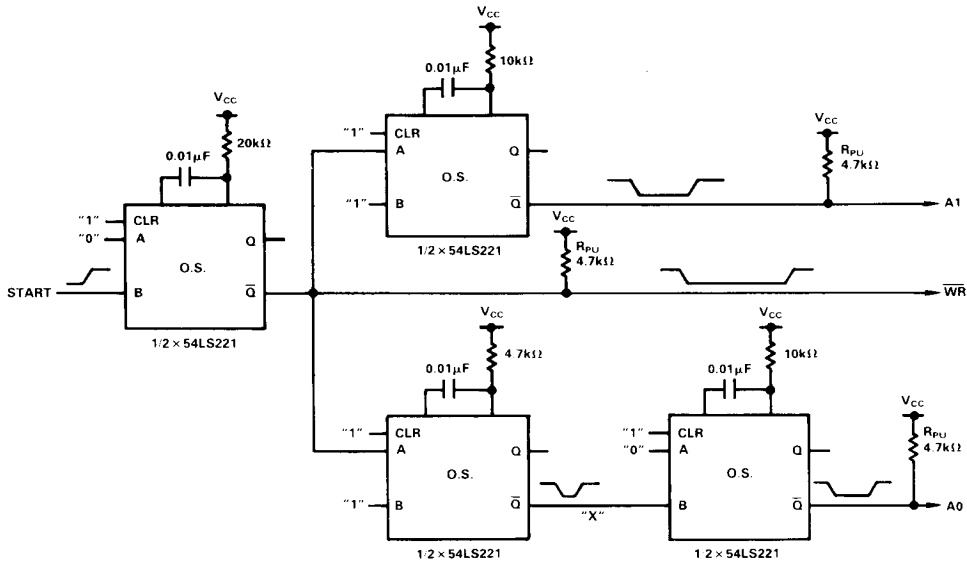


Figure 2. Initialization Circuit

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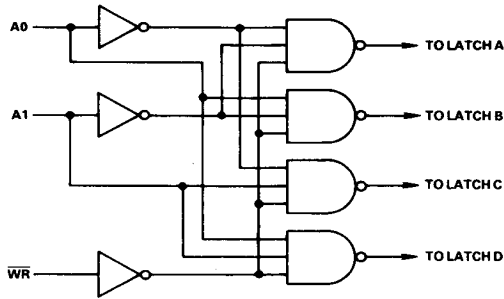
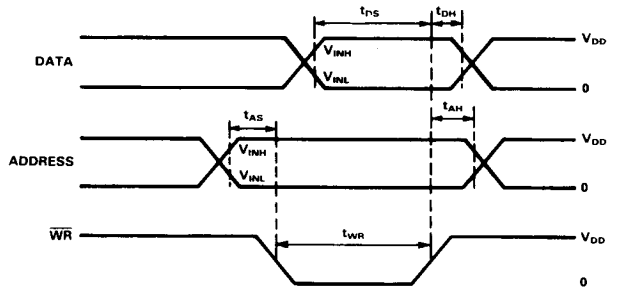


Figure 3. Input Control Logic



NOTES

1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD} .
 $t_r = t_f = 20\text{ns}$ OVER V_{DD} RANGE
2. TIMING MEASUREMENT REFERENCE LEVEL IS
 $\frac{V_{NH} + V_{INL}}{2}$
3. SELECTED INPUT LATCH IS TRANSPARENT WHILE \overline{WR} IS LOW. THUS INVALID DATA DURING THIS TIME CAN CAUSE SPURIOUS OUTPUTS.

Figure 4. Write Cycle Timing Diagram

Table 3. AD7226 Truth Table

| AD7226 Control Inputs | | | AD7226 Operation |
|-----------------------|----|----|-------------------------------------|
| \overline{WR} | A1 | A0 | |
| H | X | X | No Operation Device Not Selected |
| L | L | L | DAC A Transparent |
| L | L | L | DAC A Latched |
| L | L | H | DAC B Transparent |
| L | L | H | DAC B Latched |
| L | H | L | DAC C Transparent |
| L | H | L | DAC C Latched |
| L | H | H | DAC D Transparent |
| L | H | H | DAC D Latched |

L = Low State, H = High State, X = Don't Care