SBAS320A − FEBRUARY 2005

12-Bit, 80 MSPS Analog-to-Digital Converter

FEATURES

- 12-Bit Resolution
- 80 MSPS Sample Rate
- High SNR: 69.7 dBFS at 100 MHz f_{IN}
- High SFDR: 83.0 dBc at 100 MHz f_{IN}
- 2.3 V_{PP} Differential Input Voltage
- Internal Voltage Reference
- 3.3-V Single-Supply Voltage
- Analog Power Dissipation: 541 mW
  - Output Buffer Power Dissipation: 122 mW
- Serial Programming Interface
- TQFP-64 PowerPAD™ Package

Pin-Compatible with:

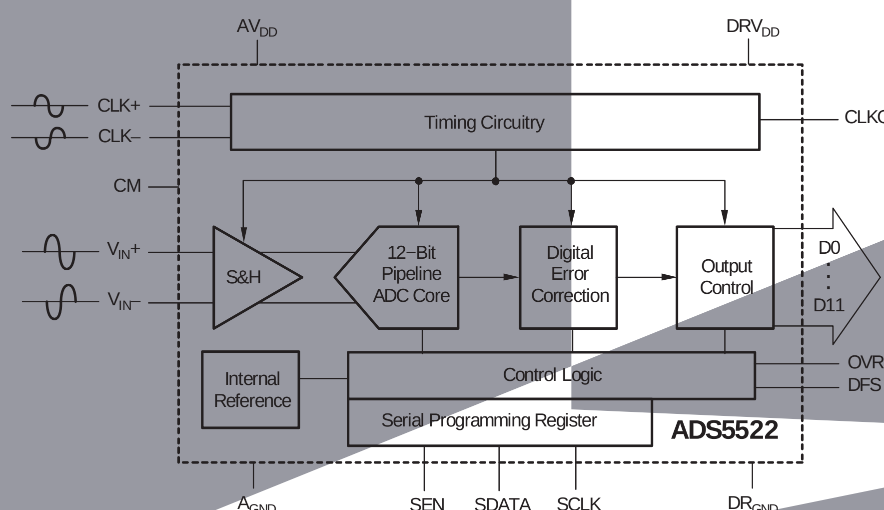
- ADS5500 (14-Bit, 125 MSPS)
- ADS5541 (14-Bit, 105 MSPS)
- ADS5542 (14-Bit, 80 MSPS)
- ADS5520 (12-Bit, 125 MSPS)
- ADS5521 (12-Bit, 105 MSPS)
- Recommended Op Amps: OPA695, OPA847, THS3202, THS3201, THS4503, THS9001

APPLICATIONS

- Wireless Communication
  - Communication Receivers
  - Base Station Infrastructure
- Test and Measurement Instrumentation
- Single and Multichannel Digital Receivers
- Communication Instrumentation
  - Radar, Infrared
- Video and Imaging
- Medical Equipment
- Military Equipment

DESCRIPTION

The ADS5522 is a high-performance, 12-bit, 80 MSPS analog-to-digital converter (ADC). To provide a complete converter solution, it includes a high-bandwidth linear sample-and-hold stage (S&H) and internal reference. Designed for applications demanding the highest speed and highest dynamic performance in very little space, the ADS5522 has excellent analog power dissipation of 541 mW and output buffer power dissipation of 122 mW from 3.3-V single-supply voltage. This allows an even higher system integration density. The provided internal reference simplifies system design requirements. The parallel CMOS compatible outputs ensure seamless interfacing with common logic.



DESCRIPTION (continued)

The ADS5522 is available in a 64-pin TQFP PowerPAD package and is pin-compatible to the ADS5500, ADS5541, ADS5542, ADS5520, and ADS5521. This device is specified over the full temperature range of −40°C to +85°C.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5522	HTQFP-64(2) PowerPAD	PAP	−40°C to +85°C	ADS5522I	ADS5522IPAP	Tray, 160
					ADS5522IPAPR	Tape and Reel, 1000

(1) For the most current product and ordering information, see the Package Option Addendum located at the end of this data sheet.
(2) Thermal pad size: 3,5 mm x 3,5 mm (min), 4 mm x 4 mm (max). θ_{JA} = 21.47°C/W and θ_{JC} = 2.99°C/W, when used with 2oz. copper trace and pad soldered directly to a JEDEC standard 4 layer 3in x 3in PCB.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		ADS5522	UNIT
Supply Voltage	AV_{DD} to A_{GND}, DRV_{DD} to DR_{GND}	−0.3 to +3.7	V
	A_{GND} to DR_{GND}	±0.1	V
Analog input to A_{GND}(2)		−0.3 to +3.6	V
Logic input to DR_{GND}		−0.3 to DRV_{DD}	V
Digital data output to DR_{GND}		−0.3 to DRV_{DD}	V
Operating temperature range		−40 to +85	°C
Junction temperature		+105	°C
Storage temperature range		−65 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2): For more detail, refer to the Input Voltage Overstress section in the Application Information

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Supplies				
Analog supply voltage, AV_{DD}	3.0	3.3	3.6	V
Output driver supply voltage, DRV_{DD}	3.0	3.3	3.6	V
Analog Input				
Differential input range		2.3		V_{PP}
Input common-mode voltage, V_{CM}(1)	1.47	1.57	1.67	V
Digital Output				
Maximum output load		10		pF
Clock Input				
ADCLK input sample rate (sine wave) $1/t_C$	10		80	MSPS
Clock amplitude, sine wave, differential(2)	1	3		V_{PP}
Clock duty cycle(3)		50		%
Open free-air temperature range	−40		+85	°C

(1) Input common-mode should be connected to CM.
(2) See Figure 14 for more information.
(3) See Figure 13 for more information.

ELECTRICAL CHARACTERISTICS

Typ, min, and max values at T_A = +25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3 V, sampling rate = 80 MSPS, 50% clock duty cycle, 3-V_{PP} differential clock, and −1 dBFS differential input, unless otherwise noted

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Resolution				12		Bits
Analog Inputs						
Differential input range				2.3		V_{PP}
Differential input resistance	See Figure 5			6.6		kΩ
Differential input capacitance	See Figure 5			4		pF
Analog input common-mode current (per input)				200		μA
Analog input bandwidth	Source impedance = 50 Ω			750		MHz
Voltage overload recovery time				4		Clock Cycles
Internal Reference Voltages						
Reference bottom voltage, V_{REFM}				1.0		V
Reference top voltage, V_{REFP}				2.15		V
Reference error			−4	±0.6	+4	%
Common-mode voltage output, V_{CM}				1.575		V
Dynamic DC Characteristics and Accuracy						
No missing codes				Tested		
Differential nonlinearity error, DNL	f_{IN} = 10 MHz		−0.5	±0.25	0.5	LSB
Integral nonlinearity error, INL	f_{IN} = 10 MHz		−1.5	±0.55	1.5	LSB
Offset error				±1.5		mV
Offset temperature coefficient				0.02		mV/°C
DC power supply rejection ratio, DC PSRR	Δoffset error/ΔAV_{DD} from AV_{DD} = 3.0 V to AV_{DD} = 3.6 V			0.25		mV/V
Gain error				±0.3		%FS
Gain temperature coefficient				−0.02		Δ%/°C
Dynamic AC Characteristics						
Signal-to-noise ratio, SNR	f_{IN} = 10 MHz	Room temp	68.0	70.5		dBFS
		Full temp range	66.5	69.5		dBFS
	f_{IN} = 55 MHz			70.3		dBFS
	f_{IN} = 70 MHz	Room temp	68.0	70.2		dBFS
		Full temp range	66.5	69.0		dBFS
	f_{IN} = 100 MHz			69.7		dBFS
	f_{IN} = 150 MHz			68.6		dBFS
	f_{IN} = 220 MHz			67.2		dBFS
RMS idle channel noise	Input tied to common-mode			0.43		LSB
Spurious-free dynamic range, SFDR	f_{IN} = 10 MHz	Room temp	79.0	87.0		dBc
		Full temp range	76.0	84.0		dBc
	f_{IN} = 55 MHz			87.0		dBc
	f_{IN} = 70 MHz	Room temp	78.0	84.0		dBc
		Full temp range	76.0	83.0		dBc
	f_{IN} = 100 MHz			83.0		dBc
	f_{IN} = 150 MHz			78.0		dBc
	f_{IN} = 220 MHz			71.0		dBc

ELECTRICAL CHARACTERISTICS (continued)

Typ, min, and max values at T_A = +25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3 V, sampling rate = 80 MSPS, 50% clock duty cycle, 3-V_{PP} differential clock, and −1 dBFS differential input, unless otherwise noted

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Second-harmonic, HD2	f_{IN} = 10 MHz	Room temp	79.0	87.0		dBc
		Full temp range	76.0	86.0		dBc
	f_{IN} = 55 MHz			86.0		dBc
	f_{IN} = 70 MHz	Room temp	78.0	84.0		dBc
		Full temp range	76.0	83.0		dBc
	f_{IN} = 100 MHz			83.0		dBc
	f_{IN} = 150 MHz			78.0		dBc
	f_{IN} = 220 MHz			71.0		dBc
Third-harmonic, HD3	f_{IN} = 10 MHz	Room temp	79.0	91.0		dBc
		Full temp range	76.0	87.0		dBc
	f_{IN} = 55 MHz			90.0		dBc
	f_{IN} = 70 MHz	Room temp	78.0	83.0		dBc
		Full temp range	76.0	83.0		dBc
	f_{IN} = 100 MHz			83.0		dBc
	f_{IN} = 150 MHz			86.0		dBc
	f_{IN} = 220 MHz			84.0		dBc
Worst-harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz	Room temp		90.0		dBc
	f_{IN} = 70 MHz	Room temp		89.0		dBc
Signal-to-noise + distortion, SINAD	f_{IN} = 10 MHz	Room temp	67.5	70.4		dBFS
		Full temp range	66.0	69.0		dBFS
	f_{IN} = 55 MHz			70.1		dBFS
	f_{IN} = 70 MHz	Room temp	67.5	69.9		dBFS
		Full temp range	66.0	68.5		dBFS
	f_{IN} = 100 MHz			69.4		dBFS
	f_{IN} = 150 MHz			68.1		dBFS
	f_{IN} = 220 MHz					

ELECTRICAL CHARACTERISTICS (continued)

Typ, min, and max values at T_A = +25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3 V, sampling rate = 80 MSPS, 50% clock duty cycle, 3-V_{PP} differential clock, and −1 dBFS differential input, unless otherwise noted

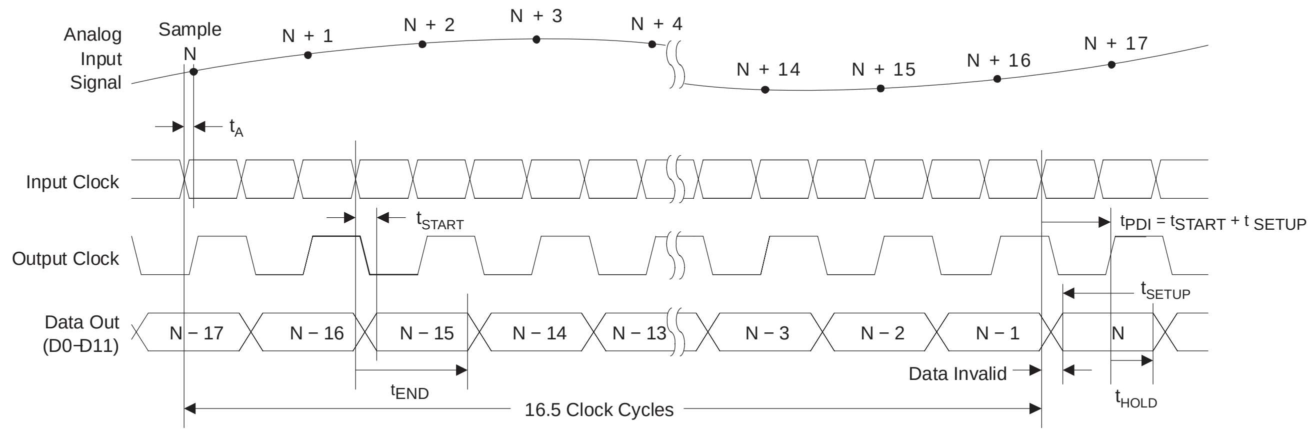
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation	Analog only		541	594	mW
	Output buffer power with 10pF load on digital output to ground		122	165	mW
Standby power	With clocks running		180	250	mW

DIGITAL CHARACTERISTICS

Valid over full temperature range of T_{MIN} = −40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3 V, unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current				10	μA
Low-level input current				10	μA
Input current for RESET			−20		μA
Input capacitance			4		pF
Digital Outputs					
Low-level output voltage	C_{LOAD} = 10 pF		0.3	0.4	V
High-level output voltage	C_{LOAD} = 10 pF	2.4	3.0		V
Output capacitance			3		pF

TIMING CHARACTERISTICS



NOTE: It is recommended that the loading at CLKOUT and all data lines are accurately matched to ensure that the above timing matches closely with the specified values.

Figure 1. Timing Diagram

TIMING CHARACTERISTICS(3)(4)

Typ, min, and max values at T_A = +25°C, full temperature range is T_{MIN} = −40°C to t_{MAX} = +85°C, sampling rate = 80 MSPS, 50% clock duty cycle, AV_{DD} = DRV_{DD} = 3.3 V, and 3-V_{PP} differential clock, unless otherwise noted(4)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Switching Specification					
Aperture delay, t_A	Input CLK falling edge to data sampling point		1		ns
Aperture jitter (uncertainty)	Uncertainty in sampling instant		300		fs
Data setup time, t_{SETUP}	Data valid(1) to 50% of CLKOUT rising edge	3.6	4.7		ns
Data hold time, t_{HOLD}	50% of CLKOUT rising edge to data becoming invalid(1)	1.8	3.1		ns
Input clock to output data valid start, t_{START}(5)	Input clock to Data valid start delay		3.3	4.7	ns
Input clock to output data valid end, t_{END}(5)	Input clock to Data valid end delay	8.2	11.1		ns
Data rise time, t_{RISE}	Data rise time measured from 20% to 80% of DRV_{DD}		5.6	6.1	ns
Data fall time, t_{FALL}	Data fall time measured from 80% to 20% of DRV_{DD}		4.4	5.1	ns
Output enable (OE) to data output delay	Time required for outputs to have stable timings w.r.t Input Clock(2) after OE is activated			1000	Clock Cycles

(1) Data valid refers to 2.0 V for LOGIC HIGH and 0.8 V for LOGIC LOW.
(2): Data outputs are available within a clock from assertion of OE; however it takes 1000 clock cycles to ensure stable timing with respect to input clock.
(3): Timing parameters are ensured by design and characterization, and not tested in production.
(4): See Table 5 in the *Application Information* section for timing information at additional sampling frequencies.
(5): Refer to the *Output Information* section for details on using the input clock for data capture.

RESET TIMING CHARACTERISTICS

Typ, min, and max values at T_A = +25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3 V, and 3-V_{PP} differential clock, unless otherwise noted

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Switching Specification					
Power−on delay, t_1	Delay from power−on of AV_{DD} and DRV_{DD} to RESET pulse active	10			ms
Reset pulse width, t_2	Pulse width of active RESET signal	2			µs
Register write delay, t_3	Delay from RESET disable to SEN active	2			µs

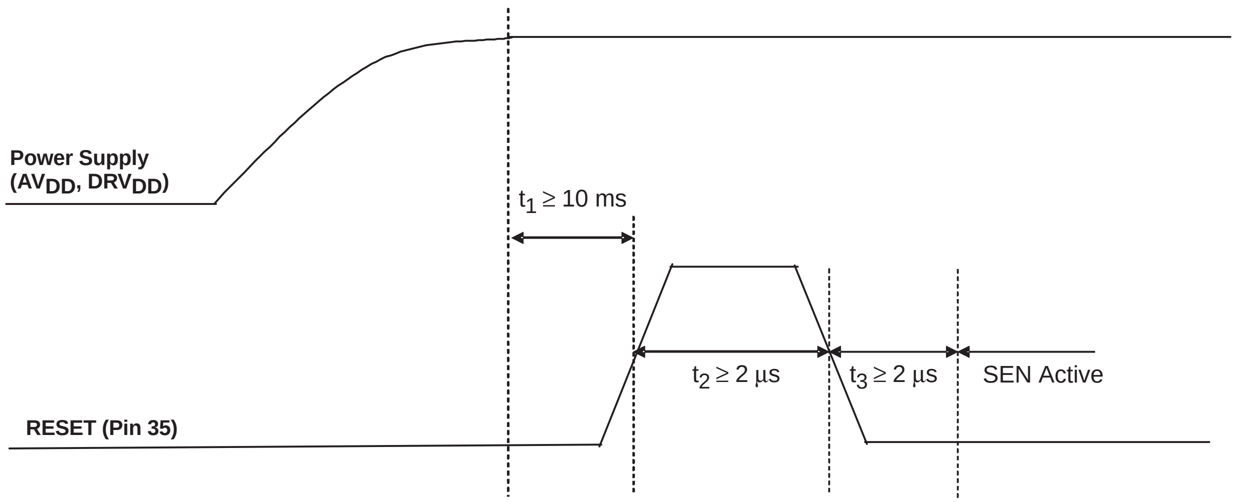


Figure 2. Reset Timing Diagram

SERIAL PROGRAMMING INTERFACE CHARACTERISTICS

The device has a three-wire serial interface. The device latches the serial data SDATA on the falling edge of serial clock SCLK when SEN is active.

- Serial shift of bits is enabled when SEN is low. SCLK shifts serial data at falling edge.
- Minimum width of data stream for a valid loading is 16 clocks.
- Data is loaded at every 16th SCLK falling edge while SEN is low.
- In case the word length exceeds a multiple of 16 bits, the excess bits are ignored.
- Data can be loaded in multiple of 16-bit words within a single active SEN pulse.
- The first 4-bit nibble is the address of the register while the last 12 bits are the register contents.

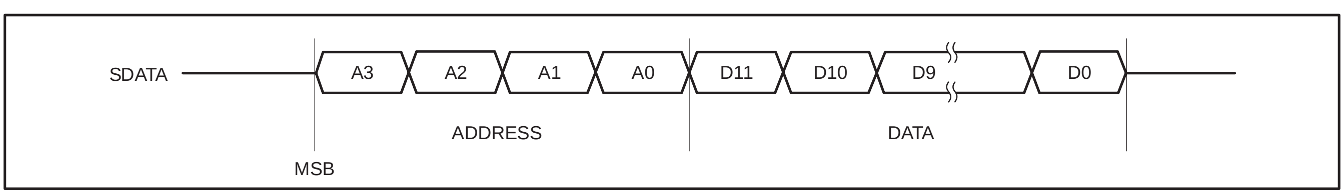


Figure 3. DATA Communication is 2-Byte, MSB First

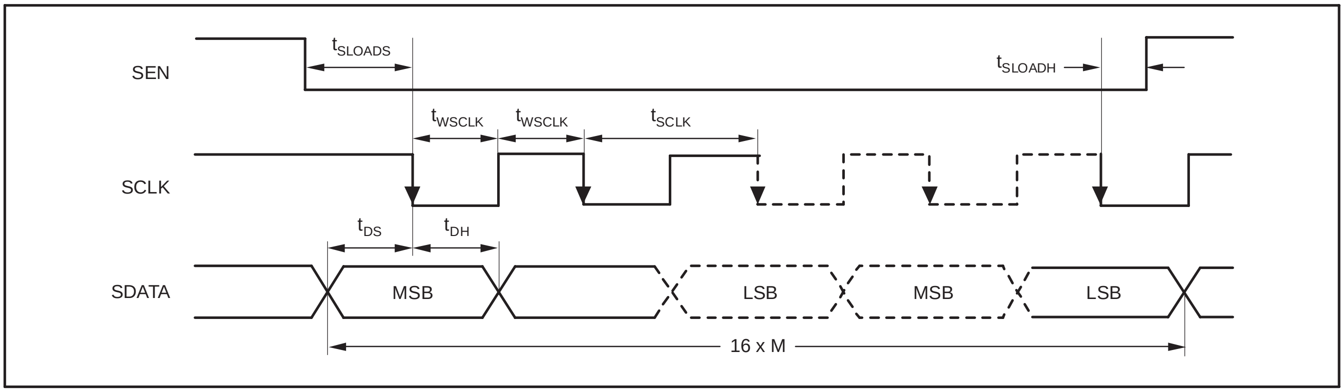


Figure 4. Serial Programming Interface Timing Diagram

Table 1. Serial Programming Interface Timing Characteristics

SYMBOL	PARAMETER	MIN(1)	TYP(1)	MAX(1)	UNIT
t_{SCLK}	SCLK Period	50			ns
t_{WSCLK}	SCLK Duty Cycle	25	50	75	%
t_{SLOADS}	SEN to SCLK setup time	8			ns
t_{SLOADH}	SCLK to SEN hold time	6			ns
t_{DS}	Data Setup Time	8			ns
t_{DH}	Data Hold Time	6			ns

(1) Typ, min, and max values are characterized, but not production tested.

Table 2. Serial Register Table

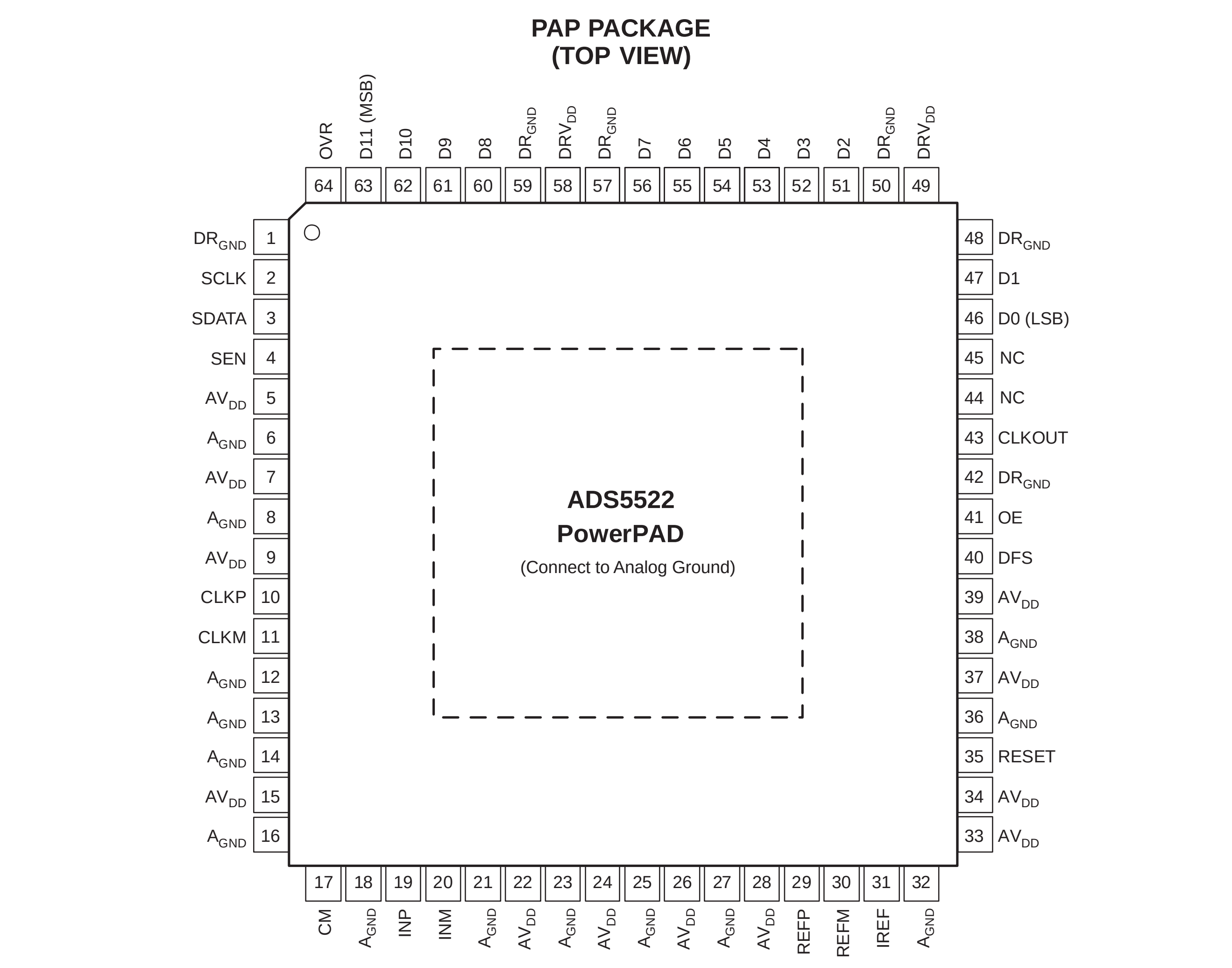
A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	1	1	0	0	TP<1>	TP<0>	0	0	0	0	0	0	0	0	0	TP<1:0> − Test modes for output data capture TP<1:0> = 00: Normal mode of operation TP<1:0> = 01: All outputs forced to 0 TP<1:0> = 10: All outputs forced to 1 TP<1:0> = 11: Each output bit toggles between 0 and 1. There is no ensured relationship between the bits See Note 2
1	1	1	1	PDN	0	0	0	0	0	0	0	0	0	0	0	PDN = 0 : Normal mode of operation, PDN = 1 : Device is put in power down (low current) mode

(1) All register contents default to zero on reset.
(2) The patterns given are applicable to the straight offset binary output format. If 2’s complement output format is selected, the test mode outputs will be the 2’s complement equivalent of these patterns.

Table 3. DATA FORMAT SELECT (DFS TABLE)

DFS-PIN VOLTAGE (V_{DFS})	DATA FORMAT	CLOCK OUTPUT POLARITY
$V_{DFS} < \frac{2}{12} \times AV_{DD}$	Straight Binary	Data valid on rising edge
$\frac{4}{12} \times AV_{DD} < V_{DFS} < \frac{5}{12} \times AV_{DD}$	2’s Complement	Data valid on rising edge
$\frac{7}{12} \times AV_{DD} < V_{DFS} < \frac{8}{12} \times AV_{DD}$	Straight Binary	Data valid on falling edge
$V_{DFS} > \frac{10}{12} \times AV_{DD}$	2’s Complement	Data valid on falling edge

PIN CONFIGURATION



PIN ASSIGNMENTS

TERMINAL		NO.		
NAME	NO.	OF PINS	I/O	DESCRIPTION
AV_{DD}	5, 7, 9, 15, 22, 24, 26, 28, 33, 34, 37, 39	12	I	Analog power supply
A_{GND}	6, 8, 12, 13, 14, 16, 18, 21, 23, 25, 27, 32, 36, 38	14	I	Analog ground
DRV_{DD}	49, 58	2	I	Output driver power supply
DR_{GND}	1, 42, 48, 50, 57, 59	6	I	Output driver ground
NC	44, 45	2	—	Not connected
INP	19	1	I	Differential analog input (positive)
INM	20	1	I	Differential analog input (negative)
REFP	29	1	O	Reference voltage (positive); 1-µF capacitor in series with a 1-Ω resistor to GND
REFM	30	1	O	Reference voltage (negative); 1-µF capacitor in series with a 1-Ω resistor to GND
IREF	31	1	I	Current set; 56-kΩ resistor to GND; do not connect capacitors
CM	17	1	O	Common-mode output voltage
RESET	35	1	I	Reset (active high)
OE	41	1	I	Output enable (active high)
DFS	40	1	I	Data format and clock out polarity select(1)
CLKP	10	1	I	Data converter differential input clock (positive)
CLKM	11	1	I	Data converter differential input clock (negative)
SEN	4	1	I	Serial interface chip select
SDATA	3	1	I	Serial interface data
SCLK	2	1	I	Serial interface clock
D0 (LSB)−D11 (MSB)	46, 47, 51−56, 60−63	12	O	Parallel data output
OVR	64	1	O	Over-range indicator bit
CLKOUT	43	1	O	CMOS clock out in sync with data

NOTE: PowerPAD must be connected to analog ground.

(1) Table 3 defines the voltage levels for each mode selectable via the DFS pin.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay
The delay in time between the falling edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle
The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Maximum Conversion Rate
The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate
The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL)
The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error
The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error does not account for variations in the internal reference voltages (see the Electrical Specifications section for limits on the variation of V_{REFP} and V_{REFM}).

Offset Error
The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift
The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree celcius of the parameter from T_{MIN} to T_{MAX}. It is calcuated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}-T_{MIN}$.

Signal-to-Noise Ratio
SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at DC and the first eight harmonics.

$$SNR = 10Log_{10}\frac{P_S}{P_N}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)
SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log_{10}\frac{P_S}{P_N + P_D}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB)
The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first eight harmonics (P_D).

$$THD = 10Log_{10}\frac{P_S}{P_D}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

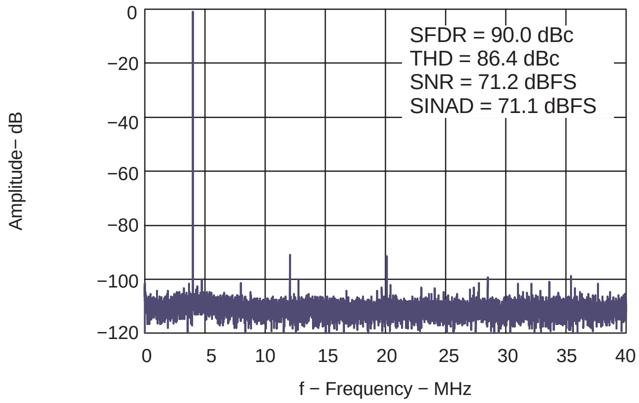
Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1-f_2$ or $2f_2-f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

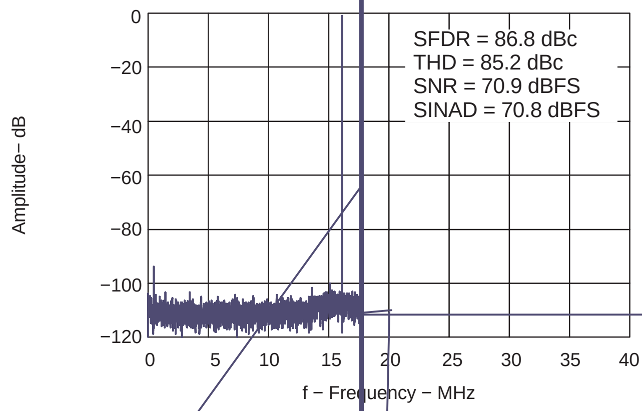
TYPICAL CHARACTERISTICS

Typ, min, and max values at T_A = +25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3 V, sampling rate = 80 MSPS, 50% clock duty cycle, 3-V_{PP} differential clock, and −1 dBFS differential input, unless otherwise noted

SPECTRAL PERFORMANCE
(FFT for 4 MHz Input Signal)



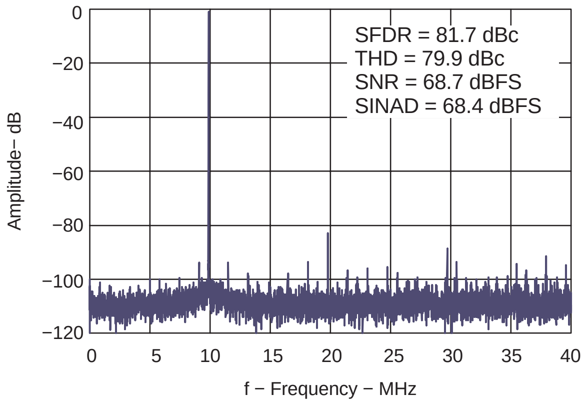
SPECTRAL PERFORMANCE
(FFT for 16 MHz Input Signal)



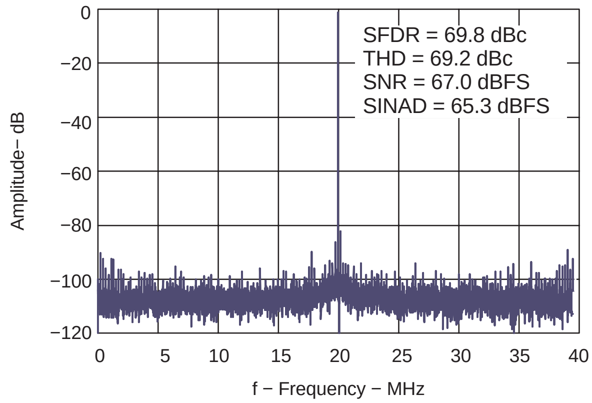
TYPICAL CHARACTERISTICS

Typ, min, and max values at T_A = +25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3 V, sampling rate = 80 MSPS, 50% clock duty cycle, 3-V_{PP} differential clock, and −1 dBFS differential input, unless otherwise noted

SPECTRAL PERFORMANCE
(FFT for 150 MHz Input Signal)

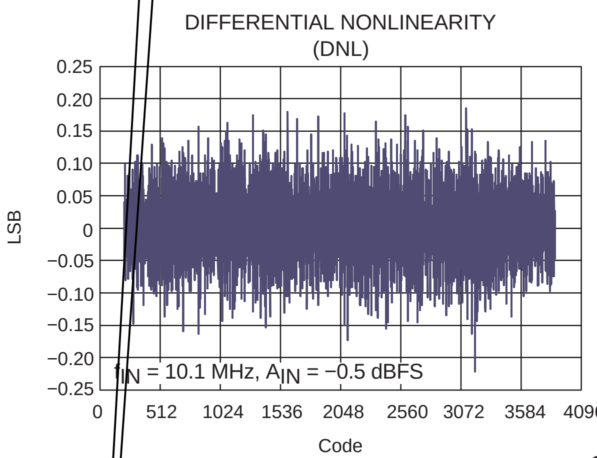


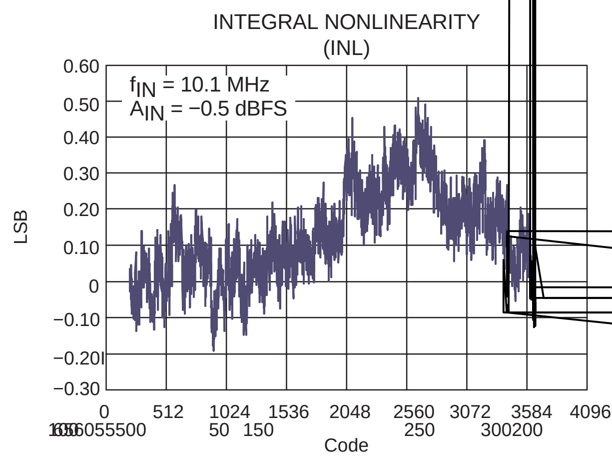
SPECTRAL PERFORMANCE
(FFT for 220 MHz Input Signal)



TYPICAL CHARACTERISTICS

Typ, min, and max values at T_A = +25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3 V, sampling rate = 80 MSPS, 50% clock duty cycle, 3-V_{PP} differential clock, and −1 dBFS differential input, unless otherwise noted



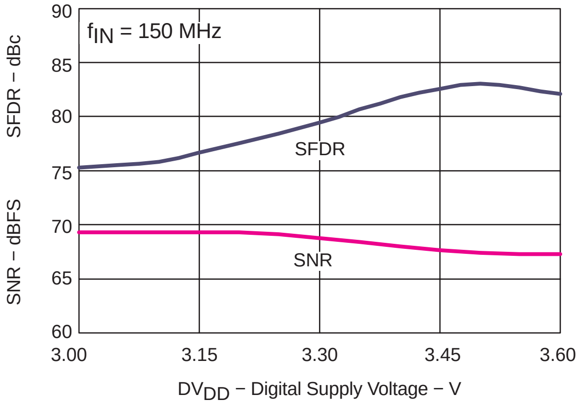


8580fS
1656055500 50 150 250 300200
1660071 50 150 250 300200
70fS
8075
7065
603580 3.15 3480 3.60

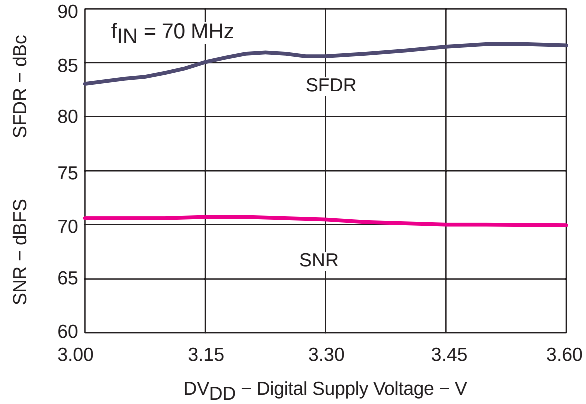
TYPICAL CHARACTERISTICS

Typ, min, and max values at T_A = +25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3 V, sampling rate = 80 MSPS, 50% clock duty cycle, 3-V_{PP} differential clock, and −1 dBFS differential input, unless otherwise noted

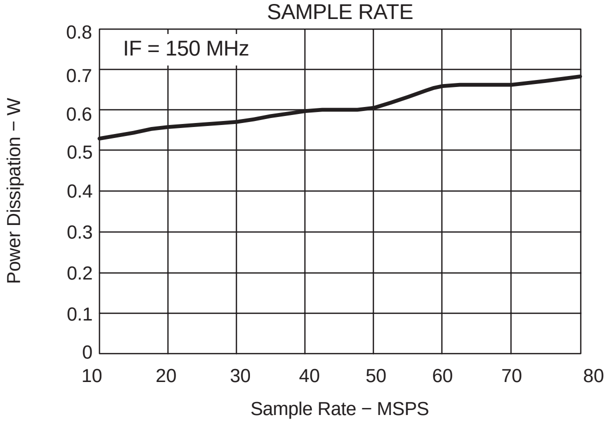
AC PERFORMANCE
vs
DIGITAL SUPPLY VOLTAGE



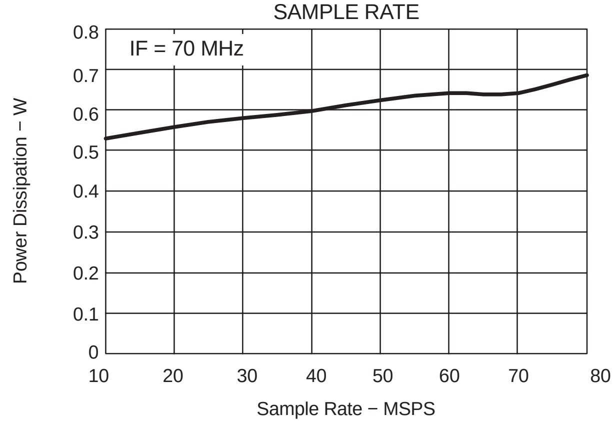
AC PERFORMANCE
vs
DIGITAL SUPPLY VOLTAGE



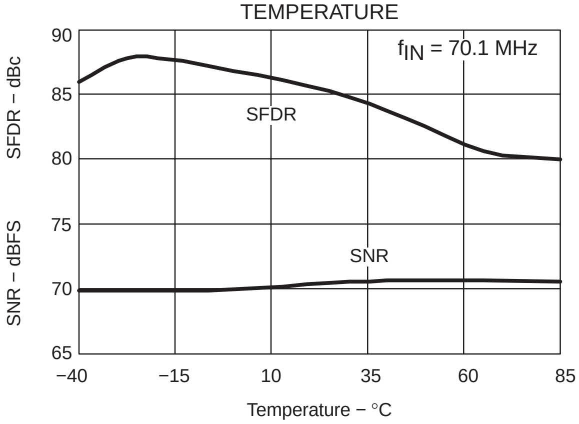
POWER DISSIPATION
vs.
SAMPLE RATE



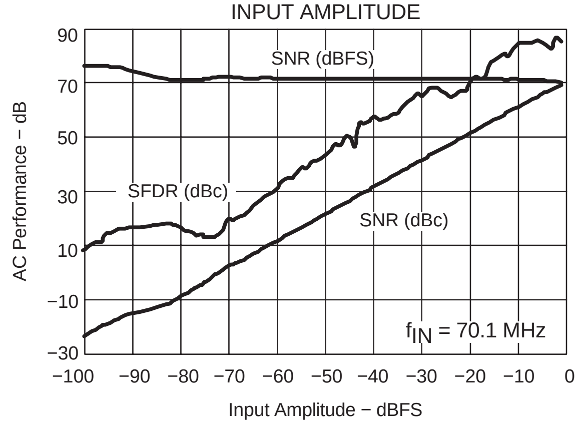
POWER DISSIPATION
vs.
SAMPLE RATE



AC PERFORMANCE
vs
TEMPERATURE



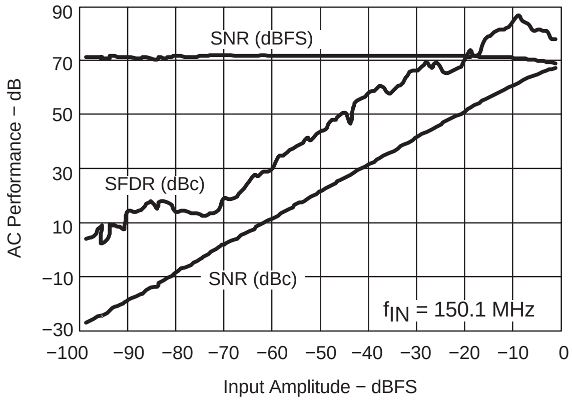
AC PERFORMANCE
vs
INPUT AMPLITUDE



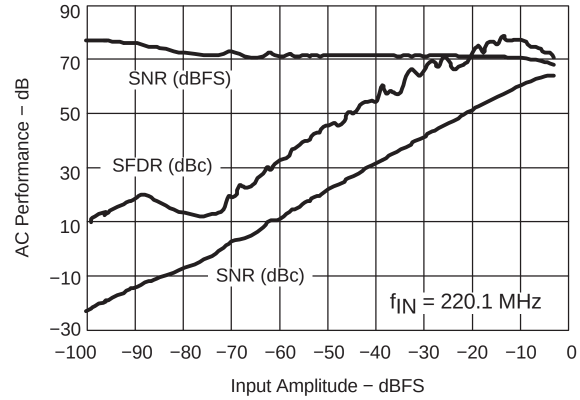
TYPICAL CHARACTERISTICS

Typ, min, and max values at T_A = +25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3 V, sampling rate = 80 MSPS, 50% clock duty cycle, 3-V_{PP} differential clock, and −1 dBFS differential input, unless otherwise noted

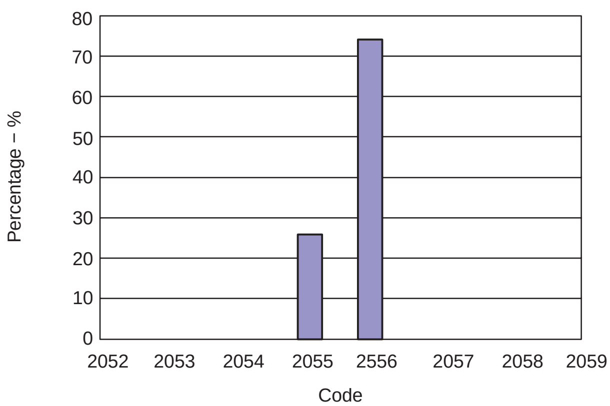
AC PERFORMANCE
vs
INPUT AMPLITUDE



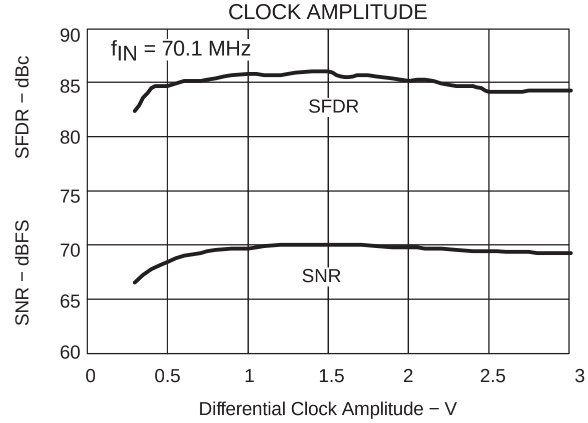
AC PERFORMANCE
vs
INPUT AMPLITUDE



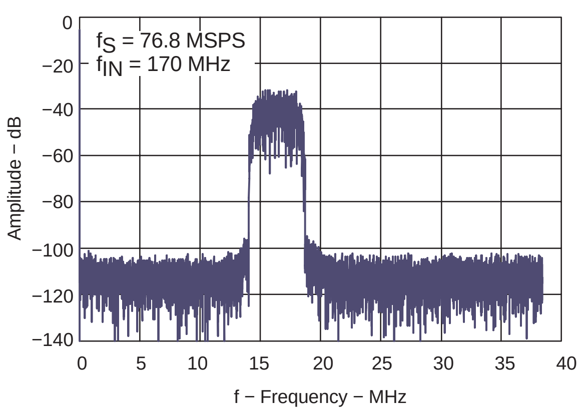
OUTPUT NOISE HISTOGRAM



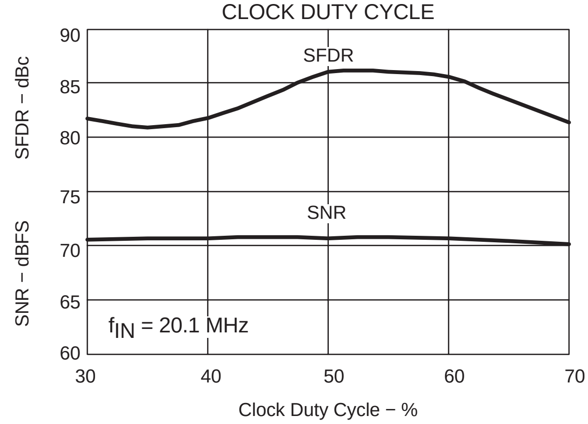
AC PERFORMANCE
vs
CLOCK AMPLITUDE



WCDMA CARRIER



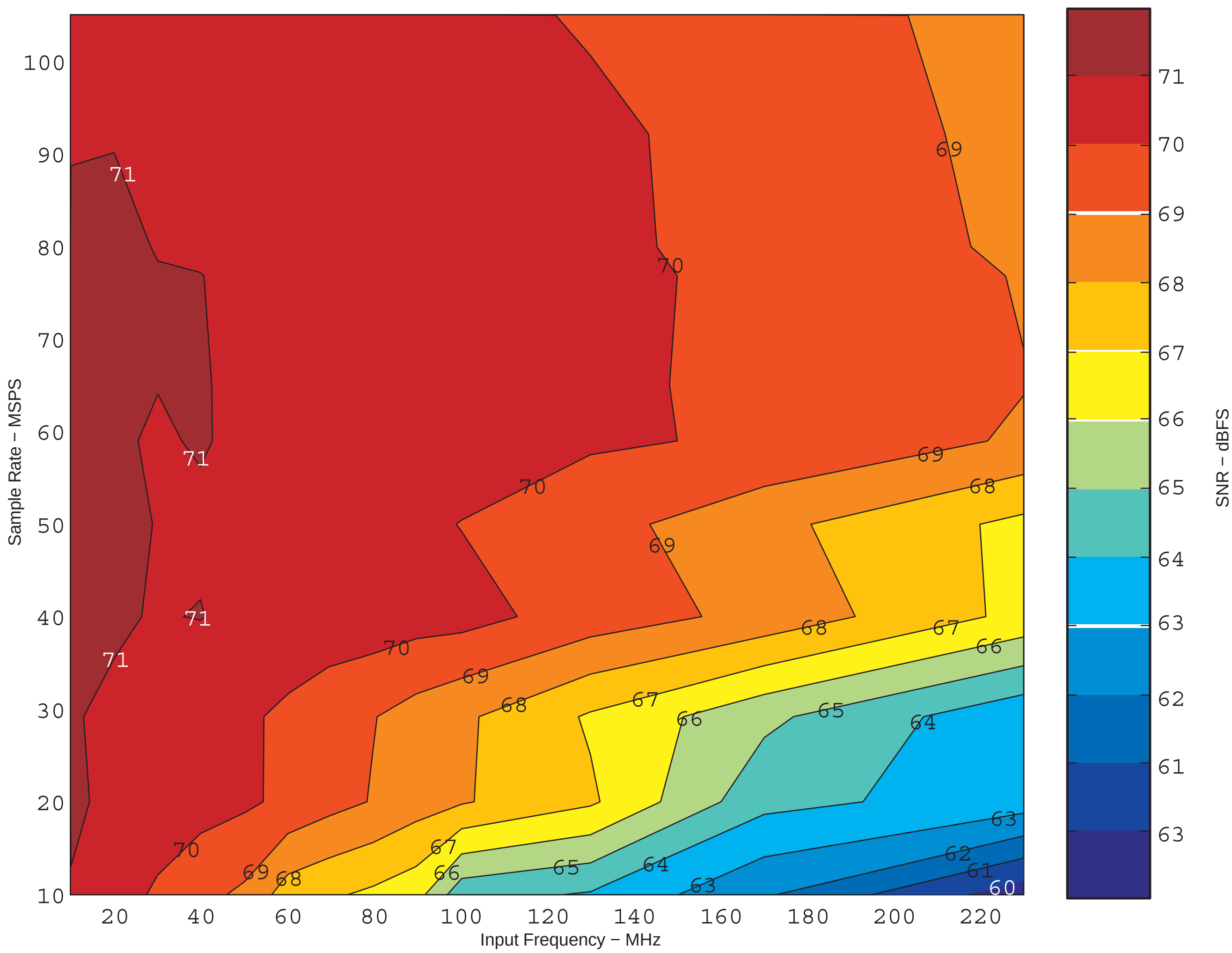
AC PERFORMANCE
vs
CLOCK DUTY CYCLE



TYPICAL CHARACTERISTICS

Typ, min, and max values at T_A = +25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3 V, 50% clock duty cycle, 3-V_{PP} differential clock, and −1 dBFS differential input, unless otherwise noted

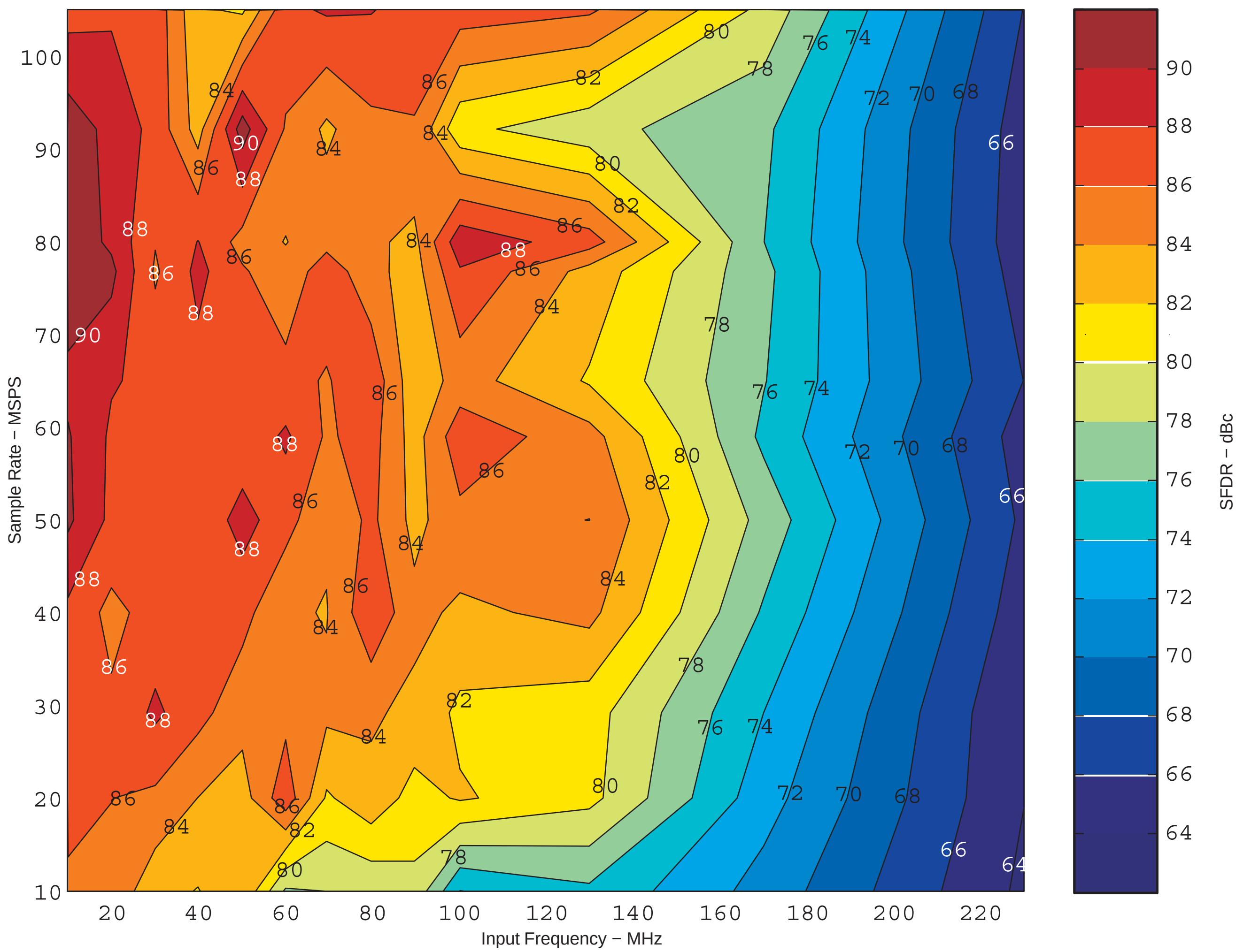
SIGNAL-TO-NOISE RATIO (SNR)



TYPICAL CHARACTERISTICS

Typ, min, and max values at T_A = +25°C, full temperature range is T_{MIN} = −40°C to T_{MAX} = +85°C, AV_{DD} = DRV_{DD} = 3.3 V, 50% clock duty cycle, 3-V_{PP} differential clock, and −1 dBFS differential input, unless otherwise noted

SPURIOUS-FREE DYNAMIC RANGE (SFDR)



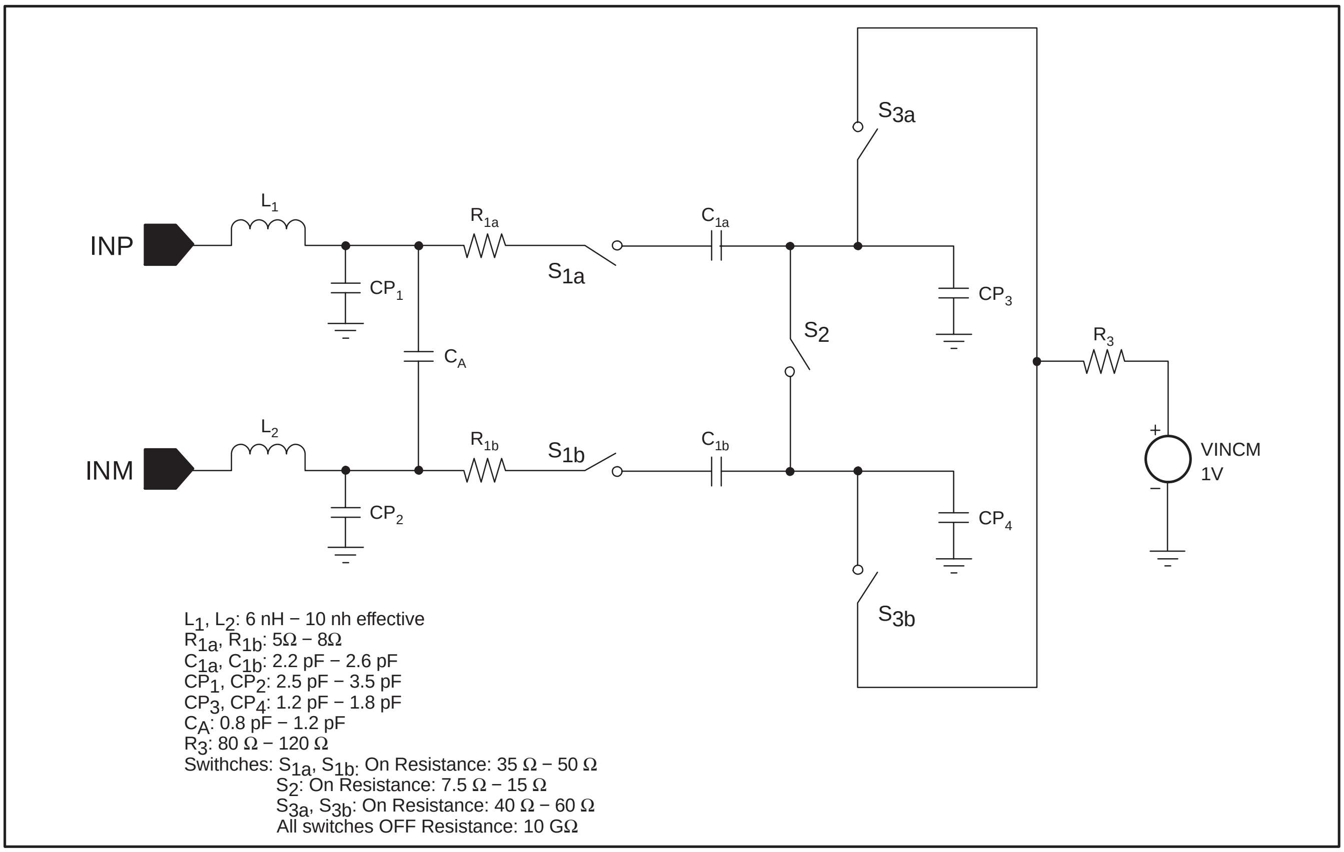
APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5522 is a low-power, 12-bit, 80 MSPS, CMOS, switched capacitor, pipeline ADC that operates from a single 3.3-V supply. The conversion process is initiated by a falling edge of the external input clock. Once the signal is captured by the input S&H, the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 16.5 clock cycles, after which the output data is available as a 12-bit parallel word, coded in either straight offset binary or binary two's complement format.

INPUT CONFIGURATION

The analog input for the ADS5522 consists of a differential sample-and-hold architecture implemented using a switched capacitor technique, shown in Figure 5.



NOTE: All Switches are ON in sampling phase which is approximately one half of a clock period.

Figure 5. Analog Input Stage

This differential input topology produces a high level of AC performance for high sampling rates. It also results in a high usable input bandwidth, especially important for high intermediate-frequency (IF) or undersampling applications. The ADS5522 requires each of the analog inputs (INP, INM) to be externally biased around the common-mode level of the internal circuitry (CM, pin 17). For a full-scale differential input, each of the differential lines of the input signal (pins 19 and 20) swings symmetrically between CM + 0.575 V and CM – 0.575 V. This means that each input is driven with a signal of up to CM ± 0.575V, so that each input has a maximum differential signal of 1.15 V_{PP} for a total differential input signal swing of 2.3 V_{PP}. The maximum swing is determined by the two reference voltages, the top reference (REFP, pin 29), and the bottom reference (REFM, pin 30).

The ADS5522 attains optimum performance when the analog inputs are driven differentially. The circuit shown in Figure 6 shows one possible configuration using an RF transformer.

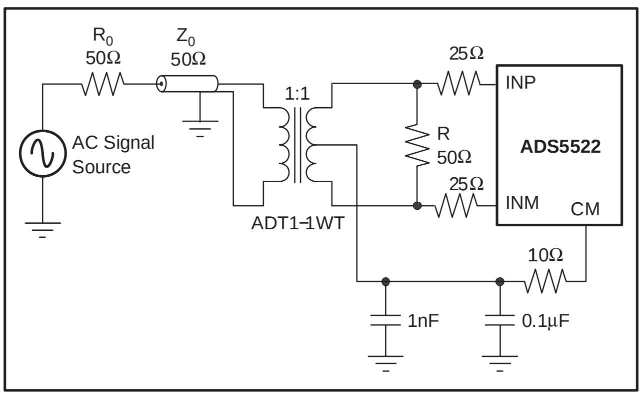


Figure 6. Transformer Input to Convert Single-Ended Signal to Differential Signal

The single-ended signal is fed to the primary winding of an RF transformer. Placing a 25-Ω resistor in series with INP and INM is recommended to dampen ringing due to ADC kickback. Since the input signal must be biased around the common-mode voltage of the internal circuitry, the common-mode voltage (V_{CM}) from the ADS5522 is connected to the center-tap of the secondary winding. To ensure a steady low-noise VCM reference, best performance is attained when the CM output (pin 17) is filtered to ground with a 10-Ω series resistor and parallel 0.1-µF and 0.001-µF low-inductance capacitors as illustrated in Figure 5.

Output V_{CM} (pin 17) is designed to directly drive the ADC input. When providing a custom CM level, be aware that the input structure of the ADC sinks a common-mode current in the order of 400 µA (200 µA per input). Equation (1) describes the dependency of the common-mode current and the sampling frequency:

$$\frac{400\ \mu A \times f_s\ (\text{in MSPS})}{80\ \text{MSPS}} \qquad (1)$$

Where:

f_S > 10MSPS.

This equation helps to design the output capability and impedance of the driving circuit accordingly.

When it is necessary to buffer or apply a gain to the incoming analog signal, it is possible to combine single-ended operational amplifiers with an RF transformer, or to use a differential input/output amplifier without a transformer, to drive the input of the ADS5522. Texas Instruments offers a wide selection of single-ended operational amplifiers (including the THS3201, THS3202, OPA847, and OPA695) that can be selected depending on the application. An RF gain block amplifier, such as Texas Instruments THS9001, can also be used with an RF transformer for high input frequency applications. The THS4503 is a recommended differential input/output amplifier. Table 4 lists the recommended amplifiers.

When using single-ended operational amplifiers (such as the THS3201, THS3202, OPA847, or OPA695) to provide gain, a three-amplifier circuit is recommended with one amplifier driving the primary of an RF transformer and one amplifier in each of the legs of the secondary driving the two differential inputs of the ADS5522. These three amplifier circuits minimize even-order harmonics. For high frequency inputs, an RF gain block amplifier can be used to drive a transformer primary; in this case, the transformer secondary connections can drive the input of the ADS5522 directly, as shown in Figure 6, or with the addition of the filter circuit shown in Figure 7.

Figure 7 illustrates how R_{IN} and C_{IN} can be placed to isolate the signal source from the switching inputs of the ADC and to implement a low-pass RC filter to limit the input noise into the ADC. It is recommended that these components be included in the ADS5522 circuit layout when any of the amplifier circuits discussed previously are used. The components allow fine-tuning of the circuit performance. Any mismatch between the differential lines of the ADS5522 input produces a degradation in performance at high input frequencies, mainly characterized by an increase in the even-order harmonics. In this case, special care should be taken to keep as much electrical symmetry as possible between both inputs.

Another possible configuration for lower-frequency signals is the use of differential input/output amplifiers that can simplify the driver circuit for applications requiring dc-coupling of the input. Flexible in their configurations (see Figure 8), such amplifiers can be used for single-ended to differential conversion and signal amplification.

Table 4. Recommended Amplifiers to Drive the Input of the ADS5522

INPUT SIGNAL FREQUENCY	RECOMMENDED AMPLIFIER	TYPE OF AMPLIFIER	USE WITH TRANSFORMER?
DC to 20MHz	THS4503	Differential In/Out Amp	No
DC to 50MHz	OPA847	Operational Amp	Yes
10MHz to 120MHz	OPA695	Operational Amp	Yes
	THS3201	Operational Amp	Yes
	THS3202	Operational Amp	Yes
Over 100MHz	THS9001	RF Gain Block	Yes

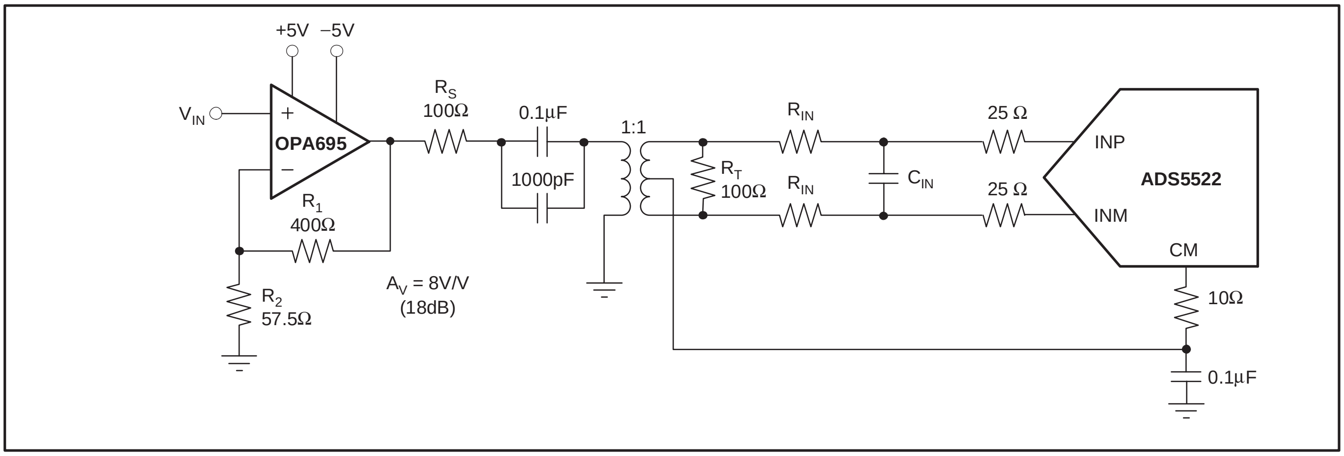


Figure 7. Converting a Single-Ended Input Signal to a Differential Signal Using an RF Transformer

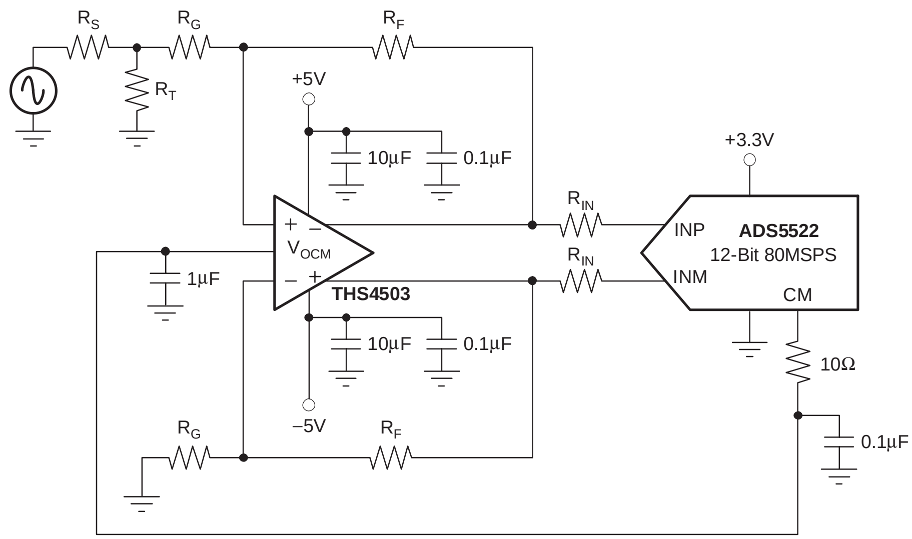


Figure 8. Using the THS4503 with the ADS5522

INPUT VOLTAGE OVER-STRESS

The ADS5522 can handle absolute maximum voltages of 3.6-V dc on the input pins INP and INM. For DC inputs between 3.6 V and 3.8 V, a 25-Ω resistor is required in series with the input pins. For inputs above 3.8 V, the device can handle only transients, which need to have less than 5% duty cycle of overstress. The input pins connect internally to an ESD diode to AV_{DD}, as well as a switched capacitor circuit. The sampling capacitor of the switched capacitor circuit connects to the input pins through a switch in the sample phase. In this phase, an input larger then 2.65 V would cause the switched capacitor circuit tp present an equivalent load of a forward biased diode to 2.65 V, in series with a 60-Ω impedance. Also, beyond the voltage on AV_{DD}, the ESD diode to AV_{DD} starts to become forward biased.

In the phase, where the sampling switch is off, the diode loading from the input switched capacitor circuit is disconnected from the pin, while the ESD loading to AV_{DD} is still present.

CAUTION:

A violation of any of the previously stated conditions could damage the device (or reduce its lifetime) either due to electromigration or gate oxide integrity. Care should be taken not to expose the device to input over-voltage for extended periods of time as it may degrade device reliability.

POWER SUPPLY SEQUENCE

The preferred mode of power supply sequencing is to power-up AV_{DD} first, followed by DRV_{DD}. Raising both supplies simultaneously is also a valid power supply sequence. In the event that DRV_{DD} powers up before AV_{DD} in the system, AV_{DD} must power up within 10 ms of DRV_{DD}.

POWER DOWN

The device will enter power-down mode in one of two ways: either by reducing the clock speed to between dc and 1 MHz, or by setting a bit through the serial programming interface. If reducing the clock speed, power-down may be initiated for any clock frequency below 10 MHz. The actual frequency at which the device powers down varies from device to device.

The device can be powered down by programming the internal register (see *Serial Programming Interface* section). The outputs are put into a high-impedance state and only the internal reference is powered up to shorten the power-up time. The power-down mode reduces power dissipation to approximately 180 mW.

REFERENCE CIRCUIT

The ADS5522 has built-in internal reference generation, requiring no external circuitry on the printed circuit board (PCB). For optimum performance, it is best to connect both REFP and REFM to ground with a 1-µF decoupling capacitor in series with a 1-Ω resistor, as shown in Figure 9. In addition, an external 56-kΩ resistor should be connected from IREF (pin 31) to AGND to set the proper current for the operation of the ADC, as shown in Figure 9. No capacitor should be connected between pin 31 and ground; only the 56-kΩ resistor should be used.

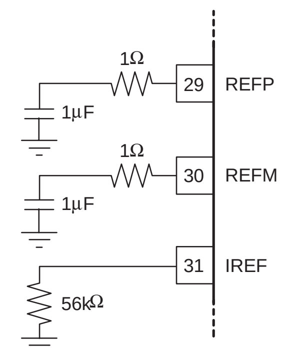


Figure 9. REFP, REFM, and IREF Connections for Optimum Performance

CLOCK INPUT

The ADS5522 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. The common-mode voltage of the clock inputs is set internally to CM (pin 17) using internal 5-kΩ resistors that connect CLKP (pin 10) and CLKM (pin 11) to CM (pin 17), as shown in Figure 10.

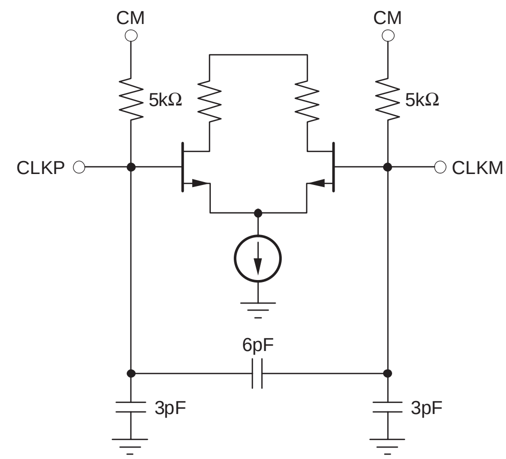


Figure 10. Clock Inputs

When driven with a single-ended CMOS clock input, it is best to connect CLKM (pin 11) to ground with a 0.01-µF capacitor, while CLKP is ac-coupled with a 0.01-µF capacitor to the clock source, as shown in Figure 11.

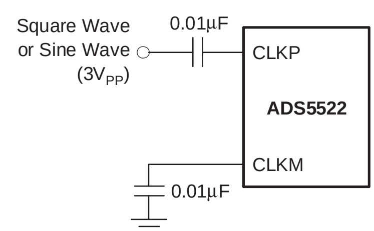


Figure 11. AC-Coupled, Single-Ended Clock Input

The ADS5522 clock input can also be driven differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.01-µF capacitors, as shown in Figure 12.

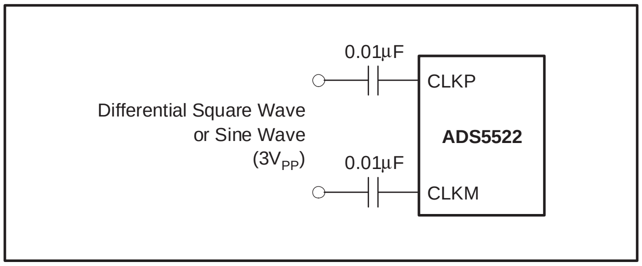


Figure 12. AC-Coupled, Differential Clock Input

For high input frequency sampling, it is recommended to use a clock source with low jitter. Additionally, the internal ADC core uses both edges of the clock for the conversion process. This means that, ideally, a 50% duty cycle should be provided. Figure 13 shows the performance variation of the ADC versus clock duty cycle.

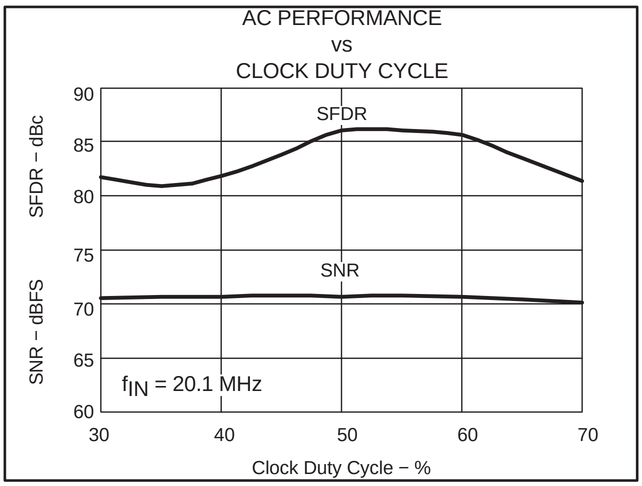


Figure 13. AC Performance vs Clock Duty Cycle

Bandpass filtering of the source can help produce a 50% duty cycle clock and reduce the effect of jitter. When using a sinusoidal clock, the clock jitter will further improve as the amplitude is increased. In that sense, using a differential clock allows for the use of larger amplitudes without exceeding the supply rails and absolute maximum ratings of the ADC clock input. Figure 14 shows the performance variation of the device versus input clock amplitude. For detailed clocking schemes based on transformer or PECL-level clocks, refer to the ADS5522EVM User's Guide, available for download from www.ti.com.

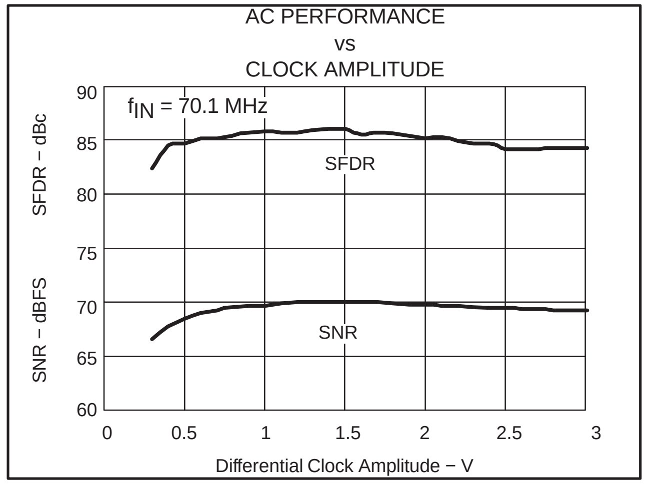


Figure 14. AC Performance vs Clock Amplitude

OUTPUT INFORMATION

The ADC provides 12 data outputs (D11 to D0, with D11 being the MSB and D0 the LSB), a data-ready signal (CLKOUT, pin 43), and an out-of-range indicator (OVR, pin 64) that equals 1 when the output reaches the full-scale limits.

Two different output formats (straight offset binary or two's complement) and two different output clock polarities (latching output data on rising or falling edge of the output clock) can be selected by setting DFS (pin 40) to one of four different voltages. Table 3 details the four modes. In addition, output enable control (OE, pin 41, active high) is provided to put the outputs into a high-impedance state.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full scale level. For a positive overdrive, the output code is 0xFFF in straight offset binary output format, and 0x7FF in 2's complement output format. For a negative input overdrive, the output code is 0x000 in straight offset binary output format, and 0x800 in 2's complement output format. These outputs to an overdrive signal are ensured through design and characterization

The output circuitry of the ADS5522, by design, minimizes the noise produced by the data switching transients, and, in particular, its coupling to the ADC analog circuitry. Output D2 (pin 51) senses the load capacitance and adjusts the drive capability of all the output pins of the ADC to maintain the same output slew rate described in the timing diagram of Figure 1. Care should be taken to ensure that all output lines (including CLKOUT) have nearly the same load as D2 (pin 51). This circuit also reduces the sensitivity of the output timing versus supply voltage or temperature. Placing external resistors in series with the outputs is **not** recommended.

The timing characteristics of the digital outputs change for sampling rates below the 80 MSPS maximum sampling frequency. Table 5 shows the timing parameters for sampling rates of 20 MSPS, 40 MSPS, and 65 MSPS.

To use the input clock as the data capture clock, it is necessary to delay the input clock by a delay, t_d, that results in the desired setup or hold time. Use either of the following equations to calculate the value of t_d.

$$\text{Desired setup time} = t_d - t_{START}$$

$$\text{Desired hold time} = t_{END} - t_d$$

SERIAL PROGRAMMING INTERFACE

The ADS5522 has internal registers that enable the programming of the device into modes as described in previous sections. Programming is done through a 3-wire serial interface. The timing diagram and register settings in the *Serial Programming Interface* section describe the use of this interface.

Table 2 shows the different modes and the bit values to be written to the register to enable them.

The ADS5522 internal registers default to all zeros on reset. The device is reset by applying a high pulse on the RESET pin (pin 35) for a minimum of 2 μs at least 10 ms after both the AV_{DD} and DRV_{DD} power supplies have come up (as illustrated in Figure 2) In reset, the ADC outputs are forced low. Note that the RESET pin has a 200-kΩ pullup resistor to AV_{DD}.

If the ADS5522 is to be used solely in the default mode set at reset, the serial interface pins can be tied to fixed voltages. In this case, tie SCLK high, SEN low, and SDATA to either a high or low voltage.

PowerPAD Package

The PowerPAD package is a thermally enhanced standard size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the printed circuit board (PCB), using the PCB as a heatsink.

Table 5. Timing Characteristics at Additional Sampling Frequencies

F_S (MSPS)	t_{setup} (ns)			t_{hold} (ns)			t_{START} (ns)			t_{END} (ns)			t_{RISE} (ns)			t_{FALL} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
65	4.7	6.0		2.1	3.1			2.4	4.2	8.3	12.0			6.6	7.2		5.5	6.4
40	8.5	11.0		2.8	3.5			−1.0	1.5	8.9	14.5			7.5	8.0		7.3	7.8
20	17.0	25.7		2.5	4.7			−9.8	2.0	9.5	21.6			7.5	8.0		7.6	8.0

Assembly Process

1. Prepare the PCB top−side etch pattern including etch for the leads as well as the thermal pad as illustrated in the Mechanical Data section.
2. Place a 5-by-5 array of thermal vias in the thermal pad area. These holes should be 13 mils in diameter. The small size prevents wicking of the solder through the holes.
3. It is recommended to place a small number of 25 mil diameter holes under the package, but outside the thermal pad area to provide an additional heat path.
4. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
5. Do not use the typical web or spoke via connection pattern when connecting the thermal vias to the ground plane. The spoke pattern increases the thermal resistance to the ground plane.
6. The top−side solder mask should leave exposed the terminals of the package and the thermal pad area.
7. Cover the entire bottom side of the PowerPAD vias to prevent solder wicking.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

For more detailed information regarding the PowerPAD package and its thermal properties, see either the SLMA004B Application Brief *PowerPAD Made Easy* or the SLMA002 Technical Brief *PowerPAD Thermally Enhanced Package.*

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265