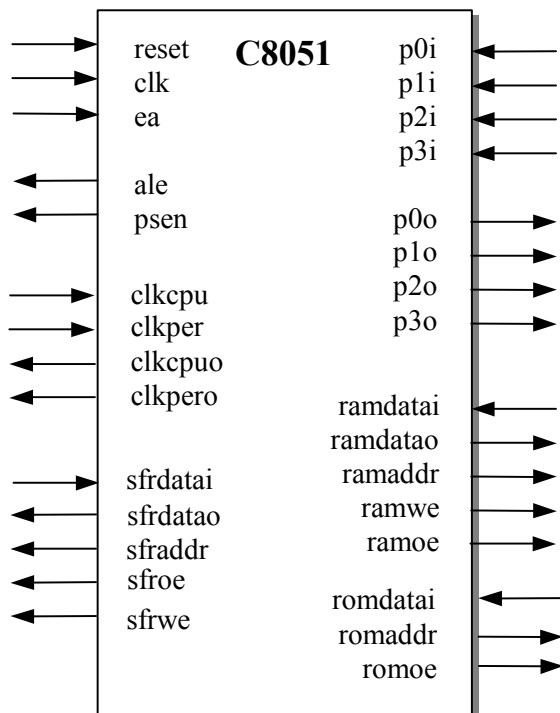


### General Description

The C8051 processor core is a single-chip, 8-bit microcontroller that executes all ASM51 instructions and has the same instruction set and timing of the 80C31. On-chip debugging is an option.

The microcode-free design was developed for reuse in ASICs and FPGAs. It is strictly synchronous, with positive-edge clocking (except for a flip-flop for internal reset and two flip-flops for gated clocks in the PMU), no internal tri-states and a synchronous reset. Scan insertion is therefore straightforward.

### Symbol



### Features

- 8-bit Control Unit
- 8-bit Arithmetic-Logic Unit with 8-bit multiplication and division
- Instruction decoder
- Four 8-bit Input / Output ports
- Two 16-bit Timer/Counters
- Serial Peripheral Interface in full duplex mode
- Synchronous mode, fixed baud rate
- 8-bit & 9-bit UART mode, variable baud rate
- 9-bit UART mode, fixed baud rate
- Multiprocessor communication
- Two Level Priority Interrupt System
- 5 Interrupt Sources
- Internal Clock prescaler and Phase Generator
- 256 bytes of Read/Write Data Memory Space
- 64KB External Program Memory Space
- 64KB External Data Memory Space
- Services up to 107 External Special Function Registers
- Power Management Unit supports stop and idle modes

## Pin Description

The C8051 contains only unidirectional pins. For proper communications via bi-directional Ports 0-3, it is necessary to use in-circuit Open Drains.

Name	Type	Polarity/ Bus size	Description	
p0i	I	8	Port 0: 8-bit bi-directional I/O port with separated inputs and outputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memories.	
p0o	O	8		
p1i	I	8	Port 1: 8-bit bi-directional I/O port with separated inputs and outputs. Port 1 also serves the special features.	
p1o	O	8		
p2i	I	8	Port 2: 8-bit bi-directional I/O port with separated inputs and outputs. Port 2 emits the high-order address byte during fetches from external program memory that use 16-bit addresses (MOVX @DPTR).	
p2o	O	8		
p3i	I	8	Port 3: 8-bit bi-directional I/O port with separated inputs and outputs. Port 3 also serves special features.	
p3o	O	8		
clk	I	Rise	Clock: A pulse for internal clock counters and all synchronous circuits.	
reset	I	High	Hardware reset input: Resets the device when this pin is held high for two clock cycles while the oscillator is running.	
ale	O	High	Address Latch Enable: A pulse for latching the low byte of the Address during an access to external memory. In normal operations, 'ale' is driven at a constant rate of 1/6 the oscillator frequency.	
ea	I	Low	External Access Enable: The 'ea' must be externally held low to enable the device to fetch code from external program memory 0000H and 0FFFH. If 'ea' is held high, the device executes from in-circuit program memory unless the Program counter contains an address greater than 0FFFH.	
psen	O	Low	Program Store Enable: The read strobe to external program memory. When the C8051 is executing code from the external program memory, 'psen' is activated each machine cycle; 'psen' is not activated during fetches from in-circuit program memory.	
romdatai	O	8	Internal Program Memory interface: Memory data bus	
romaddr	O	14		Memory address bus
romoe	O	High		Memory output enable
ramdatai	I	8	Internal Data Memory interface: Memory data bus input	
ramdatao	O	8		Memory data bus output
ramaddr	O	8		Memory address bus
ramwe	O	High		Memory write enable
ramoe	O	High		Memory output enable
sfrdatai	I	8	External Special Function Registers interface: SFR data bus input	
sfrdatao	O	8		SFR data bus output
sfraddr	O	7		SFR address bus
sfrwe	O	High		SFR write enable
sfro	O	High		SFR output enable
clkcpu	I	Rise	Engine clock A pulse for internal circuits that are stopped when the C8051 is in IDLE or STOP mode	
clkper	I	Rise	Peripheral clock A pulse for internal circuits that are stopped when the C8051 is in STOP mode	
clkcpuo	O	Rise	Engine clock output The gated clkcpu clock. Clkcpuo stays low when the C8051 enters IDLE or STOP mode. The clkcpuo is dedicated to off-core connection to the clkcpu input.	
clkpero	O	Rise	Peripheral clock output The gated clkper clock. Clkpero stays low when the C8051 enters into STOP mode. The clkpero is dedicated to off-core connection to the clkper input.	

## Optional Features

- Fast Multiplication-Division Unit
  - 16 x 16 bit multiplication
  - 32 / 16 bit division
  - 16 / 16 bit division
  - 32 bit normalization
  - 32 bit L/R shifting
- Compare/Capture Unit
  - Four 16-bit Compare registers used for Pulse With Modulation
  - Four external Capture inputs used for Pulse With Measuring
  - 16-bit Reload register used for Pulse Generation
- Programmable Watchdog Timer
- Third 16-bit Timer/Counter
- Second Serial Peripheral Interfaces
- Real Time Clock

## Verification Methods

The C8051 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C31 chip, and the results compared with the core's simulation outputs.

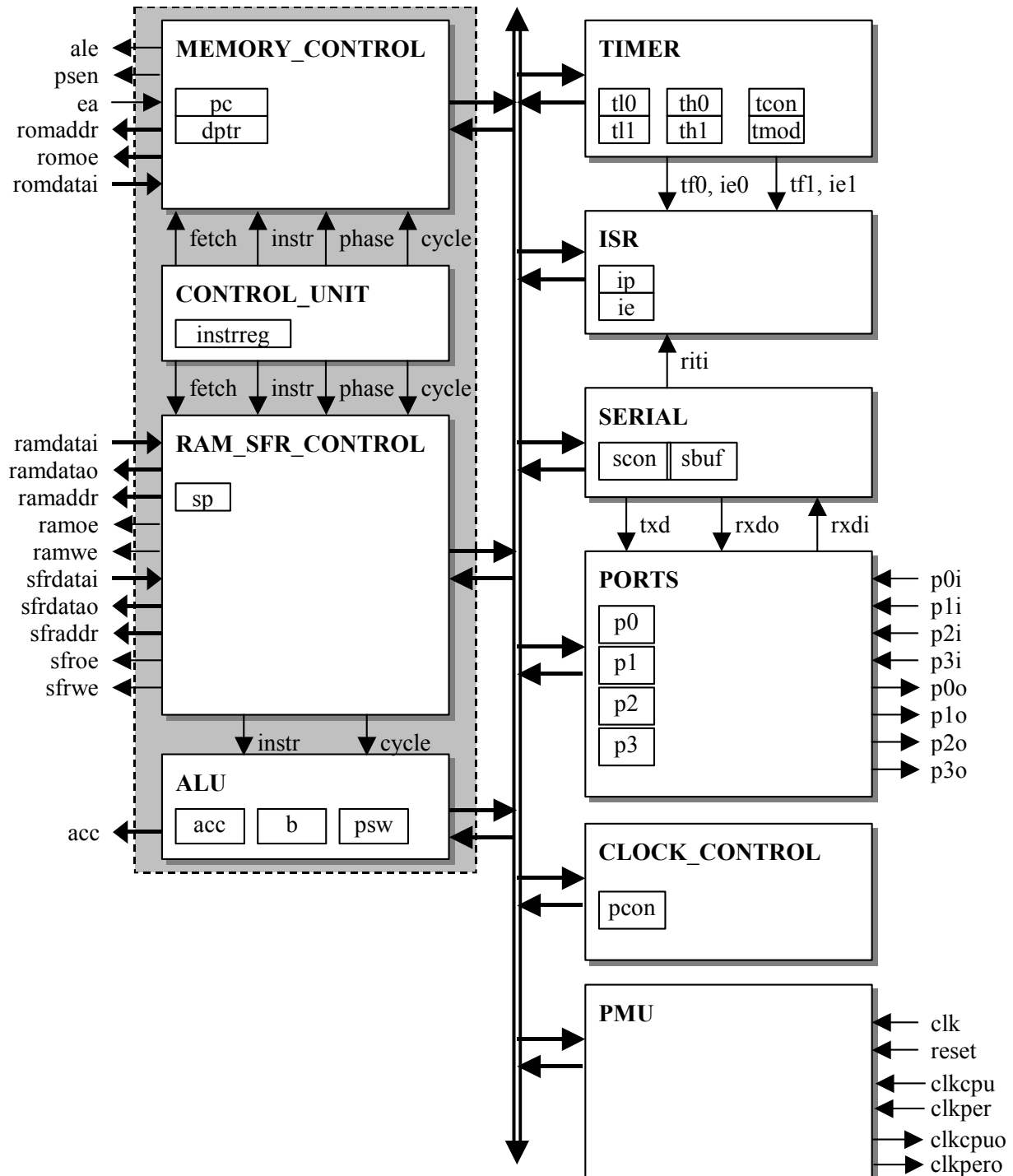
## Development Environment

- HDL source code for the C8051
- Synthesis & simulation scripts
- Example CHIP\_C8051 – 8051 compatible design
  - This design uses the C8051 and illustrates how to build and connect memories and port modules
- Extensive HDL testbench that instantiates:
  - Example design CHIP\_C8051
  - External RAM
  - External ROM
  - Clock generator
  - Process that compares your simulation results with the expected results
- A collection of 8051 assembler programs which are executed directly by the testbench
- A set of expected results
- Documentation
- Design support including consulting

## Applications

- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and video

## Block Diagram



## Related Information

8-bit Embedded Controllers, Intel, 1990

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This core developed by the  
processor experts at  
Evatronix SA

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