19-1332; Rev 1; 4/03

MAXIM

Low-Voltage, Single-Supply Multiplexer and Switch

General Description

The MAX4524/MAX4525 are low-voltage, single-supply CMOS analog switches configured as a 4-channel multiplexer/demultiplexer (MAX4524) and a double-pole/double-throw (DPDT) switch (MAX4525). Both have an inhibit input to simultaneously open all signal paths.

These devices operate from a single supply of +2V to +12V and are optimized for operation with +3V or +5V supplies. On-resistance is 200Ω with a +5V supply and 500Ω with a +3V supply. Each switch can handle Rail-to-Rail® analog signals. The off-leakage current is only 2nA at +25°C or 20nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply.

Applications

Battery-Operated Equipment

Audio and Video Signal Routing

Low-Voltage Data-Acquisition Systems

Communications Circuits

Features

- **Tiny 10-Pin Thin QFN Package**
- **Single-Supply Operation from +2V to +12V**
- **200Ω On-Resistance with +5V Supply**
- **500Ω On-Resistance with +3V Supply**
- **Guaranteed 8Ω On-Resistance Match at +5V**
- **Guaranteed 2nA Max On-Leakage at +5V**
- **TTL/CMOS-Logic Compatible**

Ordering Information

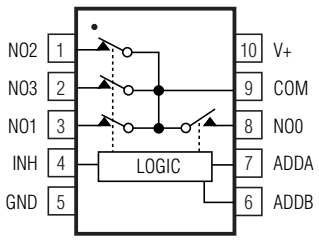
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4524CUB	0°C to +70°C	10 µMAX	—
MAX4524C/D	0°C to +70°C	Dice*	—
MAX4524EUB	-40°C to +85°C	10 µMAX	—
MAX4524ETB	-40°C to +85°C	10 Thin QFN (3mm x 3mm)	AAP
MAX4525CUB	0°C to +70°C	10 µMAX	—
MAX4525C/D	0°C to +70°C	Dice*	—
MAX4525EUB	-40°C to +85°C	10 µMAX	—
MAX4525ETB	-40°C to +85°C	10 Thin QFN (3mm x 3mm)	AAQ

**Contact factory for availability.*

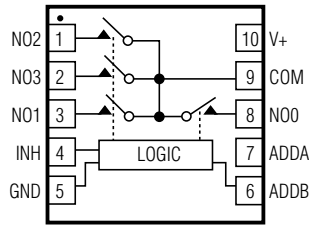
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW

MAXIM
MAX4524

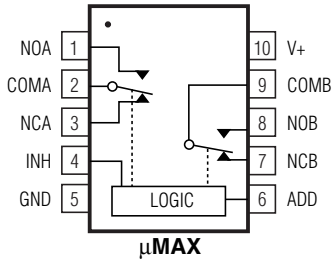


µMAX

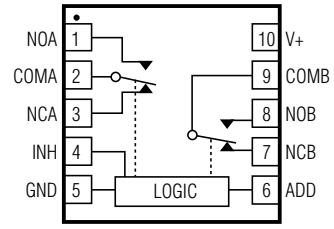


THIN QFN

MAXIM
MAX4525



µMAX



THIN QFN

MAX4525

INH	ADD	ON SWITCH
1	X	NONE
0	0	COMA-NCA, COMB-NCB
0	1	COMA-NOA, COMB-NOB

MAX4524

INH	ADDB	ADDA	ON SWITCH
1	X	X	NONE
0	0	0	COM-NO0
0	0	1	COM-NO1
0	1	0	COM-NO2
0	1	1	COM-NO3

X = DON'T CARE

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Low-Voltage, Single-Supply Multiplexer and Switch

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V+ .....-0.3V, +13V
Voltage into any terminal (Note 1) .....-0.3V to (V+ + 0.3V)
Continuous Current into any Terminal .....±20mA
Peak Current, NO, NC or COM_
(pulsed at 1ms,10% duty cycle).....±40mA
ESD per Method 3015.7 .....>2000V

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW
10-Pin Thin QFN (derate 24.4mW/°C above +70°C) ..1951mW
Operating Temperature Ranges
MAX452_C_ _ .....0°C to +70°C
MAX452_E_ _.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C

Note 1: Voltages exceeding V+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = 4.5V to 5.5V, GND = 0V, V_{AH} = 2.4V, V_{AL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 7)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
					(Note 2)			
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E	V-		V+	V
COM-NO/NC On-Resistance	R_{ON}	V+ = 4.5V, I_{COM} = 1mA, V_{COM} = 3.5V		+25°C		90	150	Ω
				C, E			200	
COM-NO/NC On-Resistance Match Between Channels (Note 3)	ΔR_{ON}	V+ = 4.5V, I_{COM} = 1mA, V_{COM} = 3.5V		+25°C		2	10	Ω
				C, E			15	
COM-NO/NC On-Resistance Flatness (Note 4)	R_{FLAT}	V+ = 5.5V; I_{COM} = 1mA; V_{COM} = 1.5V, 2.5V, 3.5V		+25°C		5	12	Ω
NO/NC Off-Leakage (Note 5)	$I_{NO(OFF)}$, $I_{NC(OFF)}$,	V+ = 5.5V; V_{NO} = 1V, 4.5V; V_{COM} = 4.5V, 1V		+25°C	-1		+1	nA
				C, E	-10		+10	
COM Off-Leakage (Note 5)	$I_{COM(OFF)}$	V+ = 5.5V; V_{NO} = 1V, 4.5V; V_{COM} = 4.5V, 1V	MAX4524	+25°C	-2		+2	nA
				C, E	-50		+50	
			MAX4525	+25°C	-1		+1	
				C, E	-25		+25	
COM On-Leakage (Note 5)	$I_{COM(ON)}$	V+ = 5.5V; V_{COM} = 4.5V, 1V	MAX4524	+25°C	-2		+2	nA
				C, E	-50		+50	
			MAX4525	+25°C	-1		+1	
				C, E	-25		+25	
DIGITAL I/O								
Logic Input Logic Threshold High	V_{IH}			C, E		1.5	2.4	V
Logic Input Logic Threshold Low	V_{IL}			C, E	0.8	1.5		V
Input Current High	I_{IH}	V_A = V_{INH} = 2.4V		C, E	-1		+1	µA
Input Current Low	I_{IH}	V_A = V_{INH} = 0.8V		C, E	-1		+1	µA

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = 4.5V to 5.5V, GND = 0V, V_{AH} = 2.4V, V_{AL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 7)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS								
Inhibit Turn-On Time	$t_{(ON)}$	$V_{NO\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Figure 2		+25°C		90	150	ns
				C, E			200	
Inhibit Turn-Off Time	$t_{(OFF)}$	$V_{NO\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Figure 2		+25°C		40	120	ns
				C, E			180	
Address Transition Time	t_{TRANS}	$V_{NO\_}$ = 3V/0V, R_L = 300Ω, C_L = 35pF, Figure 1		+25°C		90	150	ns
				C, E			200	
Break-Before-Make Time	t_{BBM}	$V_{NO\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Figure 3		+25°C	5	20		ns
Charge Injection (Note 6)	Q	C = 1nF, R_S = 0Ω, V_S = 2.5V, Figure 4		+25°C		0.8	5	pC
NO/NC Off-Capacitance	$C_{NO(OFF)}$	$V_{NO\_}$ = 0V, f = 1MHz, Figure 6		+25°C		4		pF
COM Off-Capacitance	$C_{COM(OFF)}$	$V_{NO\_}$ = 0V, f = 1MHz, Figure 6	MAX4524	+25°C		14		pF
			MAX4525	+25°C		6		
COM On-Capacitance	$C_{COM(ON)}$	$V_{NO\_}$ = 0V, f = 1MHz, Figure 6	MAX4524	+25°C		20		pF
			MAX4525	+25°C		12		
Off-Isolation	V_{ISO}	R_L = 50Ω, f = 1MHz, Figure 5		+25°C		-75		dB
Channel-to-Channel Crosstalk (MAX4525)	V_{CT}	R_L = 50Ω, f = 1MHz, Figure 5		+25°C		-74		dB
Total Harmonic Distortion	THD	R_L = 600Ω, V_{COM} = 2.5Vp-p, 20Hz to 20kHz		+25°C		0.2		%
POWER SUPPLY								
Power-Supply Range	V+			C, E	2		12	V
Power-Supply Current	I+	V+ = 5.5V, V_{ADD} = V_{INH} = V+ or 0V		+25°C	-1		+1	µA
				C, E	-10		+10	

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = 2.7V to 3.6V, GND = 0V, V_{AH} = 2.0V, V_{AL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 7)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E	V-		V+	V
COM-NO/NC On-Resistance	R_{ON}	V+ = 2.7V, I_{COM} = 0.1mA, V_{COM} = 1.5V		+25°C		190	400	Ω
				C, E			500	
NO/NC Off-Leakage (Note 6)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V+ = 3.6V; V_{NO} = 1V, 3V; V_{COM} = 3V, 1V		+25°C	-1		+1	nA
				C, E	-10		+10	
COM Off-Leakage (Note 6)	$I_{COM(OFF)}$	V+ = 3.6V; V_{NO} = 1V, 3V; V_{COM} = 3V, 1V	MAX4524	+25°C	-2		+2	nA
				C, E	-50		+50	
			MAX4525	+25°C	-1		+1	
				C, E	-25		+25	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = 2.7V to 3.6V, GND = 0V, V_{AH} = 2.0V, V_{AL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 7)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP (Note 2)	MAX	UNITS
COM On-Leakage (Note 6)	$I_{COM(ON)}$	V+ = 3.6V; V_{COM} = 3V, 1V	MAX4524	+25°C	-2		+2	nA
				C, E	-50		+50	
			MAX4525	+25°C	-1		+1	
				C, E	-25		+25	
DIGITAL I/O								
Logic Input Logic Threshold High	V_{IH}			C, E		1.0	2.0	V
Logic Input Logic Threshold Low	V_{IL}			C, E	0.5	1.0		V
Input Current High	I_{IH}	V_A = V_{INH} = 2.0V		C, E	-1		+1	µA
Input Current Low	I_{IH}	V_A = V_{INH} = 0.5V		C, E	-1		+1	µA
SWITCH DYNAMIC CHARACTERISTICS (Note 6)								
Inhibit Turn-On Time	$t_{(ON)}$	$V_{NO\_}$ = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 2		+25°C		170	300	ns
				C, E			400	
Inhibit Turn-Off Time	$t_{(OFF)}$	$V_{NO\_}$ = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 2		+25°C		50	200	ns
				C, E			300	
Address Transition Time	t_{TRANS}	$V_{NO\_}$ = 1.5V/0V, R_L = 300Ω, C_L = 35pF, Figure 1		+25°C		130	300	ns
				C, E			400	
Break-Before-Make Time	t_{BBM}	Figure 3, $V_{NO\_}$ = 1.5V, R_L = 300Ω, C_L = 35pF		+25°C	5	40		ns
POWER SUPPLY								
Power-Supply Current	I+	V+ = 3.6V, V_{ADD} = V_{INH} = V+ or 0V		+25°C	-1		+1	µA
				C, E	-10		+10	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: ΔR_{ON} = $R_{ON(MAX)}$ - $R_{ON(MIN)}$

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., V_{NO} = 3V to 0V and 0V to 3V.

Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.

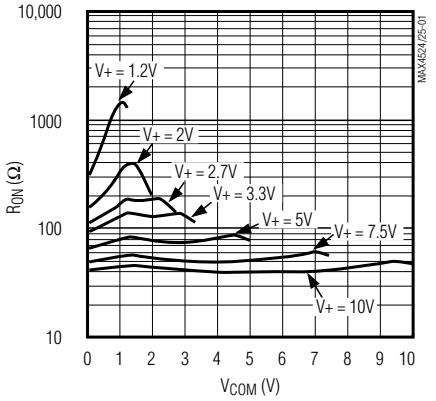
Note 6: Guaranteed by design, not production tested.

Note 7: Thin QFN parts are tested at +25°C and are guaranteed by design and correlation over the entire temperature range.

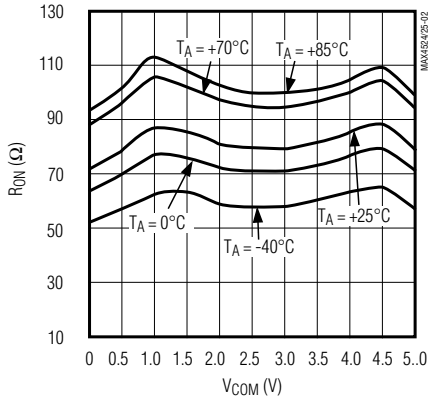
Typical Operating Characteristics

(V+ = 5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

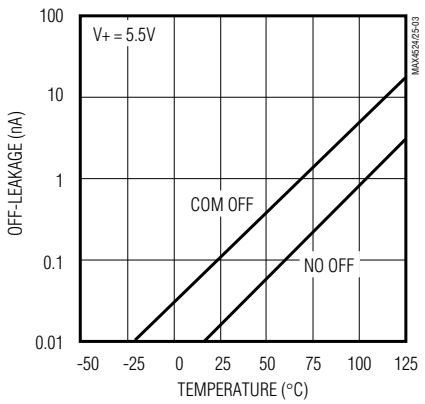
ON-RESISTANCE vs. V_{COM}



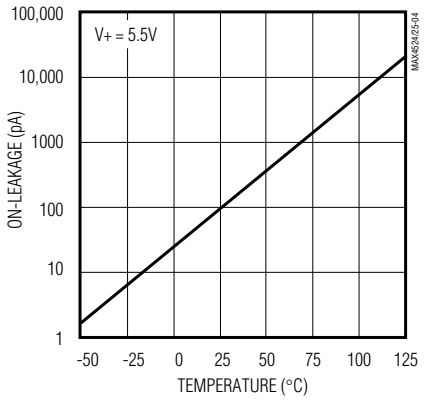
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



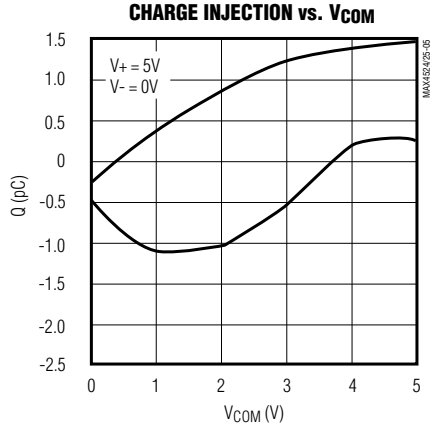
OFF-LEAKAGE vs. TEMPERATURE



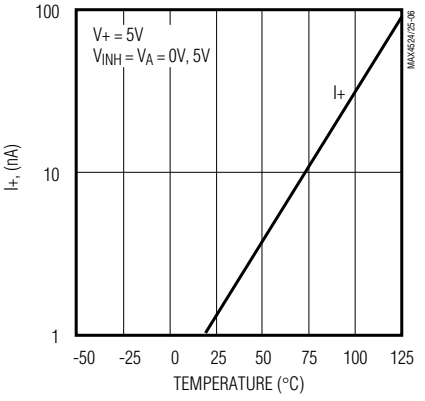
ON-LEAKAGE vs. TEMPERATURE



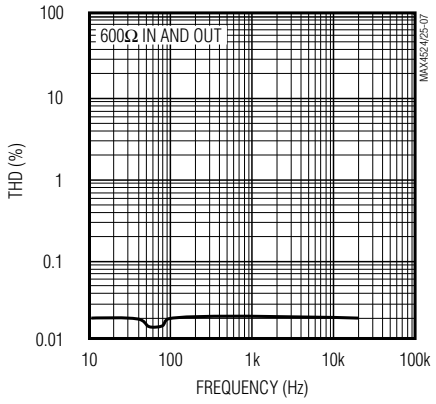
CHARGE INJECTION vs. V_{COM}



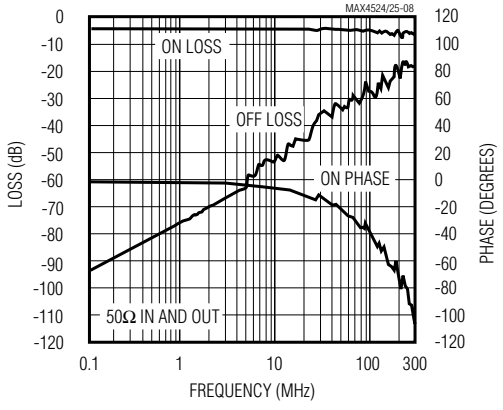
SUPPLY CURRENT vs. TEMPERATURE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



FREQUENCY RESPONSE

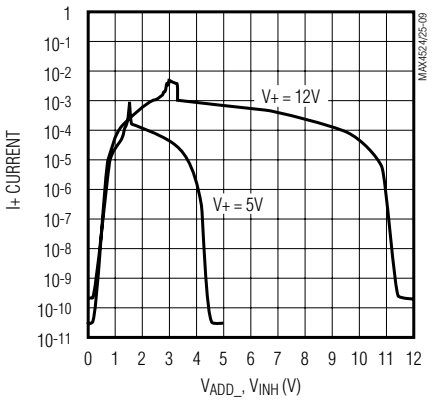


Low-Voltage, Single-Supply Multiplexer and Switch

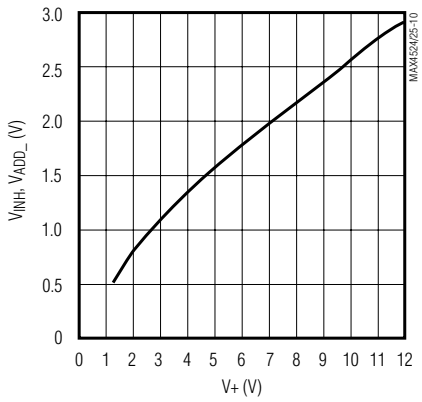
Typical Operating Characteristics (continued)

(V+ = +5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

V+ CURRENT vs. LOGIC LEVEL



LOGIC-LEVEL THRESHOLD vs. V+



Pin Description

MAX4524	MAX4525	NAME	FUNCTION
1	—	NO2	Analog Switch Normally Open Input 2
—	1	NOA	Analog Switch “A” Normally Open Input
2	—	NO3	Analog Switch Normally Open Input 3
—	2	COMA	Analog Switch “A” Common
3	—	NO1	Analog Switch Normally Open Input 1
—	3	NCA	Analog Switch “A” Normally Closed Input
4	4	INH	Inhibit. Connect to GND for normal operation. Connect to logic-level high to turn all switches off.
5	5	GND	Ground. Connect to digital ground (analog signals have no ground reference, but are limited to V+ and GND).
6	—	ADDB	Logic-Level Address Input (see *Truth Tables*)
—	6	ADD	Logic-Level Address Input (see *Truth Tables*)
7	—	ADDA	Logic-Level Address Input (see *Truth Tables*)
—	7	NCB	Analog Switch “B” Normally Closed Input
8	—	NO0	Analog Switch Normally Open Input 0
—	8	NOB	Analog Switch “B” Normally Open Input
9	—	COM	Analog Switch Common
—	9	COMB	Analog Switch “A” Common
10	10	V+	Positive Analog and Digital Supply-Voltage Input

Note: NO_, NC_, and COM_ analog signal pins are identical and interchangeable. Any may be considered an input or output; signals pass equally well in both directions.

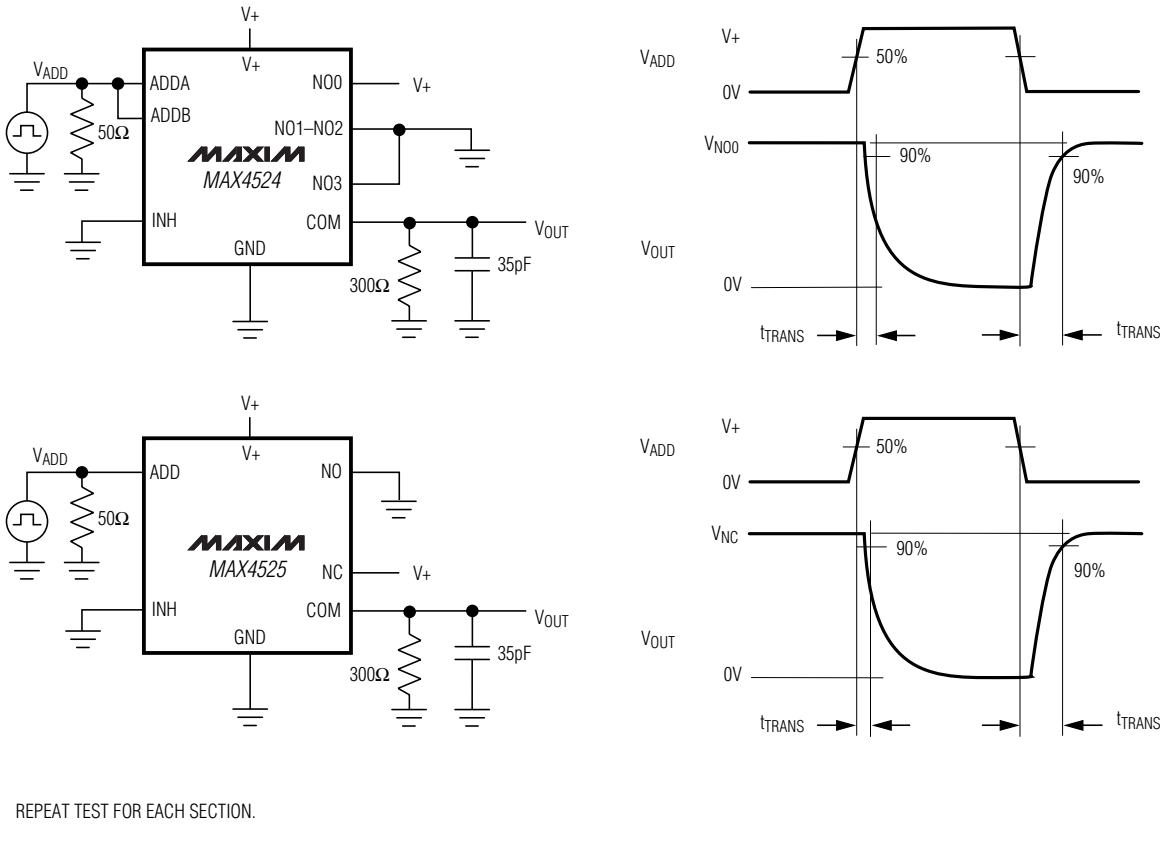
Applications Information

Power-Supply Considerations

The MAX4524/MAX4525's construction is typical of most CMOS analog switches. They have two supply pins: V+ and GND. V+ and GND are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and GND. If any analog signal exceeds V+ or GND, one of these diodes will conduct. During normal operation, these (and other) reverse-biased ESD diodes leak, forming the only current drawn from V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse-biased differently. Each is biased by either V+ or GND and the analog signal. This means that leakage will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

Test Circuits/Timing Diagrams



REPEAT TEST FOR EACH SECTION.

Figure 1. Address Transition Time

Low-Voltage, Single-Supply Multiplexer and Switch

There is no connection between the analog signal paths and GND. V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels into switched V+ and GND signals to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. V+ has an ESD-protection diode to GND.

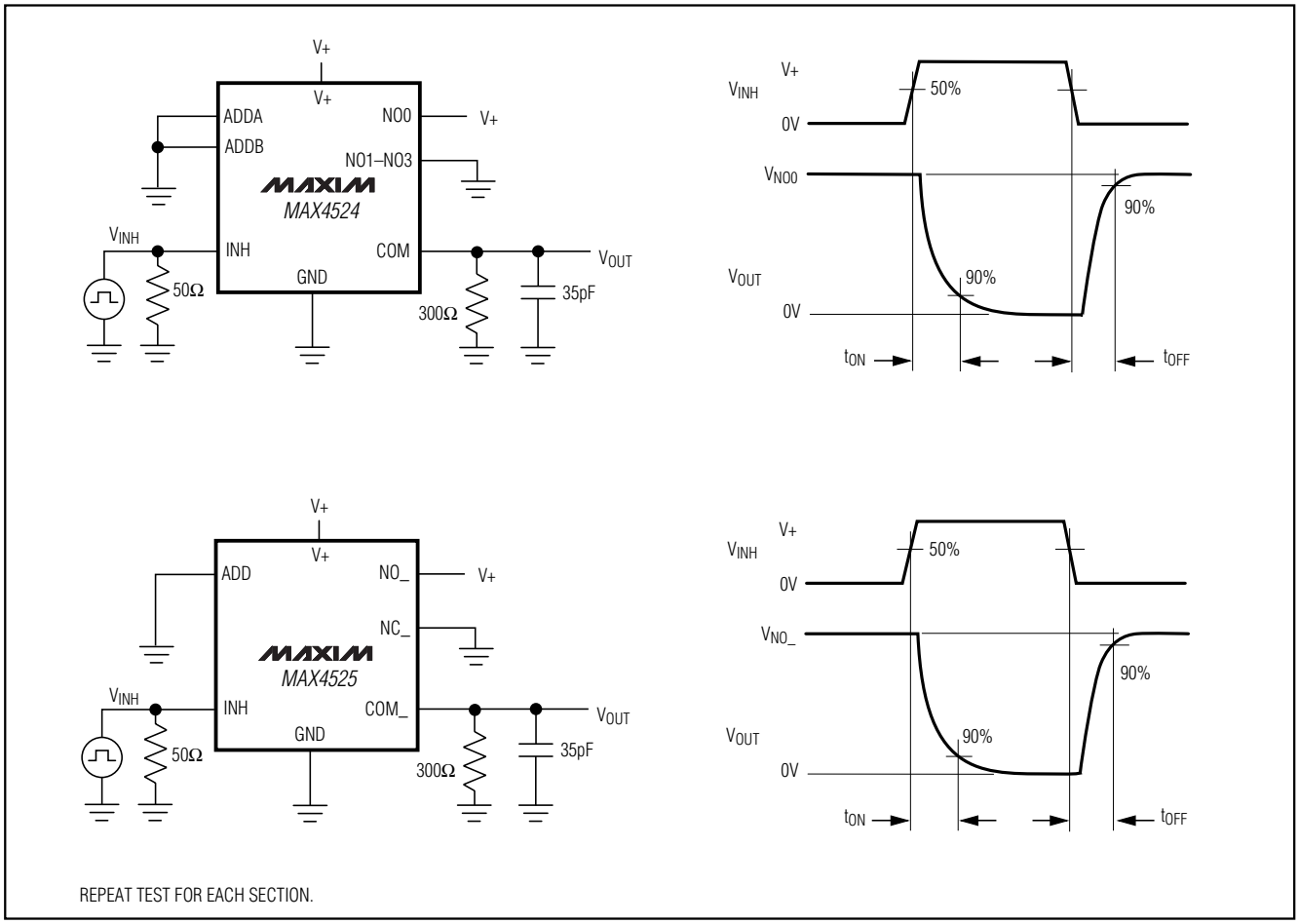
Low-Voltage Operation

These devices operate from a single supply between +2V and +12V. At room temperature, they actually "work" with a single supply at near or below +1.7V, although as supply voltage decreases, switch on-resistance and switching times become very high.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on-response has several minor peaks, which are highly layout dependent. The problem is not turning the switch on, but turning it off. The off-state switch acts like a capacitor, and passes higher frequencies with less attenuation. At 10MHz, off-isolation is about -50dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also degrade off-isolation. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is entirely due to capacitive coupling.

Test Circuits/Timing Diagrams (continued)



REPEAT TEST FOR EACH SECTION.

Figure 2. Inhibit Switching Times

Test Circuits/Timing Diagrams (continued)

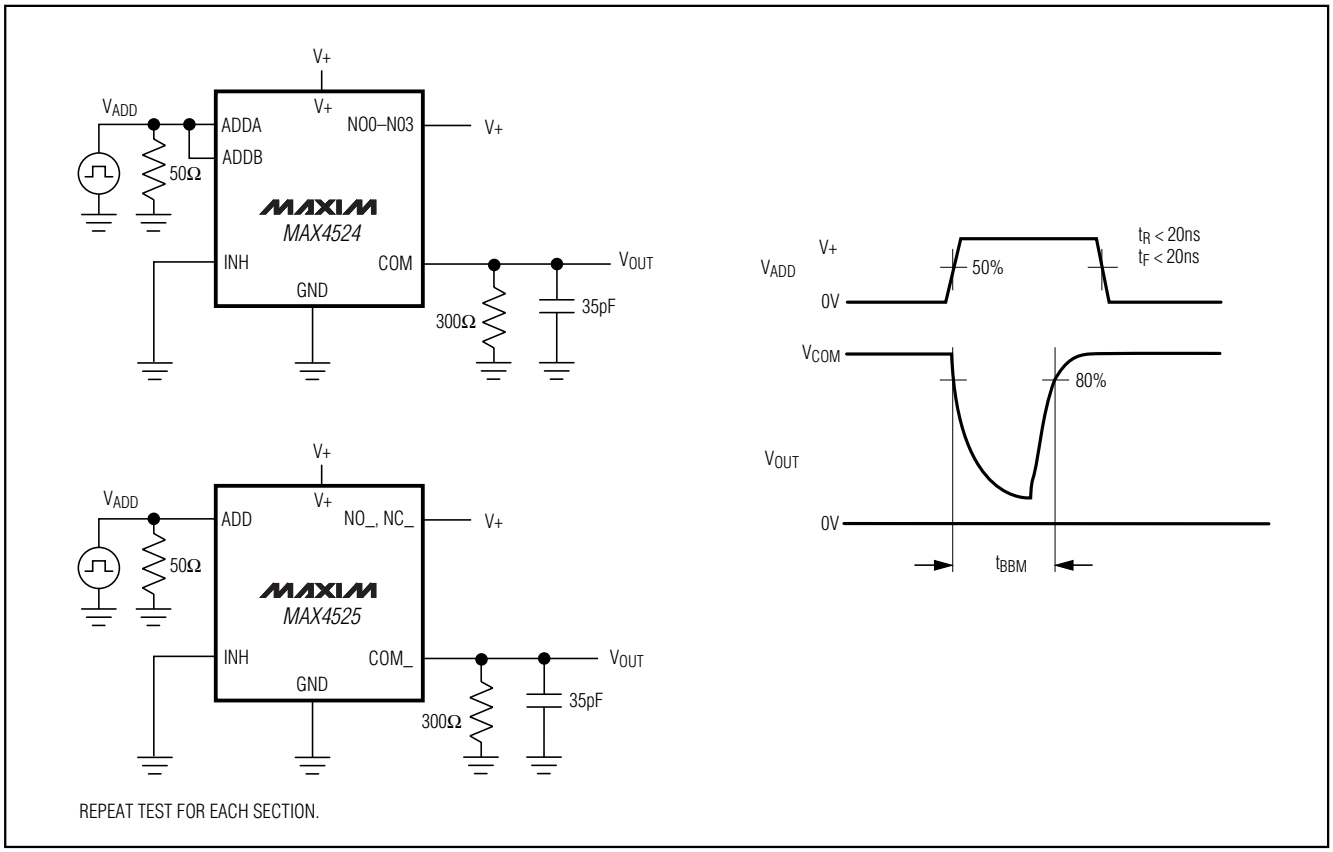


Figure 3. Break-Before-Make Interval

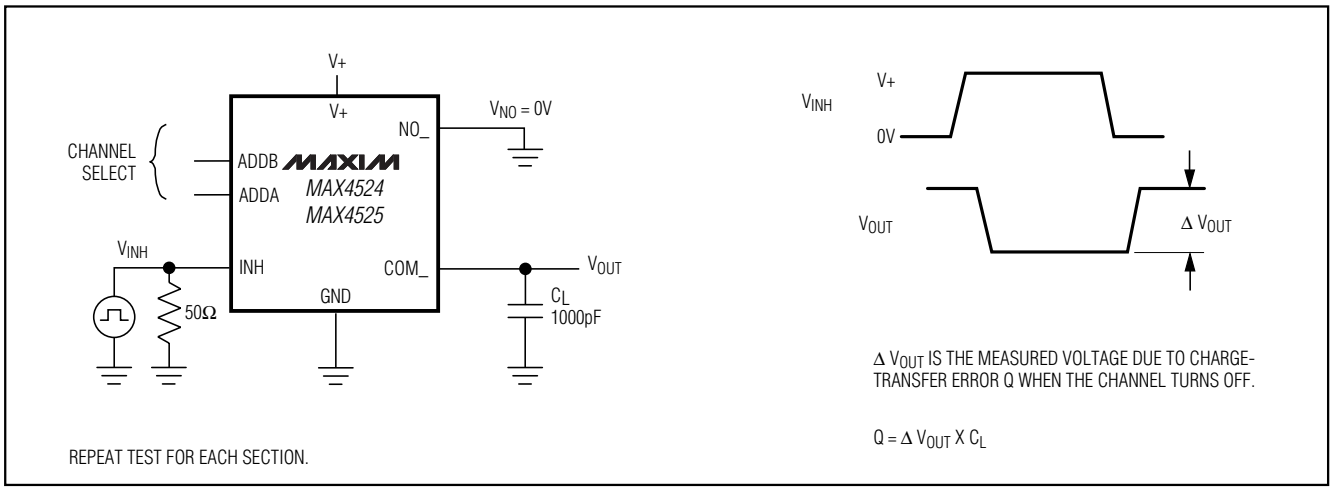
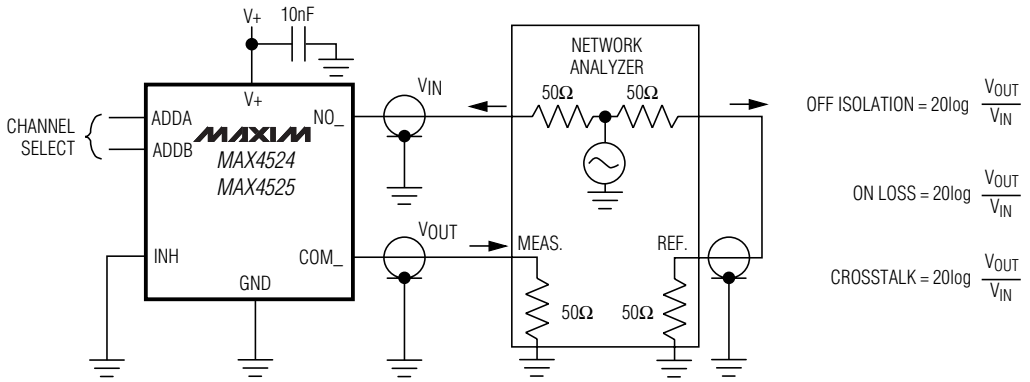


Figure 4. Charge Injection

Low-Voltage, Single-Supply Multiplexer and Switch

Test Circuits/Timing Diagrams (continued)



MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.
OFF-ISOLATION IS MEASURED BETWEEN COM AND "OFF" NO TERMINAL ON EACH SWITCH.
ON-LOSS IS MEASURED BETWEEN COM AND "ON" NO TERMINAL ON EACH SWITCH.
CROSSTALK (MAX4524) IS MEASURED FROM ONE CHANNEL (A, B) TO OTHER CHANNEL.
SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.

Figure 5. Off-Isolation, On-Loss, and Crosstalk

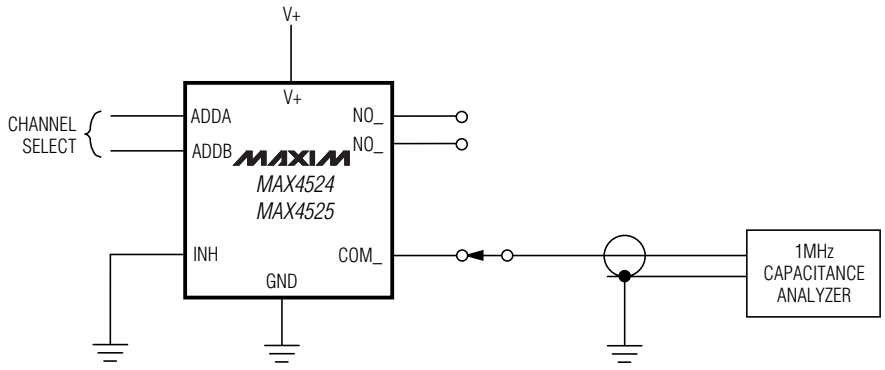
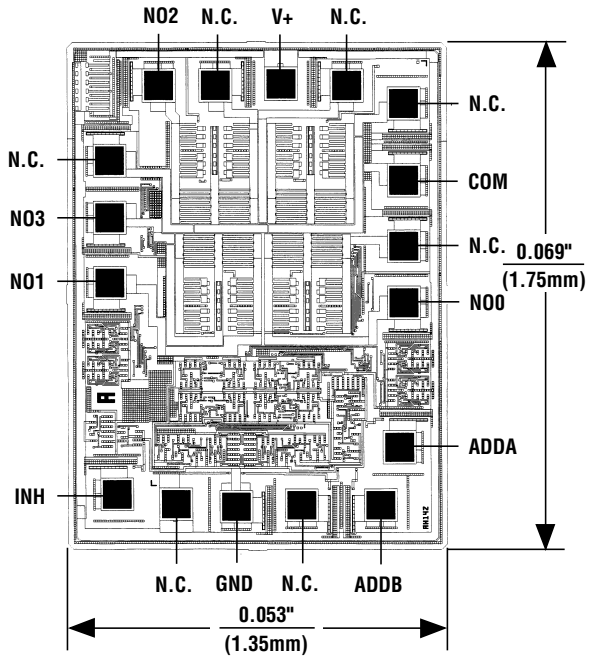


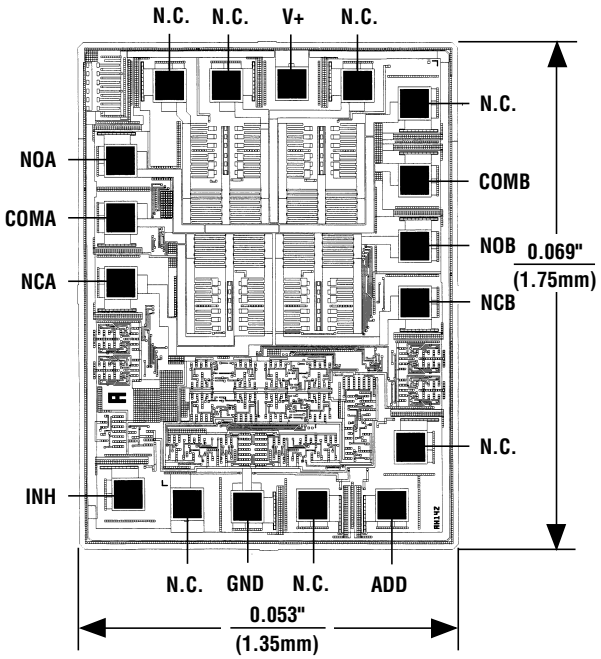
Figure 6. NO/COM Capacitance

Chip Topographies

MAX4524



MAX4525



N.C. = No Connection

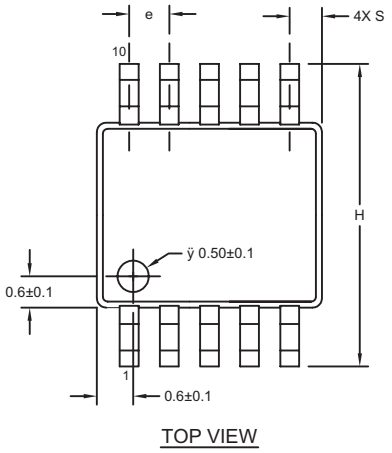
TRANSISTOR COUNT: 219
SUBSTRATE CONNECTED TO V+

Low-Voltage, Single-Supply Multiplexer and Switch

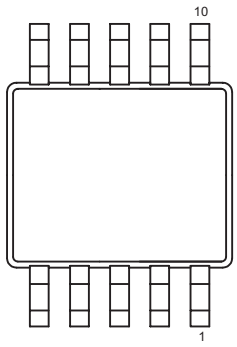
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

10LUMAX.EPS

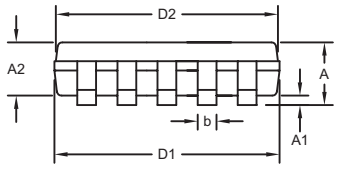


TOP VIEW

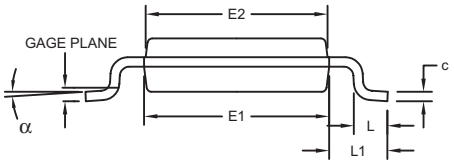


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0∞	6∞	0∞	6∞



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

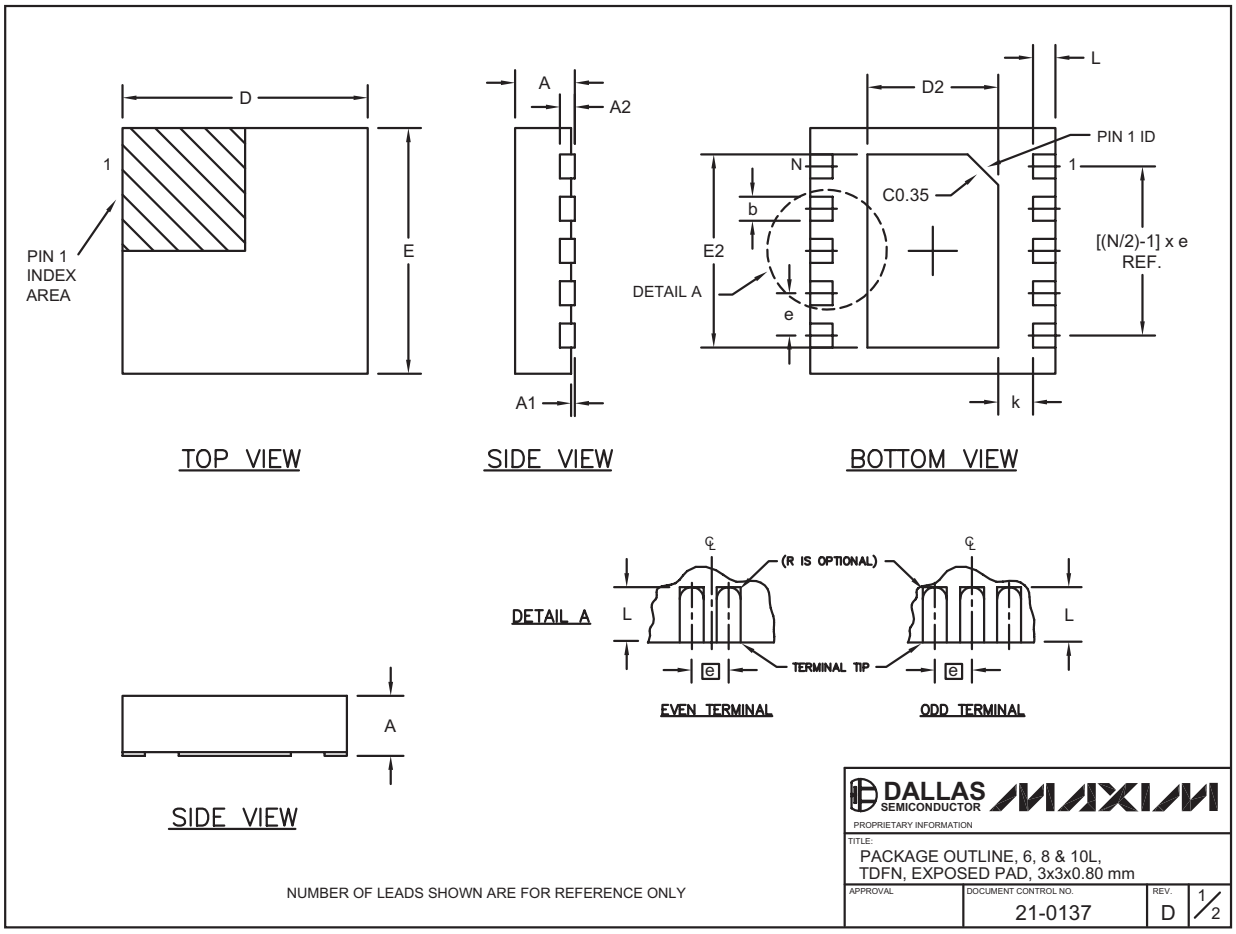
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Low-Voltage, Single-Supply Multiplexer and Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2".
6. "N" IS THE TOTAL NUMBER OF LEADS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 6, 8 & 10L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	D	2/2