50 Hz to 2.7 GHz 60 dB TruPwr™ Detector

AD8362

FEATURES

Complete fully calibrated measurement/control system
Accurate rms-to-dc conversion from 50 Hz to 2.7 GHz
Input dynamic range of >60 dB: –52 dBm to +8 dBm in 50 Ω
Waveform and modulation independent, such as GSM/CDMA/TDMA
Linear-in-decibels output, scaled 50 mV/dB
Law conformance error of 0.5 dB
All functions temperature and supply stable
Operates from 4.5 V to 5.5 V at 24 mA from –40°C to +85°C
Power-down capability to 1.3 mW

APPLICATIONS

Power amplifier linearization/control loops
Transmitter power control
Transmitter signal strength indication (TSSI)
RF instrumentation

FUNCTIONAL BLOCK DIAGRAM

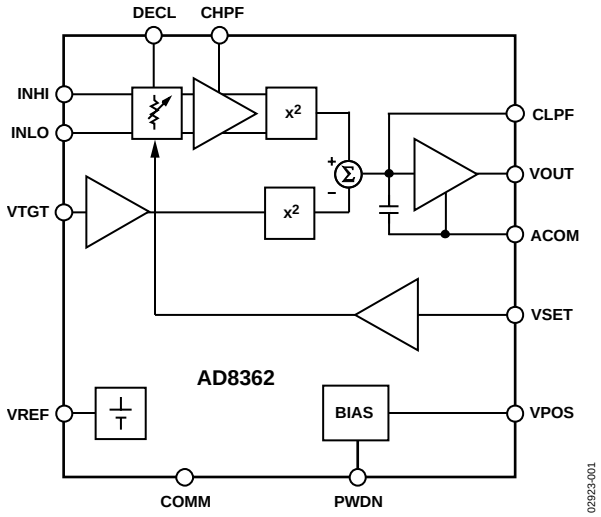

Figure 1.

GENERAL DESCRIPTION

The AD8362 is a true rms-responding power detector that has a 60 dB measurement range. It is intended for use in a variety of high frequency communication systems and in instrumentation requiring an accurate response to signal power. It is easy to use, requiring only a single supply of 5 V and a few capacitors. It can operate from arbitrarily low frequencies to over 2.7 GHz and can accept inputs that have rms values from 1 mV to at least 1 Vrms, with large crest factors, exceeding the requirements for accurate measurement of CDMA signals.

The input signal is applied to a resistive ladder attenuator that comprises the input stage of a variable gain amplifier. The 12 tap points are smoothly interpolated using a proprietary technique to provide a continuously variable attenuator, which is controlled by a voltage applied to the VSET pin. The resulting signal is applied to a high performance broadband amplifier. Its output is measured by an accurate square-law detector cell. The fluctuating output is then filtered and compared with the output of an identical squarer, whose input is a fixed dc voltage applied to the VTGT pin, usually the accurate reference of 1.25 V provided at the VREF pin.

The difference in the outputs of these squaring cells is integrated in a high gain error amplifier, generating a voltage at the VOUT pin with rail-to-rail capabilities. In a controller mode, this low noise output can be used to vary the gain of a host system's RF amplifier, thus balancing the set point against the input power. Optionally, the voltage at VSET may be a replica of the RF signal's amplitude modulation, in which case the overall effect is to remove the modulation component prior to detection and low-pass filtering. The corner frequency of the averaging filter may be lowered without limit by adding an external capacitor at the CLPF pin. The AD8362 can be used to determine the true power of a high frequency signal having a complex low frequency modulation envelope, or simply as a low frequency rms voltmeter. The high-pass corner generated by its offset-nulling loop can be lowered by a capacitor added on the CHPF pin.

Used as a power measurement device, VOUT is strapped to VSET. The output is then proportional to the logarithm of the rms value of the input. In other words, the reading is presented directly in decibels and is conveniently scaled 1 V per decade, or 50 mV/dB; other slopes are easily arranged. In controller modes, the voltage applied to VSET determines the power level required at the input to null the deviation from the setpoint. The output buffer can provide high load currents.

The AD8362 has a 1.3 mW power consumption when powered down by a logic high applied to the PWDN pin. It powers up within about 20 µs to its nominal operating current of 20 mA at 25°C. The AD8362 is supplied in a 16-lead TSSOP package for operation over the industrial temperature range of –40°C to +85°C. An evaluation board is available.

Rev. C

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2/03—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T = 25°C, Z_O = 50 Ω, differential input drive via balun[1], VTGT connected to VREF, VOUT tied to VSET, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Maximum Input Frequency			2.7		GHz
Input Power Range (Differential)	dB referred to 50 Ω impedance level, f ≤ 2.7 GHz, into 1:4 balun[1]				
Nominal Low End of Range			−52		dBm
Nominal High End of Range			+8		dBm
Input Voltage Range (Differential)	RMS voltage at input terminals, f ≤ 2.7 GHz, into input of the device				
Nominal Low End of Range			1.12		mV rms
Nominal High End of Range			1.12		V rms
Input Power Range (S-Sided)	Single-ended drive, CW input, f ≤ 2.7 GHz, into input resistive network[2]				
Nominal Low End of Range			−40		dBm
Nominal High End of Range			0		dBm
Input Voltage Range (S-Sided)	RMS voltage at input terminals, f ≤ 2.7 GHz				
Nominal Low End of Range			2.23		mV rms
Nominal High End of Range			223		V rms
Output Voltage Range	R_L ≥ 200 Ω to ground				
Nominal Low End of Range			+100		mV
Nominal High End of Range	In general, V_S − 0.1 V		+4.9		V
Output Scaling (Log Slope)			50		mV/dB
Law Conformance Error	Over central 60 dB range, f ≤ 2.7 GHz		±0.5		dB
RF INPUT INTERFACE	Pins INHI, INLO, ac-coupled				
Input Resistance	Single-ended drive, with respect to DECL		100		Ω
	Differential drive		200		Ω
OUTPUT INTERFACE	Pin VOUT				
Available Output Range	R_L ≥ 200 Ω to ground	0.1		4.9	V
Absolute Voltage Range					
Nominal Low End of Range	Measurement mode, f = 900 MHz, P_{IN} = −52 dBm	0.32		0.48	V
Nominal High End of Range	Measurement mode, f = 900 MHz, P_{IN} = +8 dBm	3.44		3.52	V
Source/Sink Current	VOUT held at V_S/2, to 1% change		48		mA
Slew Rate Rising	C_L = open		60		V/µs
Slew Rate Falling	C_L = open		5		V/µs
Rise Time, 10% to 90%	0.2 V to 1.8 V, CLPF = 0		45		ns
Fall Time, 90% to 10%	1.8 V to 0.2 V, CLPF = 0		0.4		µs
Wideband Noise	CLPF = 1000 pF, f_{SPOT} ≤ 100 kHz		70		nV/√Hz
VSET INTERFACE	Pin VSET				
Nominal Input Voltage Range	To ±1 dB error	0.5		3.75	V
Input Resistance			68		kΩ
Scaling (Log Slope)	f = 900 MHz	46	50	54	mV/dB
Scaling (Log Intercept)	f = 900 MHz, into 1:4 balun	−64	−60	−56	dBm
		−77	−73	−69	dBV
VOLTAGE REFERENCE	Pin VREF				
Output Voltage	25°C	1.225	1.25	1.275	V
Temperature Sensitivity	−40°C ≤ T_A ≤ +85°C		0.08		mV/°C
Output Resistance			8		Ω

Parameter	Conditions	Min	Typ	Max	Unit
RMS TARGET INTERFACE	Pin VTGT				
Nominal Input Voltage Range	Measurement range = 60 dB, to ±1 dB error	0.625		2.5	V
Input Bias Current	VTGT = 1.25 V		−28		µA
	VTGT = 0 V		−52		µA
Incremental Input Resistance			52		kΩ
POWER-DOWN INTERFACE	Pin PWDN				
Logic Level to Enable	Logic low enables			1	V
Logic Level to Disable	Logic high disables	3			V
Input Current	Logic high		230		µA
	Logic low		5		µA
Enable Time	From PWDN low to VOUT within 10% of final value, CLPF = 1000 pF		14.5		ns
Disable Time	From PWDN high to VOUT within 10% of final value, CLPF = 1000 pF		2.5		µs
POWER SUPPLY INTERFACE	Pin VPOS				
Supply Voltage		4.5	5	5.5	V
Quiescent Current			20	22	mA
Supply Current	When disabled		0.2		mA
900 MHz					
Dynamic Range	Error referred to best fit line (linear regression)				
	±1.0 dB linearity, CW input		65		dB
	±0.5 dB linearity, CW input		62		dB
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−1.7		dB
	−40°C < T_A < +85°C; P_{IN} = −20 dBm		−1.4		dB
	−40°C < T_A < +85°C; P_{IN} = +5 dBm		−1		dB
Logarithmic Slope		46	50	54	mV/dB
Logarithmic Intercept		−64	−60	−56	dBm
Deviation from CW Response	5.5 dB peak-to-rms ratio (IS95 reverse link)		0.2		dB
	12.0 dB peak-to-rms ratio (WCDMA 4 channels)		0.2		dB
	18.0 dB peak-to-rms ratio (WCDMA 15 channels)		0.5		dB
1.9 GHz					
Dynamic Range	Error referred to best fit line (linear regression)				
	±1 dB linearity, CW input		65		dB
	±0.5 dB linearity, CW input		62		dB
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−0.6		dB
	−40°C < T_A < +85°C; P_{IN} = −20 dBm		−0.5		dB
	−40°C < T_A < +85°C; P_{IN} = +5 dBm		−0.3		dB
Logarithmic Slope			51		mV/dB
Logarithmic Intercept			−59		dBm
Deviation from CW Response	5.5 dB peak-to-rms ratio (IS95 reverse link)		0.2		dB
	12.0 dB peak-to-rms ratio (WCDMA 4 channels)		0.2		dB
	18.0 dB peak-to-rms ratio (WCDMA 15 channels)		0.5		dB

Parameter	Conditions	Min	Typ	Max	Unit
2.2 GHz					
Dynamic Range	Error referred to best fit line (linear regression)				
	±1.0 dB linearity, CW input		65		dB
	±0.5 dB linearity, CW input		65		dB
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−1.8		dB
	−40°C < T_A < +85°C; P_{IN} = −20 dBm		−1.6		dB
	−40°C < T_A < +85°C; P_{IN} = +5 dBm		−1.3		dB
Logarithmic Slope			50.5		mV/dB
Logarithmic Intercept			−61		dBm
Deviation from CW Response	5.5 dB peak-to-rms ratio (IS95 reverse link)		0.2		dB
	12.0 dB peak-to-rms ratio (WCDMA 4 channels)		0.2		dB
	18.0 dB peak-to-rms ratio (WCDMA 15 channels)		0.5		dB
2.7 GHz					
Dynamic Range	Error referred to best fit line (linear regression)				
	±1.0 dB linearity, CW input		63		dB
	±0.5 dB linearity, CW input		62		dB
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = −40 dBm		−5.3		dB
	−40°C < T_A < +85°C; P_{IN} = −15 dBm		−5.5		dB
	−40°C < T_A < +85°C; P_{IN} = +15 dBm		−4.8		dB
Logarithmic Slope			50.5		mV/dB
Logarithmic Intercept			−58		dBm
Deviation from CW Response	5.5 dB peak-to-rms ratio (IS95 reverse link)		0.2		dB
	12.0 dB peak-to-rms ratio (WCDMA 4 channels)		0.2		dB
	18.0 dB peak-to-rms ratio (WCDMA 15 channels)		0.4		dB

[1] 1:4 balun transformer, M/A-COM ETC 1.6-4-2-3.
[2] See Figure 43.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameters	Ratings
Supply Voltage VPOS	5.5 V
Input Power (Into Input of Device)	13 dBm
Equivalent Voltage	2 V rms
Internal Power Dissipation	500 mW
θ_{JA}	125°C/W
Maximum Junction Temperature	125°C/W
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

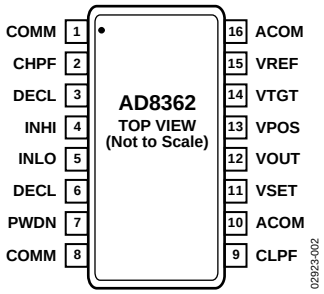


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description	Equivalent Circuit
1, 8	COMM	Common Connection. Connect via low impedance to system common.	
2	CHPF	Input HPF. Connect to common via a capacitor to determine 3 dB point of input signal high-pass filter.	
3, 6	DECL	Decoupling Terminals for INHI and INLO. Connect to common via a large capacitance to complete input circuit.	
4, 5	INHI , INLO	Differential Signal Input Terminals. Input Impedance = 200 Ω. Can also be driven single-ended, in which case the input impedance reduces to 100 Ω.	Circuit A
7	PWDN	Disable/Enable Control Input. Apply logic high voltage to shut down the AD8362.	
9	CLPF	Connection for Ground Referenced Loop Filter Integration (Averaging) Capacitor.	
10, 16	ACOM	Analog Common Connection for Output Amplifier.	
11	VSET	Setpoint Input. Connect directly to VOUT for measurement mode. Apply setpoint input to this pin for controller mode.	Circuit B
12	VOUT	RMS Output. In measurement mode, VOUT is normally connected directly to VSET.	Circuit C
13	VPOS	Connect to 5 V Power Supply.	
14	VTGT	The Logarithmic Intercept Voltage is Proportional to the Voltage Applied to this Pin. The use of a lower target voltage increases the crest factor capacity. Normally connected to VREF.	Circuit D
15	VREF	General Purpose Reference Voltage Output of 1.25 V. Usually connected only to VTGT.	Circuit E

EQUIVALENT CIRCUITS

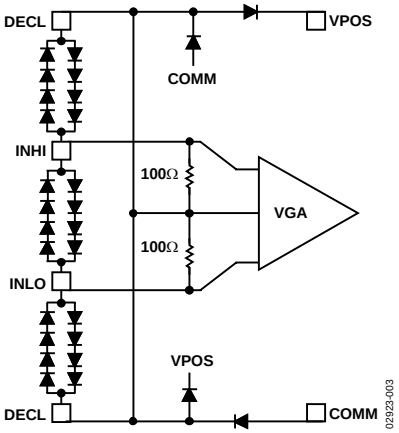


Figure 3. Circuit A

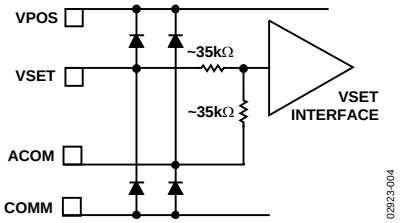


Figure 4. Circuit B

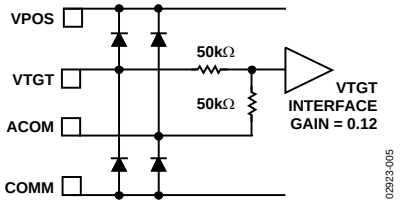


Figure 5. Circuit C

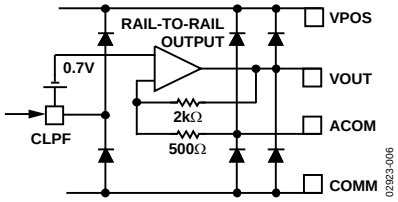


Figure 6. Circuit D

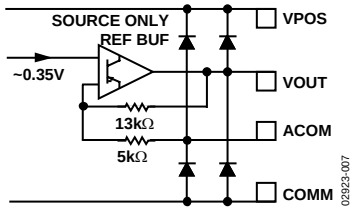


Figure 7. Circuit E

TYPICAL PERFORMANCE CHARACTERISTICS

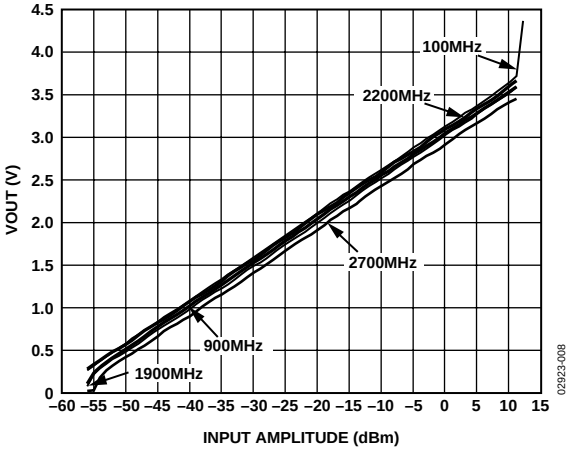


Figure 8. Output Voltage (VOUT) vs. Input Amplitude (dBm), Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, 2700 MHz, Sine Wave, Differential Drive

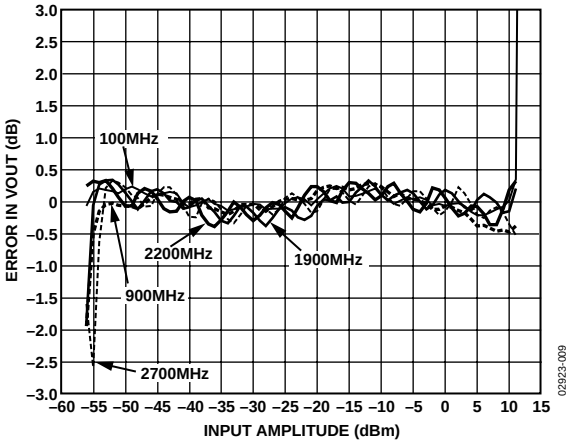


Figure 9. Logarithmic Law Conformance vs. Input Amplitude Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, 2700 MHz, Sine Wave, Differential Drive

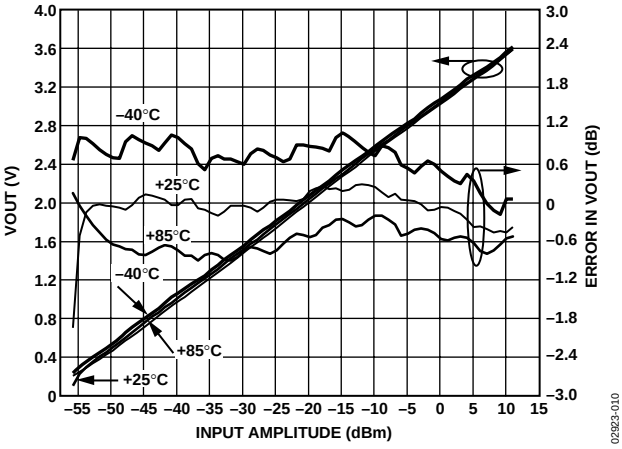


Figure 10. VOUT and Law Conformance vs. Input Amplitude, Frequency 900 MHz, Sine Wave, Temperature −40°C, +25°C, and +85°C

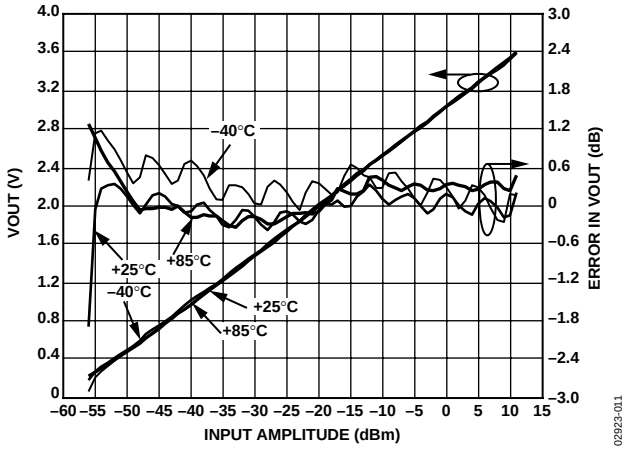


Figure 11. VOUT and Law Conformance vs. Input Amplitude, Frequency 1900 MHz, Sine Wave, Temperature −40°C, +25°C, and +85°C

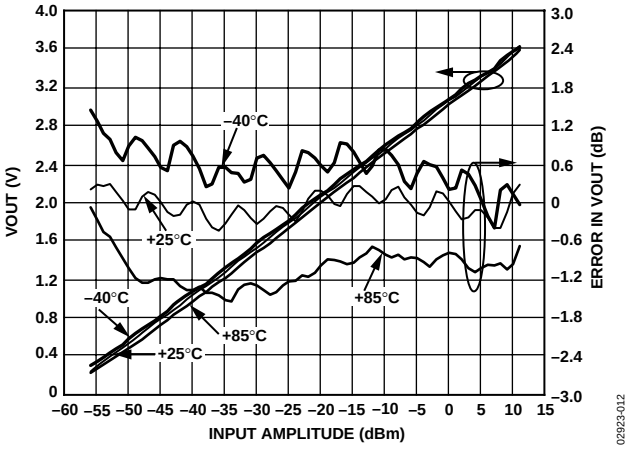


Figure 12. VOUT and Law Conformance vs. Input Amplitude, Frequency 2200 MHz, Sine Wave, Temperature −40°C, +25°C, and +85°C

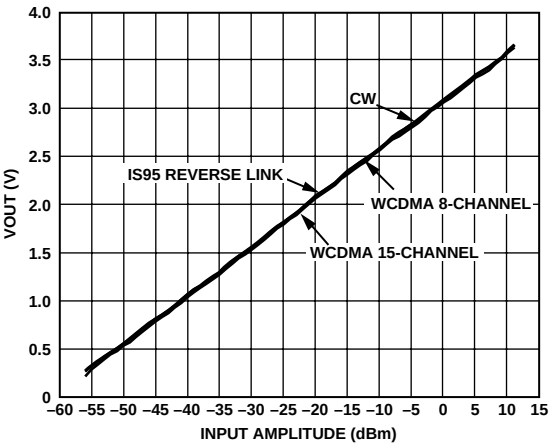


Figure 13. VOUT vs. Input Amplitude with Different Waveforms, CW, IS95 Reverse Link, WCDMA 8-Channel, WCDM 15-Channel, Frequency 900 MHz

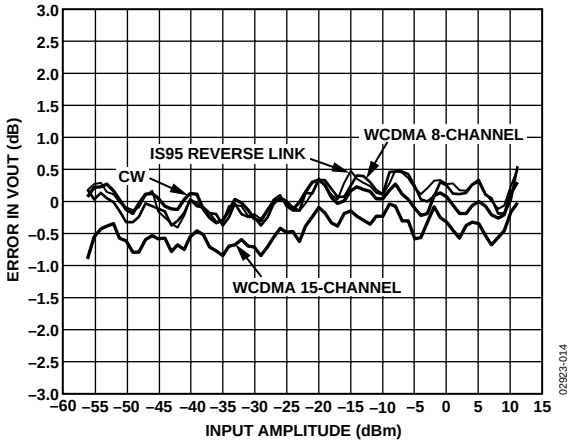


Figure 14. Output Error from CW Linear Reference vs. Input Amplitude with Different Waveforms, CW, IS95 Reverse Link, WCDMA 8-Channel, WCDMA 15-Channel, Frequency 900 MHz, V_{TGT} = 1.25 V

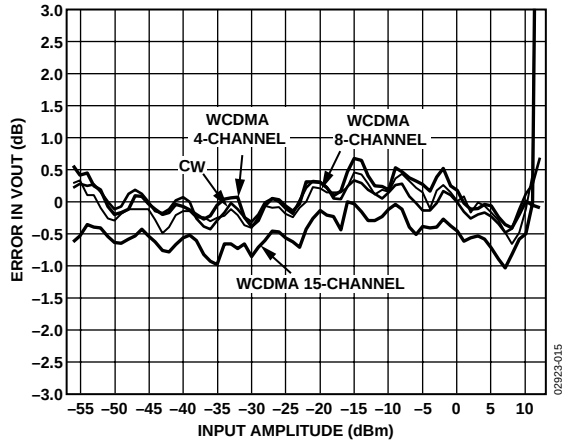


Figure 15. Output Error from CW Linear Reference vs. Input Amplitude with Different WCDMA Channel Loading, 4-Channel, 8-Channel, 15-Channel, Frequency 2200 MHz, V_{TGT} = 1.25 V

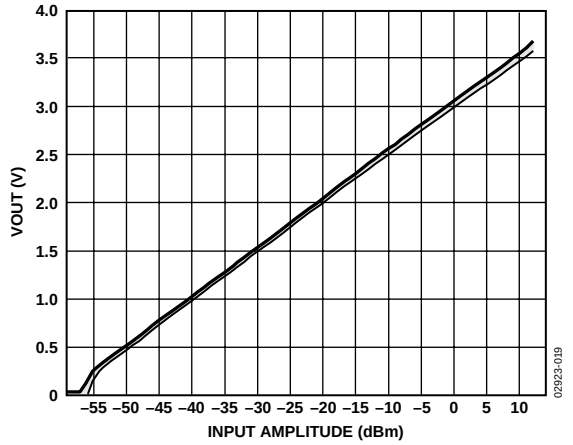


Figure 16. VOUT vs. Input Amplitude, 3 Sigma to Either Side of Mean, Sine Wave, Frequency 900 MHz, Part-to-Part Variation

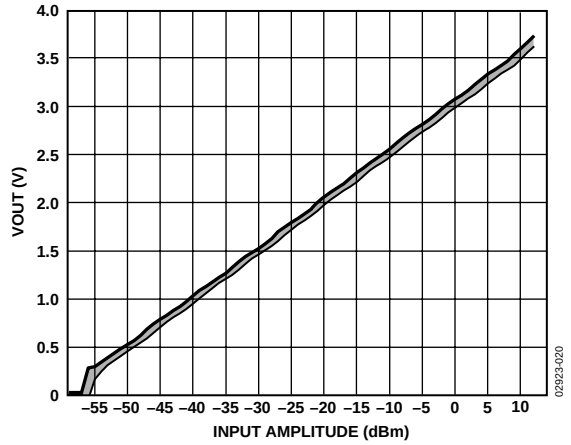


Figure 17. VOUT vs. Input Amplitude, 3 Sigma to Either Side of Mean, Sine Wave, Frequency 1900 MHz, Part-to-Part Variation

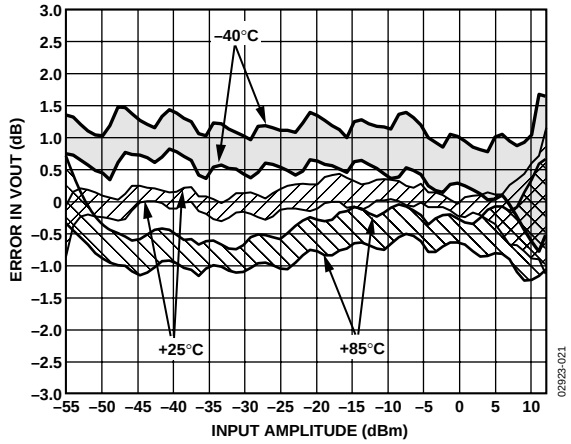


Figure 18. Logarithmic Law Conformance vs. Input Amplitude, 3 Sigma to Either Side of Mean, Sine Wave, Frequency 900 MHz, Temperature –40°C, +25°C, and +85°C

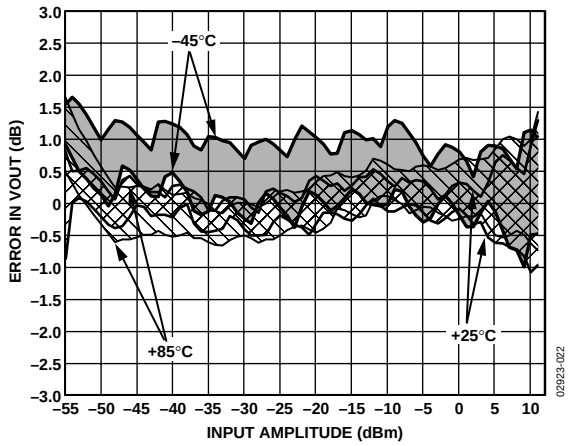


Figure 19. Logarithmic Law Conformance vs. Input Amplitude, 3 Sigma to Either Side of Mean, Sine Wave, Frequency 1900 MHz, Temperature –40°C, +25°C, and +85°C

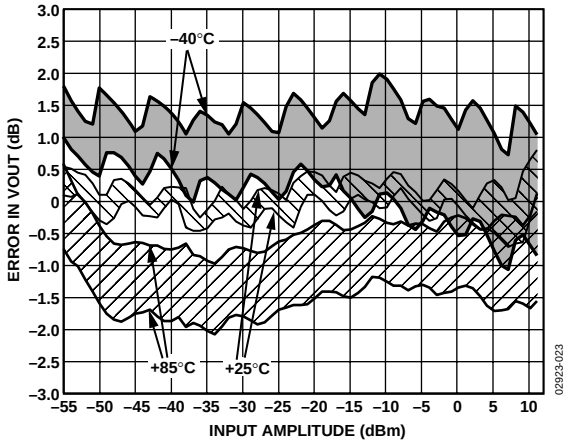


Figure 20. Logarithmic Law Conformance vs. Input Amplitude, 3 Sigma to Either Side of Mean, Sine Wave, Frequency 2200 MHz, Temperature –40°C, +25°C, and +85°C

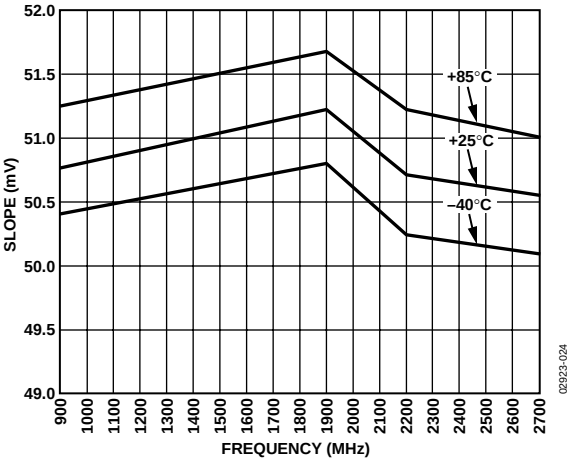


Figure 21. Logarithmic Slope vs. Frequency, Temperature –40°C, +25°C, and +85°C

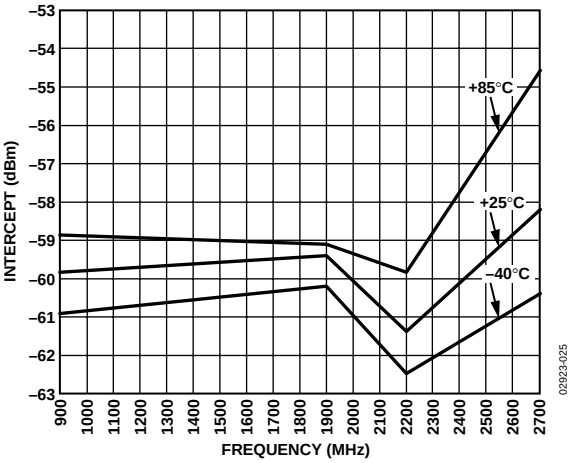


Figure 22. Logarithmic Intercept vs. Frequency, Temperature –40°C, +25°C, and +85°C

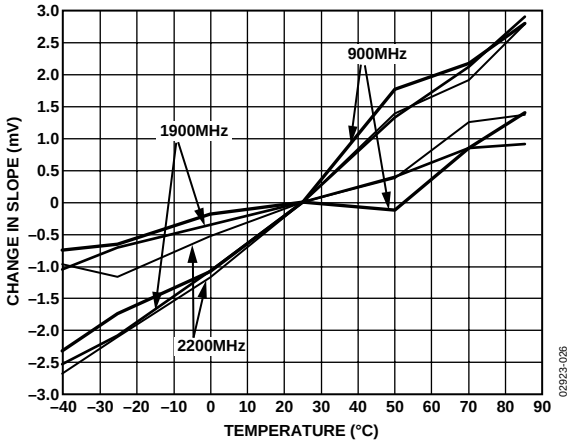


Figure 23. Change in Logarithmic Slope vs. Temperature, 3 Sigma to Either Side of Mean, Frequencies 900 MHz, 1900 MHz, 2200 MHz

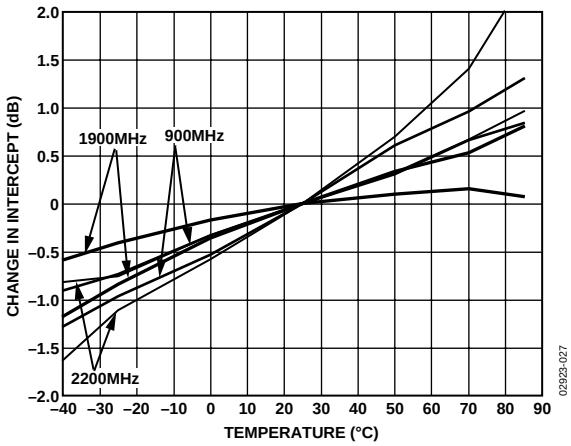


Figure 24. Change in Logarithmic Intercept vs. Temperature, 3 Sigma to Either Side of Mean, Frequencies 900 MHz, 1900 MHz, 2200 MHz

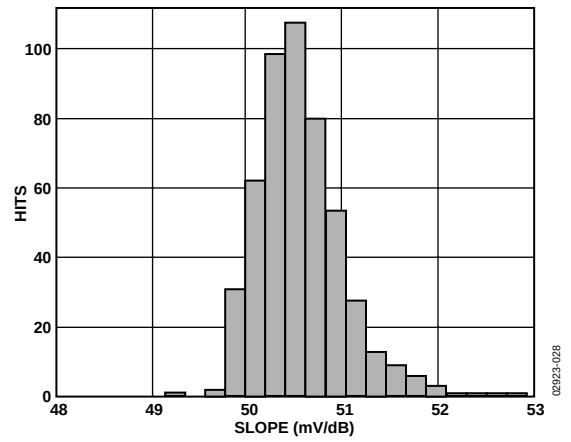


Figure 25. Slope Distribution, Frequency 900 MHz

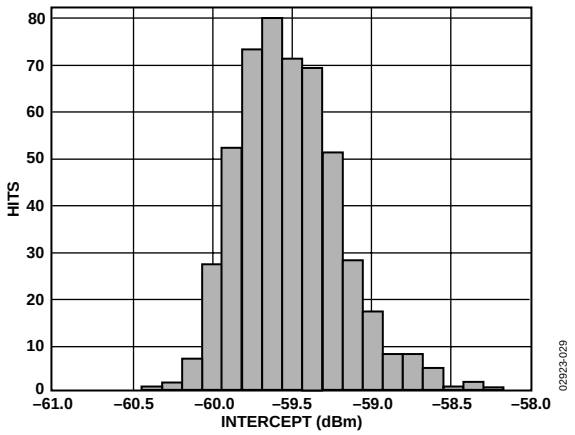


Figure 26. Logarithmic Intercept Distribution, Frequency 900 MHz

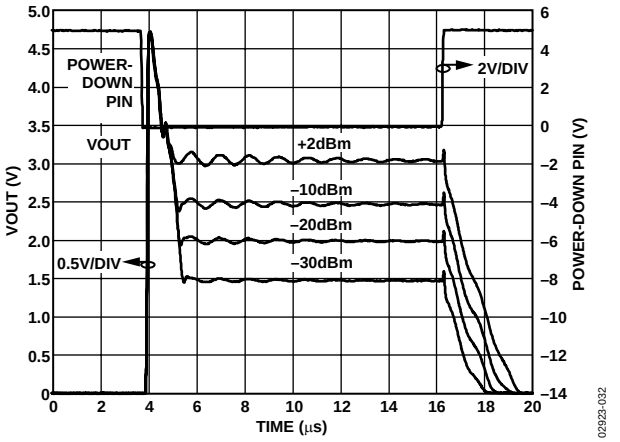


Figure 29. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency 900 MHz, CLPF = 0

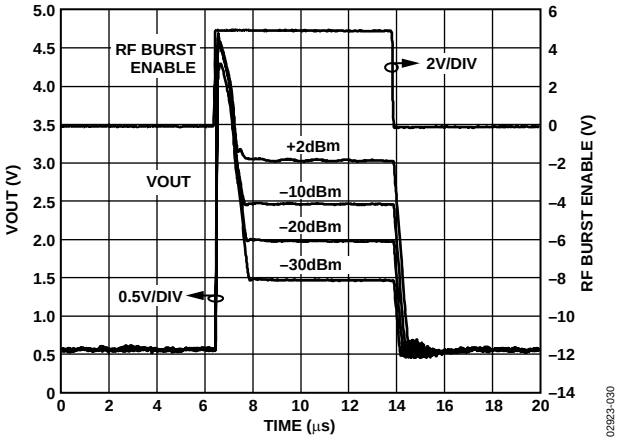


Figure 27. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency 900 MHz, CLPF = Open

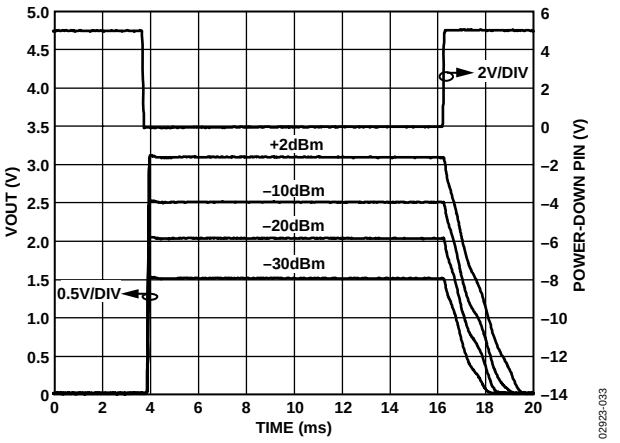


Figure 30. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency 900 MHz, CLPF = 0.1 µF

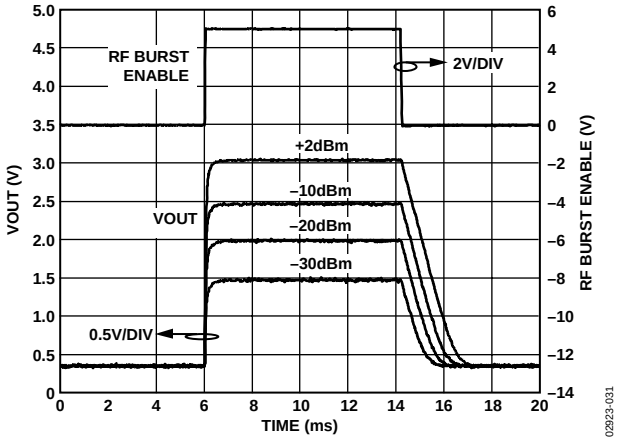


Figure 28. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency 900 MHz, CLPF = 0.1 µF

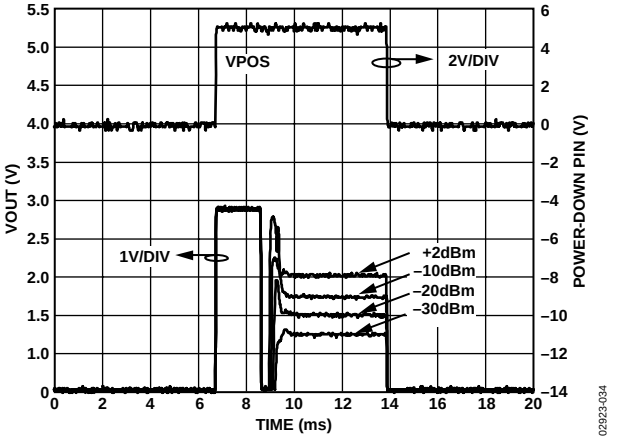


Figure 31. Output Response to Gating on Power Supply for Various RF Input Levels, Carrier Frequency 900 MHz, CLPF = 0

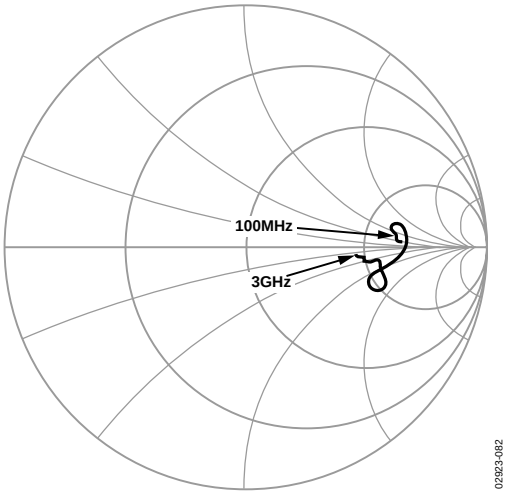


Figure 32. INHI, INLO Differential Input Impedance, 100 MHz to 3 GHz

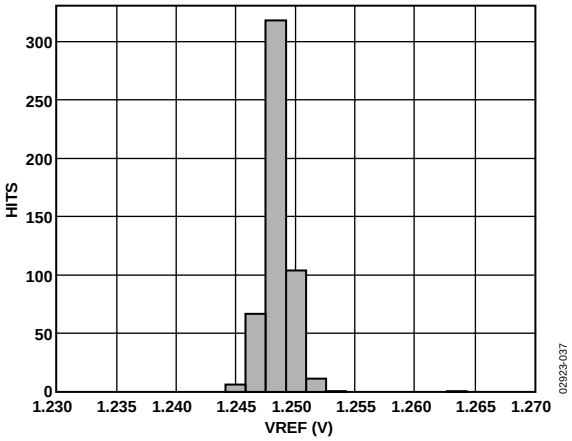


Figure 34. VREF Distribution

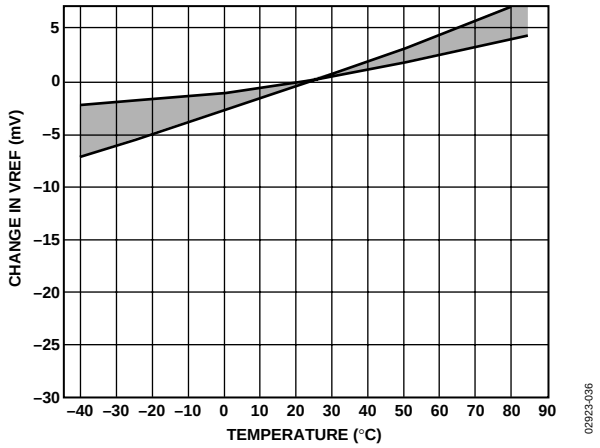


Figure 33. Change in VREF vs. Temperature, 3 Sigma to Either Side of Mean

CHARACTERIZATION SETUP

EQUIPMENT

The general hardware configuration used for most of the AD8362 characterization is shown in Figure 35. The signal source is a Rohde & Schwarz SMIQ03B. A 1:4 balun transformer is used to transform the single-ended RF signal to differential form. For the response measurements in Figure 27 and Figure 28, the configuration shown in Figure 36 is used. For Figure 29 and Figure 30, the configuration shown in Figure 37 is used. For Figure 31, the configuration shown in Figure 38 is used.

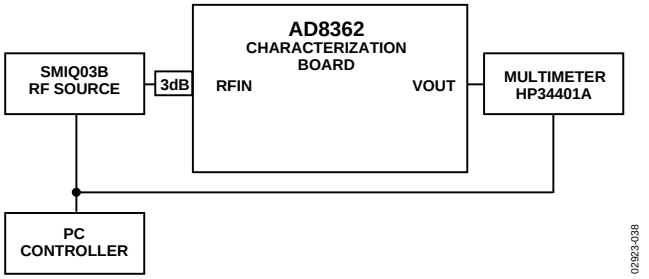


Figure 35. Primary Characterization Setup

ANALYSIS

The slope and intercept are derived using the coefficients of a linear regression performed on data collected in its central operating range. Error is stated in two forms: error from linear response to CW waveform, and output delta from 25°C performance.

The error from linear response to CW waveform is the decibel difference in output from the ideal output defined by the conversion gain and output reference. This is a measure of the linearity of the device response to both CW and modulated waveforms. The error in dB is calculated by

$$Error\,(\mathrm{dB}) = \frac{VOUT - Slope \times (P_{IN} - P_Z)}{Slope}$$

where P_Z is the x intercept, expressed in dBm.

Error from the linear response to CW waveform is not a measure of absolute accuracy since it is calculated using the slope and intercept of each device. However, it verifies the linearity and the effect of modulation on the device response. Error from 25°C performance uses the performance of a given device and waveform type as the reference; it is predominantly a measurement of output variation with temperature.

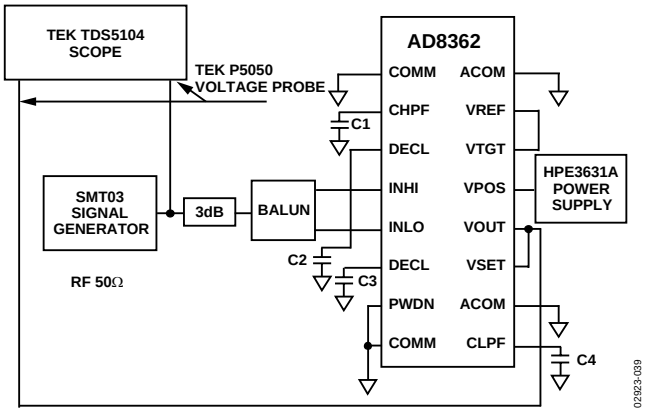


Figure 36. Response Measurement Setup for Modulated Pulse

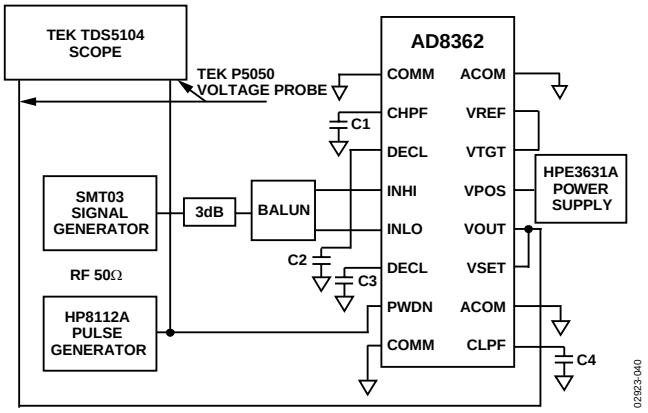


Figure 37. Response Measurement Setup for Power-Down Step

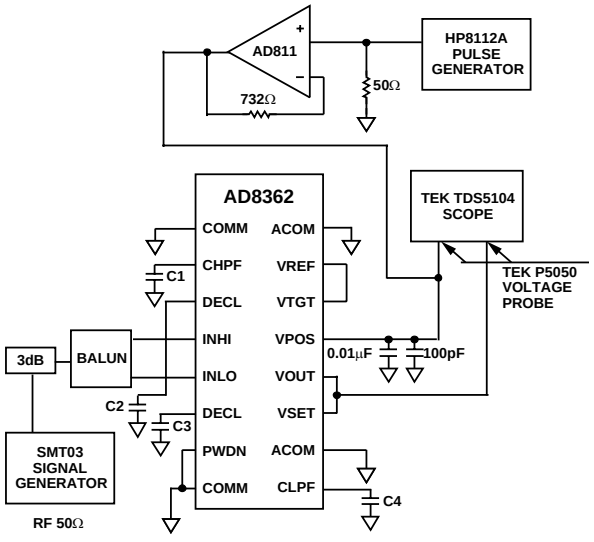


Figure 38. Response Measurement Setup for Gated Supply

CIRCUIT DESCRIPTION

The AD8362 is a fully calibrated, high accuracy, rms-to-dc converter providing a measurement range of over 60 dB. It is capable of operating from signals as low in frequency as a few hertz to at least 2.7 GHz. Unlike earlier rms-to-dc converters, the response bandwidth is completely independent of the signal magnitude. The −3 dB point occurs at about 3.5 GHz. The capacity of this part to accurately measure waveforms having a high peak-to-rms ratio (crest factor) is independent of either the signal frequency or its absolute magnitude, over a wide range of conditions.

This unique combination allows the AD8362 to be used as a calibrated RF wattmeter covering a power ratio of >1,000,000:1, a power controller in closed-loop systems, a general-purpose rms-responding voltmeter, and in many other low frequency applications.

The part comprises the core elements of a high performance AGC loop (Figure 39), laser-trimmed during manufacture to close tolerances while fully operational at a test frequency of 100 MHz. Its linear, wideband, variable gain amplifier (VGA) provides a general voltage gain, G_{SET}; this may be controlled in a precisely exponential (linear-in-dB) manner over the full 68 dB range from −25 dB to +43 dB by a voltage V_{SET}. However, to provide adequate guard-banding, only the central 60 dB of this range, from −21 dB to +39 dB, is normally used. The Adjusting VTGT to Accommodate Signals with Very High Crest Factors section shows how this basic range may be shifted up or down.

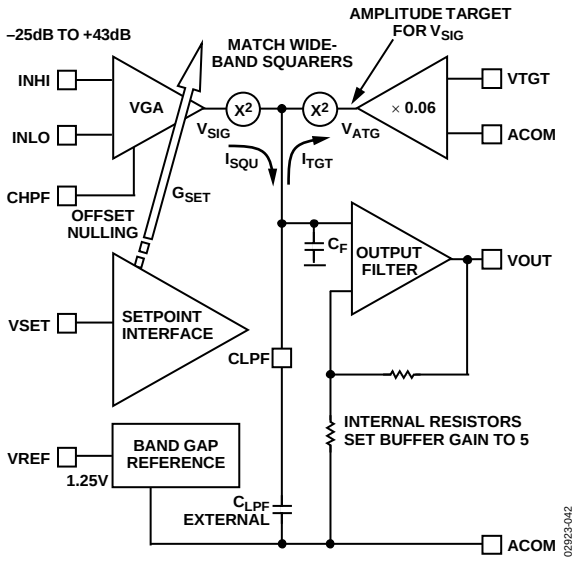


Figure 39. Basic Structure of the AD8362

The VGA gain has the form

$$G_{SET} = G_O \exp(-VSET/V_{GNS}) \quad (1)$$

where G_O is a basic fixed gain and V_{GNS} is a scaling voltage that defines the gain slope (the dB change per volt). Note that the gain decreases with V_{SET}.

The VGA output is

$$V_{SIG} = G_{SET}V_{IN} = G_OV_{IN} \exp(VSET/V_{GNS}) \quad (2)$$

where V_{IN} is the ac voltage applied to the input terminals of the AD8362.

As is explained more fully in the Recommended Input Coupling section, the input drive may either be single-sided or differential, although dynamic range is maximized with a differential input drive. The effect of high frequency imbalances when using a single-sided drive is less apparent at low frequencies (from 50 Hz to 500 MHz), but the peak input voltage capacity is always halved relative to differential operation.

SQUARE LAW DETECTION

The output of the variable-gain amplifier (V_{SIG}) is applied to a wideband square law detector, which provides a true rms response to this alternating signal that is essentially independent of waveform. Its output is a fluctuating current (I_{SQU}) that has a positive mean value. This current is integrated by an on-chip capacitance (C_F), which is usually augmented by an external capacitance (CLPF) to extend the averaging time. The resulting voltage is buffered by a gain-of-5, dc-coupled amplifier whose rail-to-rail output (VOUT) may be used for either measurement or control purposes.

In most applications, the AGC loop is closed via the setpoint interface pin, VSET, to which the VGA gain-control voltage on VOUT is applied. In measurement modes, the closure is direct and local by a simple connection from the output of the VOUT pin to the VSET pin. In controller modes, the feedback path is around some larger system, but the operation is the same.

The fluctuating current (I_{SQU}) is balanced against a fixed setpoint target current (I_{TGT}) using current mode subtraction. With the exact integration provided by the capacitor(s), the AGC loop equilibrates when

$$\text{MEAN}(I_{SQU}) = I_{TGT} \quad (3)$$

The current I_{TGT} is provided by a second-reference squaring cell whose input is the amplitude-target voltage V_{ATG}. This is a fraction of the voltage VTGT applied to a special interface that accepts this input at the VTGT pin. Since the two squaring cells are electrically identical and are carefully implemented in the IC, process and temperature-dependent variations in the detailed behavior of the two square-law functions cancel.

Accordingly, VTGT (and its fractional part V_{ATG}) determines the output that must be provided by the VGA for the AGC loop to settle. Since the scaling parameters of the two squarers are accurately matched, it follows that Equation 3 is satisfied only when

$$\text{MEAN}(V_{SIG}^2) = V_{ATG}^2 \quad (4)$$

In a formal solution, extract the square root of both sides to provide an explicit value for the root-mean-square (rms) value. However, it is apparent that by forcing this identity through varying the VGA gain and extracting the mean value by the filter provided by the capacitor(s), the system inherently establishes the relationship

$$\text{rms}(V_{SIG}) = V_{ATG} \quad (5)$$

Substituting the value of V_{SIG} from Equation 2,

$$\text{rms}[G_O V_{IN} \exp(-VSET/V_{GNS})] = V_{ATG} \quad (6)$$

As a measurement device, V_{IN} is the unknown quantity and all other parameters can be fixed by design. To solve Equation 6,

$$\text{rms}[G_O V_{IN}/V_{ATG}] = \exp(VSET/V_{GNS}) \quad (7)$$

so

$$VSET = V_{GNS} \log[\text{rms}(V_{IN})/V_Z] \quad (8)$$

The quantity $V_Z = V_{ATG}/G_O$ is defined as the intercept voltage because *VSET* must be 0 when rms (V_{IN}) = V_Z.

When connected as a measurement device, the output of the buffer is tied directly to VSET, which closes the AGC loop. Making the substitution *VOUT* = *VSET* and changing the log base to 10, as needed in a decibel conversion,

$$VOUT = V_{SLP} \log_{10}[\text{rms}(V_{IN})/V_Z] \quad (9)$$

where V_{SLP} is the slope voltage, that is, the change in output voltage for each decade of change in the input amplitude. Note that $V_{SLP} = V_{GNS} \log(10) = 2.303\ V_{GNS}$.

In the AD8362, V_{SLP} is laser trimmed to 1 V using a 100 MHz test signal. Because a decade corresponds to 20 dB, this slope may also be stated as 50 mV/dB. It is shown in the Altering the Slope section how the effective value of V_{SLP} may be altered by the user. The intercept V_Z is also laser trimmed to 224 µV (−60 dBm relative to 50Ω). In an ideal system, VOUT would cross zero for an rms input of that value. In a single-supply realization of the function, VOUT cannot run fully down to ground; here, V_Z is the extrapolated value.

VOLTAGE VS. POWER CALIBRATION

The AD8362 can be used as an accurate rms voltmeter from arbitrarily low frequencies to microwave frequencies. For low frequency operation, the input is usually specified either in volts rms or in dBV (decibels relative to 1 V rms).

At high frequencies, signal levels are commonly specified in power terms. In these circumstances, the source and termination impedances are an essential part of the overall scaling. For this condition, the output voltage can be expressed as

$$VOUT = SLOPE \times (P_{IN} - P_Z) \quad (10)$$

where P_{IN} and the intercept P_Z are expressed in dBm.

In practice, the response deviates slightly from the ideal straight line suggested by Equation 10. This deviation is called the law conformance error. In defining the performance of high accuracy measurement devices, it is customary to provide plots of this error. In general terms, it is computed by extracting the best straight line to the measured data using linear regression over a substantial region of the dynamic range and under clearly specified conditions.

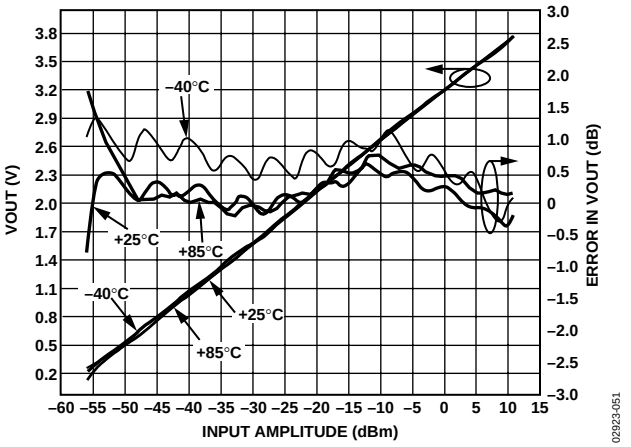


Figure 40. Output Voltage and Law Conformance Error @ T_A = −40°C, +25°C, and +85°C

Figure 40 shows the output of the circuit of Figure 42 over the full input range. The agreement with the ideal function (law conformance) is also shown. This was determined by linear regression on the data points over the central portion of the transfer function for the +25°C data.

The error at −40°C, +25°C, and +85°C was then calculated by subtracting the ideal output voltage at each input signal level from the actual output, and dividing this quantity by the mean slope of the regression equation to provide a measurement of the error in decibels (scaled on the right-hand axis of Figure 40).

The error curves generated in this way reveal not only the deviations from the ideal transfer function at a nominal temperature, but also all of the additional errors caused by temperature changes. Notice that there is a small temperature dependence in the intercept (the vertical position of the error plots).

Figure 40 further reveals a periodic ripple in the conformance curves. This is due to the interpolation technique used to select the signals from the attenuator, not only at discrete tap points, but anywhere in between; thus providing continuous attenuation values. The selected signal is then applied to the 3.5 GHz, 40 dB fixed gain amplifier in the remaining stages of the VGA of the AD8362.

An approximate schematic of the signal input section of the AD8362 is shown in Figure 41. The ladder attenuator is composed of 11 sections (12 taps), each of which progressively attenuates the input signal by 6.33 dB. Each tap is connected to a variable transconductance cell whose bias current determines the signal weighting given to that tap. The interpolator determines which stages are active by generating a discrete set of bias currents, each having a Gaussian profile. These are arranged to move from left to right, thereby determining the attenuation applied to the input signal as the gain is progressively lowered over the 69.3 dB range under control of the VSET input. The detailed manner in which the transconductance of adjacent stages varies as the virtual tap point slides along the attenuator accounts for the ripple observed in the conformance curves. Its magnitude is slightly temperature dependent and also varies with frequency (see Figure 10, Figure 11 and Figure 12). Notice that the system's responses to signal inputs at INHI and INLO are not completely independent; these pins do not constitute a fully floating differential input.

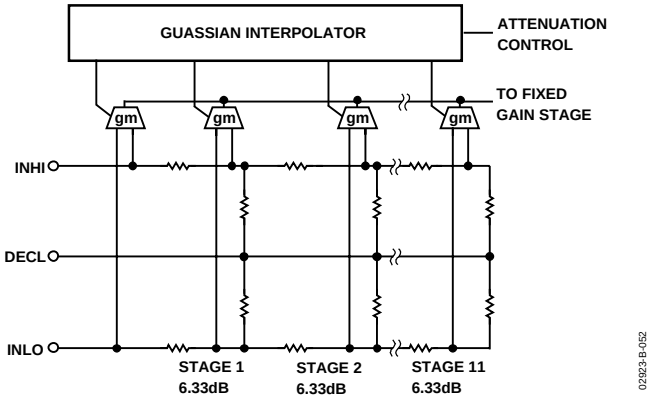


Figure 41. Simplified Input Circuit

OFFSET ELIMINATION

To address the small dc offsets that arise in the variable gain amplifier, an offset-nulling loop is used. The high-pass corner frequency of this loop is internally preset to 1 MHz, sufficiently low for most high frequency applications. When using the AD8362 in low frequency applications, the corner frequency can be reduced as needed by the addition of a capacitor from the CHPF pin to ground having a nominal value of 200 μF/Hz. For example, to lower the high-pass corner frequency to 150 Hz, a capacitance of 1.33 μF is required. The offset voltage varies depending on the actual gain at which the VGA is operating, and thus on the input signal amplitude.

Baseline variations of this sort are a common aspect of all VGAs, but they are more evident in the AD8362 because of the method of its implementation, which causes the offsets to ripple along the gain axis with a period of 6.33 dB. When an excessively large value of CHPF is used, the offset correction process may lag the more rapid changes in the VGA's gain, which may increase the time required for the loop to fully settle for a given steady input amplitude.

TIME-DOMAIN RESPONSE OF THE CLOSED LOOP

The external low-pass averaging capacitance (CLPF) added at the output of the squaring cell is chosen to provide adequate filtering of the fluctuating detected signal. The optimum value depends on the application; as a guideline, a value of roughly 900 μF/Hz should be used. For example, a capacitance of 5 μF provides adequate filtering down to 180 Hz. Note that the fluctuation in the quasi-dc output of a squaring cell operating on a sine wave input is a raised cosine at twice the signal frequency, easing this filtering function.

In the standard connections for the measurement mode, the VSET pin is tied to VOUT. For small changes in input amplitude (a few decibels), the time-domain response of this loop is essentially linear, with a 3 dB low-pass corner frequency of nominally $f_{LP} = 1/(CLPF \times 1.1\ k\Omega)$. Internal time delays around this local loop set the minimum recommended value of this capacitor to about 300 pF, giving $f_{LP} = 3$ MHz.

When large and abrupt changes of input amplitude occur, the loop response becomes nonlinear and exhibits slew rate limitations.

OPERATION IN RF MEASUREMENT MODE

BASIC CONNECTIONS

Basic connections for operating the AD8362 in measurement mode are shown in Figure 42. While the AD8362 requires a single supply of nominally 5 V, its performance is essentially unaffected by variations of up to ±10%.

The supply is connected to the VPOS pin using the decoupling network also displayed in Figure 42. The capacitors used in this network must provide a low impedance over the full frequency range of the input, and should be placed as close as possible to the VPOS pin. Two different capacitors are used in parallel to reduce the overall impedance since these have different resonant frequencies. The measurement accuracy is not critically dependent on supply decoupling, however, because the high frequency signal path is confined to the relevant input pins. Lead lengths from both DECL pins to ground and from INHI/INLO to the input coupling capacitors should be as short as possible. All COMM pins should also connect directly to the ground plane.

To place the device in measurement mode, connect VOUT to VSET, and connect VTGT directly to VREF.

DEVICE DISABLE

The AD8362 is disabled by a logic high on the PWDN pin, which may be directly grounded for continuous operation. When enabled, the supply current is nominally 20 mA and essentially independent of supply voltage and input signal strength. When powered down by a logic low on PWDN, the supply current is reduced to 230 μA.

RECOMMENDED INPUT COUPLING

The full dynamic range of the AD8362, particularly at very high frequencies (above 500 MHz), is realized only when the input is presented to it in differential (balanced) form. In Figure 42, a transmission line balun is used at the input. Having a 1:4 impedance ratio (1:2 turns ratio), the 200 Ω differential input resistance of the AD8362 becomes 50 Ω at the input to the balun.

The balun outputs must be ac-coupled to the input of the AD8362. The balun used in this example (M/A-COM ETC 1.6-4-2-3) is also used in the AD8362 evaluation board and is specified for operation from 0.5 GHz to 2.5 GHz.

If a center-tapped flux-coupled transformer is used, connect the center tap to the DECL pins, which are biased to the same potential as the inputs (~3.6 V).

At lower frequencies where impedance matching is not necessary, the AD8362 can be driven from a low impedance differential source, remembering the inputs must be ac-coupled.

Choosing Input Coupling Capacitors

As noted, the inputs must be ac-coupled. The input coupling capacitors combine with the 200 Ω input impedance to create an input high pass corner frequency equal to

$$F_{HP} = 1/(200 \times \pi \times C_C)$$

Typically, F_{HP} should be set to at least one tenth the lowest input frequency of interest.

Single-Ended Input Drive

As already noted, the input stages of the AD8362 are optimally driven from a fully balanced source, which should be provided wherever possible. In many cases, unbalanced sources can be applied directly to one or the other of the two input pins. The chief disadvantage of this driving method is a 10 dB to 15 dB reduction in dynamic range at frequencies above 500 MHz.

Figure 43 illustrates one of many ways of coupling the signal source to the AD8362. Because the input pins are biased to about 3.6 V (for V_S = 5 V), dc-blocking capacitors are required when driving from a grounded source. For signal frequencies >5 MHz, a value of 1 nF is adequate. While either INHI or INLO may be used, INHI is chosen here.

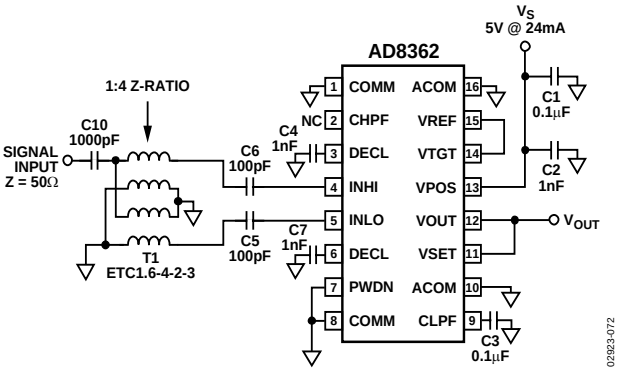


Figure 42. Basic Connections for RF Power Measurement

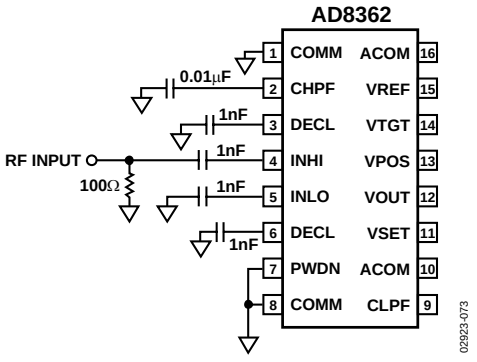


Figure 43. Input Coupling from a Single-Ended 50 Ω Source

An external 100 Ω shunt resistor combines with the internal 100 Ω single-ended input impedance to provide a broadband 50 Ω match. The unused input (in this case, INLO) is ac-coupled to ground. Figure 44 shows the transfer function of the AD8362 at various frequencies when driven single-ended. The results show that transfer function linearity at the top end of the range is degraded by the single-ended drive.

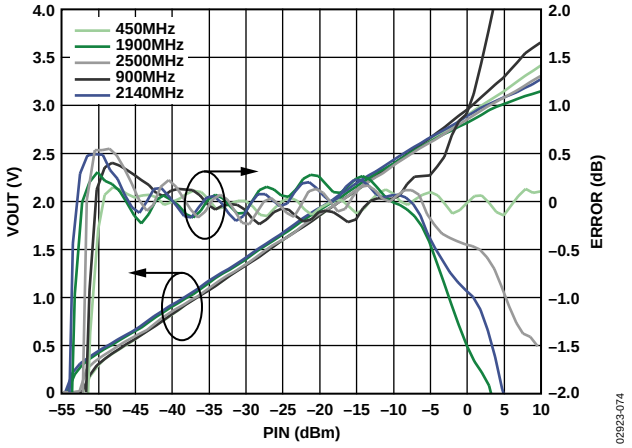


Figure 44. Transfer Function at Various Frequencies when RF Input is Driven Single-Ended.

OPERATION AT LOW FREQUENCIES

In conventional rms-to-dc converters based on junction techniques, the effective signal bandwidth is proportional to the signal amplitude. In contrast, the 3.5 GHz VGA bandwidth in the AD8362 is independent of its gain. Because this amplifier is internally dc-coupled, the system is also used as a high accuracy rms voltmeter at low frequencies, retaining its temperature-stable decibel-scaled output; for example, in seismic, audio, and sonar instrumentation.

While the AD8362 can be operated at arbitrarily low frequencies, an ac-coupled input interface must be maintained. In such cases, the input coupling capacitors should be large enough so that the lowest frequency components of the signal to be included in the measurement are minimally attenuated. For example, for a 3 dB reduction at 1.5 kHz, capacitances of 1 µF are needed because the input resistance is 100 Ω at each input pin (200 Ω differentially), and the calculation is $1/(2\pi \times 1.5\ k\Omega \times 100) = 1\ \mu F$. In addition, to lower the high-pass corner frequency of the VGA, a large capacitor must be connected between the CHPF pin and ground (see the Choosing a Value for CHPF section).

More information on operation of the AD8362 and other RF power detectors at low frequency is available in Application Note AN-691: Operation of RF Detector Products at Low Frequency.

CHOOSING A VALUE FOR CHPF

The 3.5 GHz variable gain amplifier of the AD8362 includes an offset cancellation loop, which introduces a high-pass filter effect in its transfer function. To properly measure the amplitude of the input signal, the corner frequency (f_{HP}) of this filter must be well below that of the lowest input signal in the desired measurement bandwidth frequency. The required value of the external capacitor is given by

$$CHPF = 200\ \mu F/f_{HP}\ (f_{HP}\ in\ \text{Hz}) \quad (12)$$

For operation at frequencies as low as 100 kHz, set f_{HP} to approximately 25 kHz (CHPF = 8 nF). For frequencies above approximately 2 MHz, no external capacitance is required because there is adequate internal capacitance on this node.

CHOOSING A VALUE FOR CLPF

In the standard connections for the measurement mode, the VSET pin is tied to VOUT. For small changes in input amplitude such as a few decibels, the time-domain response of this loop is essentially linear with a 3 dB low-pass corner frequency of nominally $f_{LP} = 1/(CLPF \times 1.1\ k\Omega)$. Internal time delays around this local loop set the minimum recommended value of this capacitor to about 300 pF, making $f_{LP} = 3$ MHz.

For operation at lower signal frequencies, or whenever the averaging time needs to be longer, use

$$CLPF = 900\ \mu F/f_{LP}\ (f_{LP}\ in\ \text{Hz}) \quad (13)$$

When the input signal exhibits large crest factors, such as a CDMA or WCDMA signal, CLPF must be much larger than might seem necessary. This is due to the presence of significant low frequency components in the complex, pseudo-random modulation, which generates fluctuations in the AD8362's output. Increasing CLPF will also increase the step response of the AD8362 to a change at its input.

Table 4 shows recommended values of CLPF for popular modulation schemes. In each case, CLPF is increased until residual output noise falls below 50 mV. A 10% to 90% step response to an input step is also listed. Where the increased response time is unacceptably high, CLPF must be reduced. If the output of the AD8362 is sampled by an ADC, averaging in the digital domain can further reduce the residual noise.

Table 4. Recommended CLPF Values for Various Modulation Schemes

Modulation Scheme/Standard	Crest Factor	CLPF	Residual Ripple	Response Time (Rise/Fall) 10% to 90%
WCDMA, Single-Carrier, Test Model 1-64	12.0 dB	0.1 µF	28 mVpp	171 µs/1.57 ms
WCDMA 4-Carrier, Test Model 1-64	11.0 dB	0.1 µF	20 mVpp	162 µs/1.55 ms
CDMA2000, Single-Carrier, 9CH Test Model	9.1 dB	0.1 µF	38 mVpp	179 µs /1.55 ms
CDMA2000, 3-Carrier, 9CH Test Model	11.0 dB	0.1 µF	29 mVpp	171 µs/1.55 ms
WiMax 802.16 (64QAM, 256 Subcarriers, 10 MHz Bandwidth)	14.0 dB	0.1 µF	30 mVpp	157 µs/1.47 ms

Figure 45 shows how residual ripple and rise/fall times vary with filter capacitance when the AD8362 is driven by a single carrier WCDMA signal (Test Model 1-64) at 2140 MHz.

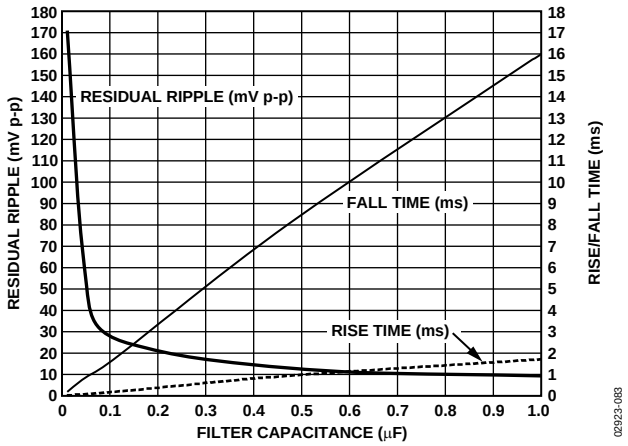


Figure 45. Residual Ripple, Rise and Fall Times vs. Filter Capacitance, Single Carrier WCDMA Input Signal, Test Model 1-64

ADJUSTING VTGT TO ACCOMMODATE SIGNALS WITH VERY HIGH CREST FACTORS

An external direct connection between VREF (1.25 V) and VTGT sets up the internal target voltage, which is the rms voltage that must be provided by the VGA to balance the AGC feedback loop.

In the default scheme, the VREF of 1.25 V positions this target to 0.06 × 1.25 V = 75 mV. In principle, however, VTGT may be driven by voltages that are larger or smaller than this. This technique can be used to move the intercept, which increases or decreases the input sensitivity of the device, or to improve the accuracy when measuring signals with large crest factors.

For example, if this pin is supplied from VREF via a simple resistive attenuator of 1 kΩ:1 kΩ, the output required from the VGA is halved to 37.5 mV rms. Under these conditions, the effective headroom in the signal path that drives the squaring cell is doubled. In principle, this doubles the peak crest factor that may be handled by the system.

Figure 46 and Figure 47 show the effect of varying VTGT on measurement accuracy when the AD8362 is swept with a series of signals with different crest factors, varying from CW with a crest factor of 3 dB, to a WCDMA carrier (Test Model 1-64) with a crest factor of 10.6 dB. The crest factors of each signal are listed in the plots. In Figure 46, VTGT is set to its nominal value of 1.25 V, while in Figure 47, it is reduced to 0.625 V.

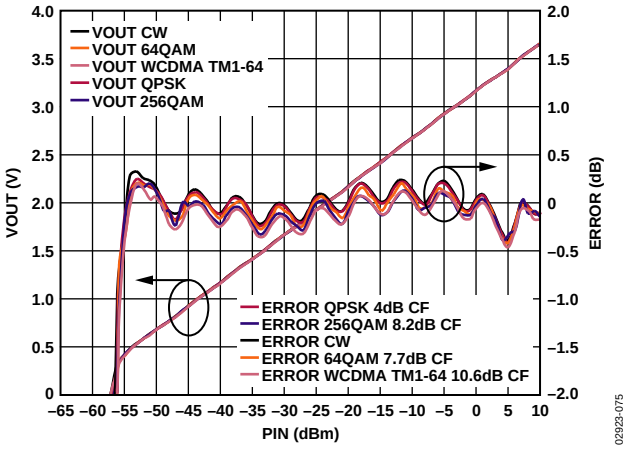


Figure 46. Transfer Function and Law Conformance for Signals with Varying Crest Factors, VTGT = 1.25

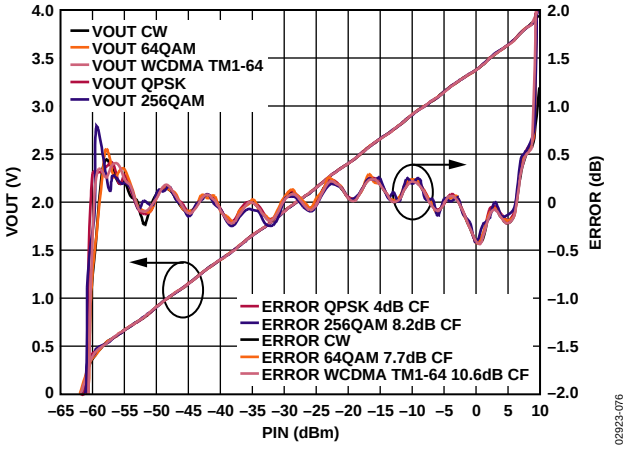


Figure 47. Transfer Function and Law Conformance for Signals with Varying Crest Factors, VTGT = 0.625 V, CLPF = 0.1 µF

Reducing VTGT also reduces the intercept. More significant in this case, however, is the behavior of the error curves. Note that in Figure 47 all of the error curves sit on one another, while in Figure 46 there is some vertical spreading. This suggests that VTGT should be reduced in those applications where a wide range of input crest factors are expected. As noted, VTGT can also be increased above its nominal level of 1.25 V. While this can be used to increase the intercept, it would have the undesirable effect of degrading measurement accuracy in situations where the crest factor of the signal being measured varies significantly.

ALTERING THE SLOPE

None of the changes in operating conditions discussed so far affect the logarithmic slope (V_{SLP}) in Equation 9. This can readily be altered by controlling the fraction of VOUT that is fed back to the setpoint interface at the VSET pin. When the full signal from VOUT is applied to VSET, the slope assumes its nominal value of 50 mV/dB. It can be increased by including a voltage divider between these pins, as shown in Figure 48.

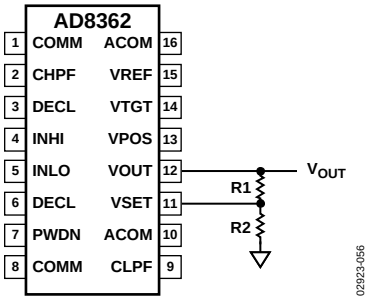


Figure 48. External Network to Raise Slope

Moderately low resistance values should be used to minimize scaling errors due to the 70 kΩ input resistance at the VSET pin. This resistor string also loads the output, and it eventually reduces the load-driving capabilities if very low values are used. To calculate the resistor values, use

$$R1 = R2' (S_D/50 - 1) \quad (15)$$

where:
S_D is the desired slope, expressed in mV/dB.
$R2'$ is the value of R2 in parallel with 70 kΩ.

For example, using R1 = 1.65 kΩ and R2 = 1.69 kΩ (R2' = 1.649 kΩ), the nominal slope is increased to 100 mV/dB. Note however, that doubling the slope in this manner will reduce the maximum input signal to approximately −10 dBm because of the limited swing of VOUT (4.9 V with a 5 V power supply).

TEMPERATURE COMPENSATION AND REDUCTION OF TRANSFER FUNCTION RIPPLE

The transfer function ripple and intercept drift of the AD8362 can be reduced using two techniques detailed in Figure 50. CLPF is reduced from its nominal value. For broadband-modulated input signals, this results in increased noise at the output that is fed back to the VSET pin.

The noise contained in this signal causes the gain of the VGA to fluctuate around a central point, moving the wiper of the Gaussian Interpolator back and forth on the R-2R ladder.

Because the gain-control voltage is constantly moving across at least one of taps of the Gaussian Interpolator, the relationship between the rms signal strength of the VGA output and the VGA control voltage becomes independent of the VGA gain control ripple (Figure 49). The signal being applied to the squaring cell is now lightly AM modulated. However, this does not change the peak-to-average ratio of the signal.

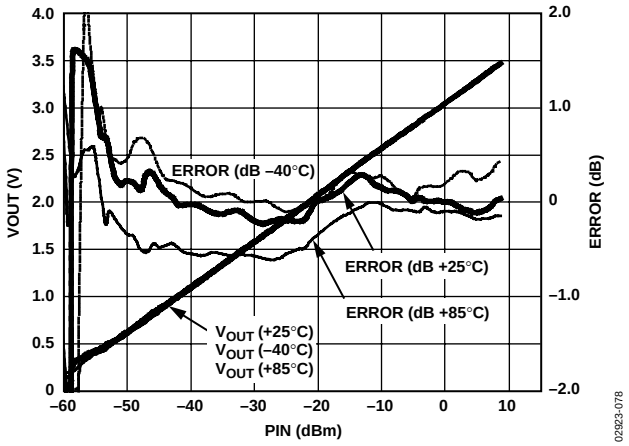
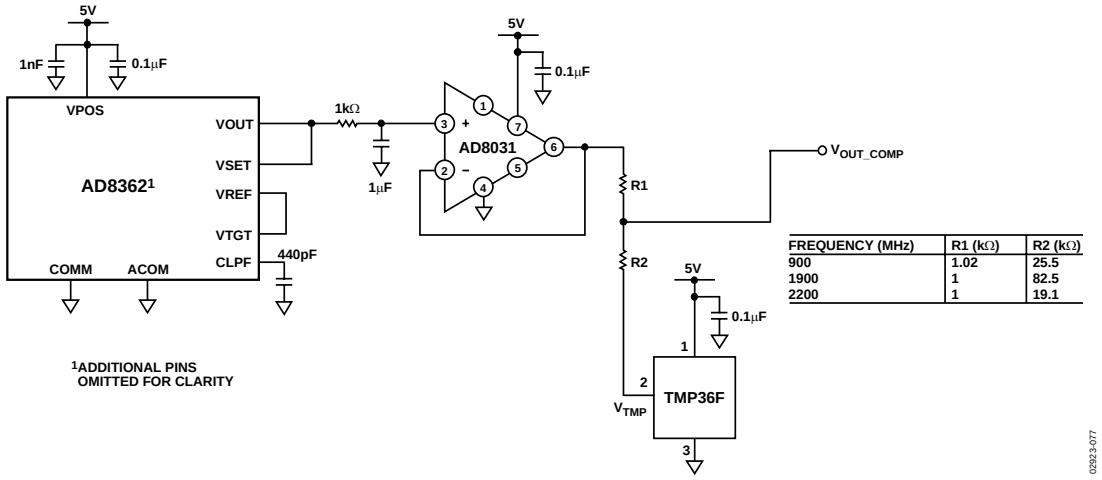


Figure 49. Transfer Function and Linearity with Combined Ripple Reduction and Temperature Compensation Circuits, Frequency = 2.14 GHz, Single-Carrier WCDMA, Test Model 1-64



FREQUENCY (MHz)	R1 (kΩ)	R2 (kΩ)
900	1.02	25.5
1900	1	82.5
2200	1	19.1

Figure 50. Temperature Compensation and Reduction of Transfer Function Ripple

Because of the reduced filter capacitor, the rms voltage appearing at the output of the error amplifier now contains significant peak-to-peak noise. While it is critical to feed this signal back to the VGA gain control input with the noise intact, the rms voltage going to the external measurement node can be filtered using a simple filter to yield a largely noise-free rms voltage.

The circuit shown in Figure 50 also incorporates a temperature sensor that compensates temperature drift of the intercept. Because the temperature drift varies with frequency, the amount of compensation required must also be varied using R1 and R2.

These compensation techniques are discussed in more detail in Application Note AN-653, Improving Temperature, Stability, and Linearity of High Dynamic Range RMS RF Power Detectors.

OPERATION IN CONTROLLER MODE

The AD8362 provides a controller mode feature at the VOUT pin. Using VSET for the setpoint voltage, it is possible for the AD8362 to control subsystems such as power amplifiers (PAs), variable gain amplifiers (VGAs), or variable voltage attenuators (VVAs), which have output power that decreases monotonically with respect to their (increasing) gain control signal.

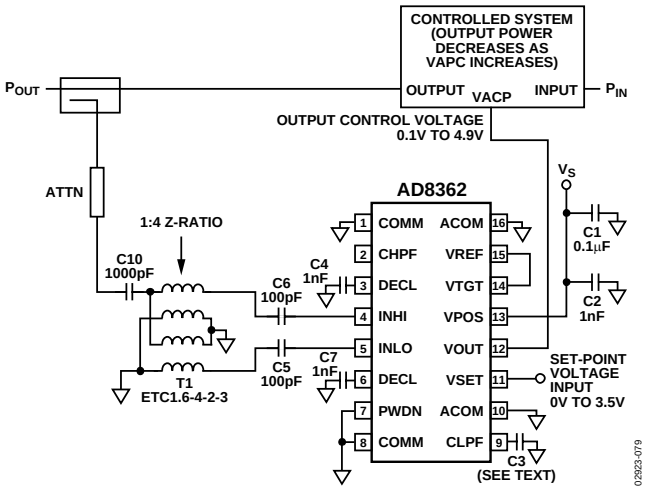


Figure 51. Basic Connections for Controller Mode Operation

To operate in controller mode, the link between VSET and VOUT is broken. A setpoint voltage is applied to the VSET input, while VOUT is connected to the gain control terminal of the variable gain amplifier (VGA), and the AD8362 RF input is connected to the output of the VGA (generally using a directional coupler or power splitter and some additional attenuation). Based on the defined relationship between VOUT and the RF input signal when the device is in measurement mode, the AD8362 will adjust the voltage on VOUT (VOUT is now an error amplifier output), until the level at the RF input corresponds to the applied VSET. For example, in a closed loop system, if VSET is set to 3 V, VOUT will increase or decrease until the input signal is equal to 0 dBm. This relationship follows directly from the measurement mode transfer function (see Figure 10, Figure 11, and Figure 12).

Therefore, when the AD8362 operates in controller mode, there is no defined relationship between VSET and VOUT. VOUT will settle to a value that results in balance between input signal level appearing at INHI/INLO and VSET.

In order for this output power control loop to be stable, a ground-referenced capacitor must be connected to the CLPF pin. This capacitor integrates the internal error current that is present when the loop is not balanced.

Increasing VSET, which corresponds to demanding a higher signal from the VGA, will tend to decrease VOUT. The VGA or VVA therefore must have a negative sense. In other words, increasing the gain control voltage decreases gain. If this is not the case, an op-amp, configured as an inverter with suitable level shifting, can be used to correct the sense of the VOUT signal.

RMS VOLTMETER WITH 90 dB DYNAMIC RANGE

The 60 dB range of the AD8362 can be extended by adding a stand alone VGA as a preamplifier whose gain control input is derived directly from VOUT. This extends the dynamic range by the gain control range of this second amplifier. When this VGA also provides a linear-in-dB (exponential) gain control function, the overall measurement remains linearly scaled in decibels. The VGA gain must decrease with an increase in its gain bias in the same way as the AD8362. Alternatively, an inverting op-amp with suitable level shifting can be used. It is convenient to select a VGA needing only a single 5 V supply and capable of generating a fully balanced differential output. All of these conditions are met by the AD8330. Figure 52 shows the schematic. Also note that the AD8131 is used to convert a single-ended input into the differential-ended input needed by the AD8330. The AD8131's gain of 2 does create a dc offset on the output of the AD8362, but this is removed by connecting 0.5 V to the VMAG on AD8330.

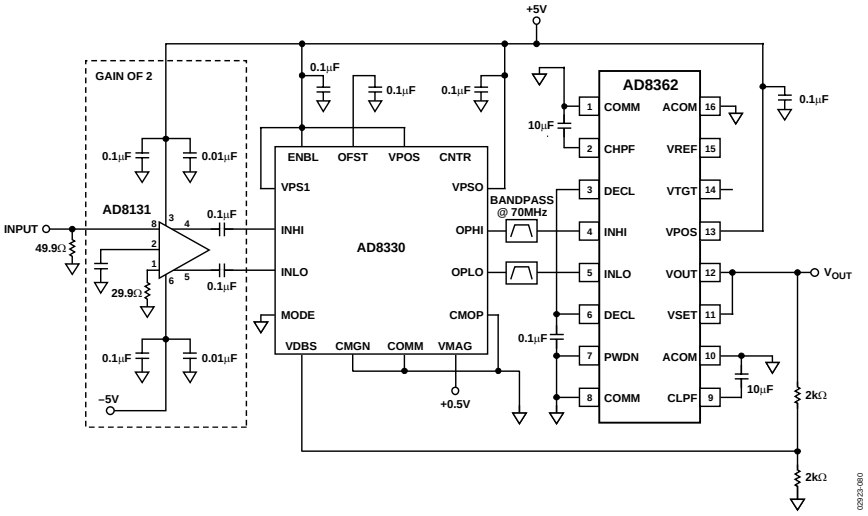


Figure 52. RMS Voltmeter with 90 dB Dynamic Range

Using the inverse gain mode (MODE pin low) of the AD8330, its gain decreases on a slope of 30 mV/dB to a minimum value of 3 dB for a gain voltage (VDBS) of 1.5 V. VDBS is 40% of the output of the AD8362. Over the 3 V range from 0.5 V to 3.5 V, the gain of the AD8330 varies by (0.4 × 3 V)/(30 mV/dB), or 40 dB. Combined with the 60 dB gain span of the AD8362, this results in a 100 dB variation for a 3 V change in VOUT. Due to the noise generated from the AD8330, the dynamic range is limited to approximately 90 dB. This can only be achieved when a band-pass filter is used at the operating frequency between the AD8330 and AD8362.

Figure 53 shows data results of the extended dynamic range at 70 MHz with error in VOUT.

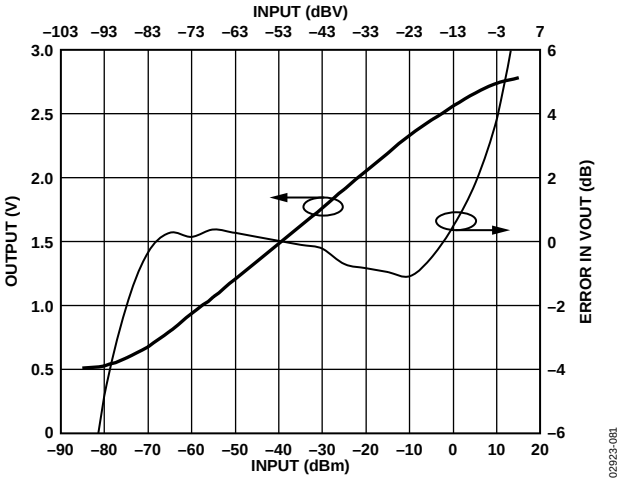


Figure 53. Output and Conformance for the AD8330/AD8362 Extended Dynamic Range Circuit

AD8362 EVALUATION BOARD

The AD8362 evaluation board provides for a number of different operating modes and configurations, including many described in this data sheet. The measurement mode is set up by positioning SW2 as shown in Figure 54. The AD8362 can be operated in controller mode by applying the setpoint voltage to the VSET connector, and flipping SW2 to its alternate position.

The internal voltage reference is used for the target voltage when SW1 is in the position shown in Figure 54. This voltage may optionally be reduced via a voltage divider implemented with R4 and R5, with LK1 in place and SW1 switched to its alternate position. Alternatively, an external target voltage may be used with SW1 switched to its alternate position, LK1 removed, and the external target voltage applied to the VTGT connector.

In measurement mode, the slope of the response at VOUT may be increased by using a voltage divider implemented with resistors in Positions R17 and R9, and with SW2 switched to its alternate position.

The AD8362 is powered up with SW3 in the position shown in Figure 54 and connector PWDN open. The part can be powered down by either connecting a logic high voltage to connector PWDN with SW3 in the position, or by switching SW3 to its alternate position.

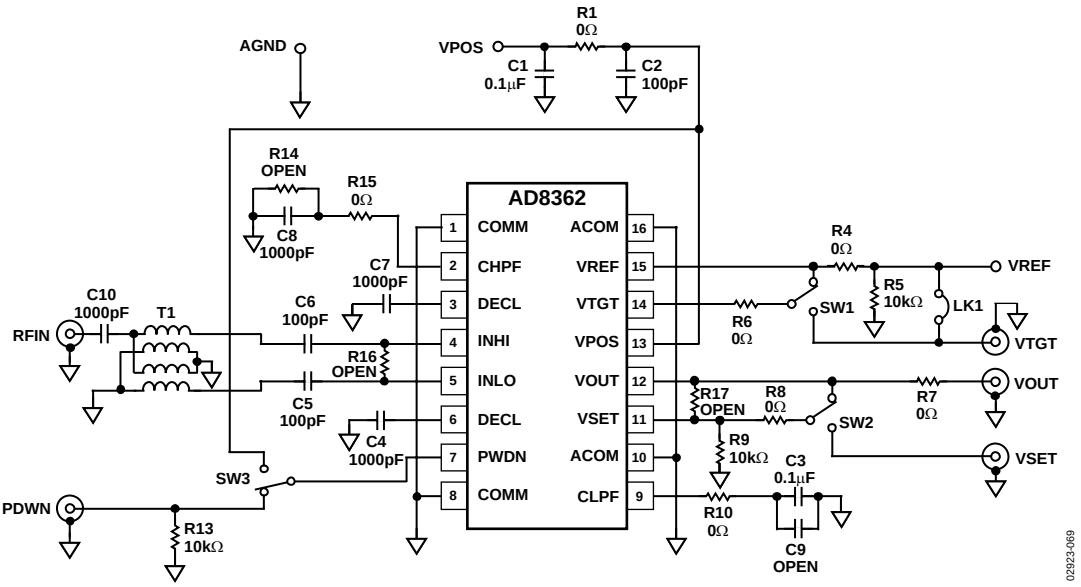


Figure 54. Evaluation Board Schematic

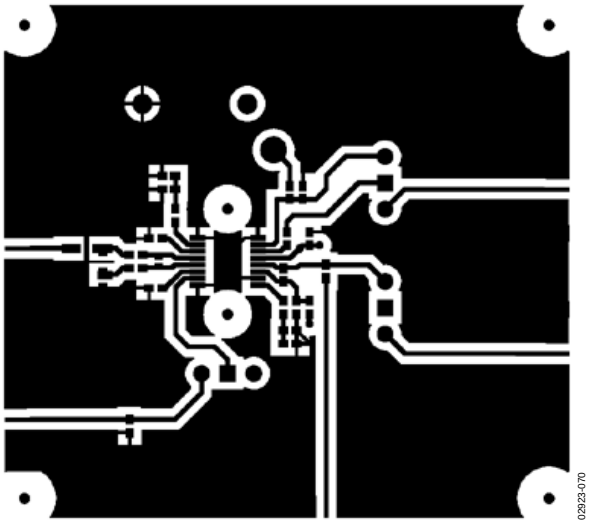


Figure 55. Component Side Metal of Evaluation Board

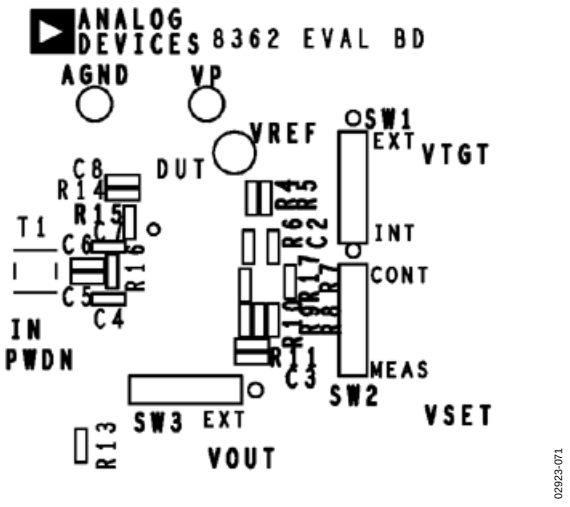


Figure 56. Component Side Silkscreen of Evaluation Board

Table 5. Evaluation Board Configuration Options

Component	Function	Part Number	Default Value
T1		ETC 1.6-4-2-3 (M/A-COM)	
C1	Supply filtering/decoupling capacitor		0.1 µF
C2	Supply filtering/decoupling capacitor		100 pF
C3	Output low-pass filter capacitor		0.1 µF
C9	Output low-pass filter capacitor		Open
C4, C7, C10	Input bias-point decoupling capacitors		1000 pF
C5, C6	Input signal coupling capacitors		100 pF
C8	Input high-pass filter capacitor		1000 pF
DUT	AD8362	AD8362ARU	
SW1, LK1, R4, R5	Use to reduce VTGT or to externally apply a voltage to VTGT		LK1 = Open, R4 = 0 Ω, R5 = 10k Ω, SW1 connects VREF to VTGT
R1, R6, R7, R8, R10, R15	Jumpers		0 Ω
R16	Not installed		Open
R9, R17	Slope adjustment resistors. See the Altering the Slope section.		R9 = 10 kΩ, R17 = Open
SW2	Measurement mode/controller mode selector		SW2 connects VSET to VOUT
SW3, R13	Power-down/power-up or external power-down selector		R13 = 10 kΩ, SW3 connects PWDN to R13

OUTLINE DIMENSIONS

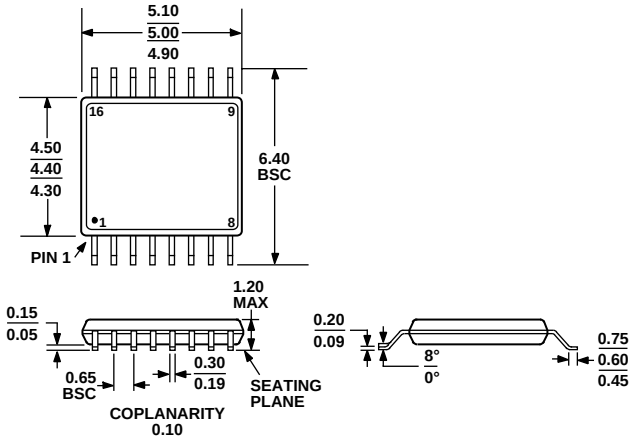


Figure 57. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8362ARU	−40°C to +85°C	16-Lead TSSOP, Tube	RU-16
AD8362ARU-REEL7	−40°C to +85°C	16-Lead TSSOP, 7" Tape and Reel	RU-16
AD8362ARUZ[1]	−40°C to +85°C	16-Lead TSSOP, Tube	RU-16
AD8362ARUZ-REEL7[1]	−40°C to +85°C	16-Lead TSSOP, 7" Tape and Reel	RU-16
AD8362-EVAL		Evaluation Board	

[1] Z = Pb-free part.

NOTES

C02923-0-9/05(C)