DATA SHEET

C-Array: Class 2, X7R 16 V, 25 V and 50 V
Noble Metal Electrode
Surface mount ceramic multilayer capacitors

Product specification
Supersedes data of 1st November 1999
File under Discrete Ceramics, ACM2

2000 Jul 18

Philips Components

PHILIPS

Surface mount ceramic multilayer capacitors

C-Array: Class 2, X7R 16 V, 25 V and 50 V Noble Metal Electrode

FEATURES

- 0612 (4 × 0603) capacitors (of the same capacitance value) per array
- Less than 50% board space of an equivalent discrete component
- High volumetric efficiency
- Dense dielectric layers
- Supplied in tape on reel or loose in bag
- Increased throughput, by time saved in mounting
- Cost savings on manufacturing time.

APPLICATIONS

- Professional electronics
- High density consumer electronics
- Automotive.

DESCRIPTION

Each capacitor element consists of a rectangular block of ceramic dielectric in which a number of interleaved precious metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two terminations, silver dipped with a barrier layer of plated nickel and finally covered with a layer of plated tin (NiSn). An outline of the structure is shown in Fig.1.

QUICK REFERENCE DATA

DESCRIPTION	VALUE
Rated voltage U_R (DC)	16 V; 25 V; 50 V (IEC)
Capacitance (E12 series):	
16 V	10 nF to 100 nF
25 V	10 nF to 68 nF
50 V	220 pF to 10 nF
Tolerance on capacitance	±10%; ±20%
Sectional specifications	IEC 60384-10, second edition 1989-04; also based on CECC 32 100
Detailed specification	based on CECC 32 101-801
Climatic category (IEC 6068)	55/125/56

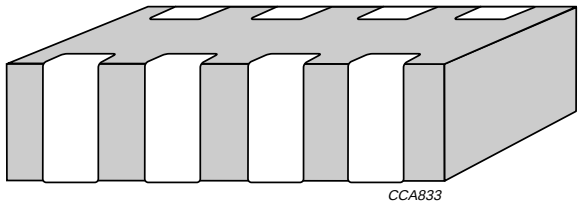
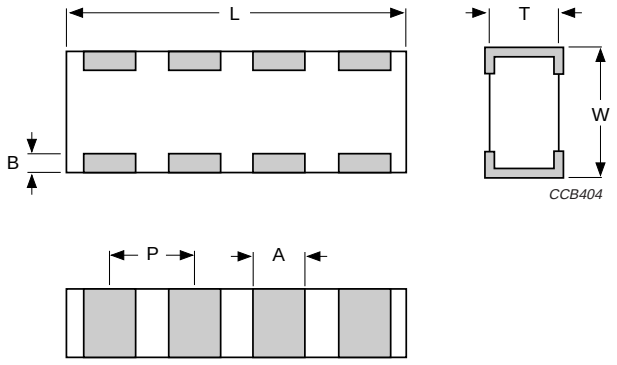


Fig.1 Simplified outline.

MECHANICAL DATA



For dimensions see Table 1.

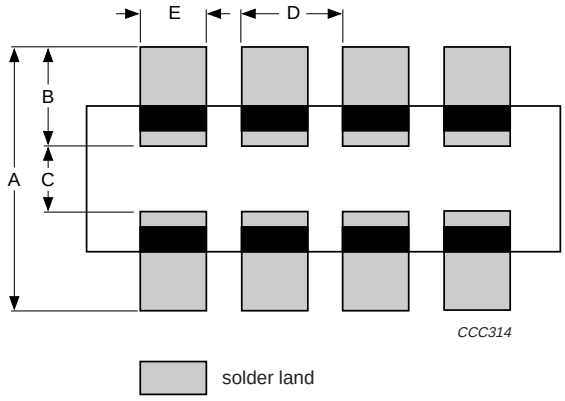
Fig.2 Dimensional outline.

Physical dimensions

Table 1 Capacitor dimensions for product size 0612 (4 × 0603); see Fig.2

CASE SIZE	L	W	T		A	B	P
			MIN.	MAX.			
Dimensions in millimetres							
0612 (4 × 0603)	3.20 ±0.15	1.60 ±0.15	0.80 ±0.10	1.20 ±0.10	0.40 ±0.1	0.30 ±0.2	0.80 ±0.1
Dimensions in inches							
0612 (4 × 0603)	0.125 ±0.006	0.063 ±0.006	0.032 ±0.004	0.048 ±0.004	0.016 ±0.004	0.012 ±0.008	0.031 ±0.004

DIMENSIONS OF SOLDER LANDS



For dimensions see Table 2.

Fig.3 Recommended dimensions of solder lands.

Table 2 Solder land dimensions; see Fig.3

CASE SIZE	FOOTPRINT DIMENSIONS (mm)				
	A	**B**	**C**	**D**	**E**
0612 (4 × 0603)	2.54 ±0.15	0.89 ±0.10	0.76 ±0.10	0.80 ±0.10	0.45 ±0.10

SELECTION CHART

C (pF)	LAST TWO DIGITS OF 12NC	16 V	25 V	50 V
		0612 (4 × 0603)		
220	14			
270	15			
330	16			
390	17			
470	18			
560	19			
680	21			
820	22			
1000	23			
1200	24			
1500	25			0.8 ±0.1
1800	26			
2200	27			
2700	28			
3300	29			
3900	31			
4700	32			
5600	33			
6800	34			
8200	35			
10000	36			
12000	37			
15000	38			
18000	39			
22000	41		0.8 ±0.1	
27000	42			
33000	43	0.8 ±0.1		
39000	44			
47000	45			
56000	46		1.2 ±0.1	
68000	47			
82000	48		Values in shaded cells indicate thickness classification.	
100000	49			

Thickness classification and packaging quantities

THICKNESS CLASSIFICATION (mm)	8 mm TAPE WIDTH AMOUNT PER REEL			
	∅180 mm; 7"		∅330 mm; 13"	
	PAPER	BLISTER	PAPER	BLISTER
0.8 ±0.1	4000	4000	10000	10000
1.2 ±0.1	4000	4000	10000	10000

ORDERING INFORMATION

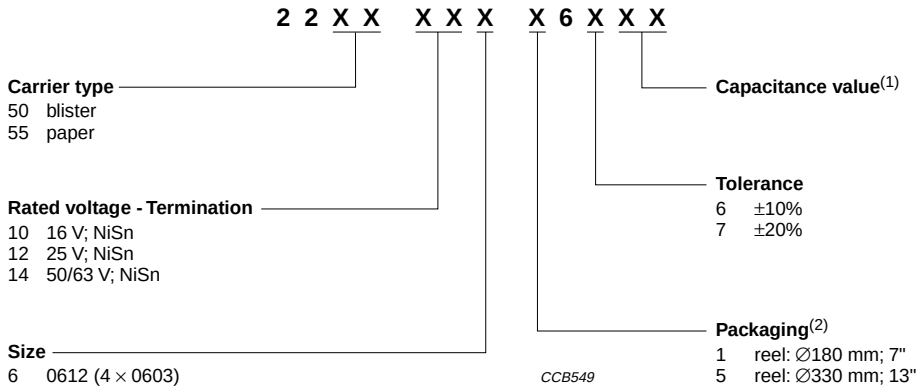
Components may be ordered by using either a simple 15-digit clear text code or Philips unique 12NC.

Clear text code

EXAMPLE: 06122R104K7B200

SIZE CODE	TEMP. CHAR.	CAPACITANCE	TOL.	VOLTAGE	TERMINATION	PACKAGING	MARKING	SERIES
0612 (4 × 0603)	2R = X7R	104 = 100000 pF; the third digit signifies the multiplying factor: 1 = × 10 2 = × 100 3 = × 1000 4 = × 10000	K = ±10% M = ±20%	7 = 16 V 8 = 25 V 9 = 50 V	B = NiSn	2 = 180 mm; 7" paper 3 = 330 mm; 13" paper B = 180 mm; 7" blister F = 330 mm; 13" blister	0 = no marking	0 = conv. ceramic

Ordering code 12NC



(1) Refer to chapter “Selection chart”.

(2) Amount on reel depends on thickness classification, see section “Thickness classification and packaging quantities”.

ELECTRICAL CHARACTERISTICS FOR CLASS 2, CAPACITORS

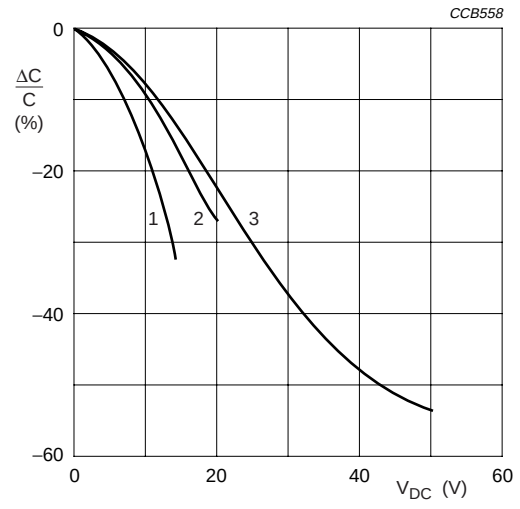
Class 2 capacitors; X7R dielectric; NiSn terminations

Unless otherwise stated all electrical values apply at an ambient temperature of 23 ±3 °C, an atmospheric pressure of 86 to 106 kPa, and a relative humidity of 63 to 67%.

DESCRIPTION	VALUE
Capacitance (E12 series):	
16 V	10 nF to 100 nF
25 V	10 nF to 68 nF
50 V	220 pF to 10 nF
Tolerance on capacitance after 1000 hours	±10%; ±20%
Test voltage (DC) for 1 minute	$2.5 \times U_R$
Tan δ; note 1:	
16 V	≤3.5%
25 V and 50 V	≤2.5%
Insulation resistance after 1 minute at U_R (DC):	
$C \leq 10$ nF	$R_{ins} \times C \geq 10^5$ MΩ
$C > 10$ nF	$R_{ins} \times C > 1000$ s
Ageing	typical 1% per time decade

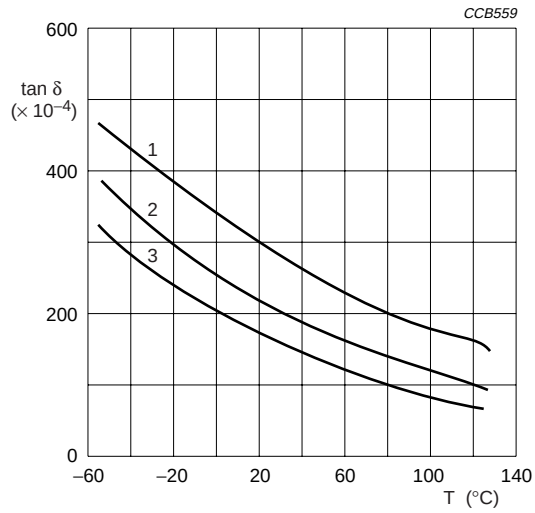
Note

1. Measured at 1 V, 1 kHz, using a four-gauge method.



Curve 1 = 16 V product.
Curve 2 = 25 V product.
Curve 3 = 50 V product.

Fig.4 Typical capacitance change with respect to the capacitance at 1 V as a function of DC voltage at 25 °C.



Curve 1 = 16 V product.
Curve 2 = 25 V product.
Curve 3 = 50 V product.

Fig.5 Typical tan δ as a function of temperature.

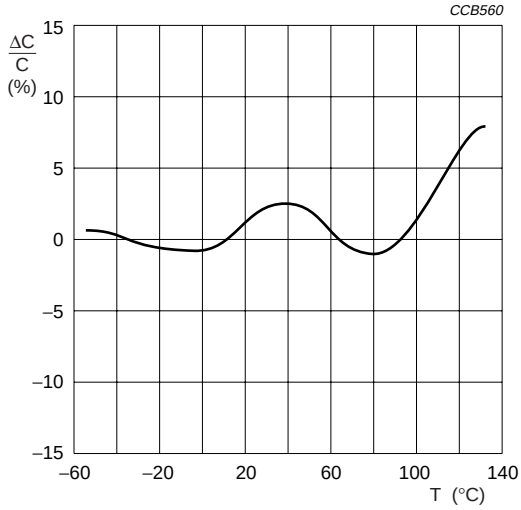


Fig.6 Typical capacitance change as a function of temperature.

TESTS AND REQUIREMENTS

Table 3 Test procedures and requirements

IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.4		mounting	the capacitors may be mounted on printed-circuit boards or ceramic substrates by applying wave soldering, reflow soldering (including vapour phase soldering) or conductive adhesive	no visible damage
4.5		visual inspection and dimension check	any applicable method using ×10 magnification	in accordance with specification
4.6.1		capacitance (measured 1000 hours after date of manufacture)	f = 1 kHz; measuring voltage 1 V_{rms} at 20 °C	within specified tolerance
4.6.2		tan δ	f = 1 kHz; measuring voltage 1 V_{rms} at 20 °C	in accordance with specification
4.6.3		insulation resistance	at U_R (DC) for 1 minute	in accordance with specification
4.6.4		voltage proof	2.5 × U_R for 1 minute	no breakdown or flashover
4.7.1		temperature characteristic	between minimum and maximum temperature	in accordance with specification
4.8		adhesion	a force of 5 N applied for 10 s to the line joining the terminations and in a plane parallel to the substrate	no visible damage
4.9		bond strength of plating on end face	mounted in accordance with IEC 60384 10, paragraph 4.4 conditions: bending 1 mm at a rate of 1 mm/s, radius jig 340 mm	no visible damage ΔC/C: ±10%
4.10	Tb	resistance to soldering heat; jig clamps to the second component in the longitudinal line	260 ±5 °C for 10 ±0.5 s in a static solder bath	the terminations shall be well tinned after recovery ΔC/C: ±10%
		resistance to leaching; jig clamps to the second component in the longitudinal line	260 ±5 °C for 30 ±1 s in a static solder bath	using visual enlargement of ×10, dissolution of the terminations shall not exceed 10%

IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.11	Ta	solderability; jig clamps to the second component in the longitudinal line	zero hour test, and test after storage (20 to 24 months) in original packing in normal atmosphere; unmounted chips completely immersed for 2 ±0.5 s in a solder bath at 235 ±5 °C	the terminations shall be well tinned
4.12	Na	rapid change of temperature	preconditioning: between minimum and maximum temperature, 5 cycles	no visible damage after 24 hours recovery: $\Delta C/C$: ≤15%
4.14	Ca	damp heat	preconditioning: 56 days at 40 °C; 90 to 95% RH; U_R applied	after 48 hours recovery: $\Delta C/C$: ±15% tan δ: 7% R_{ins}: 1000 MΩ or $R_i C_R \geq 25$ s, whichever is less
4.15		endurance	preconditioning: $2 \times U_R$ at 125 °C for 1000 hours, recovery 48 ±4 hours at room temperature	after 48 hours recovery: $\Delta C/C$: ±20% tan δ: 7% R_{ins}: 2000 MΩ or $R_i C_R \geq 50$ s, whichever is less