

# **Specification for BTHQ 240064AVB-EMN-06-LEDWhite-COG**

Version October 2003

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**Specification  
of  
LCD Module Type  
Model No.: COG-BT240064-06**

**1. General Description**

- 240 x 64 Dots STN Negative Blue Transmissive Dot Matrix LCD Module.
- Viewing Angle: 6 o'clock direction.
- Driving duty: 1/65 Duty, 1/7 bias.
- 'Epson' S1D10605D04B (COG) Dot Matrix LCD Drivers or equivalent.
- FPC
- Lightguide: White LED x 2 (Japan dies).

**2. Mechanical Specifications**

The mechanical detail is shown in Fig. 1(c) and summarized in Table 1 below.

Table 1

| Parameter          | Specifications   | Unit  |
|--------------------|--|-------|
| Outline dimensions | 120.0(W) x 194.82(H) x 5.5(D)<br>(Included FPC. Excluded LCD end seal) | mm    |
| Viewing area       | 102.4(W) x 30.22(H)  | mm    |
| Active area        | 98.38(W) x 26.22(H)  | mm    |
| Display format     | 240(W) x 64(H)   | dots  |
| Dot size           | 0.39(W) x 0.39(H)  | mm    |
| Dot spacing        | 0.02(W) x 0.02(H)  | mm    |
| Dot pitch          | 0.41(W) x 0.41(H)  | mm    |
| Weight             | TBD  | grams |





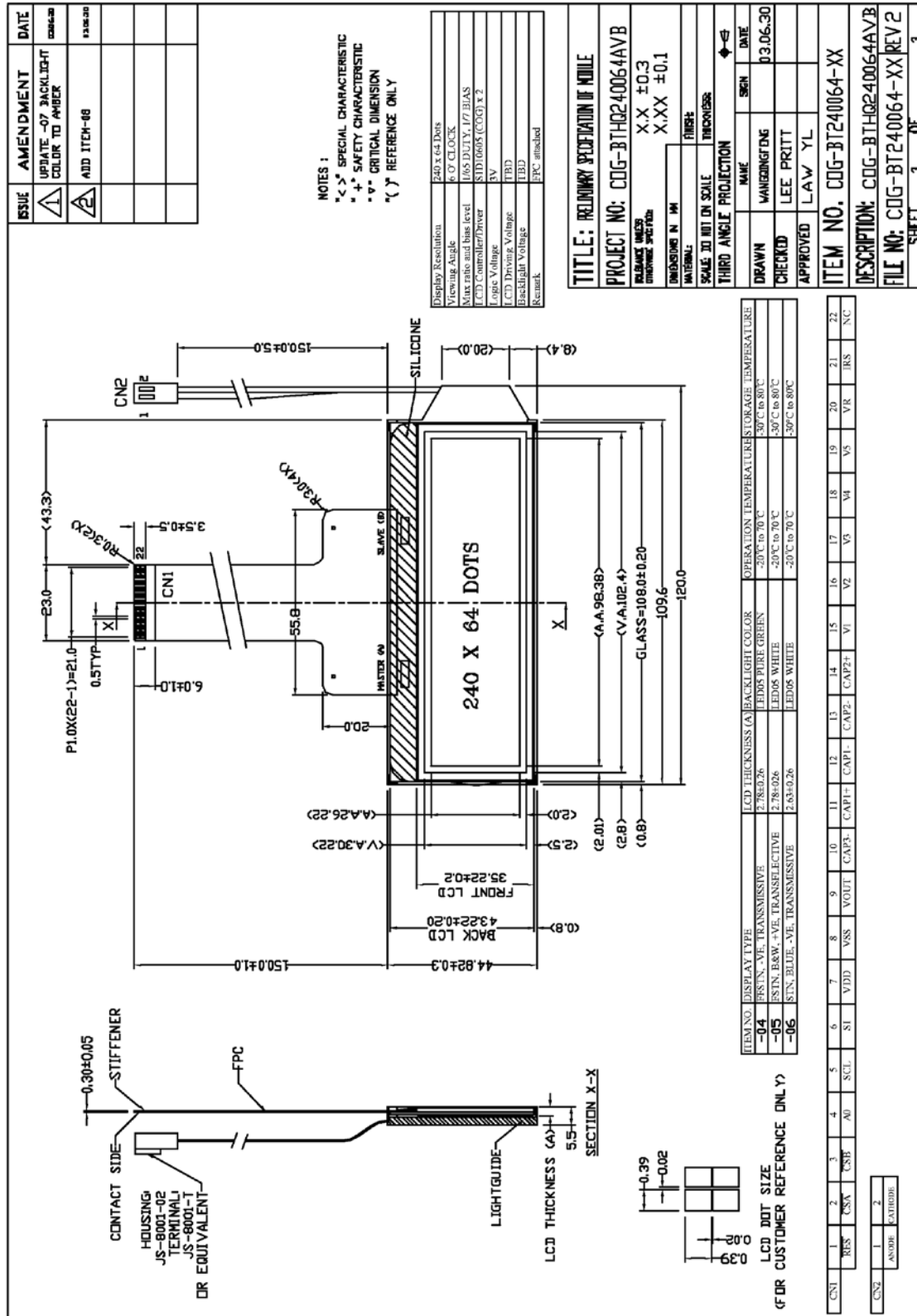


Figure 1(c): Specification Module 3

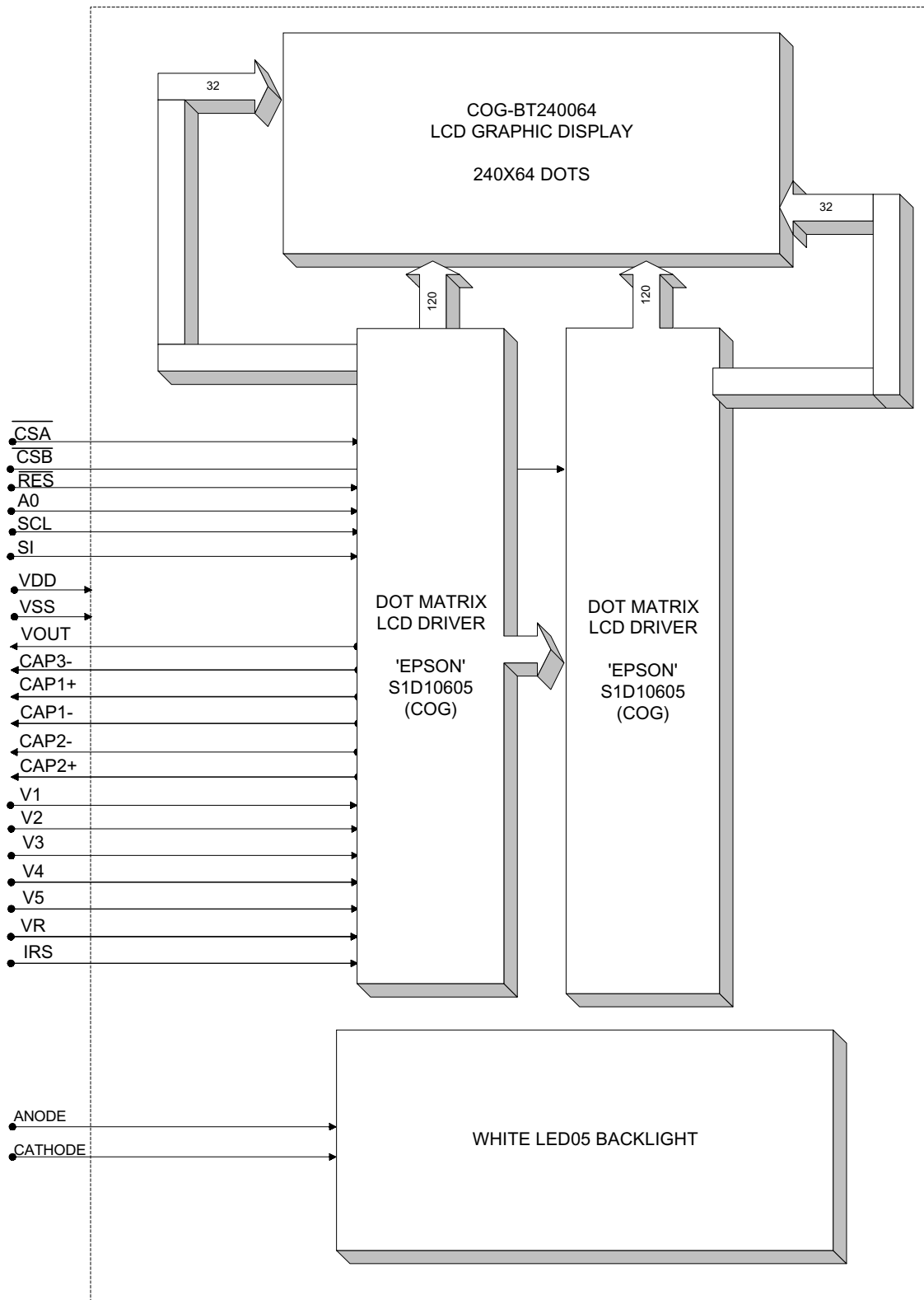


Figure 2: Block Diagram.



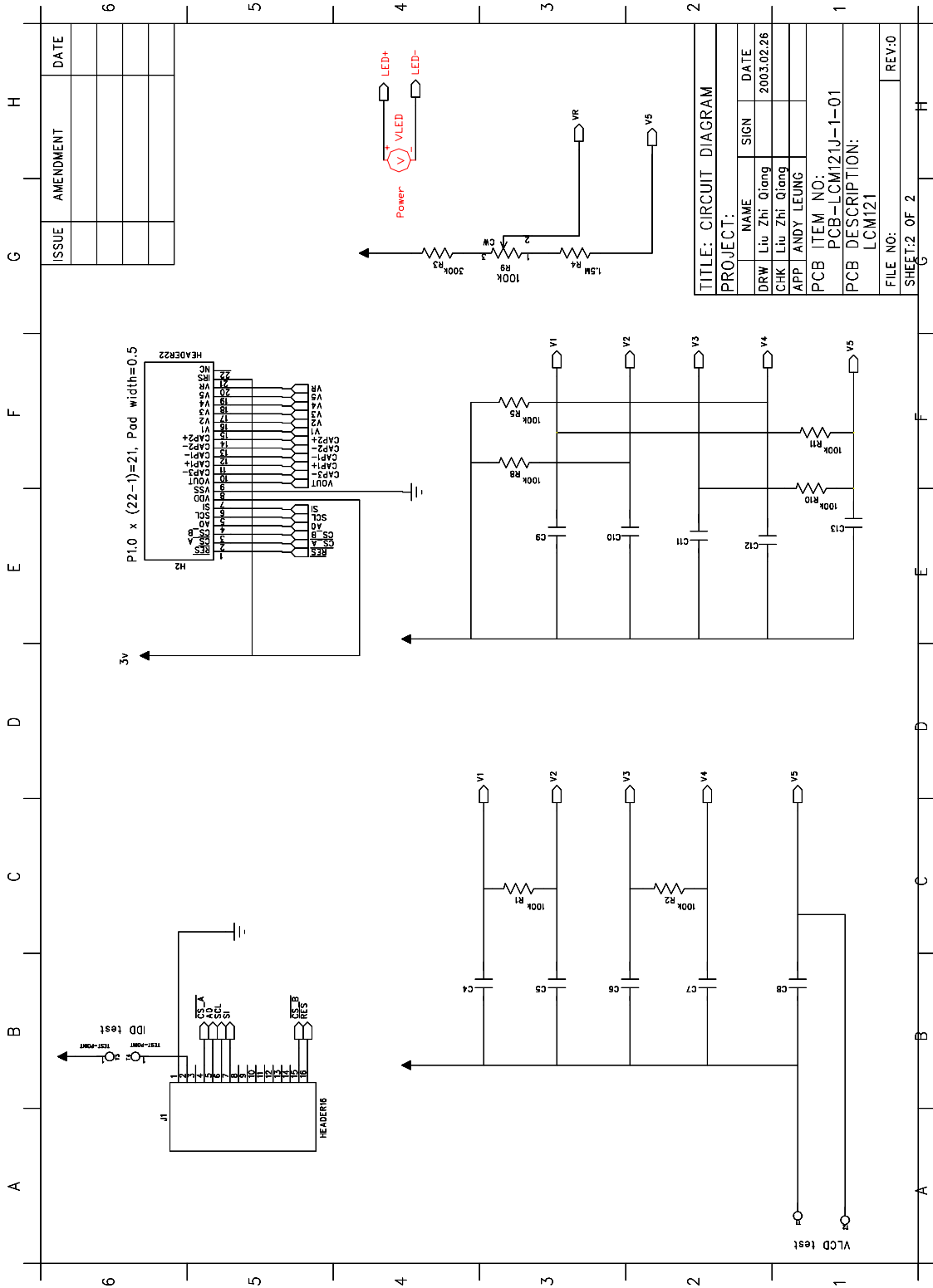


Figure 3: Reference Circuit

### 3. Interface signals

Table 2(a): Pin Assignment of CN1

| Pin No. | Symbol                  | Description   |
|---------|-------------------------|---|
| 1       | $\overline{\text{RES}}$ | When $\overline{\text{RES}}$ is set to Low, the settings are initialized.<br>The reset operation is performed by the $\overline{\text{RES}}$ signal level.  |
| 2       | $\overline{\text{CSA}}$ | This is the chip select signal for first chip.<br>When $\overline{\text{CSA}}(\text{CS1})=\text{“Low”}$ and $\text{CS2}=\text{HIGH}$ , then the chip select becomes active and the input/output of data/commands is enabled.  |
| 3       | $\overline{\text{CSB}}$ | This is the chip select signal for second chip.<br>When $\overline{\text{CSB}}(\text{CS1})=\text{“Low”}$ and $\text{CS2}=\text{HIGH}$ , then the chip select becomes active and the input/output of data/commands is enabled.   |
| 4       | A0                      | This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command.<br>A0=“High”: Indicates that SCL, and SI are display data.<br>A0=“Low”: Indicates that SCL and SI are control data.  |
| 5       | SCL                     | Serial clock input terminal.  |
| 6       | SI                      | Serial data input terminal.   |
| 7       | VDD                     | Power supply for logic(+3V).  |
| 8       | VSS                     | 0 V pin connected to the system ground (GND).   |
| 9       | VOUT                    | DC/DC voltage converter. Connects a capacitor between this terminal and VSS.  |
| 10      | CAP3-                   | DC/DC voltage converter. Connects a capacitor between this terminal and CAP1+ pin.  |
| 11      | CAP1+                   | DC/DC voltage converter. Connects a capacitor between this terminal and CAP1- pin.  |
| 12      | CAP1-                   | DC/DC voltage converter. Connects a capacitor between this terminal and CAP1+ pin.  |
| 13      | CAP2-                   | DC/DC voltage converter. Connects a capacitor between this terminal and CAP2+ pin.  |
| 14      | CAP2+                   | DC/DC voltage converter. Connects a capacitor between this terminal and CAP2- pin.  |
| 15      | V1                      | This is multi-level power supply for liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below.<br>$\text{VDD} (=V0) \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$<br><br>Master operation When the power supply turns ON, the internal power supply circuits produce V1 to V4 voltages shown below. The voltage setting are selected using the LCD bias set command.<br>For 1/7 bias: $V1=(1/7) \times V5$ , $V2=(2/7) \times V5$ , $V3=(5/7) \times V5$ , $V4=(6/7) \times V5$ . |
| 16      | V2                      |   |
| 17      | V3                      |   |
| 18      | V4                      |   |
| 19      | V5                      |   |

Table 2(b): Pin Assignment of CN1

| Pin No. | Symbol | Description  |
|---------|--------|--|
| 20      | VR     | Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divider.<br>These are only enabled when the V5 voltage regulator internal resistors are not used (IRS=LOW).<br>These cannot be used when the V5 voltage regulator resistors are used (IRS=HIGH).  |
| 21      | IRS    | This terminal selects the resistors for the V5 voltage level adjustment.<br>IRS=HIGH: Use the internal resistors.<br>IRS=LOW: Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.<br>This pin is enabled only when the master operation mode is selected.<br>It is fixed to either HIGH or LOW when the slave operation mode is selected. |
| 22      | NC     | No connection.   |

Table 2(c): Pin Assignment of CN2

| Pin No. | Symbol  | Description          |
|---------|---------|----------------------|
| 1       | ANODE   | Anode of backlight   |
| 2       | CATHODE | Cathode of backlight |

## 4. Absolute Maximum Ratings

### 4.1 Electrical Maximum Ratings(Ta = 25 °C)

Table 3

| Parameter                              | Symbol      | Min.  | Max.    | Unit |
|--|-------------|-------|---------|------|
| Power Supply voltage (Logic)           | VDD - VSS   | -0.3  | +6.0    | V    |
| Power Supply voltage(2) (VDD standard) | VSS2        | -4.0  | +0.3    | V    |
| Power Supply voltage(3) (VDD standard) | V5,VOUT     | -18.0 | +0.3    | V    |
| Power Supply voltage(4) (VDD standard) | V1,V2,V3,V4 | V5    | +0.3    | V    |
| Input voltage                          | Vin         | -0.3  | VDD+0.3 | V    |

Note:

- 1.)The modules may be destroyed if they are used beyond the absolute maximum ratings.
- 2.)All voltage values are referenced to VSS= 0V.
- 3.)The V1, V2, V3, and V4 voltages must always satisfy the condition of  $VDD \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ .

### 4.2 Environmental Condition

Table 4

| Item   | Operating Temperature (Topr)  |       | Storage Temperature (Tstg) |       | Remark          |
|--|---|-------|----------------------------|-------|-----------------|
|  | Min.  | Max.  | Min.                       | Max.  |                 |
| Ambient Temperature  | -20°C   | +70°C | -30°C                      | +80°C | Dry             |
| Humidity   | 95% max. RH for Ta ≤ 40°C<br>< 95% RH for Ta > 40°C   |       |                            |       | no condensation |
| Vibration (IEC 68-2-6) cells must be mounted on a suitable connector | Frequency: 10 ~ 55 Hz<br>Amplitude: 0.75 mm<br>Duration: 20 cycles in each direction.   |       |                            |       | 3 directions    |
| Shock (IEC 68-2-27) Half-sine pulse shape                            | Pulse duration : 11 ms<br>Peak acceleration: 981 m/s <sup>2</sup> = 100g<br>Number of shocks : 3 shocks in 3 mutually perpendicular axes. |       |                            |       | 3 directions    |

## 5. Electrical Specifications

### 5.1 Typical Electrical Characteristics

At  $T_a = +25\text{ }^\circ\text{C}$ ,  $V_{DD} = +3.0\pm 5\%$ ,  $V_{SS} = 0\text{V}$ .

Table 5

| Parameter  | Symbol           | Conditions  | Min.    | Typ. | Max.    | Unit |
|--|------------------|---|---------|------|---------|------|
| Supply voltage (Logic)                               | VDD-VSS          |   | 2.85    | 3.0  | 3.15    | V    |
| Supply voltage (LCD) (built-in)                      | VLCD =VDD-V5     | $T_a = 25\text{ }^\circ\text{C}$ , Character mode<br>VDD = +3.0V, Note 1                  | 7.8     | 8.0  | 8.2     | V    |
| Low-level input signal voltage                       | V <sub>ILC</sub> | Note 2  | VSS     | -    | 0.2xVDD | V    |
| High-level input signal voltage                      | V <sub>IHC</sub> | Note 2  | 0.8xVDD | -    | VDD     | V    |
| Supply Current (Logic & LCD)                         | IDD              | VDD = +3.0V, Note 1,<br>Character mode  | -       | 0.5  | 0.8     | mA   |
|  |                  | VDD = +3.0V, Note 1,<br>Checker board mode  | -       | 1.2  | 1.8     | mA   |
| Supply voltage of white LED05 backlight (Japan dies) | VLED             | Forward current=30mA<br>Number of dies=1x2=2<br>LED color: White (NICHIA RANK B) (Note 3) | 3.8     | 4.0  | 4.2     | V    |

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Note 2: A0, SCL, SI, CS1, RESET pins.

Note 3: Remarks for backlight:

Max allowable continuous forward current is 50 mA @ 25deg C, and for operation above +25degC the max current shall be derated linearly at the rate of - 0.72 mA/ degC.

### 5.2 Timing Specifications

#### Reset Timing

At  $T_a = -20\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DD} = +3.0\text{V}\pm 5\%$ ,  $V_{SS} = 0\text{V}$ .

Table 6

| Item                  | Signal | Symbol | Condition | Rating |      |      | Units |
|-----------------------|--------|--------|-----------|--------|------|------|-------|
|                       |        |        |           | Min.   | Typ. | Max. |       |
| Reset time            |        | tr     |           | —      | —    | 1    | μs    |
| Reset LOW pulse width | RES    | trw    |           | 1      | —    | —    | μs    |

Note : All timing is specified with 20% and 80% of VDD as the standard.

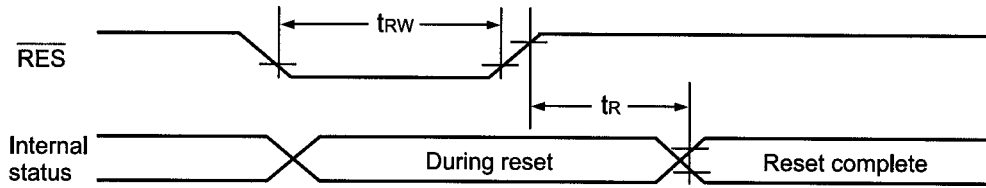


Figure 4: Reset Timing

### The serial interface

At  $T_a = -20\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DD} = +3.0\text{V} \pm 5\%$ ,  $V_{SS} = 0\text{V}$ .

Table 7

| Item                 | Signal | Symbol | Condition | Rating |      | Units |
|----------------------|--------|--------|-----------|--------|------|-------|
|                      |        |        |           | Min.   | Max. |       |
| Serial Clock Period  | SCL    | tSCYC  |           | 250    | —    | ns    |
| SCL HIGH pulse width |        | tSHW   |           | 100    | —    | ns    |
| SCL LOW pulse width  |        | tSLW   |           | 100    | —    | ns    |
| Address setup time   | A0     | tsAS   |           | 150    | —    | ns    |
| Address hold time    |        | tSAH   |           | 150    | —    | ns    |
| Data setup time      | SI     | tsDS   |           | 100    | —    | ns    |
| Data hold time       |        | tsDH   |           | 100    | —    | ns    |
| CS-SCL time          | CS     | tCSS   |           | 150    | —    | ns    |
|                      |        | tCSH   |           | 150    | —    | ns    |

Note 1: The input signal rise and fall ( $t_r$ ,  $t_f$ ) are specified at 15ns or less.

Note 2: All timing is specified using 20% and 80% of VDD as the standard.

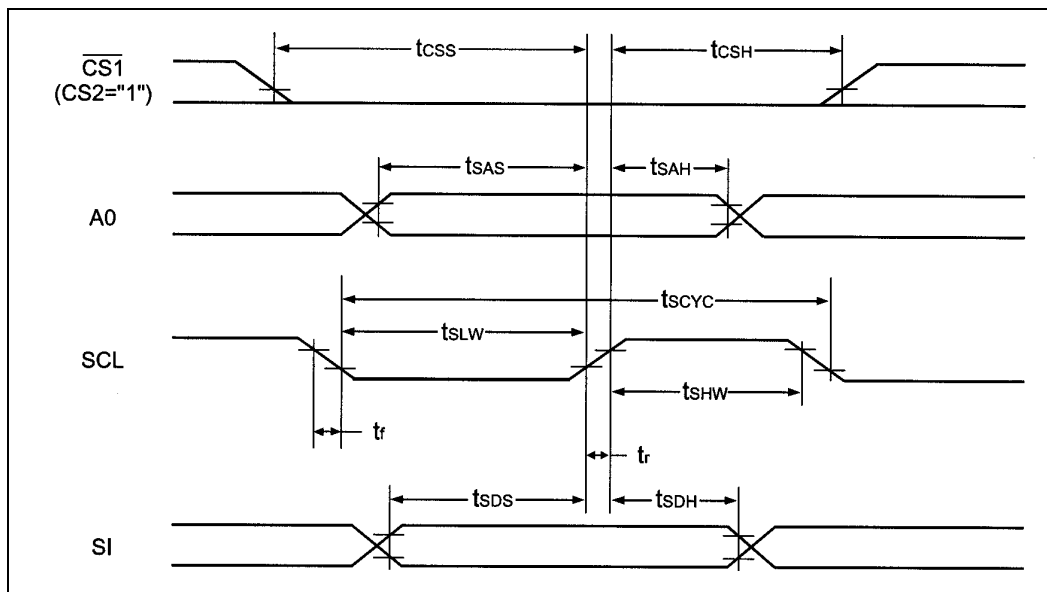


Figure 5: The timing diagram of serial interface

## 6. Command Table

Table 8

| Command   | Command Code |    |    |            |    |                         |    |                                  |                |      |    | Function  |   |
|---|--------------|----|----|------------|----|-------------------------|----|----------------------------------|----------------|------|----|---|---|
|   | A0           | RD | WR | D7         | D6 | D5                      | D4 | D3                               | D2             | D1   | D0 |   |   |
| (1) Display ON/OFF                                    | 0            | 1  | 0  | 1          | 0  | 1                       | 0  | 1                                | 1              | 1    | 0  | 1   | LCD display ON/OFF<br>0: OFF, 1: ON   |
| (2) Display start line set                            | 0            | 1  | 0  | 0          | 1  | Display start address   |    |                                  |                |      |    | Sets the display RAM display start line address |   |
| (3) Page address set                                  | 0            | 1  | 0  | 1          | 0  | 1                       | 1  | Page address                     |                |      |    |   | Sets the display RAM page address   |
| (4) Column address set upper bit                      | 0            | 1  | 0  | 0          | 0  | 0                       | 1  | Most significant column address  |                |      |    |   | Sets the most significant 4 bits of the display RAM column address.   |
| Column address set lower bit                          | 0            | 1  | 0  | 0          | 0  | 0                       | 0  | Least significant column address |                |      |    |   | Sets the least significant 4 bits of the display RAM column address.  |
| (5) Status read                                       | 0            | 0  | 1  | Status     |    |                         |    | 0                                | 0              | 0    | 0  |   | Reads the status data   |
| (6) Display data write                                | 1            | 1  | 0  | Write data |    |                         |    |                                  |                |      |    |   | Writes to the display RAM   |
| (7) Display data read                                 | 1            | 0  | 1  | Read data  |    |                         |    |                                  |                |      |    |   | Reads from the display RAM  |
| (8) ADC select  | 0            | 1  | 0  | 1          | 0  | 1                       | 0  | 0                                | 0              | 0    | 0  | 1   | Sets the display RAM address SEG output correspondence<br>0: normal, 1: reverse   |
| (9) Display normal/reverse                            | 0            | 1  | 0  | 1          | 0  | 1                       | 0  | 0                                | 1              | 1    | 0  | 1   | Sets the LCD display normal/reverse<br>0: normal, 1: reverse  |
| (10) Display all points ON/OFF                        | 0            | 1  | 0  | 1          | 0  | 1                       | 0  | 0                                | 1              | 0    | 0  | 1   | Display all points<br>0: normal display<br>1: all points ON   |
| (11) LCD bias set                                     | 0            | 1  | 0  | 1          | 0  | 1                       | 0  | 0                                | 0              | 1    | 0  | 1   | Sets the LCD drive voltage bias ratio<br>S1D10605***** .... 0: 1/9, 1: 1/7<br>S1D10606*****<br>/S1D10608*****<br>/S1D10609***** ... 0: 1/8, 1: 1/6<br>S1D10607***** .... 0: 1/6, 1: 1/5 |
| (12) Read/modify/write                                | 0            | 1  | 0  | 1          | 1  | 1                       | 0  | 0                                | 0              | 0    | 0  | 0   | Column address increment<br>At write: +1<br>At read: 0  |
| (13) End  | 0            | 1  | 0  | 1          | 1  | 1                       | 0  | 1                                | 1              | 1    | 0  | 0   | Clear read/modify/write   |
| (14) Reset  | 0            | 1  | 0  | 1          | 1  | 1                       | 0  | 0                                | 0              | 1    | 0  | 0   | Internal reset  |
| (15) Common output mode select                        | 0            | 1  | 0  | 1          | 1  | 0                       | 0  | 0                                | *              | *    | *  | *   | Select COM output scan direction<br>0: normal direction,<br>1: reverse direction  |
| (16) Power control set                                | 0            | 1  | 0  | 0          | 0  | 1                       | 0  | 1                                | Operating mode |      |    |   | Select internal power supply operating mode   |
| (17) Vs voltage regulator internal resistor ratio set | 0            | 1  | 0  | 0          | 0  | 1                       | 0  | 0                                | Resistor ratio |      |    |   | Select internal resistor ratio (Rb/Ra) mode   |
| (18) Electronic volume mode set                       | 0            | 1  | 0  | 1          | 0  | 0                       | 0  | 0                                | 0              | 0    | 0  | 1   | Set the Vs output voltage electronic volume register  |
| Electronic volume register set                        | 0            | 1  | 0  | *          | *  | Electronic volume value |    |                                  |                |      |    |   |   |
| (19) Static indicator ON/OFF                          | 0            | 1  | 0  | 1          | 0  | 1                       | 0  | 1                                | 1              | 0    | 0  | 1   | 0: OFF, 1: ON   |
| Static indicator register set                         | 0            | 1  | 0  | *          | *  | *                       | *  | *                                | *              | Mode |    |   | Set the flashing mode   |
| (20) Power saver                                      |              |    |    |            |    |                         |    |                                  |                |      |    |   | Display OFF and display all points ON compound command  |
| (21) NOP  | 0            | 1  | 0  | 1          | 1  | 1                       | 0  | 0                                | 0              | 1    | 1  | 1   | Command for non-operation   |
| (22) Test   | 0            | 1  | 0  | 1          | 1  | 1                       | 1  | *                                | *              | *    | *  | *   | Command for IC test. Do not use this command  |

(Note) \*: disabled data