102 X 65 SINGLE CHIP LCD CONTROLLER / DRIVER

1 FEATURES

- 102 x 65 bits Display Data RAM
- Programmable MUX rate
- Programmable Frame Rate
- X,Y Programmable Carriage Return
- Dual Partial Display Mode
- Row by Row Scrolling
- N-line Inversion
- Automatic data RAM Blanking procedure
- Selectable Input Interface:
  - I^2C Bus Fast and Hs-mode (read and write)
  - 68000 & 8080 Parallel Interfaces (read and write)
  - 3-lines and 4-lines SPI Interface (read and write)
  - 3-lines 9 bit Serial Interface (read and write)
- Fully Integrated Oscillator requires no external components
- CMOS Compatible Inputs
- Fully Integrated Configurable LCD bias voltage generator with:
  - Selectable multiplication factor (up to 5X)
  - Effective sensing for High Precision Output
  - Eight selectable temperature compensation coefficients
- Designed for chip-on-glass (COG) applications.
- Low Power Consumption, suitable for battery operated systems
- Logic Supply Voltage range from 1.7 to 3.6V
- High Voltage Generator Supply Voltage range from 1.75 to 4.5V
- Display Supply Voltage range from 4.5 to 14.5V
- Backward Compatibility with STE2001/2/4

2 DESCRIPTION

The STE2004S is a low power CMOS LCD controller driver. Designed to drive a 65 rows by 102 columns graphic display, it provides all necessary functions in a single chip, including on-chip LCD supply and bias voltages generators, resulting in a minimum of externals components and in a very low power consumption.

STE2004S features six standard interfaces (3-lines Serial, 3-lines SPI, 4-lines SPI, 68000 Parallel, 8080 parallel & I^2C) for ease of interfacing with the host micro-controller.

Table 1. Order Codes

Part Numbers	Type
STE2004S DIE2	Bumped Dice on Waffle Pack

Figure 1. Block Diagram

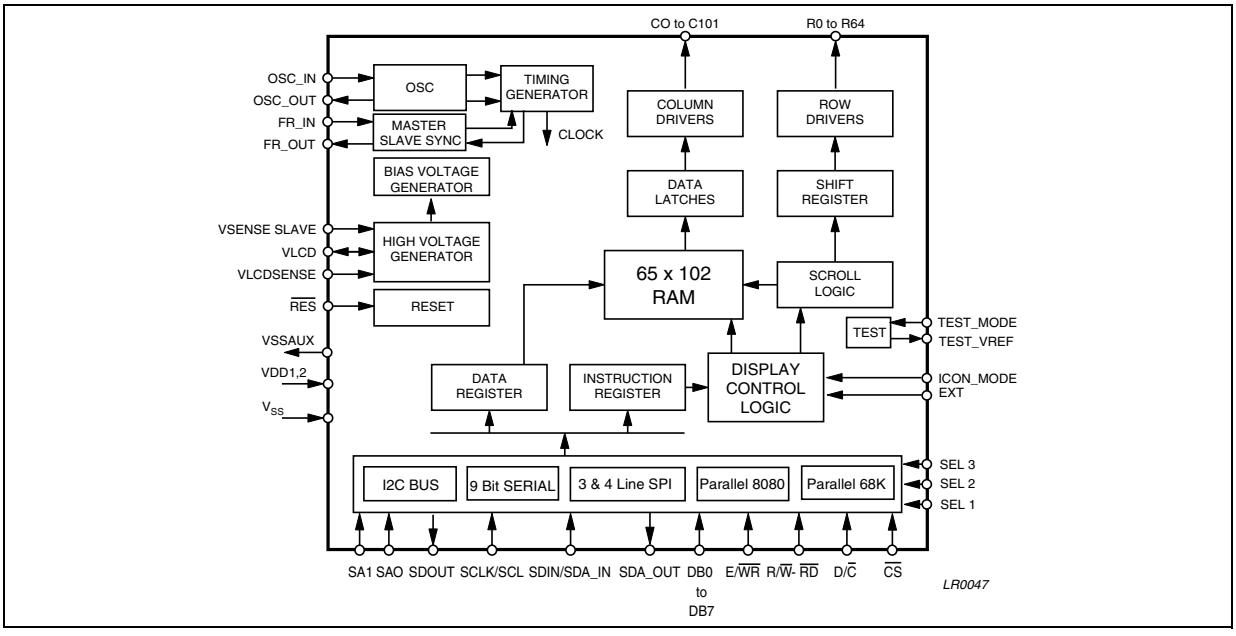


Table 2. PIN DESCRIPTION

<table>
<tr><th>N°</th><th>Pad</th><th>Type</th><th>Function</th></tr>
<tr><td>R0 to R64</td><td>1-6
109-141</td><td>O</td><td>LCD Row Driver Output</td></tr>
<tr><td>C0 to C101</td><td>6-107</td><td>O</td><td>LCD Column Driver Output</td></tr>
<tr><td>VSS</td><td>192-203</td><td>GND</td><td>Ground pads.</td></tr>
<tr><td>VDD1</td><td>156-163</td><td>Supply</td><td>IC Positive Power Supply</td></tr>
<tr><td>VDD2</td><td>164-171</td><td>Supply</td><td>Internal Generator Supply Voltages.</td></tr>
<tr><td>VLCD</td><td>205-209</td><td>Supply</td><td>Voltage Multiplier Output</td></tr>
<tr><td>VLCDSENSE</td><td>204</td><td>Supply</td><td>Voltage Multiplier Regulation Input. V_{LCDOUT} Sensing for Output Voltage Fine Tuning</td></tr>
<tr><td>V_{SENSE_SLAVE}</td><td>145</td><td>Supply</td><td>Voltage reference for SLAVE CHARGE PUMP</td></tr>
<tr><td>V_{SSAUX}</td><td>190-177-
147</td><td>O</td><td>Ground Reference for Pins Configuration</td></tr>
<tr><td>V_{DD1AUX}</td><td>142</td><td>O</td><td>VDD1 Reference for Pins Configuration</td></tr>
<tr><td>SEL1,2,3</td><td>152
153
154</td><td>I</td><td>Interface Mode Selection - CANNOT BE LEFT FLOATING
<table>
<tr><th>SEL3</th><th>SEL2</th><th>SEL1</th><th>Interface</th></tr>
<tr><td>GND / VSSAUX</td><td>GND / VSSAUX</td><td>GND / VSSAUX</td><td>I^2C</td></tr>
<tr><td>GND / VSSAUX</td><td>GND / VSSAUX</td><td>VDD1</td><td>SPI 4-Lines 8 bit</td></tr>
<tr><td>GND / VSSAUX</td><td>VDD1</td><td>GND / VSSAUX</td><td>SPI 3-Lines 8 bit</td></tr>
<tr><td>GND / VSSAUX</td><td>VDD1</td><td>VDD1</td><td>Serial 3-Lines 9 bit</td></tr>
<tr><td>VDD1</td><td>GND / VSSAUX</td><td>GND / VSSAUX</td><td>Parallel 8080-series</td></tr>
<tr><td>VDD1</td><td>GND / VSSAUX</td><td>VDD1</td><td>Parallel 68000-series</td></tr>
</table></td></tr>
<tr><td>EXT_SET</td><td>151</td><td>I</td><td>Extended Instruction Set Selection - CANNOT BE LEFT FLOATING
<table>
<tr><th>EXT PAD CONFIG</th><th>INSTRUCTION SET SELECTED</th></tr>
<tr><td>GND or VSSAUX</td><td>BASIC</td></tr>
<tr><td>VDD1</td><td>EXTENDED</td></tr>
</table></td></tr>
<tr><td>ICON_MODE</td><td>155</td><td>I</td><td>Extended Instruction Set Selection - CANNOT BE LEFT FLOATING
<table>
<tr><th>ICON MODE PAD CONFIG</th><th>ICON MODE STATUS</th></tr>
<tr><td>GND or VSSAUX</td><td>DISBLED</td></tr>
<tr><td>VDD1</td><td>ENABLED</td></tr>
</table></td></tr>
<tr><td>SDOUT</td><td>180</td><td>O</td><td>Serial & SPI Data Output - IF UNUSED MUST BE LEFT FLOATING</td></tr>
<tr><td>SDIN - SDAIN</td><td>179</td><td>I</td><td>SDIN - Serial & SPI Interface Data Input - CANNOT BE LEFT FLOATING</td></tr>
<tr><td></td><td></td><td>I</td><td>SDAIN - I^2C Bus Data In - CANNOT BE LEFT FLOATING</td></tr>
<tr><td>SCLK - SCL</td><td>181</td><td>I</td><td>SCLK - Serial & SPI Interface Clock - CANNOT BE LEFT FLOATING</td></tr>
<tr><td></td><td></td><td>I</td><td>SCL - I^2C bus Clock - CANNOT BE LEFT FLOATING</td></tr>
<tr><td>SDA_OUT</td><td>178</td><td>O</td><td>I^2C Bus Data Out IF UNUSED MUST BE LEFT FLOATING</td></tr>
<tr><td>SA0</td><td>149</td><td>I</td><td>I^2C Slave Address BIT 0 - CANNOT BE LEFT FLOATING</td></tr>
<tr><td>SA1</td><td>148</td><td>I</td><td>I^2C Slave Address BIT 1- CANNOT BE LEFT FLOATING</td></tr>
<tr><td>DB0 to DB7</td><td>182-189</td><td>I/O</td><td>Parallel Interface 8 Bit Data Bus - CANNOT BE LEFT FLOATING</td></tr>
<tr><td>R/$\overline{W}$ - $\overline{RD}$</td><td>175</td><td>I</td><td>R/$\overline{W}$ - 68000 Series Parallel Interface Read & Write Control Input
- CANNOT BE LEFT FLOATING</td></tr>
<tr><td></td><td></td><td>I</td><td>$\overline{RD}$ - 8080 Series Parallel Interface Read enable Clock Input
- CANNOT BE LEFT FLOATING</td></tr>
<tr><td>E / $\overline{WR}$</td><td>176</td><td>I</td><td>E - 68000 Series Parallel Interface Read & Write Clock Input
- CANNOT BE LEFT FLOATING</td></tr>
</table>

Table 2. PIN DESCRIPTION (continued)

<table>
<tr><th>N°</th><th>Pad</th><th>Type</th><th>Function</th></tr>
<tr><td>E / $\overline{WR}$</td><td>176</td><td>I</td><td>$\overline{WR}$ - 8080 Series Parallel Interface - Write enable clock input
- CANNOT BE LEFT FLOATING</td></tr>
<tr><td>$\overline{RES}$</td><td>172</td><td>I</td><td>Reset Input. Active Low.</td></tr>
<tr><td>D/$\overline{C}$</td><td>174</td><td>I</td><td>Interface Data/Command Selector- CANNOT BE LEFT FLOATING</td></tr>
<tr><td>$\overline{CS}$</td><td>173</td><td>I</td><td>Serial & Parallel Interfaces ENABLE. When Low the Incoming Data are Clocked In.
CANNOT BE LEFT FLOATING</td></tr>
<tr><td>TEST_MODE</td><td>191</td><td>I</td><td>Test Pad - 50 kohm internal Pull-down MUST BE CONNECTED TO VSS/VSSAUX</td></tr>
<tr><td>TEST_VREF</td><td>146</td><td>O</td><td>Test Pad - MUST BE LEFT FLOATING</td></tr>
<tr><td>OSCIN</td><td>144</td><td>I</td><td>Oscillator Input:
<table>
<tr><th>OSC_IN</th><th>Configuration</th></tr>
<tr><td>High</td><td>Internal Oscillator Enabled</td></tr>
<tr><td>Low</td><td>Internal Oscillator Disabled</td></tr>
<tr><td>External Oscillator</td><td>Internal Oscillator Disabled</td></tr>
</table></td></tr>
<tr><td>OSCOUT</td><td>210</td><td>O</td><td>Internal/External Oscillator Out - IF UNUSED MUST BE LEFT FLOATING</td></tr>
<tr><td>FR_OUT</td><td>211</td><td>O</td><td>Master Slave Frame Inversion Synchronization.
IF UNUSED MUST BE LEFT FLOATING</td></tr>
<tr><td>FR_IN</td><td>143</td><td>I</td><td>Master Slave Frame Inversion Synchronization.
CANNOT BE LEFT FLOATING</td></tr>
<tr><td>M/$\overline{S}$</td><td>100</td><td>I</td><td>Master/Slave Configuration Bit:- CANNOT BE LEFT FLOATING
<table>
<tr><th>M/$\overline{S}$ PIN</th><th>OSC_OUT</th><th>FR_OUT</th><th>FR_IN</th><th>Charge Pump</th></tr>
<tr><td>High</td><td>ENABLED</td><td>Enabled</td><td>Disabled</td><td>AuxVsense Disabled</td></tr>
<tr><td>Low</td><td>ENABLED</td><td>Enabled</td><td>Enabled</td><td>Charge Pump in Slave Mode or Ext Power</td></tr>
</table></td></tr>
</table>

Figure 2. Chip Mechanical Drawing

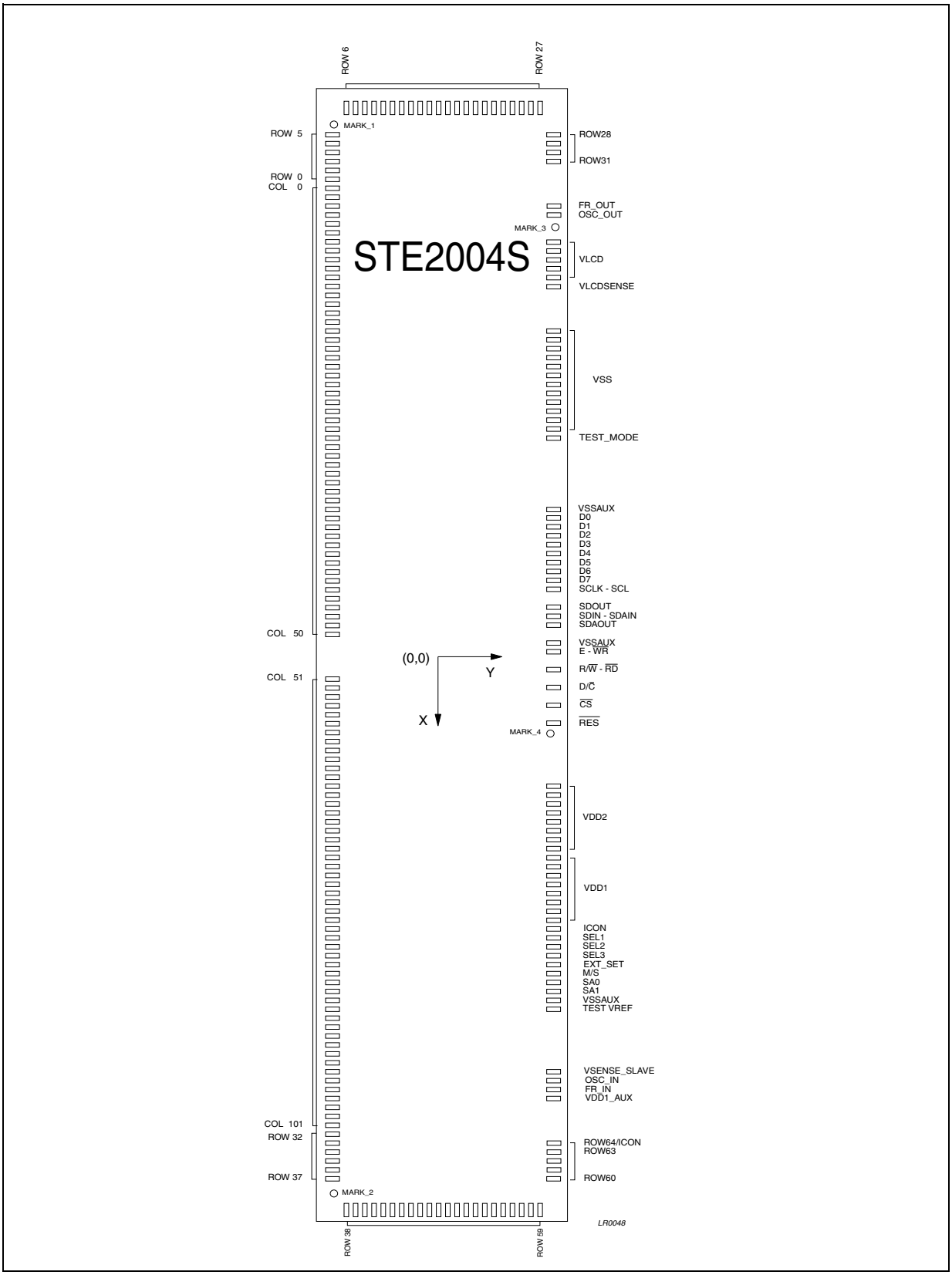
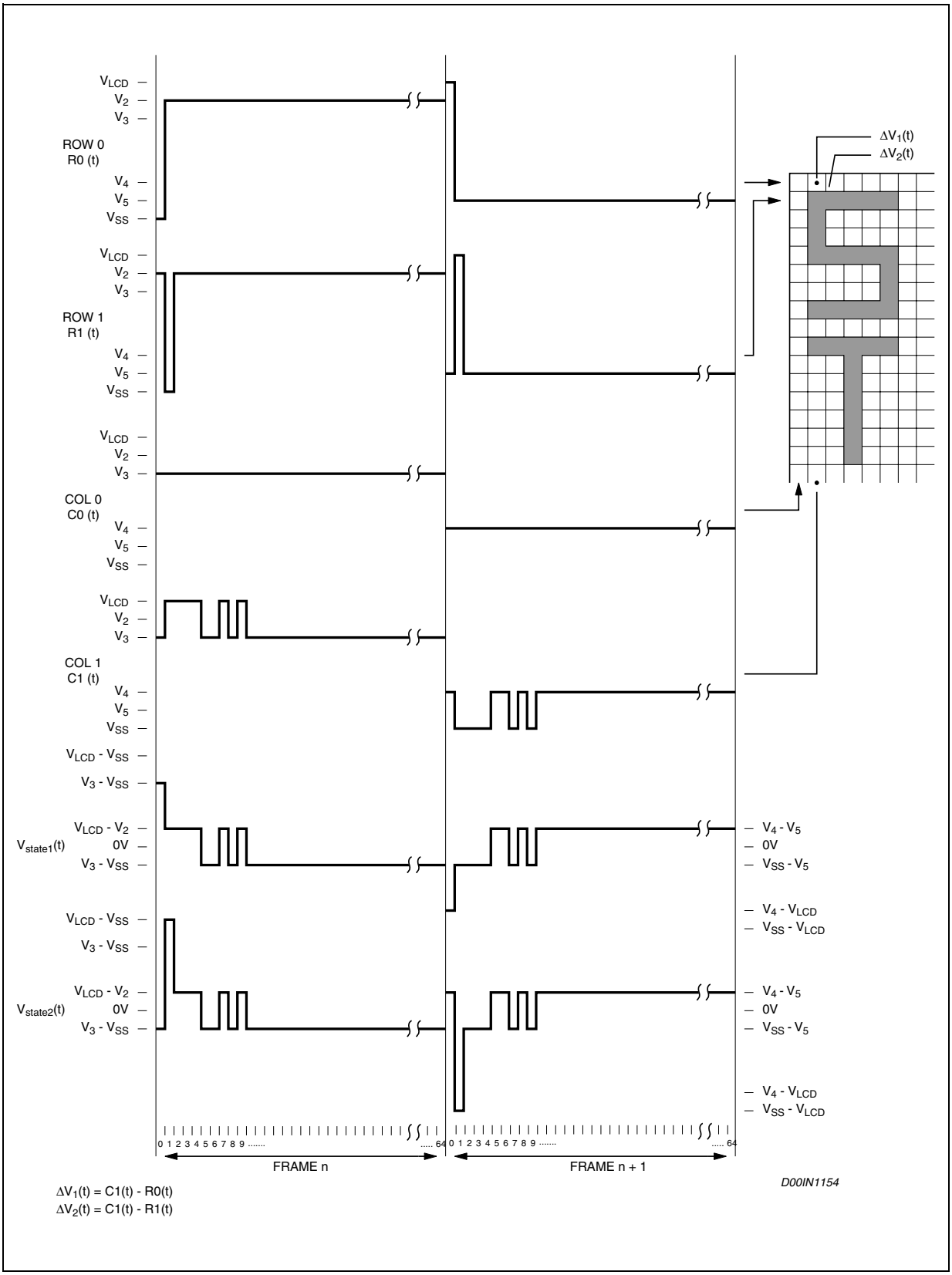


Figure 3. Improved ALTH & PLESKO Driving Method



$\Delta V_1(t) = C1(t) - R0(t)$

$\Delta V_2(t) = C1(t) - R1(t)$

3 CIRCUIT DESCRIPTION

3.1 Supplies Voltages and Grounds

V_{DD2} is supply voltages to the internal voltage generator (see below). If the internal voltage generator is not used, this should be connected to V_{DD1} pad. V_{DD1} supplies the rest of the IC. V_{DD1} supply voltage could be different form V_{DD2}.

$$V_{DD2} \geq \frac{2 \cdot VLCD}{(n+4)} + 200mV$$

3.2 Internal Supply Voltage Generator

The IC has a fully integrated (no external capacitors required) charge pump for the Liquid Crystal Display supply voltage generation. The multiplying factor can be programmed to be: Auto, X5, X4, X3, X2, using the 'set CP Multiplication' Command. If Auto is set, the multiplying factor is automatically selected to have the lowest current consumption in every condition. This make possible to have an input voltage that changes over time and a constant V_{LCD} voltage. The output voltage (V_{LCD}) is tightly controlled through the $V_{LCDSENSE}$ pad. For this voltage, eight different temperature coefficients (TC, rate of change with temperature) can be programmed using TC1 & TC0 or T2, T1 and T0 bits. This will ensure no contrast degradation over the LCD operating range.

An external supply could be connected to V_{LCD} to supply the LCD without using the internal generator. In such event the internal voltage generator must be programmed to zero (PRS = [0;0], Vop = 0 - Reset condition) and the Charge pump (CP[0;0]) set to 5x or Auto Mode.

3.3 Oscillator

A fully integrated oscillator (requires no external components) is present to provide the clock for the Display System. When used the OSC pad must be connected to V_{DD1} pad. An external oscillator could be used and fed into the OSC pin.If an external oscillator is used, it must be always present when STE2004S is not in power down mode. An oscillator out is provided on the OSCOUT Pad to cascade two or more drivers.

3.4 Master/Slave Mode

STE2004S support the Master Slave working Mode for Both Control Logic and Charge Pump. This function allows to drive matrix such as 204x65 or 102x130 using two synchronized STE2004S and the internal Charge Pump of both device.

If M/$\overline{S}$ is connected to VDD1, the driver is configured to work in Master Mode. When STE2004S is in Master Mode the Vsense_Slave Pin is disabled and is possible to control the VLCD value using Vop Bits. The Master Time Generator outputs on FR_OUT and on OSC_OUT the relevant timing references.
If M/$\overline{S}$ is connected to GND, the driver is configured to work in Slave Mode. When STE2004S is in Slave Mode, the VLCD configuration set by Vop registers and the thermal compensation slope set by TC register are neglected. The VLCD Value generated is equal to the Voltage value present on Vsense_Slave Pin so the slave configuration can follow the master configuration. The only recognized configuration is Vop=0 that forces the Charge Pump to be in off state whatever is the value of Vsense_aux.
To Synchronize the Master & Slave timing circuits, the slave driver FR_IN pad must be connected to Master Driver FR_OUT pad and Slave Driver OSC_IN pad must be connected to the master driver OSC_OUT Pad (Fig. 4). This connection ensure a synchronization at both Frame level (R0 on the master is driven together with the Slave R0 driver) and at Oscillator Level (same Frame frequency on the master and on the slave). If the Synchronization at Frame level is not required, FR_IN pin must be connected toVDD1 or to VDD1_aux (Fig. 5).

During Power Up Procesure, Master device must be forced to exit from power down before the slave device. To enter in PowerDown Mode, Slave Device must be forced in Power Down state before Master Device.

Figure 4. Master Slave Logic Connection with frame Synchronization

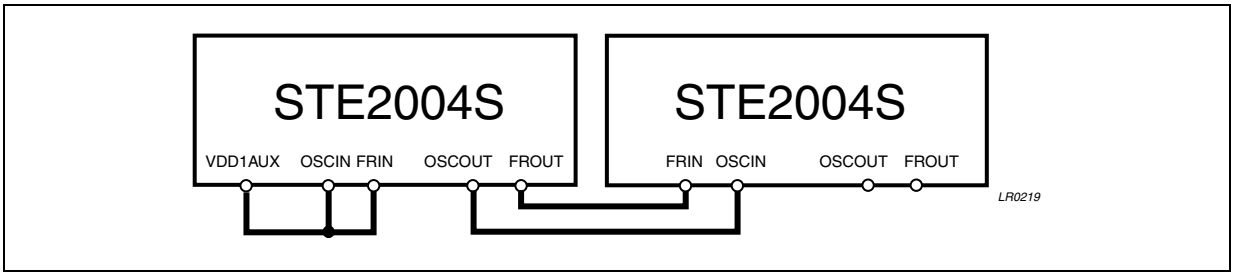
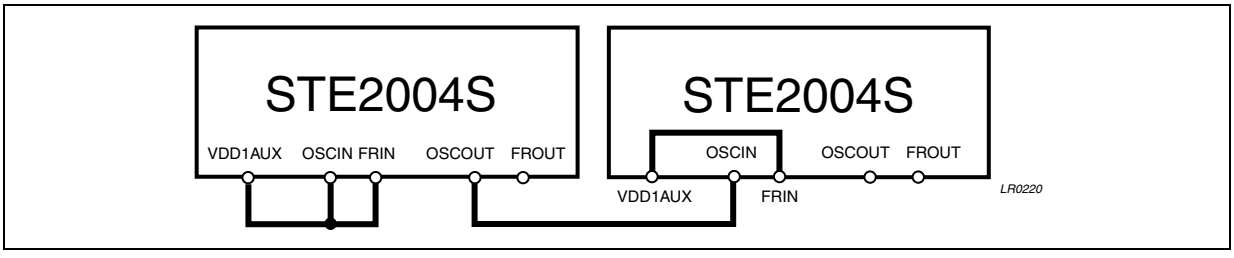


Figure 5. Master Slave Logic Connection without frame Synchronization

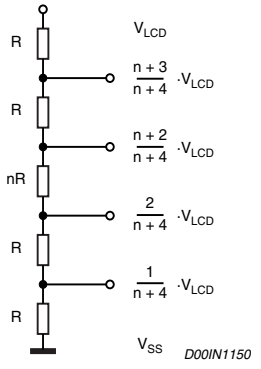


3.5 Bias Levels

To properly drive the LCD, six (Including VLCD and VSS) different voltage (Bias) levels are generated. The ratios among these levels and VLCD, should be selected according to the MUX ratio (m). They are established to be (Fig. 6):

$$V_{LCD}, \frac{n+3}{n+4} V_{LCD}, \frac{n+2}{n+4} V_{LCD}, \frac{2}{n+4} V_{LCD}, \frac{1}{n+4} V_{LCD}, V_{SS}$$

Figure 6. Bias level Generator



thus providing an 1/(n+4) ratio, with n calculated from:

$$n = \sqrt{m} - 3$$

For m = 65, n = 5 and an 1/9 ratio is set.

For m = 49, n =4 and an 1/8 ratio is set.

The STE2004S provides three bits (BS0, BS1, BS2) for programming the desired Bias Ratio as shown below:

Table 3.

BS2	BS1	BS0	n
0	0	0	7
0	0	1	6
0	1	0	5
0	1	1	4
1	0	0	3
1	0	1	2
1	1	0	1
1	1	1	0

The following table Bias Level for m = 65 and m = 49 are provided:

Table 4.

Symbol	m = 65 (1/9)	m = 49 (1/8)
V1	V_{LCD}	V_{LCD}
V2	8/9*V_{LCD}	7/8*V_{LCD}
V3	7/9*V_{LCD}	6/8*V_{LCD}
V4	2/9*V V_{LCD}	2/8*V_{LCD}
V5	1/9 *V_{LCD}	1/8*V_{LCD}
V6	V_{SS}	V_{SS}

3.6 LCD Voltage Generation

The LCD Voltage at reference temperature (To = 27°C) can be set using the VOP register content according to the following formula:

$$V_{LCD}(T=To) = V_{LCD}o = (Ai+V_{OP} \cdot B) \qquad (i=0,1,2)$$

with the following values:

Symbol	Value	Unit	Note
Ao	2.95	V	PRS = [0;0]
A1	6.83	V	PRS = [0;1]
A2	10.71	V	PRS = [1;0]
B	0.0303	V	
To	27	°C	

Note that the three PRS values produce three adjacent ranges for VLCD. If the V_{OP} register and PRS bits are set to zero the internal voltage generator is switched off.

The proper value for the VLCD is a function of the Liquid Crystal Threshold Voltage (Vth) and of the Multiplexing Rate. A general expression for this is:

$$V_{LCD} = \frac{1+\sqrt{m}}{\sqrt{2 \cdot \left(1-\frac{1}{\sqrt{m}}\right)}} \cdot V_{th}$$

For MUX Rate m = 65 the ideal V_{LCD} is:

$$V_{LCD(to)} = 6.85 \cdot V_{th}$$

than:

$$V_{op} = \frac{(6.85 \cdot V_{th} - A_i)}{0.03}$$

3.7 Temperature Coefficients

As the viscosity, and therefore the contrast, of the LCD are subject to change with temperature, there's the need to vary the LCD Voltage with temperature. STE2004S provides the possibility to change the VLCD in a linear fashion against temperature with eight different Temperature Coefficient selectable through T2, T1 and T0 bits. Only four of them are available through basic instruction set.

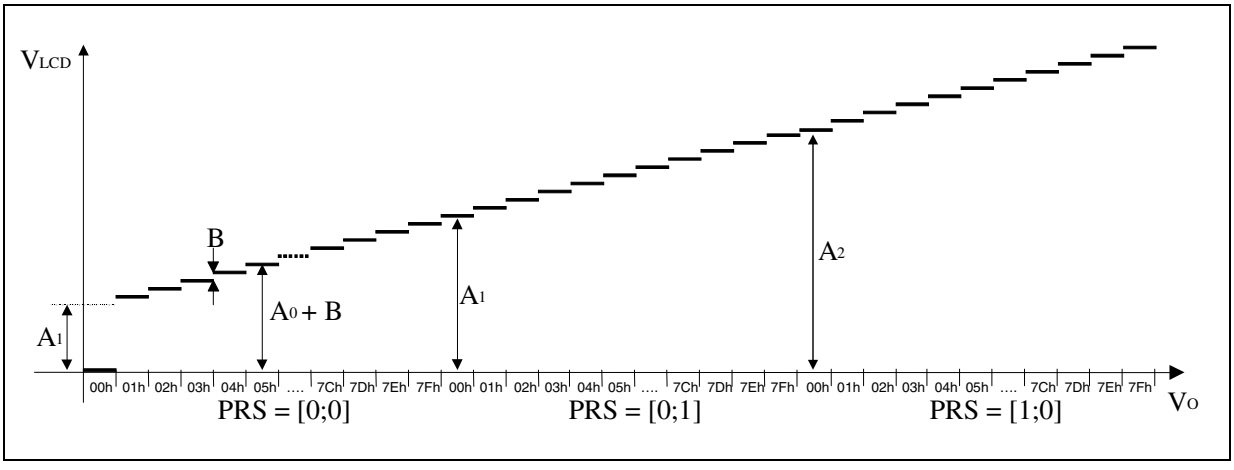
Table 5.

NAME	TC1	TC0	Value	Unit
TC0	0	0	$-0.0 \cdot 10^{-3}$	1/ °C
TC2	0	1	$-0.7 \cdot 10^{-3}$	1/°C
TC3	1	0	$-1.05 \cdot 10^{-3}$	1/°C
TC6	1	1	$-2.1 \cdot 10^{-3}$	1/°C

Table 6.

NAME	T2	T1	T0	Value	Unit
TC0	0	0	0	$-0.0 \cdot 10^{-3}$	1/ °C
TC1	0	0	1	$-0.35 \cdot 10^{-3}$	1/°C
TC2	0	1	0	$-0.7 \cdot 10^{-3}$	1/°C
TC3	0	1	1	$-1.05 \cdot 10^{-3}$	1/°C
TC4	1	0	0	$-1.4 \cdot 10^{-3}$	1/°C
TC5	1	0	1	$-1.75 \cdot 10^{-3}$	1/°C
TC6	1	1	0	$-2.1 \cdot 10^{-3}$	1/°C
TC7	1	1	1	$-2.3 \cdot 10^{-3}$	1/°C

Figure 7.



Finally, the V_{LCD} voltage at a given (T) temperature can be calculated as:

$$V_{LCD}(T) = V_{LCD}o \cdot [1 + (T\text{-}To) \cdot TC]$$

3.8 Display Data RAM

The STE2004S, provides an 102X65 bits Static RAM to store Display data. This is organized into 9 (Bank0 to Bank8) banks with 102 Bytes. One of these Banks can be used for Icons. RAM access is accomplished in either one of the Bus Interfaces provided (see below). Allowed addresses are X0 to X101 (Horizontal) and Y0 to Y8 (Vertical).

When writing to RAM, four addressing mode are provided:

- Normal Horizontal (MX=0 and V=0), having the column with address X= 0 located on the left of the memory map. The X pointer is increased after each byte written. After the last column address (X=X-Carriage), Y address pointer is set to jump to the following bank and X restarts from X=0. (Fig. 8)
- Normal Vertical (MX=0 and V=1), having the column with address X= 0 located on the left of the memory map. The Y pointer is increased after each byte written. After the last Y bank address (Y=Y-Carriage), X address pointer is set to jump to next column and Y restarts from Y=0 (Fig. 9).
- Mirrored Horizontal (MX=1 and V=0), having the column with address X= 0 located on the right of the memory map. The X pointer is increased after each byte written. After the last column address (X=X-Carriage), Y address pointer is set to jump to the next bank and X restarts from X=0 (fig. 10).
- Mirrored Vertical (MX=1 and V=1), having the column with address X= 0 located on the right of the memory map. The Y pointer is increased after each byte written. After the last Y bank address (Y=Y-Carriage), the X pointer is set to jump to next column and Y restarts from Y=0 (fig. 11).

After the last allowed address (X;Y)=(X-Carriage; Y-Carriage), the address pointers always jump to the cell with address (X;Y) = (0;0) (Fig. 12,13,14 & 15).
Data bytes in the memory could have the MSB either on top (D0 = 0, Fig.16) or on the bottom (D0=1, Fig. 17).
The STE2004S provides also means to alter the normal output addressing. A mirroring of the Display along the X axis is enabled setting to a logic one MY bit.This function doesn't affect the content of the memory map. It is only related to the memory read process.

When **ICON MODE=1** the Icon Row is not mirrored with MY and is not scrolled.
When **ICON MODE=0** the Icon Row is like an other graphic line and is mirrored and scrolled.

Three are the multiplex ratio available when the partial display mode is disabled (MUX 33, MUX 49 and MUX 65). Only a subset of writable rows are output on Row drivers in MUX 33,49 & 65 Mode.

When **Y-Carriage<MUX/8**, if Mux 49 is selected only the first 49 memory rows are visualized; if Mux 33 is selected only the first 33 memory rows are visualized. The unused output row & column drivers must be left floating.

When **Y-Carriage<=MUX/8** the icon Bank is located to BANK 8 in MUX 65 Mode, to BANK6 in MUX 49 Mode and to BANK 4 in MUX 33 Mode.

In Mux 33 & 49 Mode, when **Y-Carriage>MUX/8** lines only 33, 49 lines are visualized.

It is possible to select which lines of DDRAM are connected on the output drivers using the scrolling function (Range: 0-Y-Carriage*8). When **Y-Carriage>MUX/8** lines, the icon row is moved in DDRAM to the first row of the Bank correspondant to Y-CARRIAGE Return value, being always connected on the same output Driver.

When **MY=0**, the icon Row is output on R64 in mux 65 mode, on R56 in MUX 49 and on R48 in MUX33.

When **MY=1**, and **ICON MODE=0**, the icon Row is output on R0 whatever is the MUX Rate.

Figure 8. Automatic data RAM writing sequence with V=0 and Data RAM Normal Format (MX=0)[1]

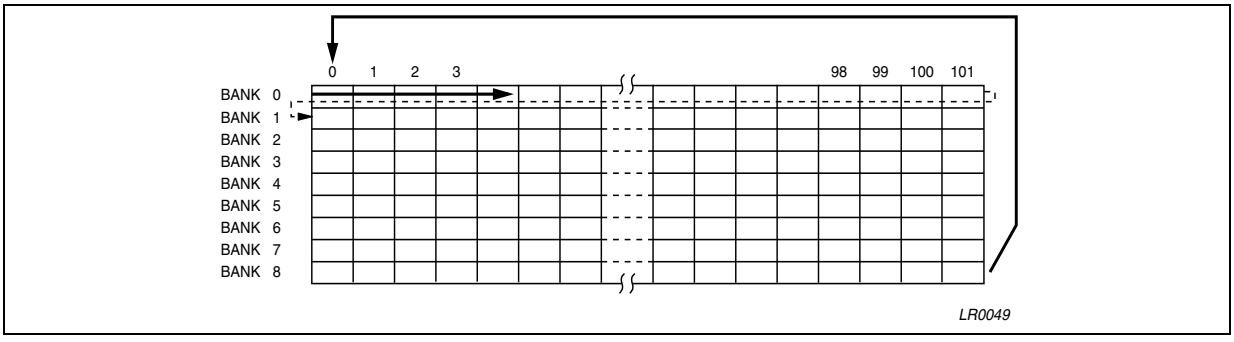


Figure 9. Automatic data RAM writing sequence with V=1 and Data RAM Normal Format (MX=0)[1]

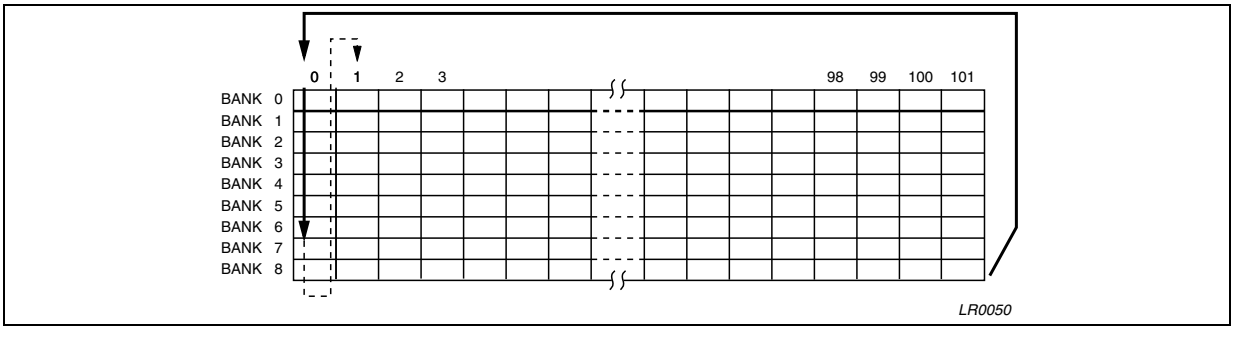


Figure 10. Automatic data RAM writing sequence with V=0 and Data RAM Mirrored Format (MX=1)[1]

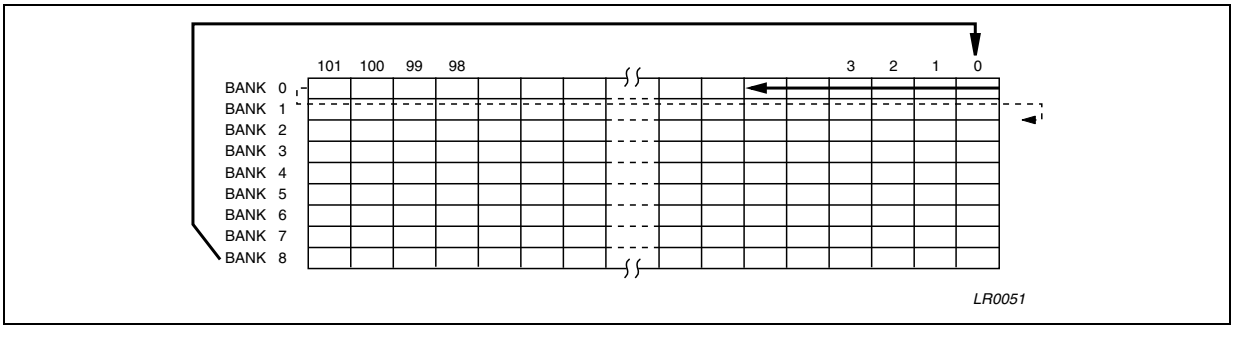
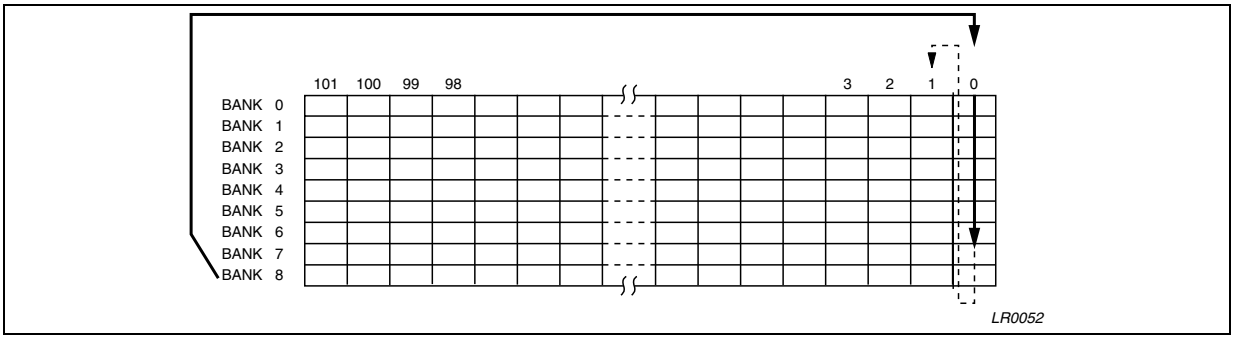


Figure 11. Automatic data RAM writing sequence with V=1 and Data RAM Mirrored Format (MX=1)[1]



1. X Carriage=101; Y-Carriage = 8

Figure 12. Automatic data RAM writing sequence with X-Y Carriage Return (V=0; MX=0)

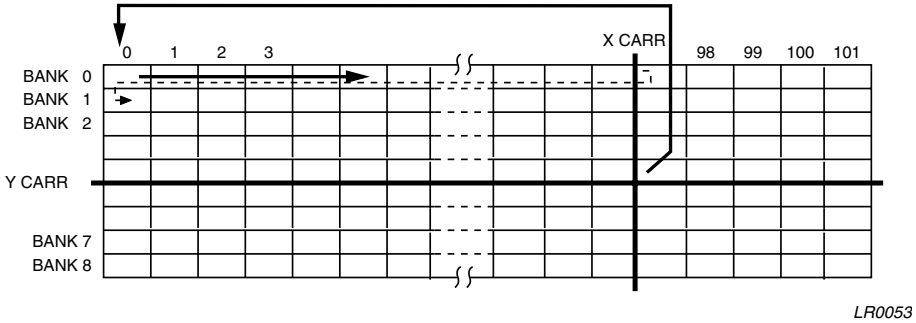


Figure 13. Automatic data RAM writing sequence with X-Y Carriage Return (V=1; MX=0)

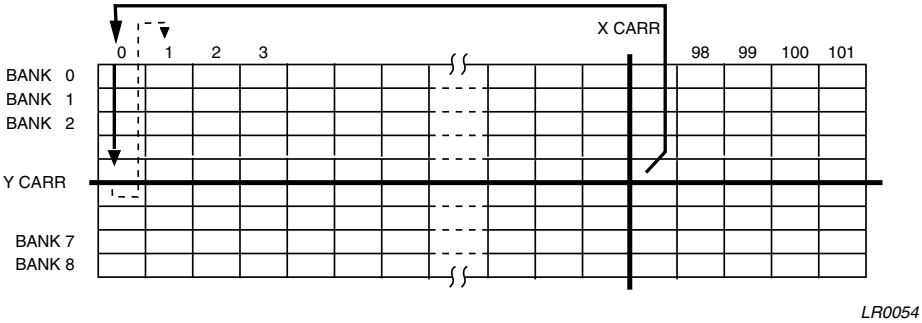


Figure 14. Automatic data RAM writing sequence with X-Y Carriage Return (V=0; MX=1)

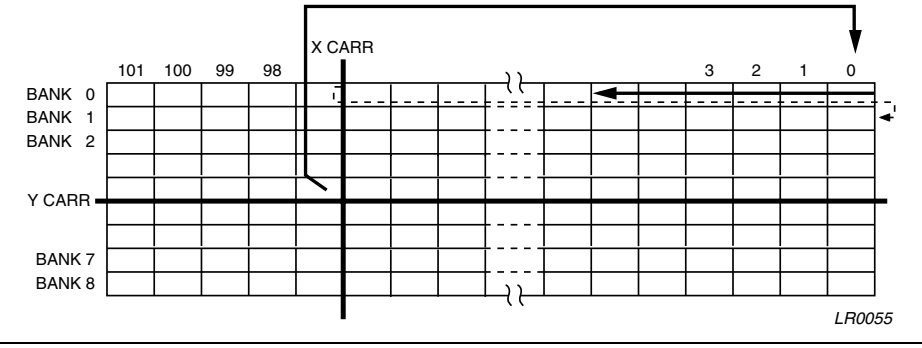


Figure 15. Automatic data RAM writing sequence with X-Y Carriage Return (V=1; MX=1)

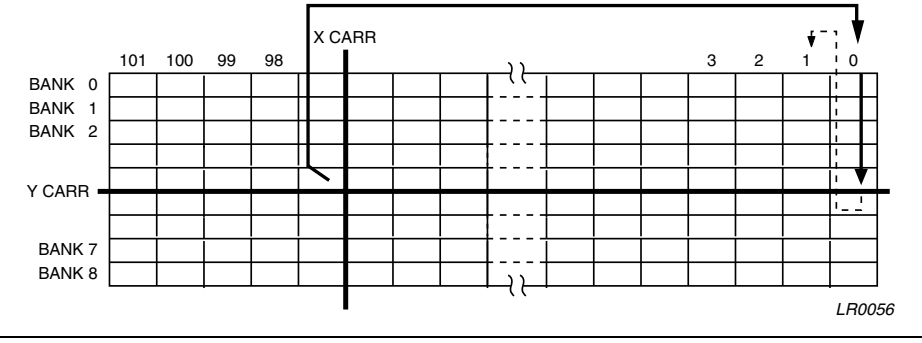


Figure 16. Data RAM Byte organization with D0 = 0

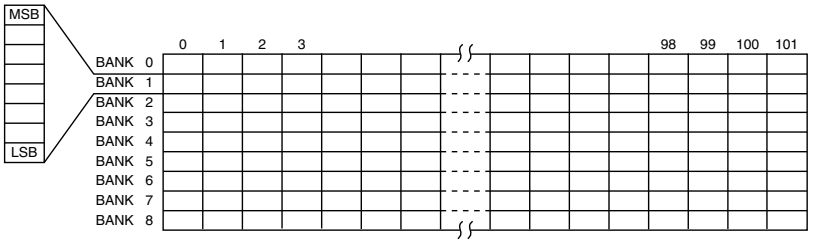


Figure 17. Data RAM Byte organization with D0 = 1

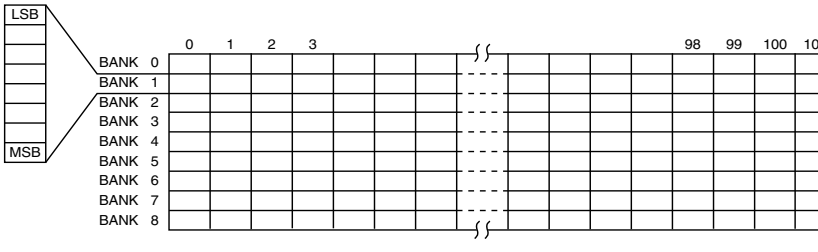


Figure 18. Memory Rows vs. Row Drivers Mapping ICON_MODE=1 and MUX 65

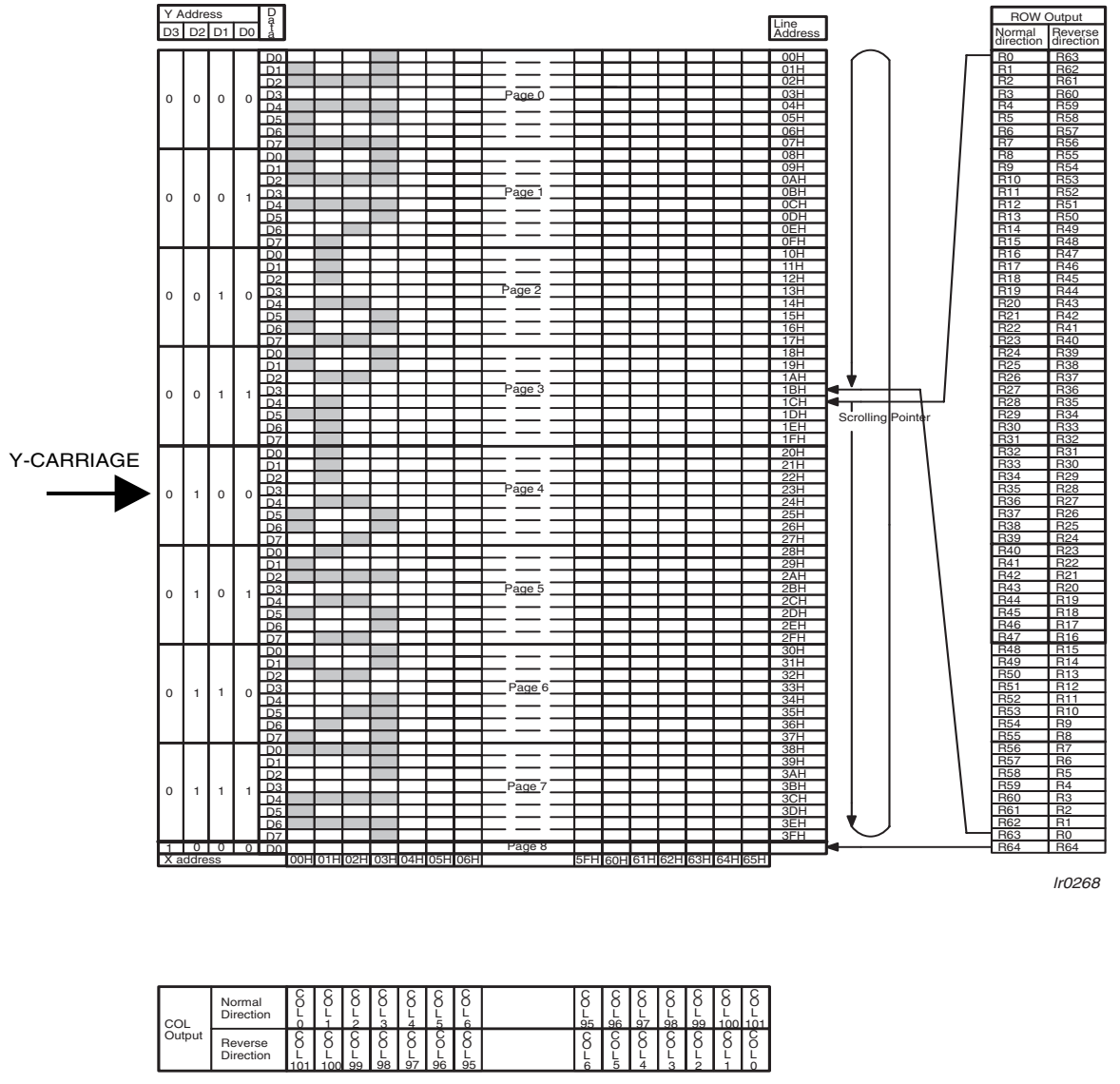


Figure 19. Memory Rows vs. Row Drivers Mapping ICON_MODE=0 and MUX 65

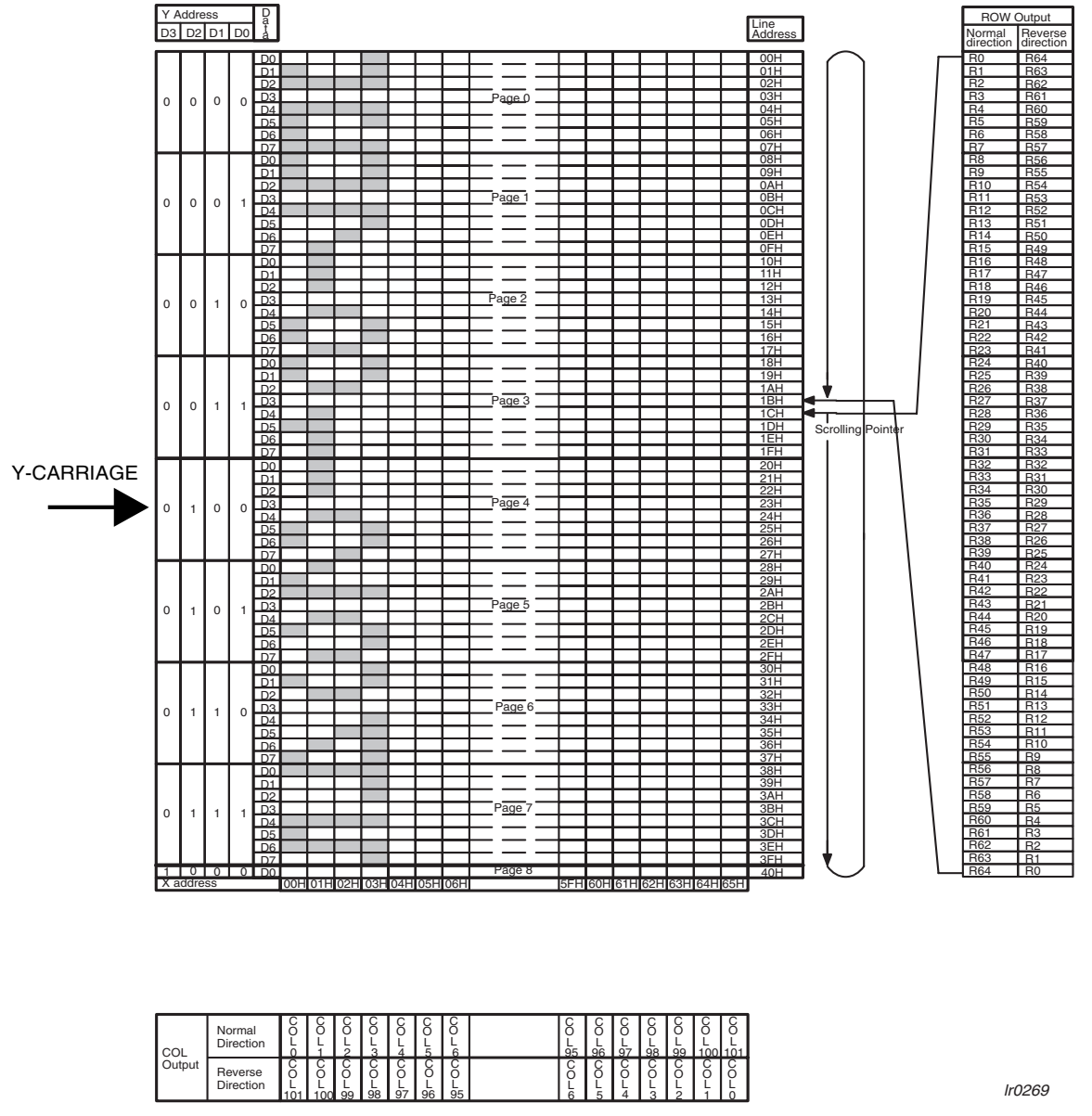


Figure 20. Memory Rows vs. Row Drivers Mapping ICON_MODE=1, Y-Carriage<=6 and MUX 49

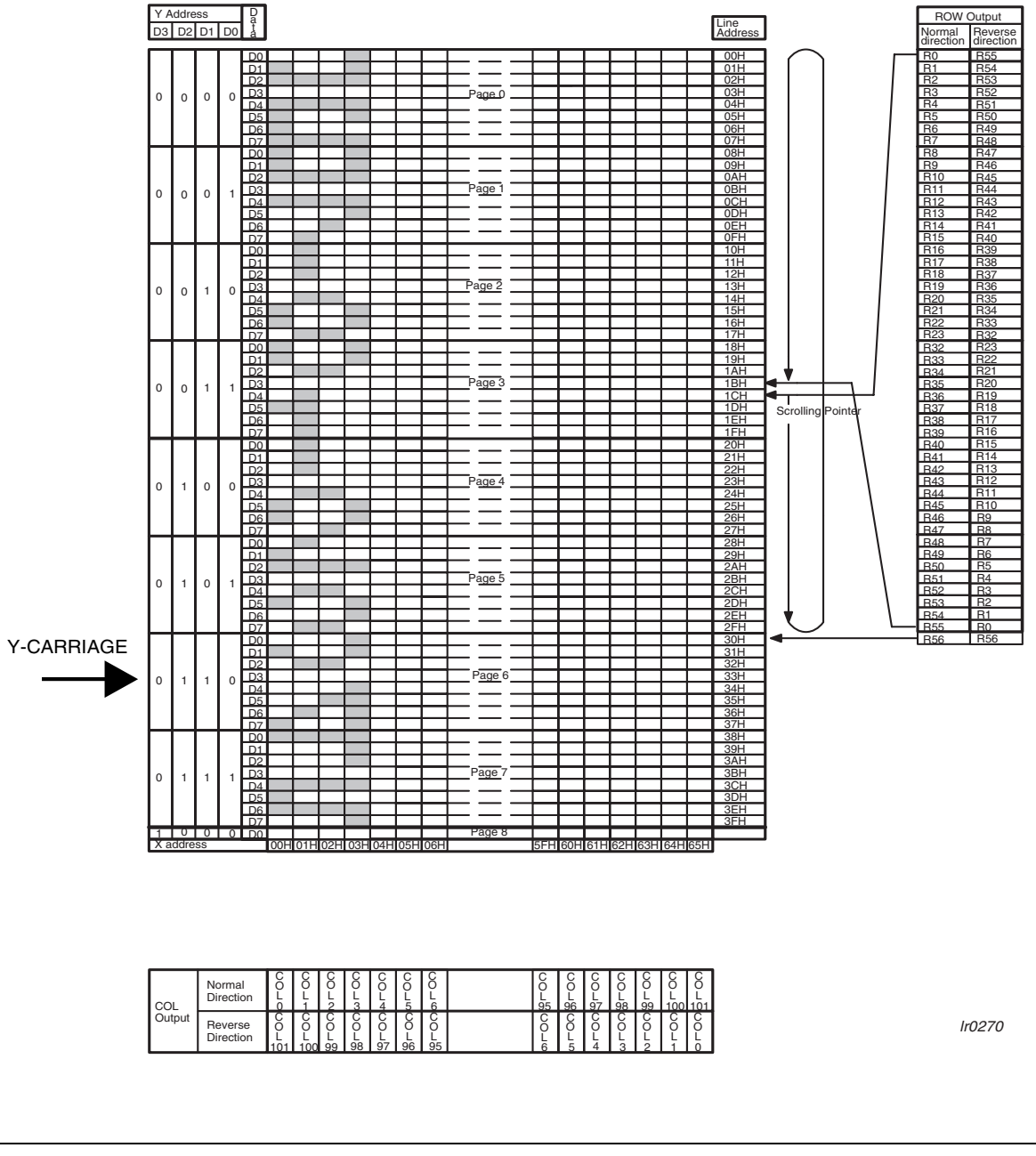


Figure 21. Memory Rows vs. Row Drivers Mapping ICON_MODE=0, Y-Carriage<=6 and MUX 49

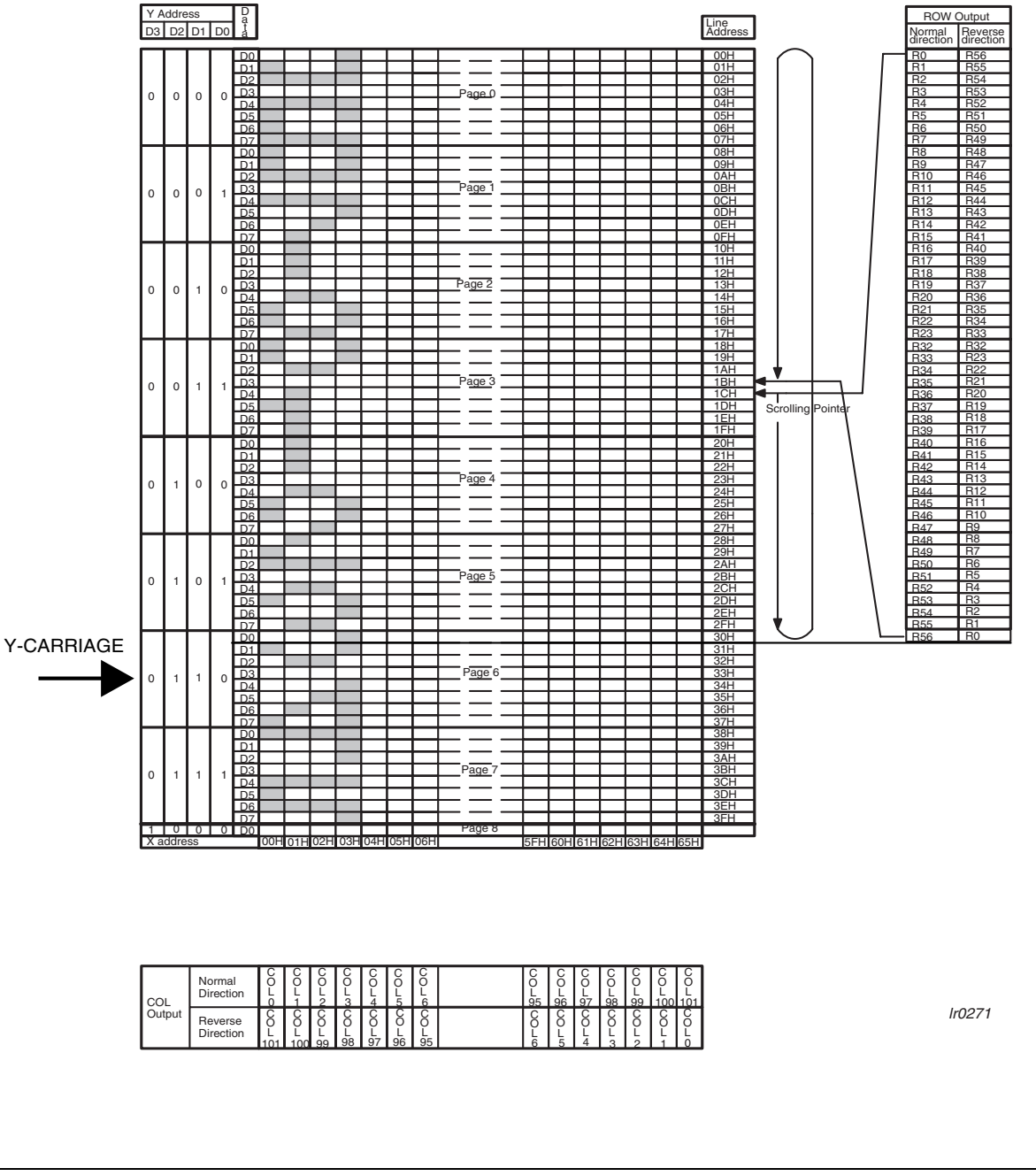


Figure 22. Memory Rows vs. Row Drivers Mapping ICON_MODE=0, Y-Carriage=7, Scrolling Pointer>07h and MUX 49

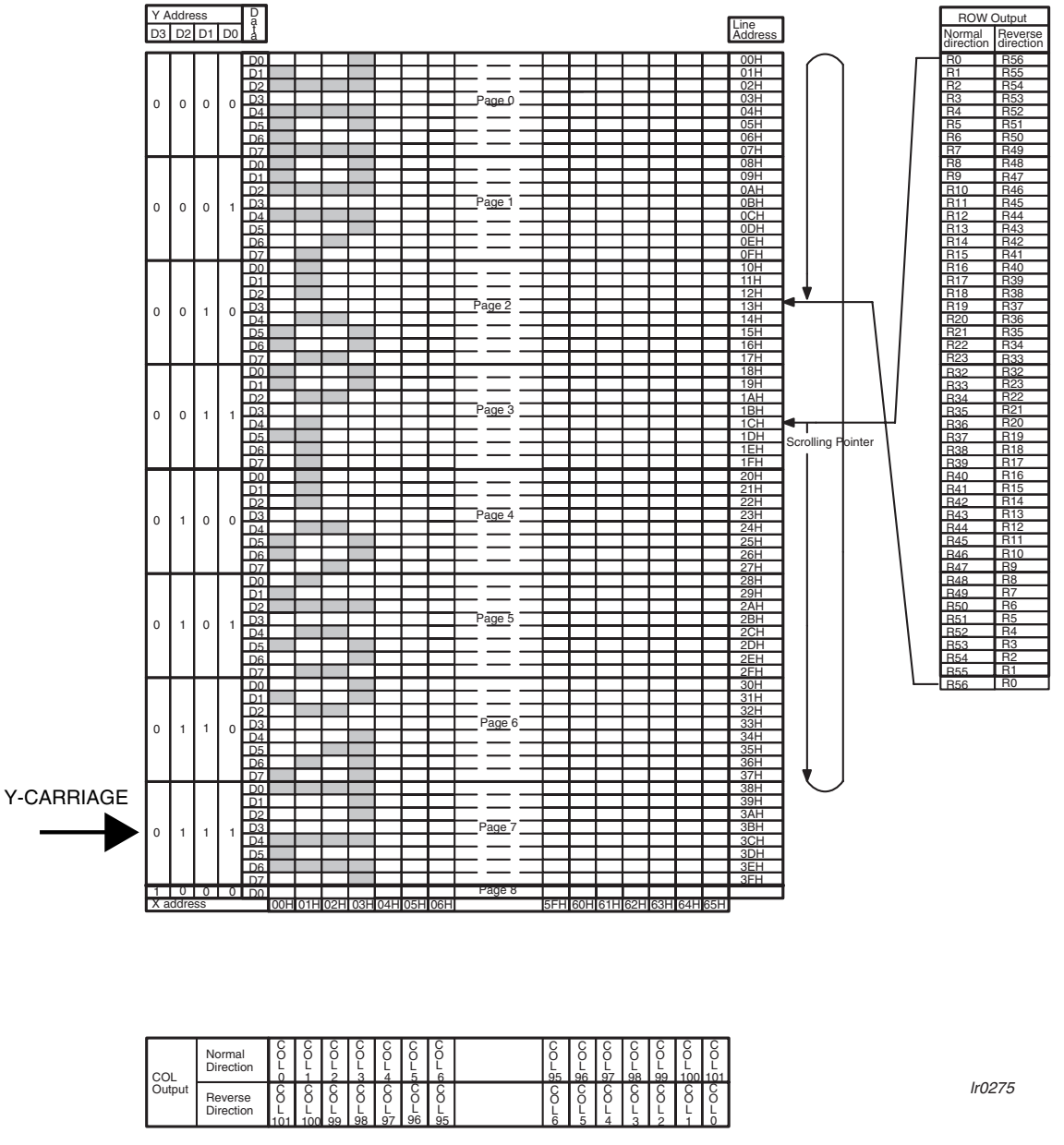


Figure 23. Memory Rows vs. Row Drivers Mapping ICON_MODE=1, Y-Carriage=7, Scrolling Pointer>07h and MUX 49

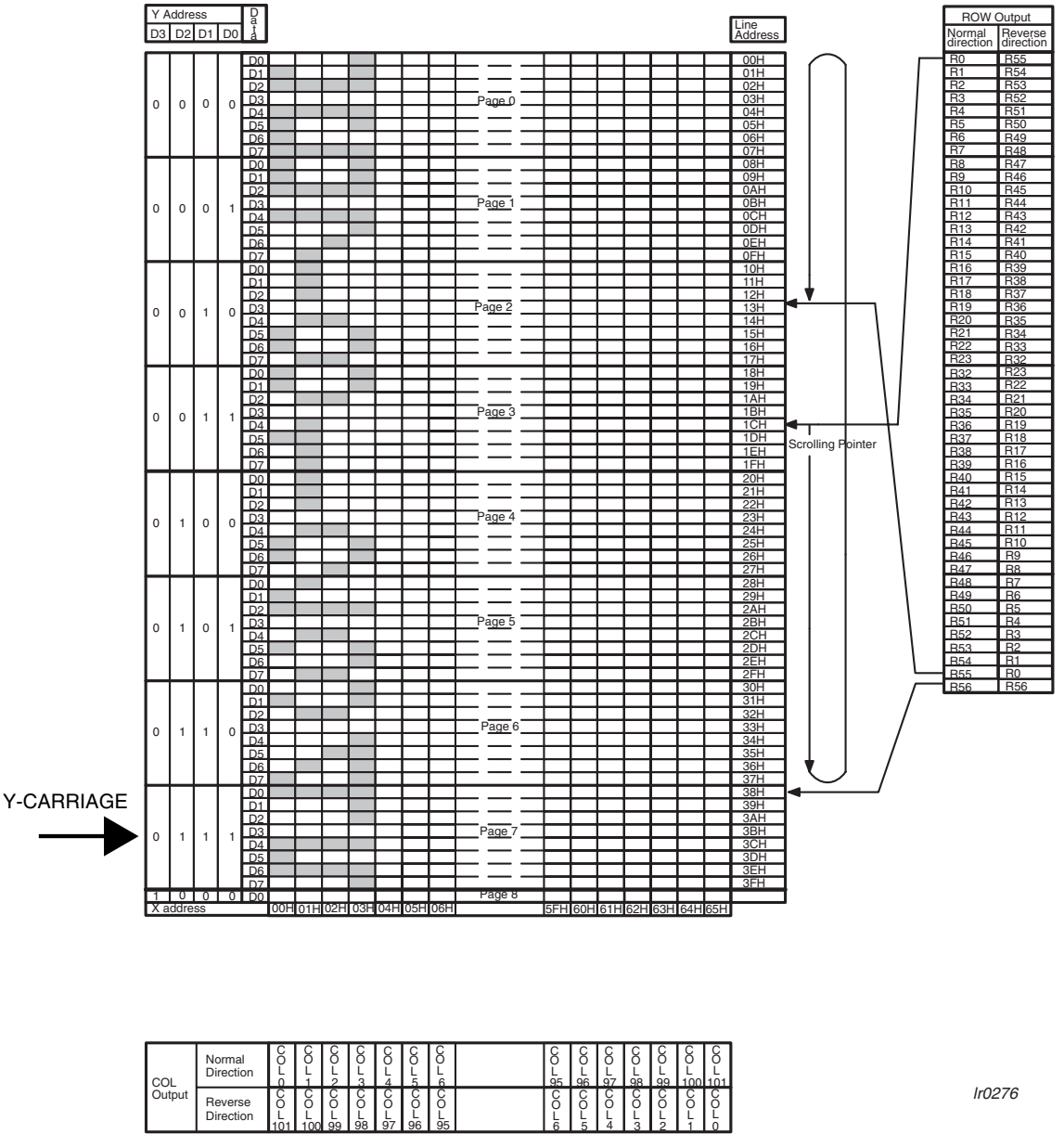


Figure 24. Memory Rows vs. Row Drivers Mapping ICON_MODE=1, Y-Carriage=8, Scrolling Pointer<10h and MUX 49

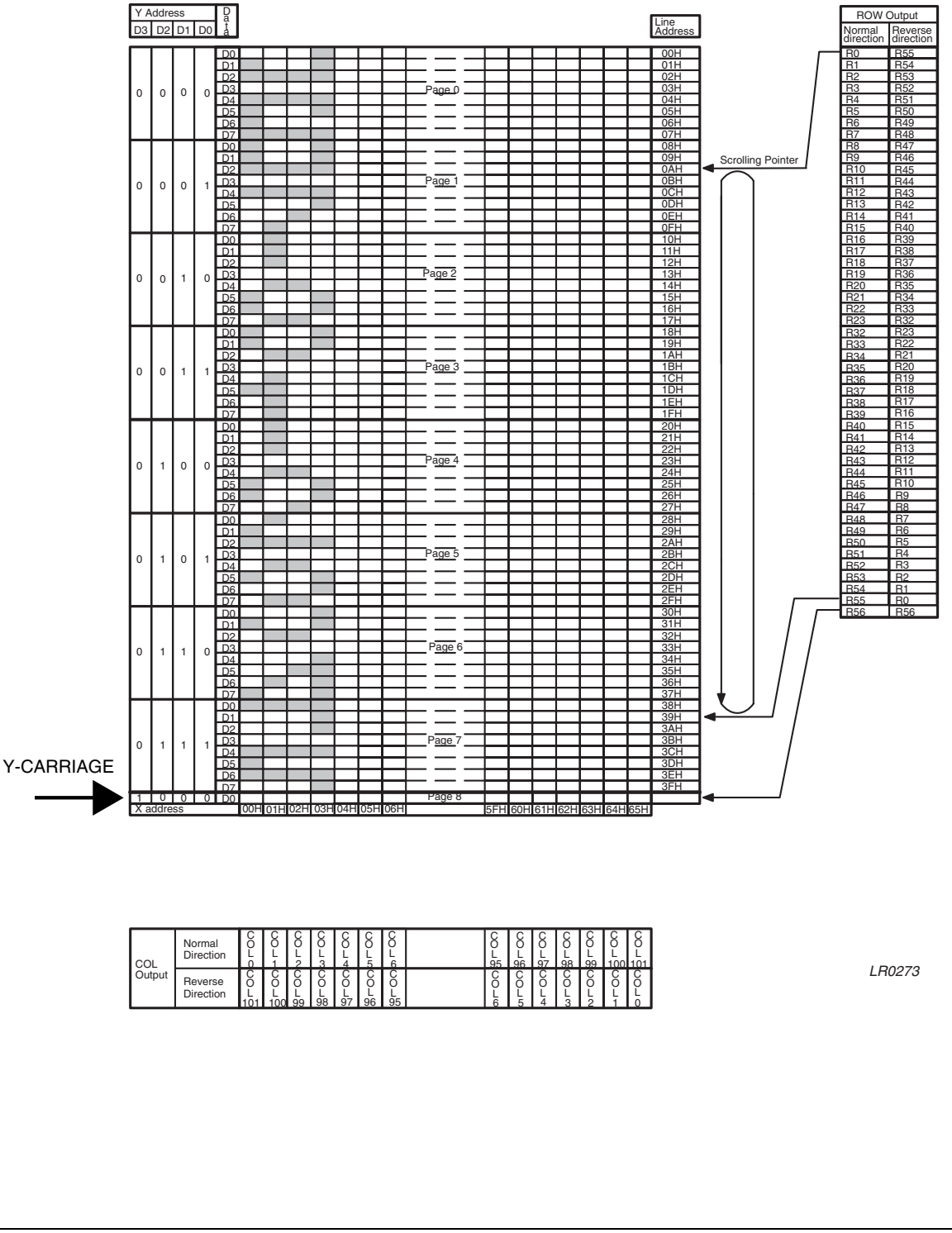


Figure 25. Memory Rows vs. Row Drivers Mapping ICON_MODE=0, Y-Carriage=8, Scrolling Pointer<10h and MUX 49

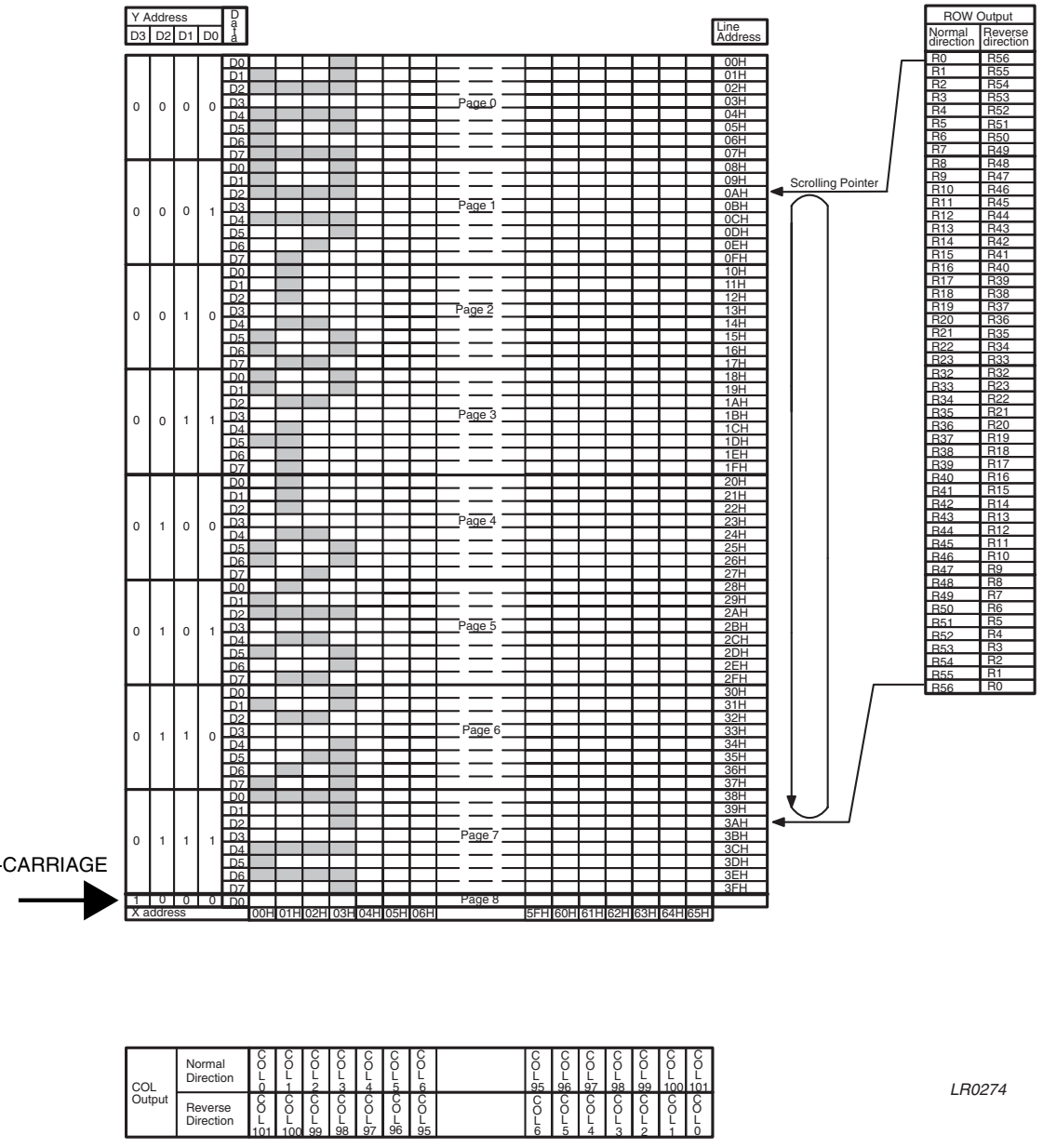


Figure 26. Memory Rows vs. Row Drivers Mapping ICON_MODE=1, Y-Carriage<=4 and MUX33

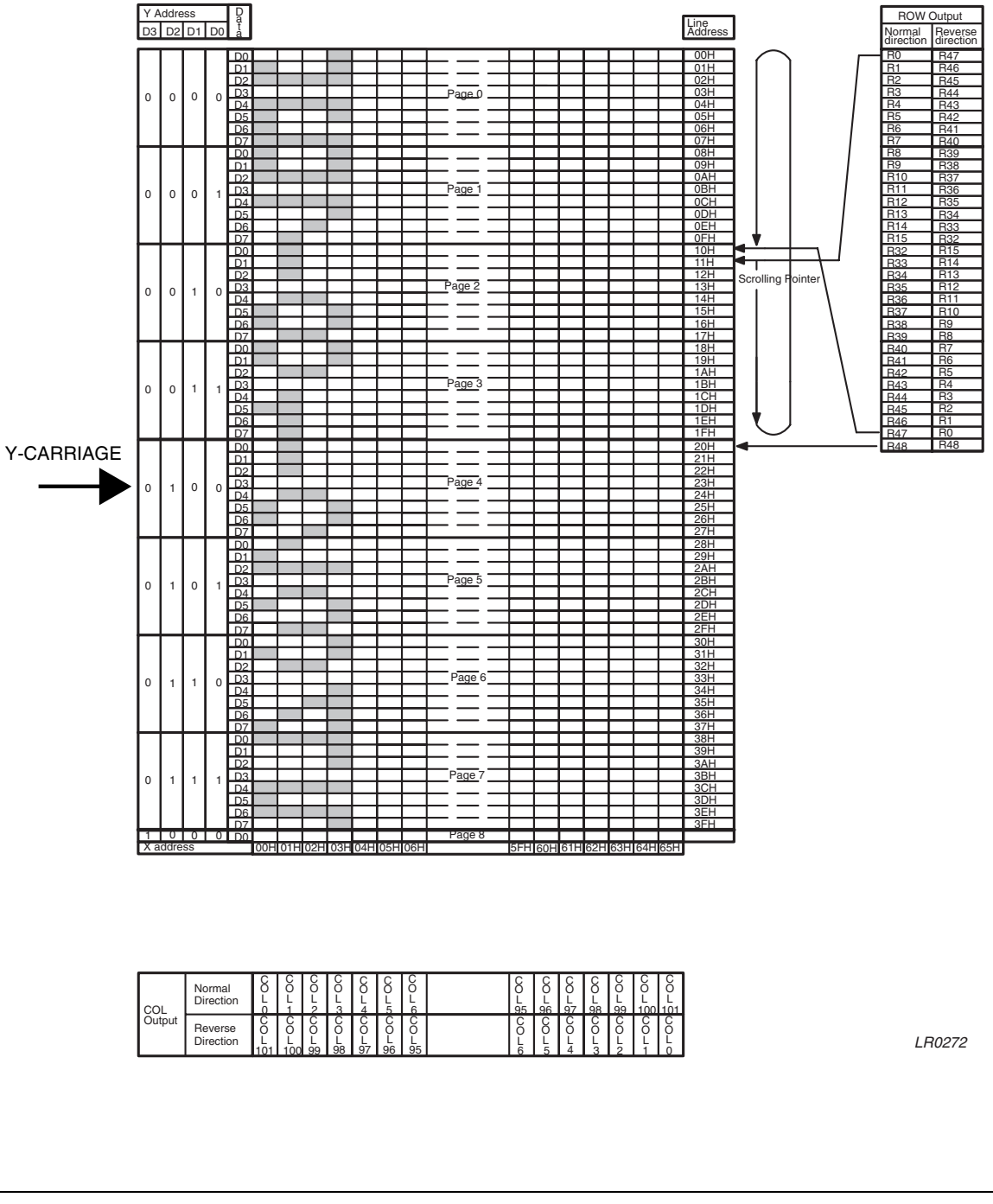


Figure 27. Memory Rows vs. Row Drivers Mapping ICON_MODE=0, Y-Carriage<=4 and MUX 33

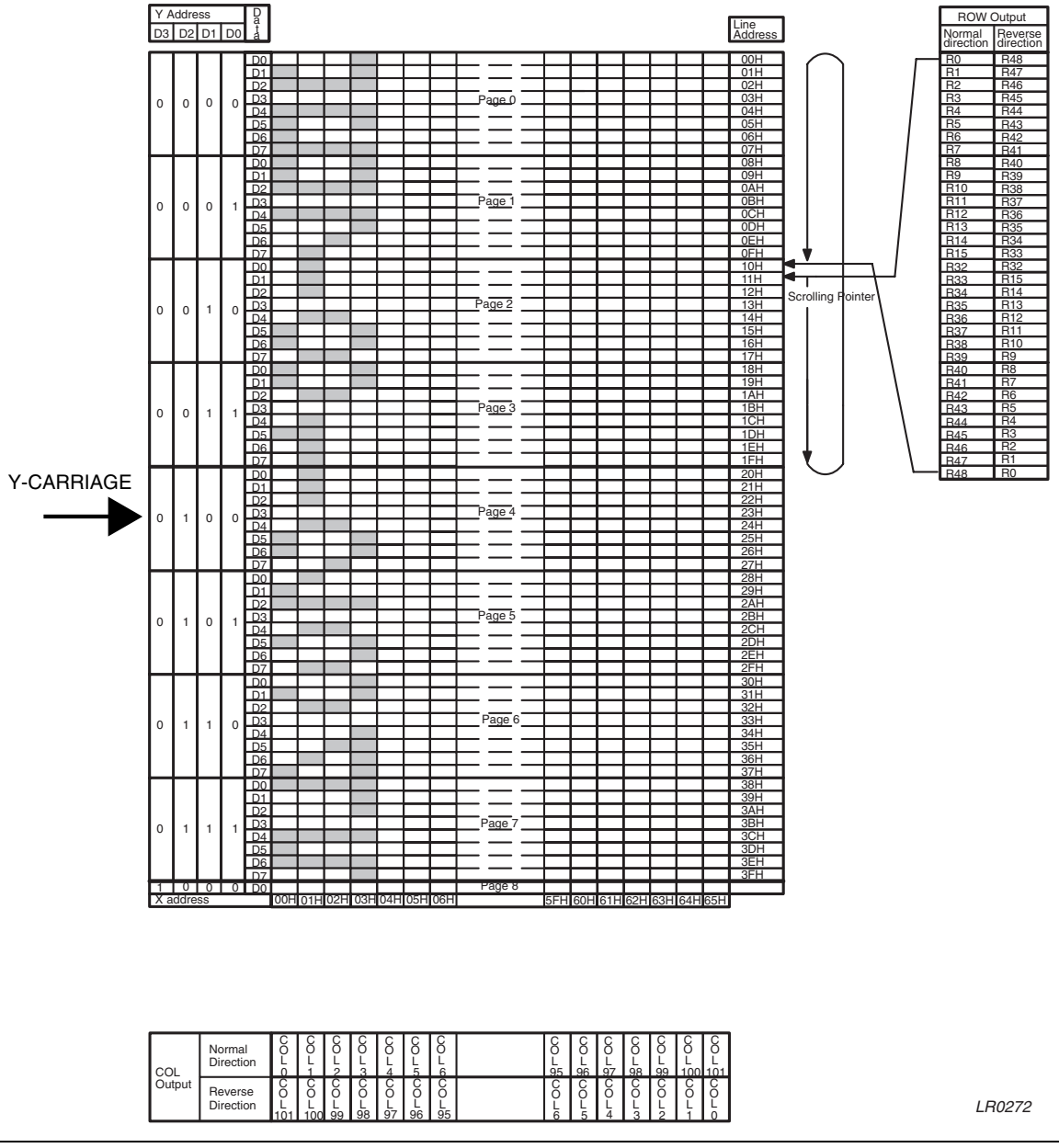


Figure 28. Row Drivers vs. LCD Panel Interconnection in MUX65 Mode

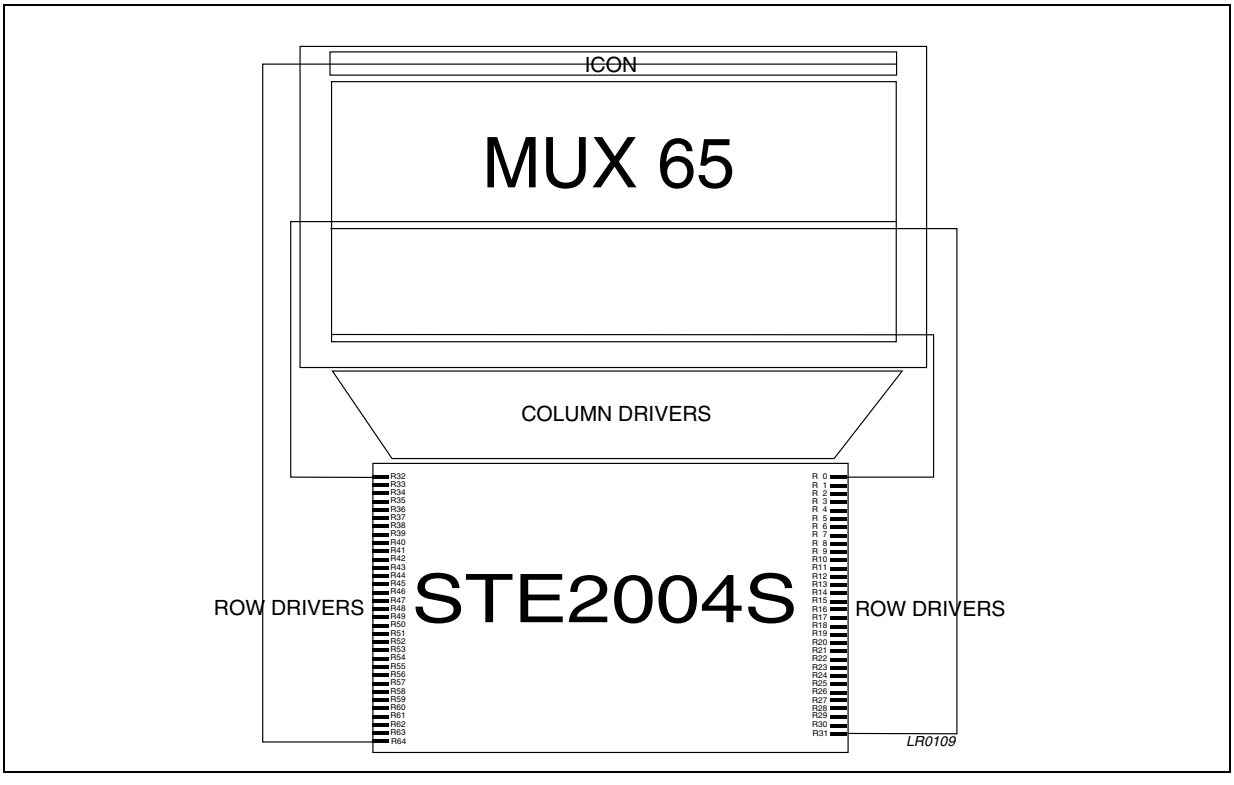


Figure 29. Row Drivers vs. LCD Panel Interconnection in MUX49 Mode

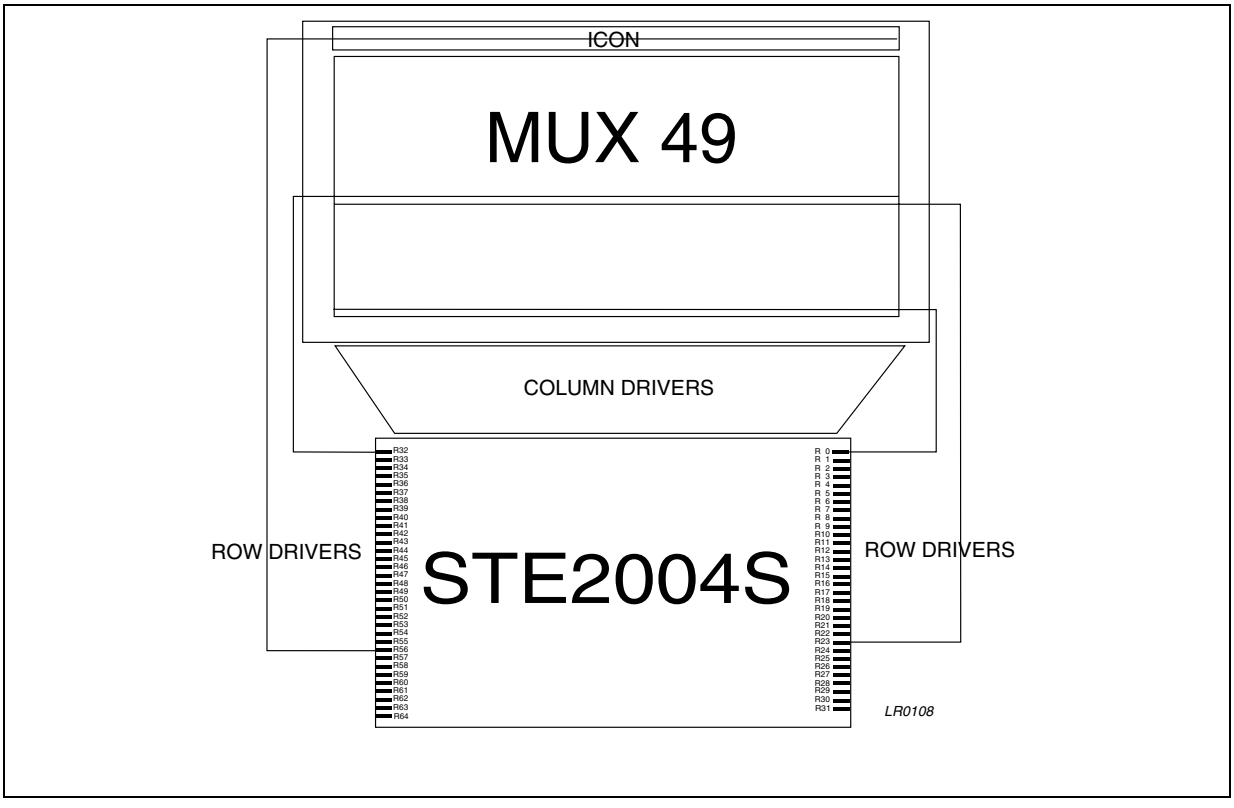
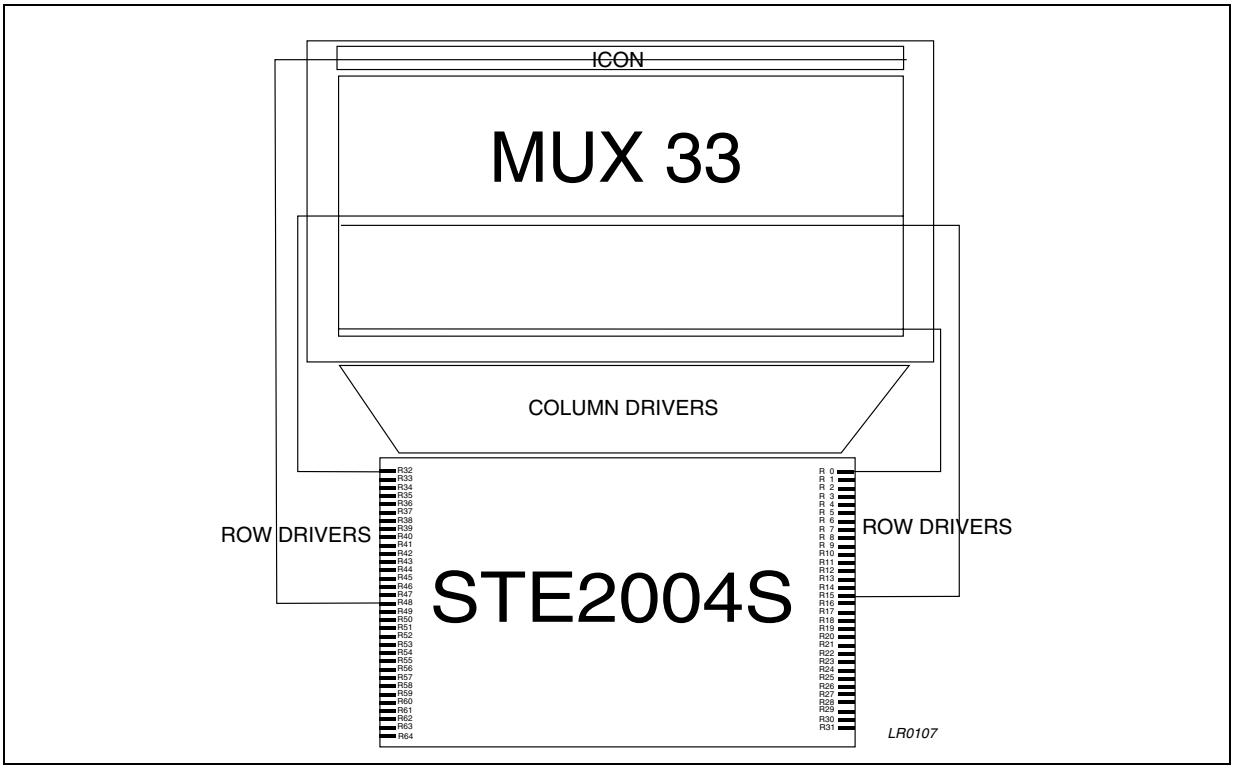


Figure 30. Row Drivers vs. LCD Panel Interconnection in MUX33 Mode



4 BUS INTERFACES

To provide the widest flexibility and ease of use the STE2004S features Six different methods for interfacing the host Controller. To select the desired interface the SEL1, SEL2 and SEL3 pads need to be connected to a logic LOW (connect to GND) or a logic HIGH (connect to VDD). All the I/O pins of the unused interfaces must be connected to GND.

All interfaces are working while the STE2004S is in Power Down.

Table 7.

SEL3	SEL2	SEL1	Interface	Note
0	0	0	I^2C	Read and Write; Fast and High Speed Mode
0	0	1	SPI 4 lines 8 bit	Read and Write
0	1	0	SPI 3 lines 8 bit	Read and Write
0	1	1	Serial 3 lines 9 bit	Read and Write
1	0	0	Parallel 8080-series	Read and Write
1	0	1	Parallel 68000-series	Read and Write

4.1 I^2C Interface

The I^2C interface is a fully complying I^2C bus specification, selectable to work in both Fast (400kHz Clock) and High Speed Mode (3.4MHz).

This bus is intended for communication between different Ics. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via an active or passive pull-up.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.

- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

BUS not busy: Both data and clock lines remain High.

Start Data Transfer: A change in the state of the data line, from High to Low, while the clock is High, define the START condition.

Stop Data Transfer: A Change in the state of the data line, from low to High, while the clock signal is High, defines the STOP condition.

Data Valid: The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and the stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with the ninth bit.

By definition, a device that gives out a message is called "transmitter", the receiving device that gets the signals is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves"

Acknowledge. Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA_IN line during the acknowledge clock pulse. Of course, setup and hold time must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line High to enable the master to generate the STOP condition.

Connecting SDA_IN and SDA_OUT together the SDA line become the standard data line. Having the acknowledge output (SDAOUT) separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDAOUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the STE2004S will not be able to create a valid logic 0 level. By splitting the SDA input from the output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDACK pad to the system SDA line to guarantee a valid LOW level.

To be compliant with the I^2C-bus Hs-mode specification the STE2004S is able to detect the special sequence "S00001xxx". After this sequence no acknowledge pulse is generated.

Since no internal modification are applied to work in Hs-mode, the device is able to work in Hs-mode without detecting the master code.

Figure 31. Bit transfer and START,STOP conditions definition

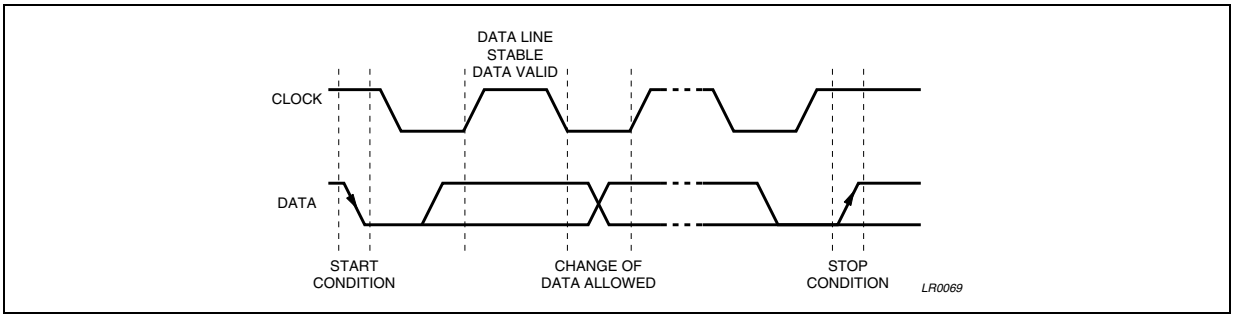
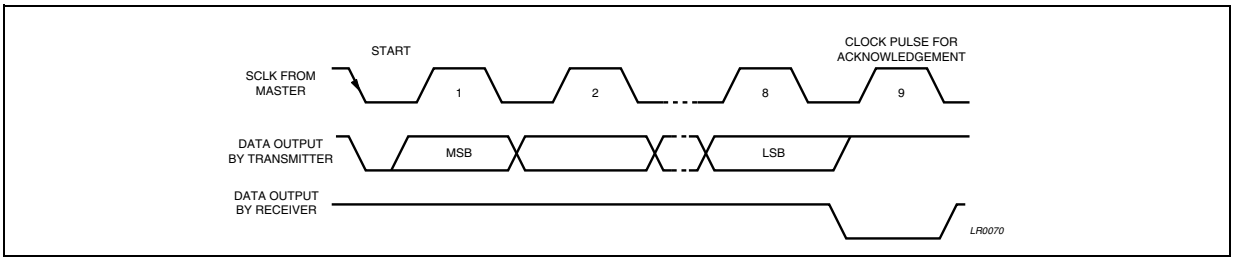


Figure 32. Acknowledgment on the I^2C-bus



4.1.1 Communication Protocol

The STE2004S is an I^2C slave. The access to the device is bi-directional since data write and status read are allowed.
Four are the device addresses available for the device. All have in common the first 5 bits (01111). The two least significant bit of the slave address are set by connecting the SA0 and SA1 inputs to a logic 0 or to a logic 1.
To start the communication between the bus master and the slave LCD driver, the master must initiate a START condition. Following this, the master sends an 8-bit byte, on the SDA bus line (Most significant bit first). This consists of the 7-bit Device select Code, and the 1-bit Read/Write Designator (R/$\overline{W}$).
All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I^2C-bus transfer.

4.1.1.1 Writing Mode.

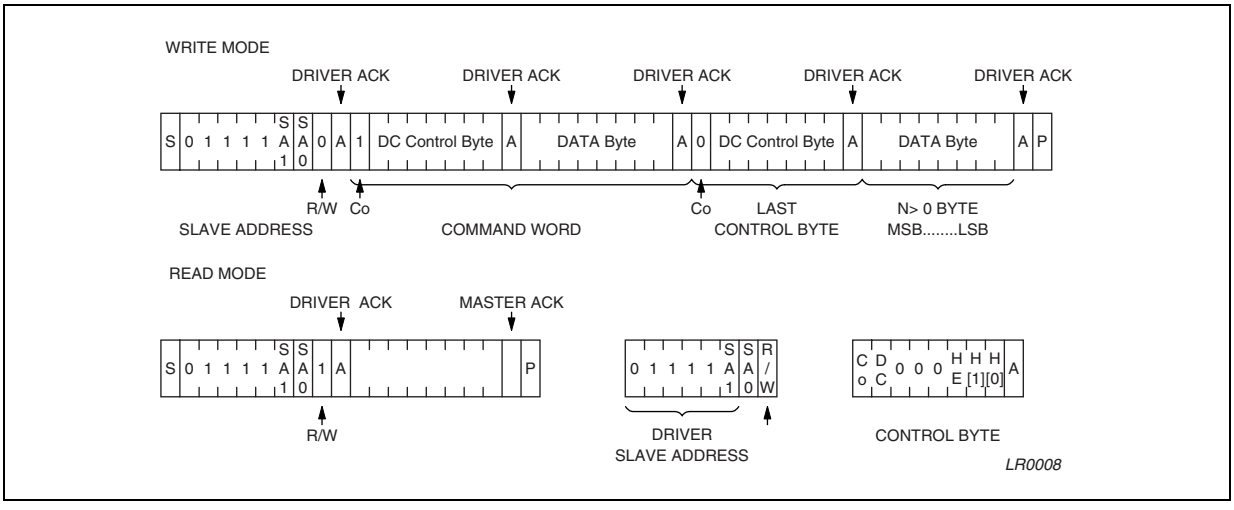
If the R/W bit is set to logic 0 the STE2004S is set to be a receiver. After the slaves acknowledge one or more command word follows to define the status of the device.
A command word is composed by three bytes. The first is a control byte which defines the Co and D/$\overline{C}$ values, the second and third are data bytes. The Co bit is the command MSB and defines if after this command will follow two data bytes and an other command word or if will follow a stream of data (Co = 1 Command word, Co = 0 Stream of data). The D/$\overline{C}$ bit defines whether the data byte is a command or RAM data (D/$\overline{C}$ = 1 RAM Data, D/$\overline{C}$ = 0 Command).
If Co =1 and D/$\overline{C}$ = 0 the incoming data byte is decoded as a command, and if Co =1 and D/$\overline{C}$ =1, the following data byte will be stored in the data RAM at the location specified by the data pointer.
Every byte of a command word must be acknowledged by all addressed units.
After the last control byte, if D/$\overline{C}$ is set to a logic 1 the incoming data bytes are stored inside the STE2004S Display RAM starting at the address specified by the data pointer. The data pointer is automatically updated after every byte written and in the end points to the last RAM location written.
Every byte must be acknowledged by all addressed units.

4.1.1.2 Reading Mode.

If the R/W bit is set to logic 1 the chip will output data immediately after the slave address. If the D/C bit

during the last write access, is set to a logic 0, the byte read is the status byte.

Figure 33. Communication Protocol



4.2 SERIAL INTERFACES

STE2004S can feature three different serial synchronized interfaces with the host controller. It is possible to select a 3-lines SPI, a 4-lines SPI or 3-line 9 bits Serial Interface.

4.2.1 4-lines SPI interface

STE2004S 4-lines serial interface is a bidirectional link between the display driver and the application supervisor.

It consists of four lines: one/two for data signals (SDIN, SOUT), one for clock signals (SCLK), one for the peripheral enable ($\overline{CS}$) and one for mode selection (SD/$\overline{C}$).

The serial interface is active only if the $\overline{CS}$ line is set to a logic 0. When $\overline{CS}$ line is high the serial peripheral power consumption is zero. While $\overline{CS}$ pin is high the serial interface is kept in reset.

The STE2004S is always a slave on the bus and receive the communication clock on the SCLK pin from the master.

Information are exchanged byte-wide. During data transfer, the data line is sampled on the positive SCLK edge.

SD/$\overline{C}$ line status indicates whether the byte is a command (SD/$\overline{C}$ =0) or a data (SD/$\overline{C}$ =1); SD/$\overline{C}$ line is read on the eighth SCLK clock pulse during every byte transfer.

If $\overline{CS}$ stays low after the last bit of a command/data byte, the serial interface expects the MSB of the next byte at the next SCLK positive edge.

A reset pulse on $\overline{RES}$ pin interrupts the transmission. No data is written into the data RAM and all the internal registers are cleared.

If $\overline{CS}$ is low after the positive edge of $\overline{RES}$, the serial interface is ready to receive data.

Throughout SDOUT can be read the driver I^2C slave address or the status byte. The Command sequence that allows to read I^2C slave address or Status byte is reported in Fig. 34 & 35. SDOUT is in High impedance in steady state and during data write.
It is possible to short circuit SDOUT and SDIN and read I2C address or status Byte without any additional lines.

Figure 34. 4-lines serial bus protocol - one byte transmission

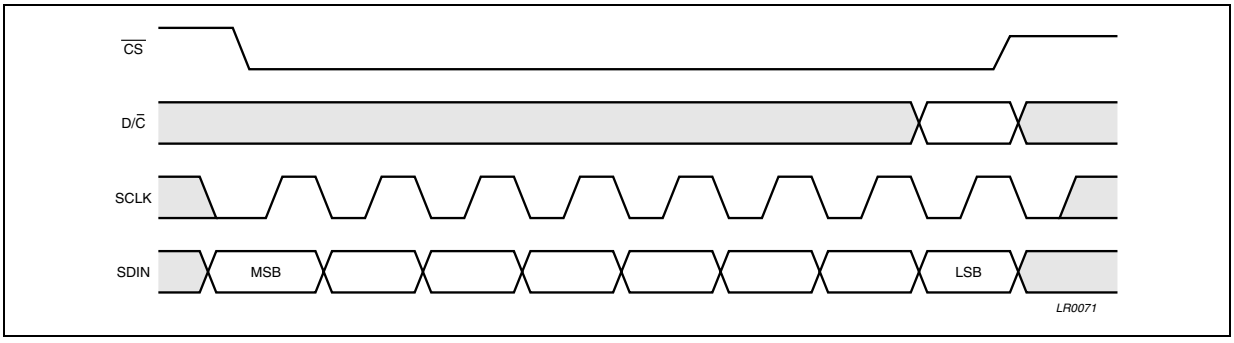


Figure 35. 4-lines serial bus protocol - several byte transmission

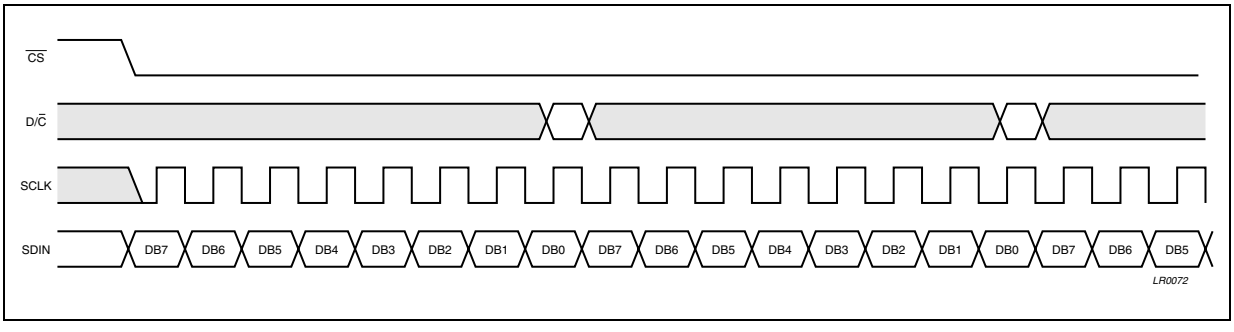


Figure 36. 4-lines serial bus protocol - I2C Address or Status Byte Read

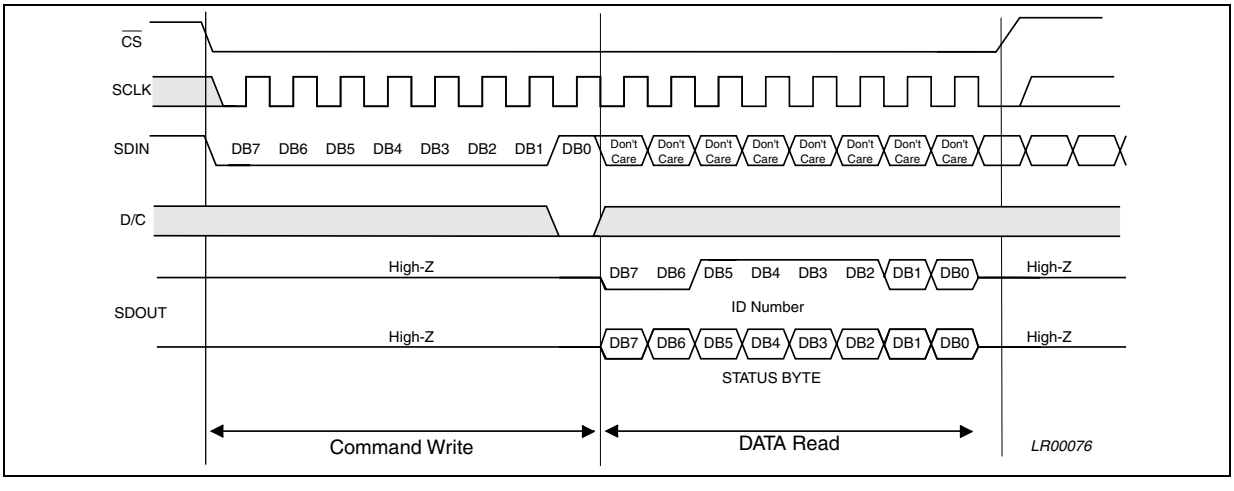
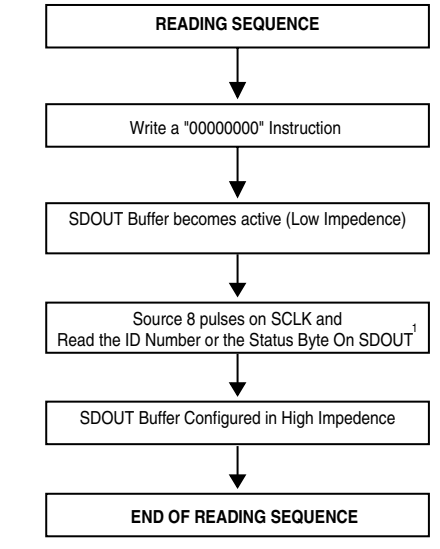


Figure 37. 4-lines SPI Reading Sequence



note: 1) these data are not read by the display Diver
2) SDIN and SDOUT can be short circuited if the processor can configure serial output buffers in high impedence during data read.

LR0078

4.2.2 3-lines SPI Interface

The STE2004S 3-lines serial Interface is a bidirectional link between the display driver and the application supervisor.
It consists of three lines: one/two for data signals (SDIN,SDOUT), one for clock signals (SCLK) and one for peripheral enable ($\overline{CS}$).
If the R/W bit is set to logic 0 the STE2004S is set to be a receiver. One or more command word follows to define the status of the device.
A command word is composed by two bytes. The first is a control byte which defines Co, D/$\overline{C}$, R/W H[1;0] and HE values, the second is a data byte (fig 39). The Co bit is the command MSB and defines if after this command will follow one data byte and an other command word or if will follow a stream of Commands or a Steam of DDRAM Data (Co = 1 Command word, Co = 0 Stream of data). The D/$\overline{C}$ bit defines whether the data byte is a command or DDRAM data (D/$\overline{C}$ = 1 RAM Data, D/$\overline{C}$ = 0 Command). The H[1;0] bits define the instruction Set Page if HE bit =1. If HE bit is set to 0 H[1;0] values are neglected and it is possible to update the instruction set page number using only the related instruction in the instruction Set.
If Co =1 and D/$\overline{C}$ = 0 the incoming data byte is decoded as a command, and if Co =1 and D/$\overline{C}$ =1, the following data byte will be stored in the data RAM at the location specified by the data pointer.
After the last control byte, if D/$\overline{C}$ is set to a logic 1 the incoming data bytes are stored inside the STE2004S Display Data RAM starting at the address specified by the data pointer. The data pointer is automatically updated after every byte written and in the end points to the last RAM location written.

Throughout SDOUT can be read the driver I^2C slave address or the status Byte. The Command sequence that allows to read I^2C slave address or the Status byte is reported in Fig. 39 & 40.

If the R bit is set to logic 0 and D/C=0, the I^2C slave address is read; If the R bit is set to logic 1 and D/C=0, the the I^2C slave address is read
SDOUT is in High impedance in steady state and during data write.
It is possible to short circuit SDOUT and SDIN and read I^2C address or status byte without any additional line.

Figure 38. 3-lines serial interface protocol in Writing Mode

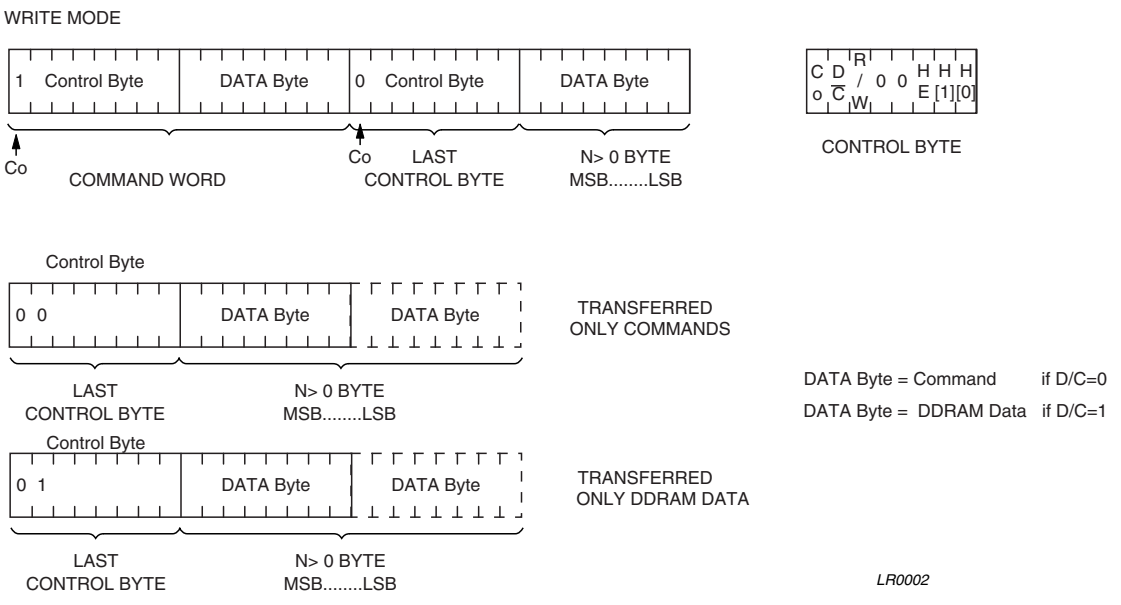


Figure 39. 3-lines SPI interface protocol in Reading Mode

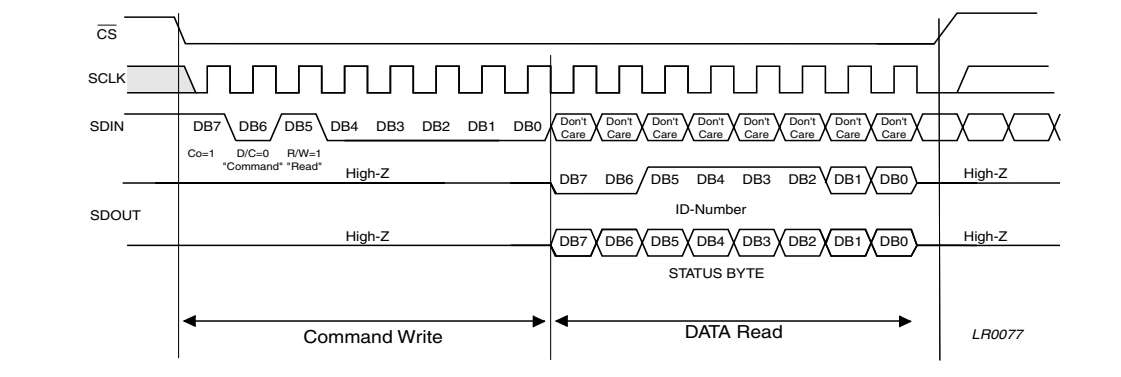
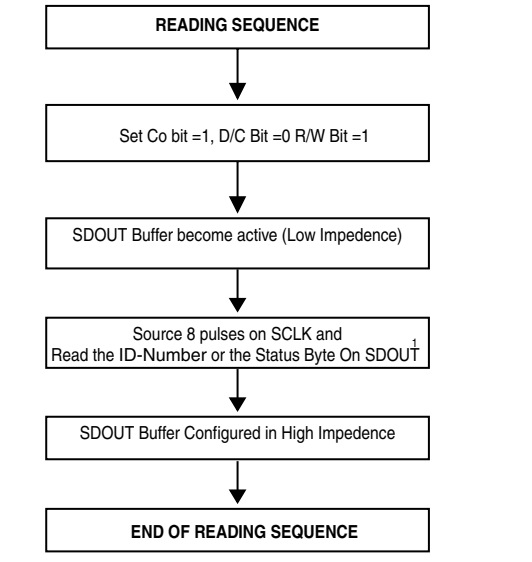


Figure 40. 3-lines SPI Reading Sequence



note: 1) these data are not read by the display Diver
2) SDIN and SDOUT can be short circuited if the processor can configure serial output buffers in high impedence during data read.

LR0079

4.2.3 3-lines 9 bits Serial Interface

The STE2004S 3-lines serial Interface is a bidirectional link between the display driver and the application supervisor.
It consists of three lines: one/two for data signals (SDIN, SDOUT), one for clock signals (SCLK) and one for peripheral enable ($\overline{CS}$).
The serial interface is active only if the $\overline{CS}$ line is set to a logic 0. When $\overline{CS}$ line is high the serial peripheral power consumption is zero. While $\overline{CS}$ pin is high the serial interface is kept in reset.
The STE2004S is always a slave on the bus and receive the communication clock on the SCLK pin from the master.
Information are exchanged word-wide. The word is composed by 9 bit. The first bit is named SD/$\overline{C}$ and indicates whether the following byte is a command (SD/$\overline{C}$ =0) or Data Byte (SD/$\overline{C}$ =1). During data transfer, the data line is sampled on the positive SCLK edge.
If $\overline{CS}$ stays low after the last bit of a command/data byte, the serial interface expects the SD/$\overline{C}$ Bit of the next word at the next SCLK positive edge.
A reset pulse on $\overline{RES}$ pin interrupts the transmission. No data is written into the data RAM and all the internal registers are cleared.
If $\overline{CS}$ is low after the positive edge of $\overline{RES}$, the serial interface is ready to receive data.
Throughout SDOUT can be read only the driver I^2C slave address or the status byte. The Command sequence that allows to read I^2C slave address or Status byte is reported in Fig. 43 & 44. SDOUT is in High impedance in steady state and during data write.
It is possible to short circuit SDOUT and SDIN and read I^2C address or status byte without any additional line.

Figure 41. 3-lines serial bus protocol - one byte transmission

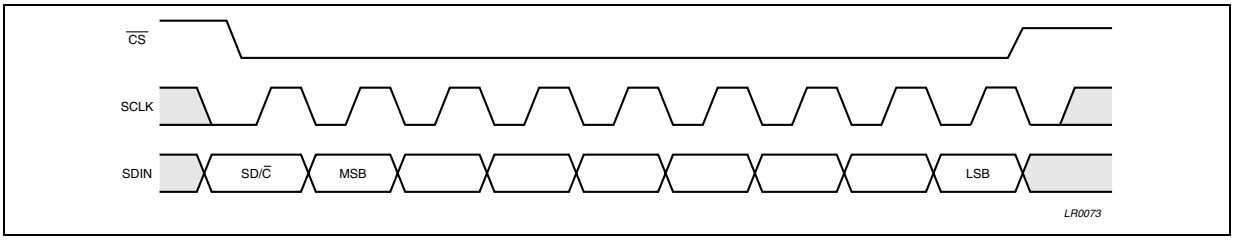


Figure 42. 3-lines serial bus protocol - several byte transmission

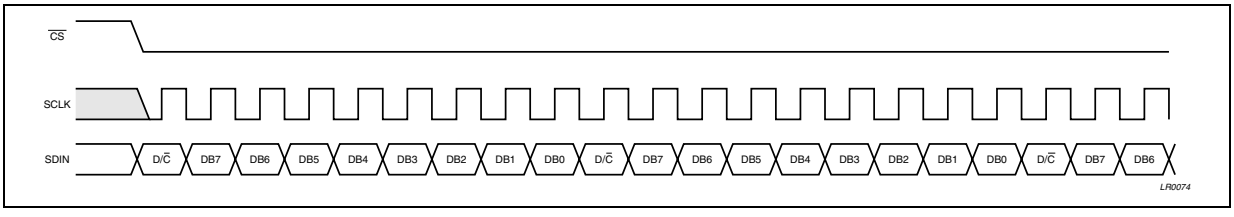


Figure 43. 3-lines serial interface protocol in Reading Mode

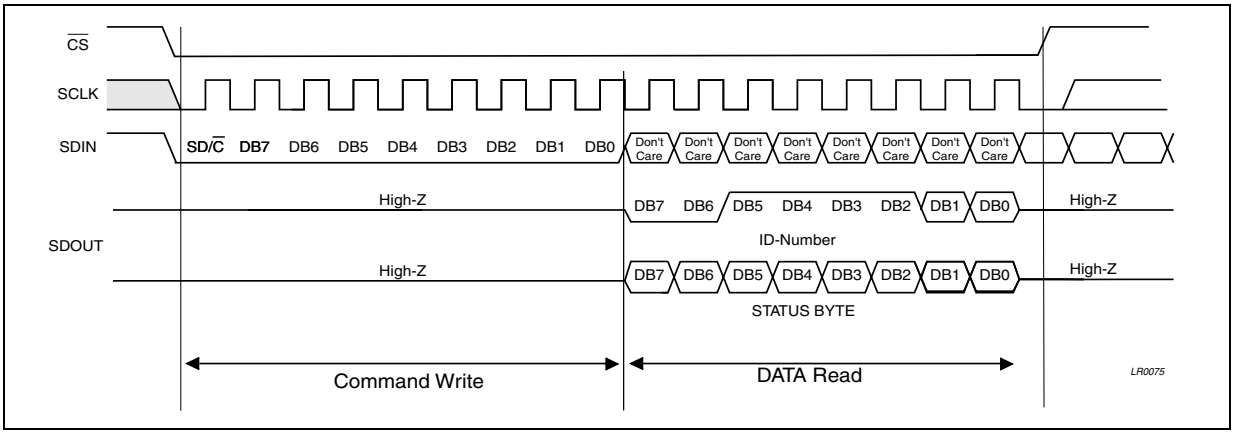
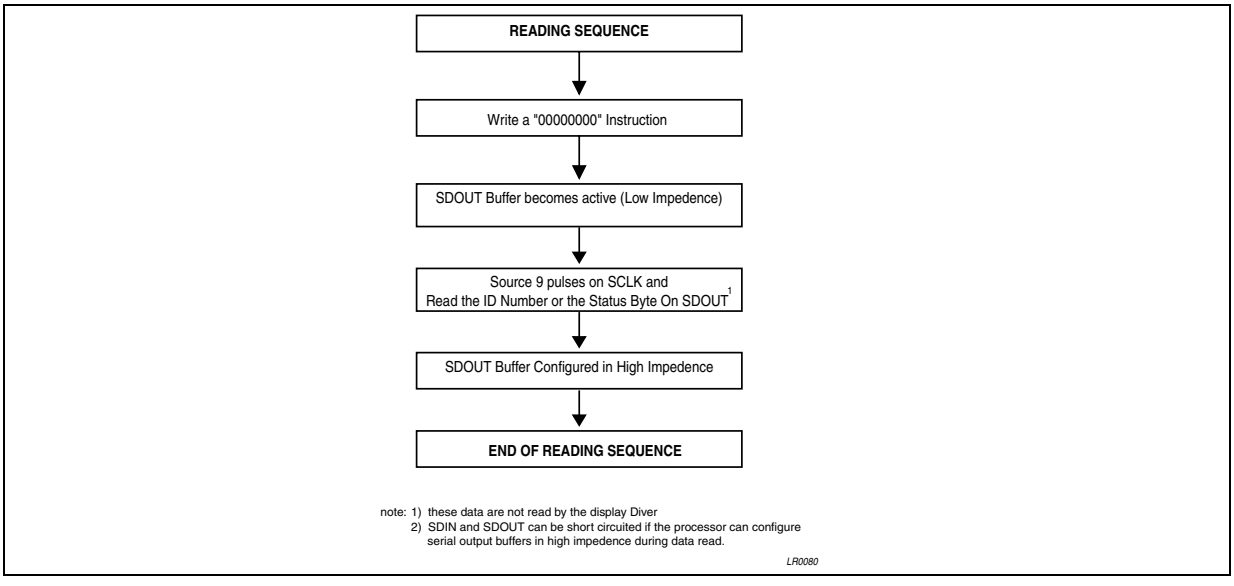


Figure 44. 3-lines Serial Reading Sequence



4.3 Parallel Interface

The STE2004S selectable parallel Interfaces are 68000-series and 8080-series. They are both an 8-bits bi-directional link between the display driver and the application supervisor.
Throughout both parallel interfaces can be read the I^2C driver slave address or the Status Byte.

4.3.1 68000-series parallel interface

If $\overline{CS}$ is low after the positive edge of $\overline{RES}$, the 68000 parallel interface is ready to receive or transmit data.

While $\overline{CS}$ pin is high the 68000 Parallel interface is kept in reset.

4.3.1.1 Write Mode

If R/W line is set to 0 Data are latched on E falling edge.

4.3.1.2 Read Mode

When R/W line is set to 1, data are output on D0-D7 bus on E rising edge. Data Bus is set in high impedance mode when E is set to logic 0.

Accordingly to R bit value I2C Address or Status Byte is output on D0-D7 bus.

Figure 45. 68000-series Parallel interface protocol - one byte transmission

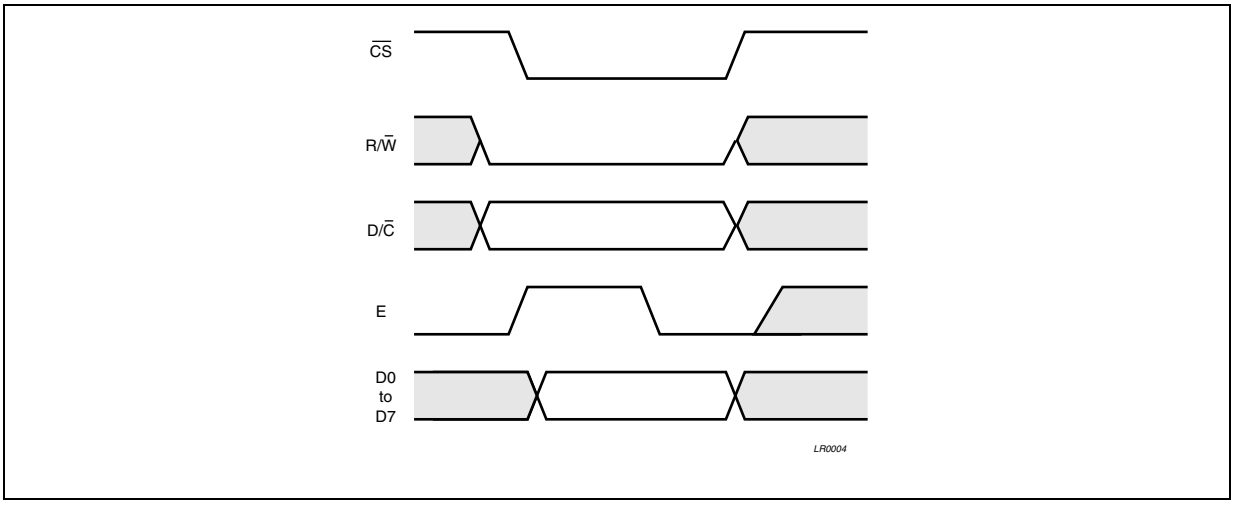


Figure 46. 68000-series Parallel interface bus protocol - Several bytes transmission

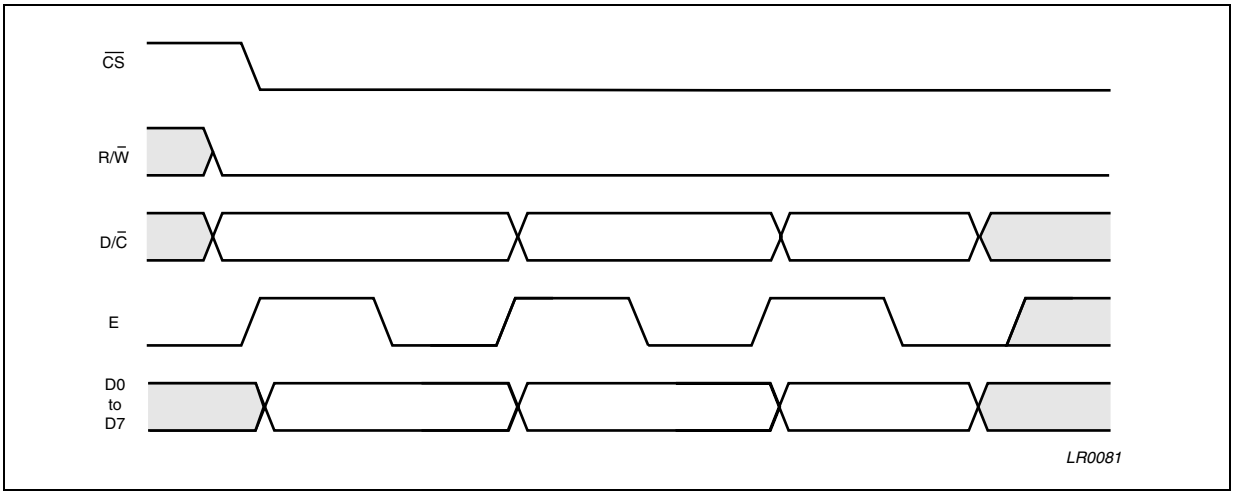


Figure 47. 68000-series Parallel interface protocol in Reading Mode

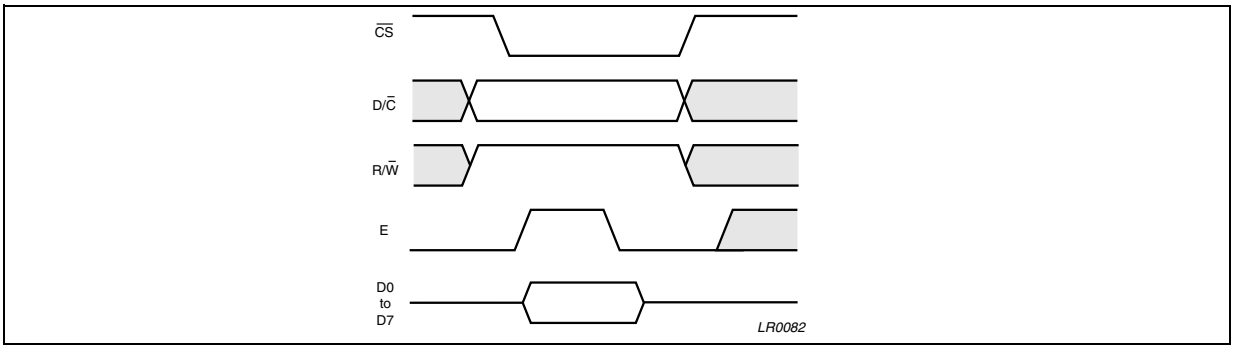
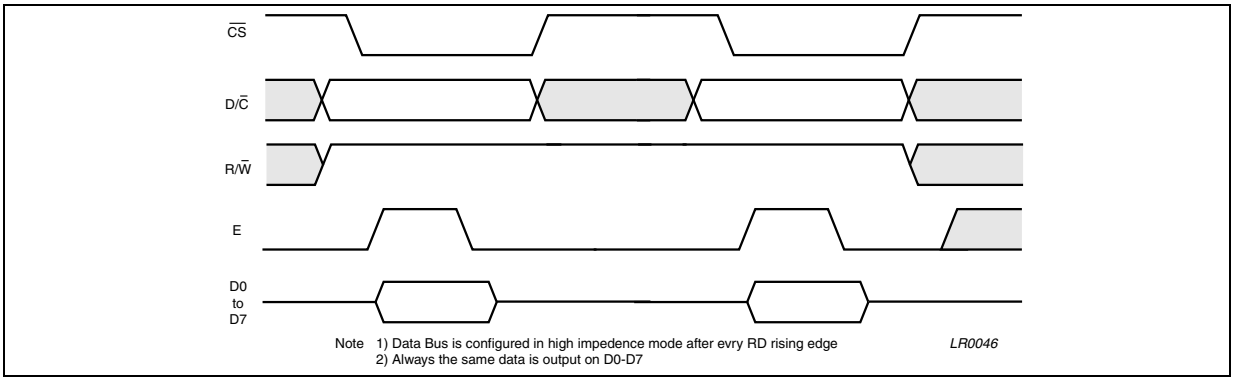


Figure 48. 68000-series Parallel interface protocol in Reading Mode (Several Bytes)



4.3.2 8080-series parallel interface

If $\overline{CS}$ is low after the positive edge of $\overline{RES}$, the 8080 parallel interface is ready to receive or transmit data.

While $\overline{CS}$ pin is high the 8080 Parallel interface is kept in reset.

4.3.2.1 Write Mode

Data are latched on WR rising edge.

4.3.2.2 Read Mode

Data are output on D0-D7 bus on RD rising edge. Data Bus is set in high impedance mode when RD is set to logic 1.

Accordingly to R bit value I2C Address or Status Byte is output on D0-D7 bus.

Figure 49. 8080-series parallel bus protocol - one byte transmission

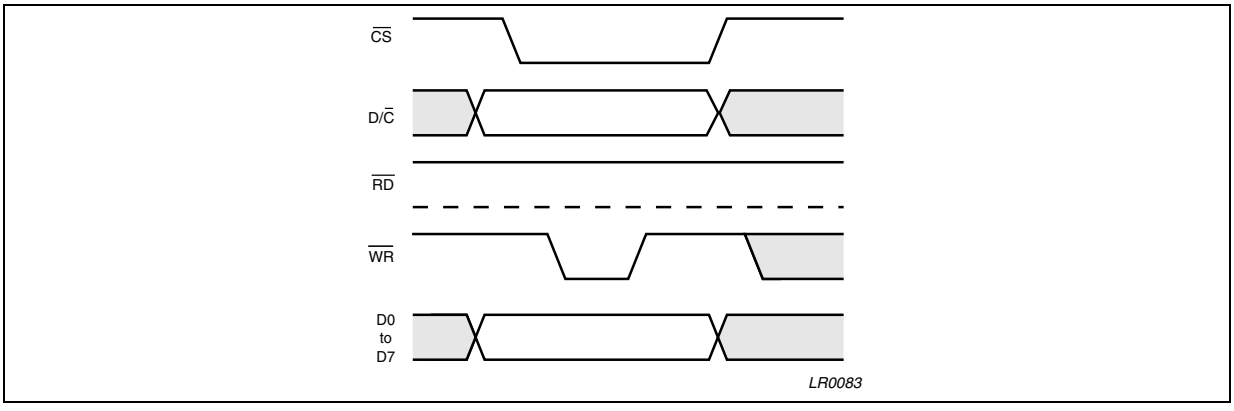


Figure 50. 8080-series parallel bus protocol - several bytes transmission

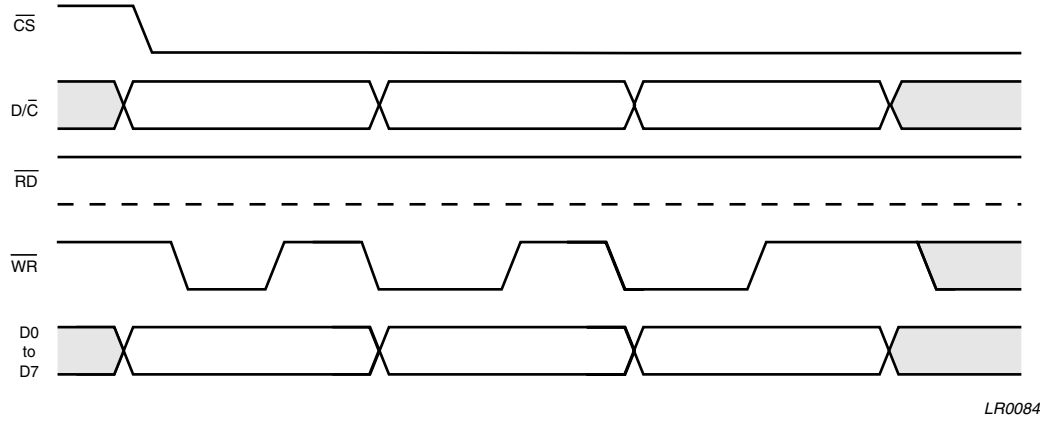


Figure 51. 8080-series Parallel interface protocol in Reading Mode

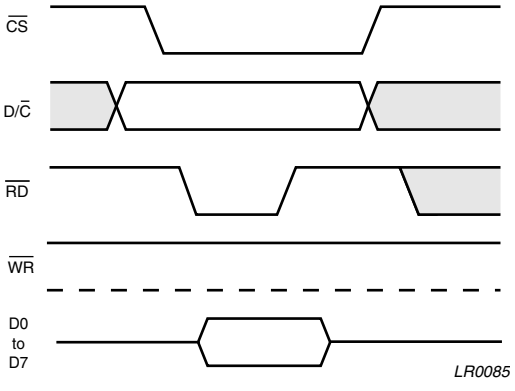
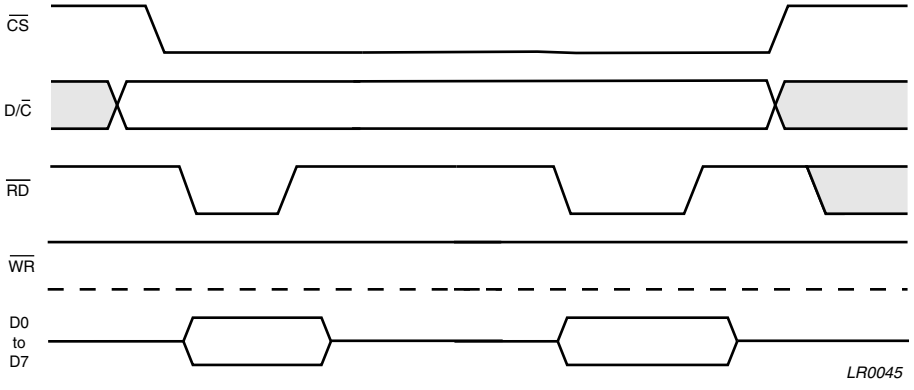


Figure 52. 8080-series Parallel interface protocol in Reading Mode (Several Bytes)



Note 1) Data Bus is configured in high impedence mode after every RD rising edge
2) Always the same data is output on D0-D7

5 INSTRUCTION SET

Two different instructions formats are provided:
- With D/$\overline{C}$ set to LOW : commands are sent to the Control circuitry.
- With D/$\overline{C}$ set to HIGH : the Data RAM is addressed.

Two different instruction set are embedded: the STE2001-like instruction set and the extended instruction set. To select the STE2001-like instruction set the EXT pad has to be connected to a logic LOW (connect to GND). To select the he extended instruction the EXT pad has to be connected to a logic HIGH (connect to VDD1).

The instructions have the syntax summarized in Table 1 (basic-set) and Table 2 (extended set)

5.1 Reset (RES)

At power-on, all internal registers are configured with the default value. The RAM content is not defined. A Reset pulse on RES pad (active low) re-initialize the internal registers content (see Tables 3,4,5,&6). Every on-going communication with the host controller is interrupted, applying a reset pulse. After the power-on, the Software Reset instruction can be used to re-load the reset configuration into the internal registers.

The Default configurations is:

- Horizontal addressing (V = 0)
- Normal instruction set (H[1:0] = 0)
- Normal display (MX = MY = 0)
- Display blank (E = D = 0)
- Address counter X[6: 0] = 0 and Y[4: 0] = 0
- Temperature coefficient (TC[1: 0] = 0)
- Bias system (BS[2: 0] = 0)
- Multiplexing Ratio (M[1:0]=0 - MUX 65)
- Frame Rate (FR[1:0]=”75Hz”)
- Power Down (PD = 1)
- Dual Partial Display Disabled (PE=0)
- V_{OP}=0
- Y-CARRIAGE=8
- X-CARRIAGE=101

A MEMORY BLANK instruction can be executed to clear the DDRAM content.

5.2 Power Down (PD = 1)

When at Power Down, all LCD outputs are kept at V_{SS} (display off). Bias generator and V_{LCD} generator are OFF (V_{LCDOUT} output is discharged to V_{SS}, and then is possible to disconnect V_{LCDOUT}). The internal Oscillator is in off state. An external clock can be provided. The RAM contents is not cleared.

5.3 Memory Blanking Procedure

This instruction allows to fill the memory with "blank" patterns, in order to delete patterns randomly generated in memory when starting up the device. This instruction substitutes (102X8) single "write" instructions. It is possible to program "Memory Blanking Procedure" only under the following conditions:

- PD bit = 0

No instruction can be programmed for a period equivalent to 102X8 internal write cycles (102X8X1/fclock). The start of Memory blanking procedure will be between one and two fclock cycles from the last active edge (E fallig edge for the parallel interface, last SCLK rising edge for the Serial & SPI interfaces, last SCL rising edge for the I^2C interface).

5.4 Checker Board Procedure

This instruction allows to fill the memory with "checker-board" pattern. It is mainly intended to developers, who can now simply obtain complex module test configuration by means of a single instruction. It is possible to program "Checker Board Procedure" only under the following conditions:

- PD bit = 0

No instruction can be programmed for a period equivalent to 102X8 internal write cycles (102X8X1/fclock). The start of Checker-board procedure will be between one and two fclock cycles from the last active edge (E falling edge for the parallel interface, last SCLK rising edge for the Serial & SPI interfaces, last SCL rising edge for the I^2C interface).

5.5 Scrolling Function

The STE2004S can scroll the graphics display in units of raster-rows. The scrolling function is achieved changing the correspondence between the rows of the logical memory map and the output row drivers. The scroll function doesn't affect the data ram content. It is only related to the visualization process. The information output on the drivers is related to the row reading sequence (the 1st row read is output on R0, the 2nd on R1 and so on). Scrolling means reading the matrix starting from a row that is sequentially increased or decreased. After every scrolling command the offset between the memory address and the memory scanning pointer is increased or decreased by one. The offset range changes in accordance with MUX Rate. After 64th/65th scrolling commands in MUX 65 mode, or after the 48th/49th scrolling commands in mux 49 mode, or after 32nd/33rd scrolling command in MUX 33 mode, the offset between the memory address and the memory scanning pointer is again zero (Cyclic Scrolling).
A Reset Scrolling Pointer instruction can be executed to force to zero the offset between the memory address and the memory scanning pointer
If ICON MODE =1, the Icon Row is not scrolled. If ICON MODE=0 the last row is like a general purpose row and it is scrolled as other lines.
If the DIR Bit is set to a logic zero the offset register is increased by one and the raster is scrolled from top down. If the DIR Bit is set to a logic one the offset register is decreased by one and the raster is scrolled from bottom-up.

Table 8.

MUX RATE	ICON MODE	DESCRIPTION	ICON Row Driver with MY=0
MUX 33	1	ICON ROW NOT SCROOLED	R48
MUX 33	0	33 LINE GRAPHIC MATRIX	R48
MUX 49	1	ICON ROW NOT SCROOLED	R56
MUX 49	0	49 LINE GRAPHIC MATRIX	R56
MUX 65	1	ICON ROW NOT SCROOLED	R64
MUX 65	0	65 LINE GRAPHIC MATRIX	R64

5.6 Dual Partial Display

If the PE Bit is set to a logic one the dual partial display mode is enabled.
Eight partial display modes are available. The offset of the two partial display zones is row by row programmable. The Icon row is accessed last in each partial display frame.
Two sets of register for the HV-generator parameters are provided (PRS[1:0], Vop[6:0], BS[2:0], CP[2:0].). This allows switching from normal mode to partial display mode only with one instruction. The HV generator is automatically re configured using the parameters related to the enabled mode. The parameters of the two sets of registers with the same function are located in the same position of the instruction set. The registers related to the normal mode are accessible when normal mode (PE=0) is selected, the others are accessible when the partial display mode is enabled (PE=1). To Setup PRS[1:0], Vop[6:0], BS[2:0], CP[2:0] values the instruction flow proposed in Fig. 54 must be followed. To setup Partial Display Sectors Start Address and Partial Display Mode no particular instruction flow has to be followed.

Figure 53. Dual Partial Display Enabling Instruction Flow

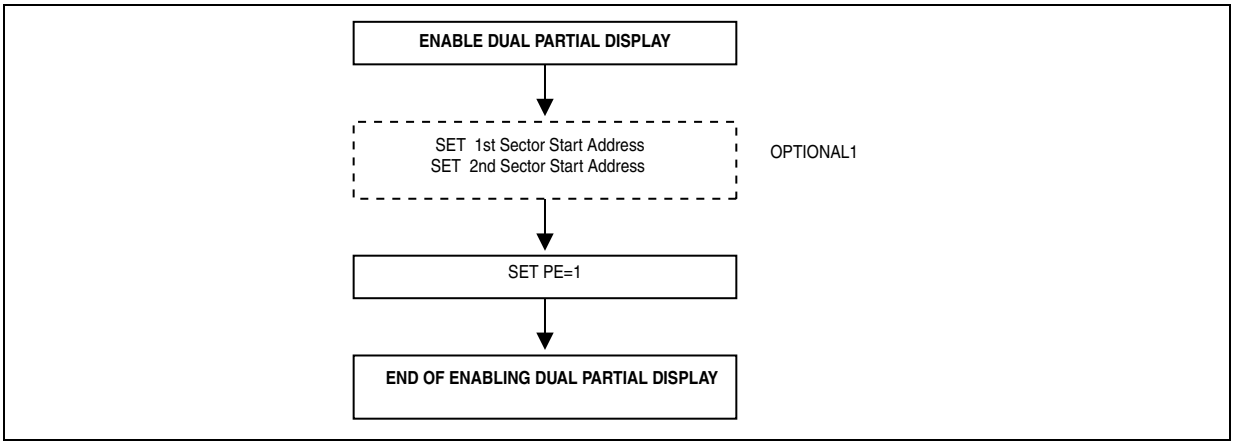


Figure 54. Dual Partial Display Mode configuration or Duty Change

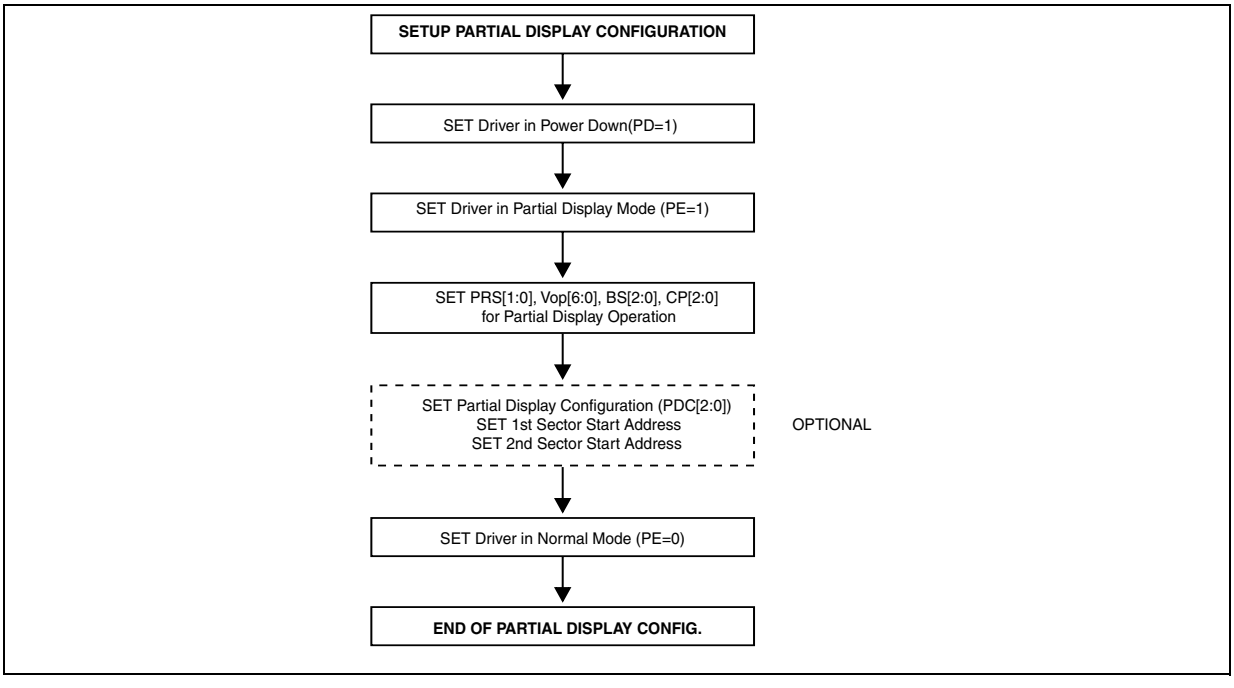


Table 9. Partial Display Configurations

PDC 2	PDC 1	PDC 0	SECTION 1	SECTION2	RESET STATE
0	0	0	0	8 + Icon Row	000
0	0	1	8	0 + Icon Row	
0	1	0	8	8 + Icon Row	
0	1	1	0	16 + Icon Row	
1	0	0	16	0 + Icon Row	
1	0	1	8	16 + Icon Row	
1	1	0	16	8 + Icon Row	
1	1	1	16	16 + Icon Row	

6 ID-NUMBER

The STE2004S allows to program a Driver Identification Number (ID-Number). This make possible to easily manage on one platform more than one LCD module with different configuration parameters.
Four are the device ID-Numbers programmable: 00111100, 00111101, 0011110 & 0011111. All have in common the first 6 bits (001111). The two least significant bit could be set connecting the SA0 and SA1 inputs to a VSS or VDD1.

The driver ID-number can be read through all communication interfaces. The way to read-out the ID-Number changes according the interface selected. The readout protocol for each interface is described in the Bus interfaces paragraph.

Table 10. STE2001/2-like instruction Set

Instruction	D/$\overline{C}$	R/$\overline{W}$	B7	B6	B5	B4	B3	B2	B1	B0	Description
H=0 or H=1											
Read Commnad	0	0	0	0	0	0	0	0	0	0	Read I^2C Address or Status Byte (with 3-Lines Serial & 4-lines SPI only)
Function Set	0	0	0	0	1	MX	MY	PD	V	H[0]	Power Down Management; Entry Mode;
Status Byte	0	1	PD	BSY	0	D	E	MX	MY	DO	(I^2C interface only)
ID Code	0	1	0	0	1	1	1	1	ID1	ID0	
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Writes data to RAM
H=0											
Memory Blank	0	0	0	0	0	0	0	0	0	1	Starts Memory Blank Procedure
Scroll	0	0	0	0	0	0	0	0	1	DIR	Scrolls by one Row UP or DOWN
V_{LCD} Range Setting	0	0	0	0	0	0	0	1	0	PRS [0]	V_{LDC} programming range selection
Display Control	0	0	0	0	0	0	1	D	0	E	Select Display Configuration
Set CP Factor	0	0	0	0	0	1	0	S2	S1	S0	Charge Pump Multiplication factor
Set RAM Y	0	0	0	1	0	0	Y3	Y2	Y1	Y0	Set Horizontal (Y) RAM Address
Set RAM X	0	0	1	X6	X5	X4	X3	X2	X1	X0	Set Vertical (X) RAM Address
H=1											
Checker Board	0	0	0	0	0	0	0	0	0	1	Starts Checker Board Procedure
Duty	0	0	0	0	0	0	0	0	1	MUX	Selects Duty factor
TC Select	0	0	0	0	0	0	0	1	TC1	TC0	Set Temperature Coefficient for V_{LDC}
Data Order	0	0	0	0	0	0	1	DO	0	0	
Bias Ratios	0	0	0	0	0	1	0	BS2	BS1	BS0	Set desired Bias Ratios
Reserved	0	0	0	1	X	X	X	X	X	X	Not to be used
Set V_{OP}	0	0	1	OP6	OP5	OP4	OP3	OP2	OP1	OP0	V_{OP} register Write instruction

Table 11. Extended Instruction Set

Instruction	D/$\overline{C}$	R/$\overline{W}$	B7	B6	B5	B4	B3	B2	B1	B0	Description
H Independent Instructions											
Read Command	0	0	0	0	0	0	0	0	0	0	Read I^2C Address or Status Byte (with 3-Lines Serial & 4-lines SPI only)
	0	0	0	0	1	MX	MY	PD	H[1]	H[0]	Page selector, Power Down Management; Entry Mode
Status Byte	0	1	PD	BSY	0	D	E	MX	MY	DO	
ID Code	0	1	0	0	1	1	1	1	ID1	ID0	
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Writes data to RAM
H=[0;0] RAM Commands											
Memory Blank	0	0	0	0	0	0	0	0	0	1	Starts Memory Blank Procedure
Scroll	0	0	0	0	0	0	0	0	1	DIR	Scrolls by one Row UP or DOWN
V_{LCD} Range Setting	0	0	0	0	0	0	0	1	PRS [1]	PRS [0]	V_{LDC} programming range selection
Display Control	0	0	0	0	0	0	1	D	0	E	Select Display Configuration
Set CP Factor	0	0	0	0	0	1	0	S2	S1	S0	Charge Pump Multiplication factor
Set RAM Y	0	0	0	1	0	0	Y3	Y2	Y1	Y0	Set Horizontal (Y) RAM Address
Set RAM X	0	0	1	X6	X5	X4	X3	X2	X1	X0	Set Vertical (X) RAM Address
H=[0;1]											
Checker Board	0	0	0	0	0	0	0	0	0	1	Starts Checker Board Procedure
	0	0	0	0	0	0	0	0	1	V	Vertical Addressing Mode
TC Select	0	0	0	0	0	0	0	1	TC1	TC0	Set Temperature Coefficient for V_{LDC}
Data Order	0	0	0	0	0	0	1	DO	0	0	MSB Position
Bias Ratios	0	0	0	0	0	1	0	BS2	BS1	BS0	Set desired Bias Ratios
Read Mode,	0	0	0	1	0	0	R	0	0	0	
Set V_{OP}	0	0	1	OP6	OP5	OP4	OP3	OP2	OP1	OP0	V_{OP} register Write instruction
H=[1;0]											
Driver Control	0	0	0	0	0	0	0	0	0	1	Software RESET
Display Control	0	0	0	0	0	0	0	0	1	PE	Partial Enable
	0	0	0	0	0	0	0	1	FR1	FR0	Frame rate Control
	0	0	0	0	0	0	1	0	M[1]	M[0]	Mux Ratio
Partial Mode	0	0	0	0	0	1	0	PDC 2	PDC 1	PDC 0	Partial Display Config
	0	0	0	1	PDY 5	PDY 4	PDY 3	PDY 2	PDY 1	PDY 0	1st Sector Start Address
	0	0	1	PDY 6	PDY 5	PDY 4	PDY 3	PDY 2	PDY 1	PDY 0	2nd Sector Start Address
H=[1;1]											
	0	0	0	0	0	0	0	0	0	1	Scrolling Pointer Reset
	0	0	0	0	0	0	0	0	1	X	Not Used
	0	0	0	0	0	0	0	1	X	X	Not Used
	0	0	0	0	0	0	1	T2	T1	T0	Set Temperature Coefficient for V_{LDC}
	0	0	0	0	0	1	NW3	NW2	NW1	NW0	N-Line Inversion
	0	0	0	1	0	0	YC-3	YC-2	YC-1	YC-0	Y-CARRIAGE RETURN
	0	0	1	XC-6	XC-5	XC-4	XC-3	XC-2	XC-1	XC-0	X CARRIAGE RETURN

Table 12. Explanations of Table 3 & 4 symbols

BIT	0	1	RESET STATE
DIR	Scroll by one down	Scroll by one up	
H[0]	Select page 0	Select page 1	0
PD	Device fully working	Device in power down	1
V	Horizontal addressing	Vertical addressing	0
MX	Normal X axis addressing	X axis address is mirrored.	0
MY	Image is displayed not vertically mirrored	Image is displayed vertically mirrored	0
DO	MSB on TOP	MSB on BOTTOM	0
PE	Partial Display disabled	Partial Display enabled	0
MUX	MUx 65 Mode	MUX 33 Mode	0
R	Read ID-Number / I2C Address	Read Status Byte	0

Table 13. PAGE SELECTION

H[1]	H[0]	DESCRIPTION	RESET STATE
0	0	Page 0	Page 0
0	1	Page 1	
1	0	Page 2	
1	1	Page 3	

Table 14. DISPLAY MODE

D	E	DESCRIPTION	RESET STATE
0	0	display blank	E=0 D=0
0	1	all display segments on	
1	0	normal mode	
1	1	inverse video mode	

Table 15. FRAME RATE CONTROL

FR[1]	FR[0]	DESCRIPTION	RESET STATE
0	0	65Hz	75Hz
0	1	70Hz	
1	0	75Hz	
1	1	80Hz	

Table 16. VLCD RANGE SELECTION

PRS[1]	PRS[0]	DESCRIPTION	RESET STATE
0	0	2.94	
0	1	6.78	
1	0	10.62	
1	1	10.62	

Table 17. MULTIPLEXING RATIO

M[1]	M[0]	DESCRIPTION	RESET STATE
0	0	49	01
0	1	65	
1	0	33	
1	1	Not Allowed	

Table 18. TEMPERATURE COEFFICIENT

T2	T1	T0	DESCRIPTION	RESET STATE
0	0	0	VLCD temperature Coefficient 0	000
0	0	1	VLCD temperature Coefficient 1	
0	1	0	VLCD temperature Coefficient 2	
0	1	1	VLCD temperature Coefficient 3	
1	0	0	VLCD temperature Coefficient 4	
1	0	1	VLCD temperature Coefficient 5	
1	1	0	VLCD temperature Coefficient 6	
1	1	1	VLCD temperature Coefficient 7	

Table 19.

TC1	TC0	DESCRIPTION	RESET STATE
0	0	VLCD temperature Coefficient 0	00
0	1	VLCD temperature Coefficient 2	
0	1	VLCD temperature Coefficient 3	
1	1	VLCD temperature Coefficient 6	

Table 20. CHARGE PUMP MULTIPLICATION FACTOR

CP2	CP1	CP0	DESCRIPTION	RESET STATE
0	0	0	Multiplication Factor X2	000
0	0	1	Multiplication Factor X3	
0	1	0	Multiplication Factor X4	
0	1	1	Multiplication Factor X5	
1	0	0	NOT USED	
1	0	1	NOT USED	
1	1	0	NOT USED	
1	1	1	AUTOMATIC	

Table 21. BIAS RATIO

BS2	BS1	BS0	DESCRIPTION	RESET STATE
0	0	0	Bias Ratio equal to 7	000
0	0	1	Bias Ratio equal to 6	
0	1	0	Bias Ratio equal to 5	
0	1	1	Bias Ratio equal to 4	
1	0	0	Bias Ratio equal to 3	
1	0	1	Bias Ratio equal to 2	
1	1	0	Bias Ratio equal to 1	
1	1	1	Bias Ratio equal to 0	

Table 22. Y CARRIAGE RETURN REGISTER

Y-C[3]	Y-C[2]	Y-C[1]	Y-C[0]	DESCRIPTION	RESET STATE
0	0	0	0	Y-CARRIAGE =0	1000
0	0	0	1	Y-CARRIAGE =1	
0	0	1	0	Y-CARRIAGE =2	
0	0	1	1	Y-CARRIAGE =3	
0	1	0	0	Y-CARRIAGE =4	
.	.	.	.		
0	1	1	0	Y-CARRIAGE =6	
0	1	1	1	Y-CARRIAGE =7	
1	0	0	0	Y-CARRIAGE =8	

Table 23. PARTIAL DISPLAY CONFIGURATION

PD2	PD1	PD0	SECTION 1	SECTION2	RESET STATE
0	0	0	0	8 + Icon Row	000
0	0	1	8	0 + Icon Row	
0	1	0	8	8 + Icon Row	
0	1	1	0	16 + Icon Row	
1	0	0	16	0 + Icon Row	
1	0	1	8	16 + Icon Row	
1	1	0	16	8 + Icon Row	
1	1	1	16	16 + Icon Row	

Table 24. N-LINE INVERSION

NW3	NW2	NW1	NW0	DESCRIPTION	RESET STATE
0	0	0	0	0-Line Inversion (Frame Inversion)	0000
0	0	0	1	2-Line Inversion	
0	0	1	0	3-Line Inversion	
0	0	1	1	4-Line Inversion	
:	:	:	:	:	
1	1	1	0	15-Line Inversion	
1	1	1	1	16-Line Inversion	

Figure 55. I2C Interface Interconnection in Master/ Slave Mode

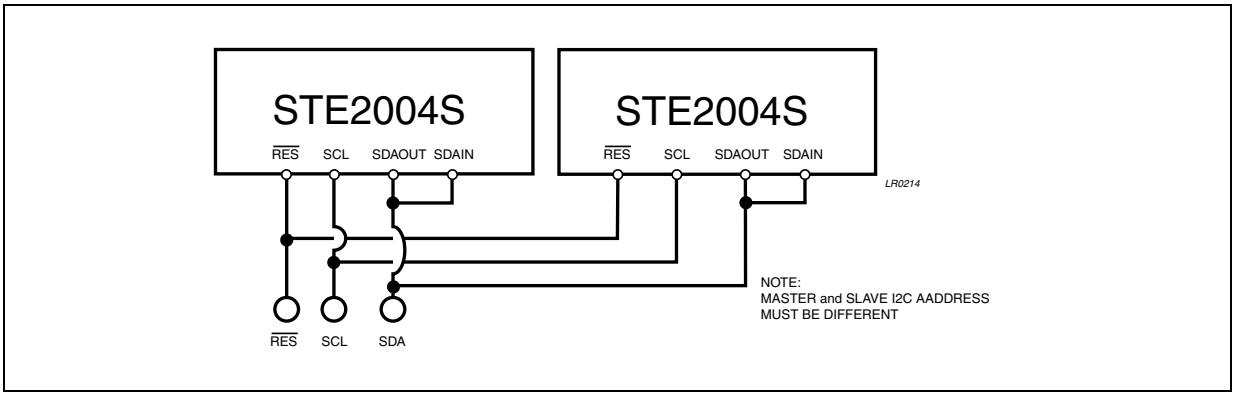


Figure 56. I3-lines SPI & 3-lines Serial Interfaces Interconnection in Master Slave Mode

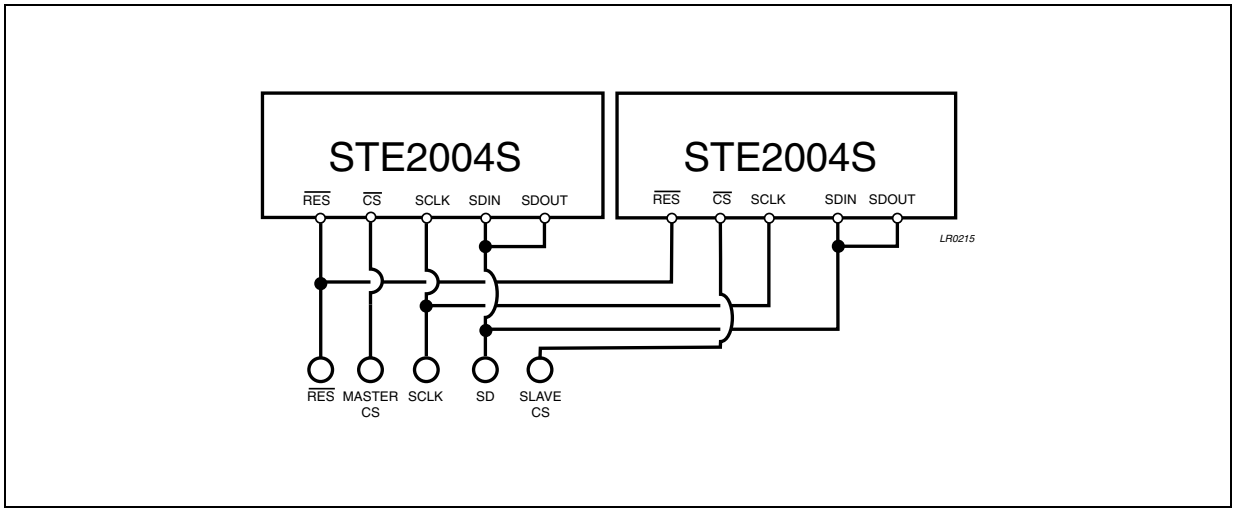


Figure 57. 4-lines SPI Interface Interconnection in Master Slave Mode

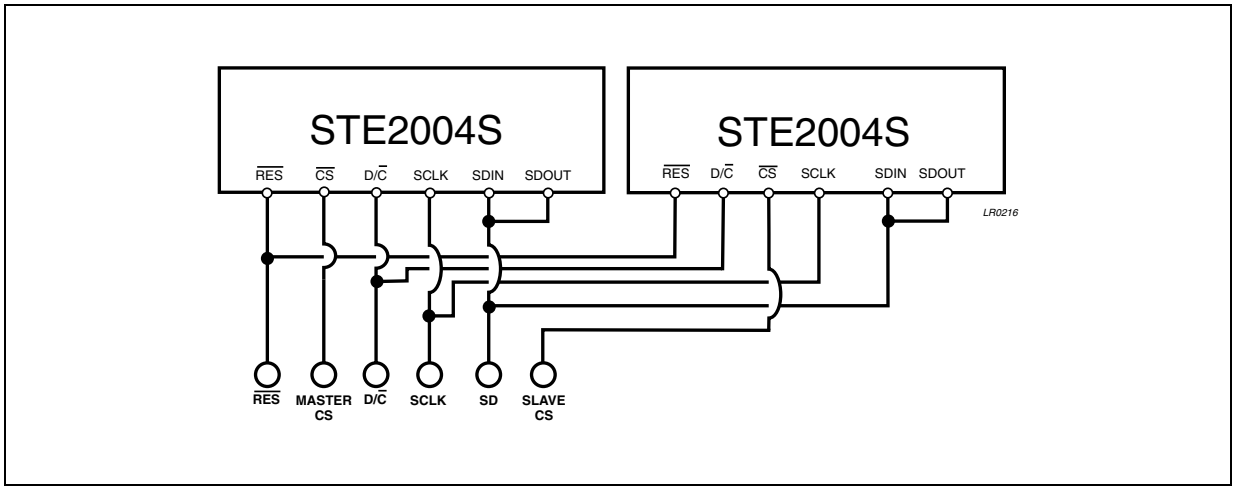


Figure 58. 8080-series & 68000-series Interface Interconnection in Master Slave Mode

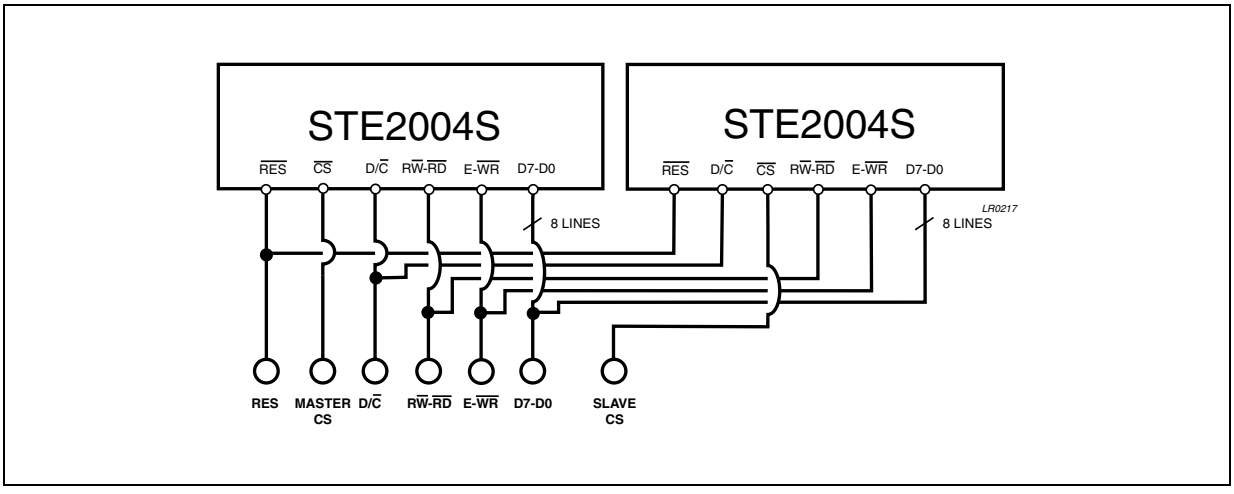


Figure 59. Host Processor Interconnection with I2C Interface

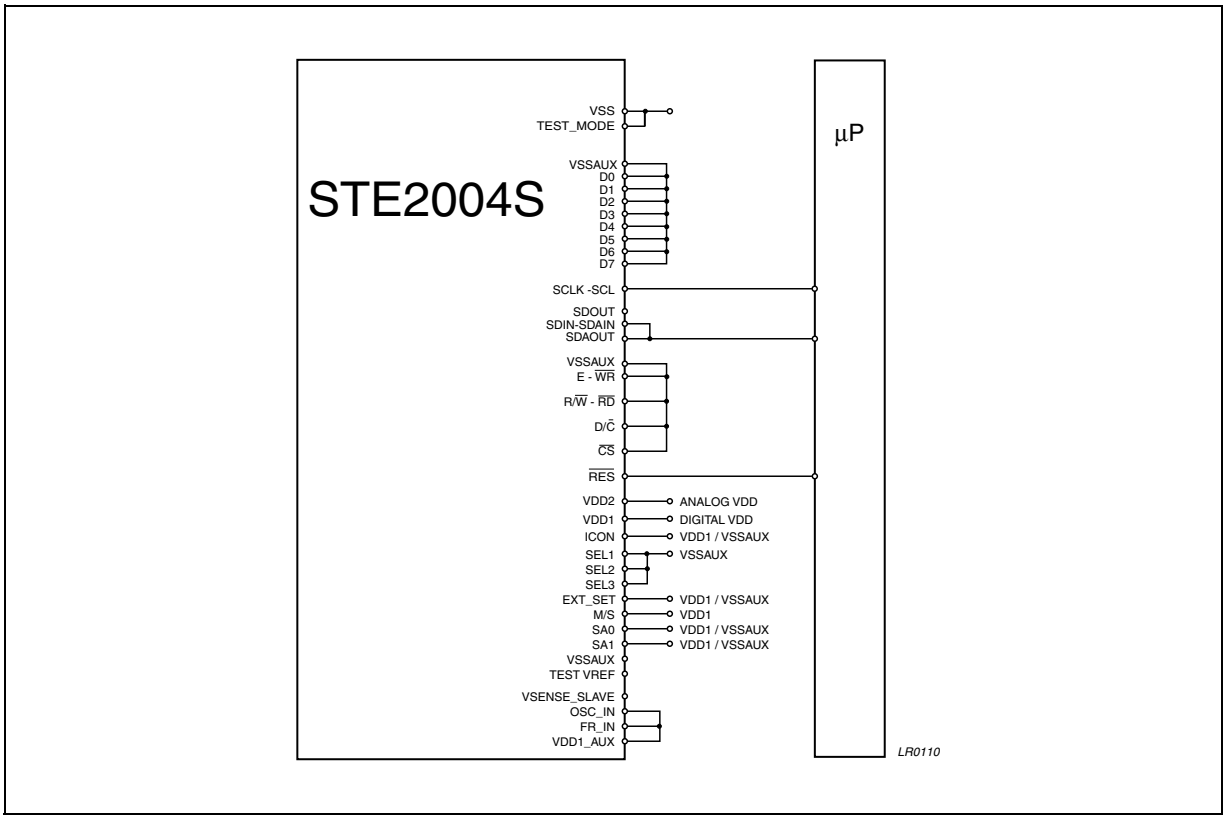


Figure 60. Host Processor Interconnection with 4-line SPI Interface

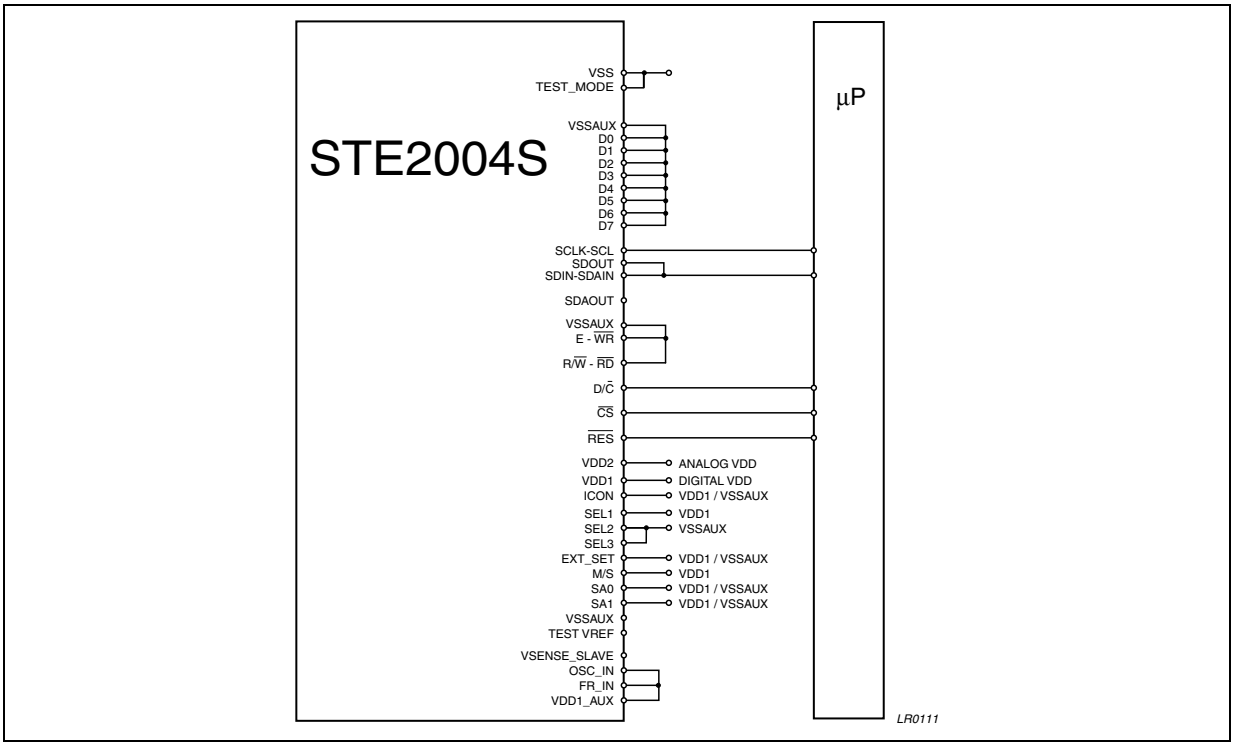


Figure 61. Host Processor Interconnection with 3-line SPI Interface

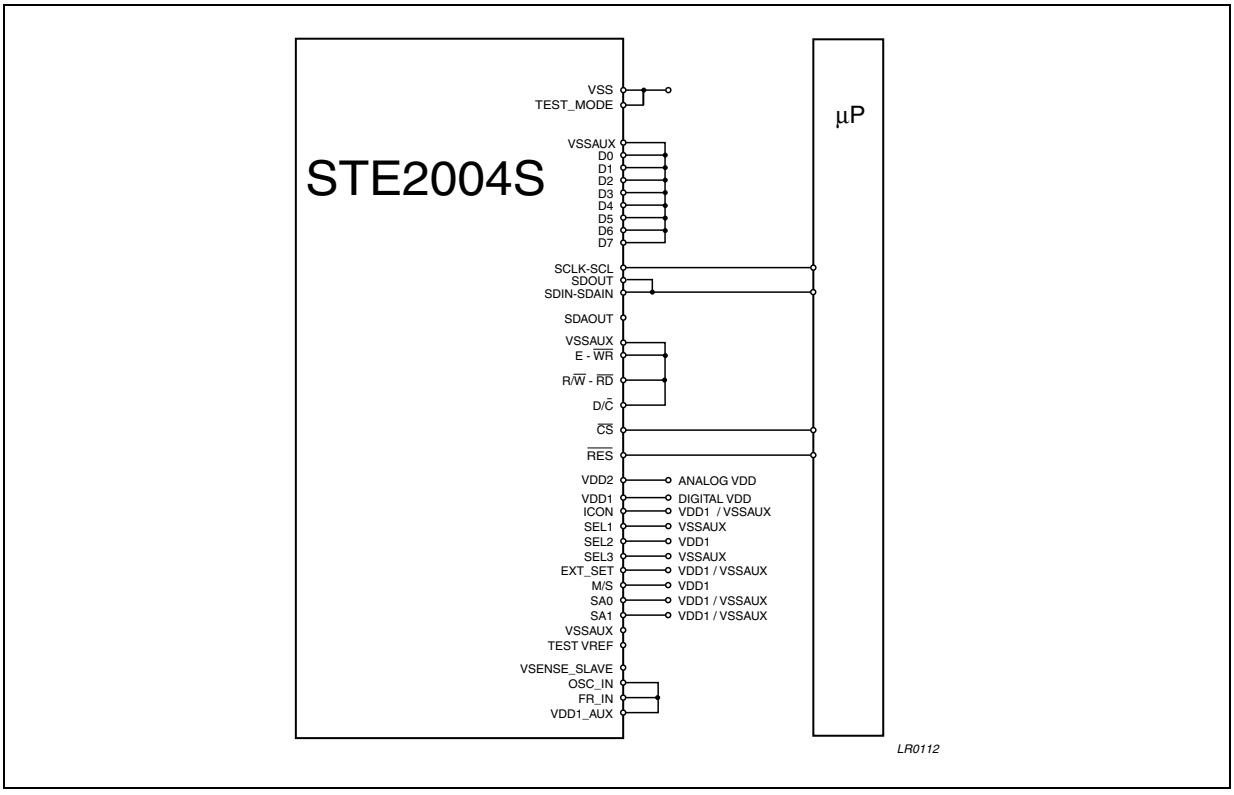


Figure 62. Host Processor Interconnection with 3-line Serial Interface

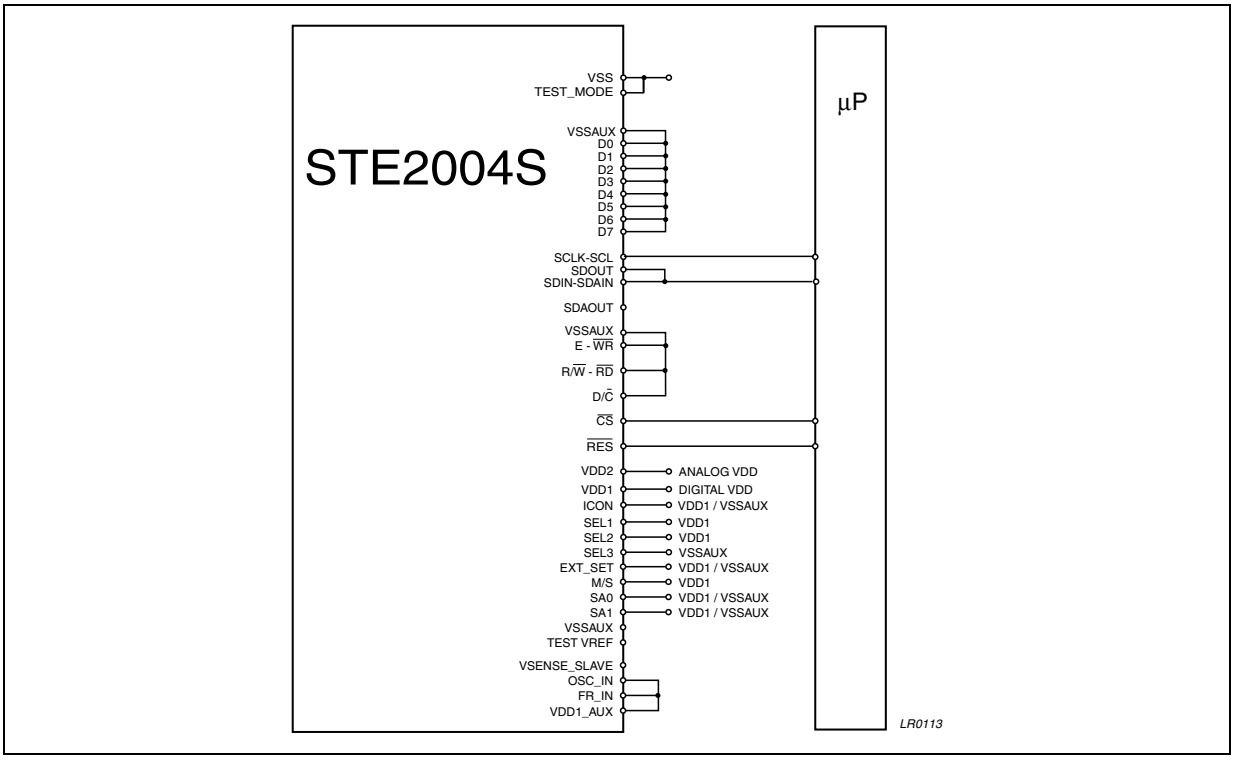


Figure 63. Host Processor Interconnection with 8080-series Parallel Interface

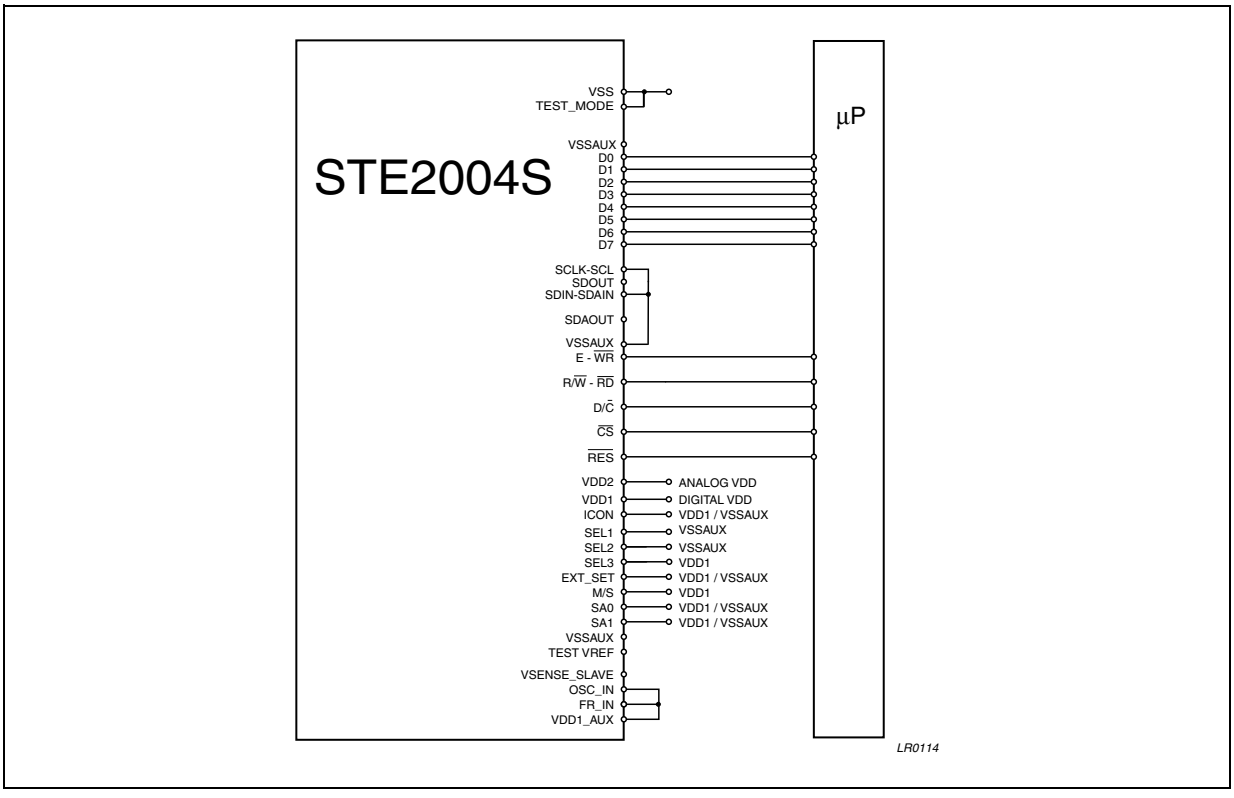


Figure 64. Host Processor Interconnection with 6800

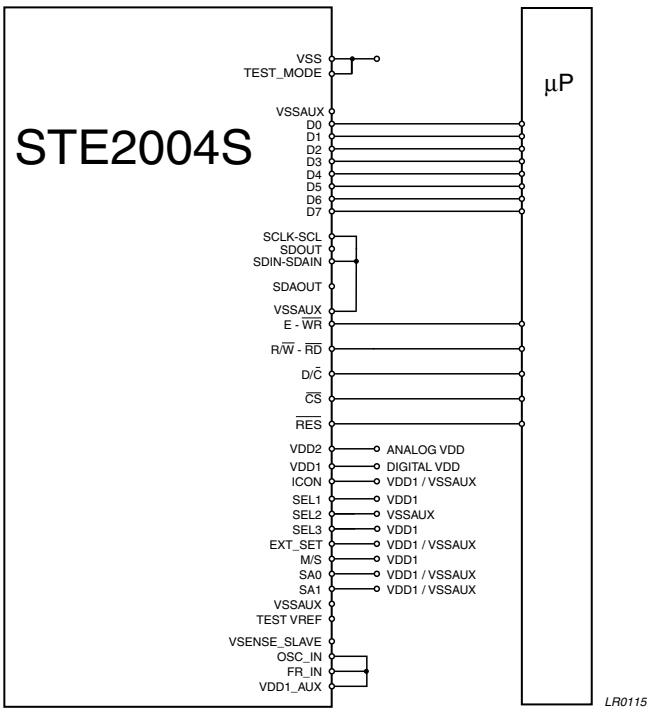


Figure 65. Application Schematic using the Internal LCD Voltage Generator and two separate supplies

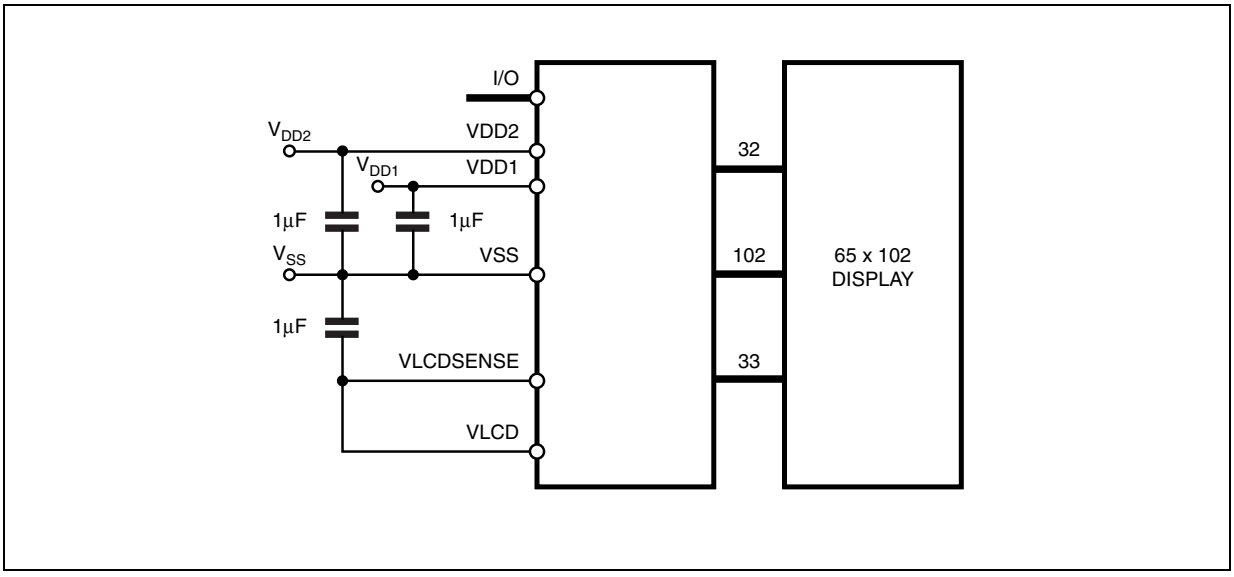


Figure 66. Application Schematic using the Internal LCD Voltage Generator and a single supply

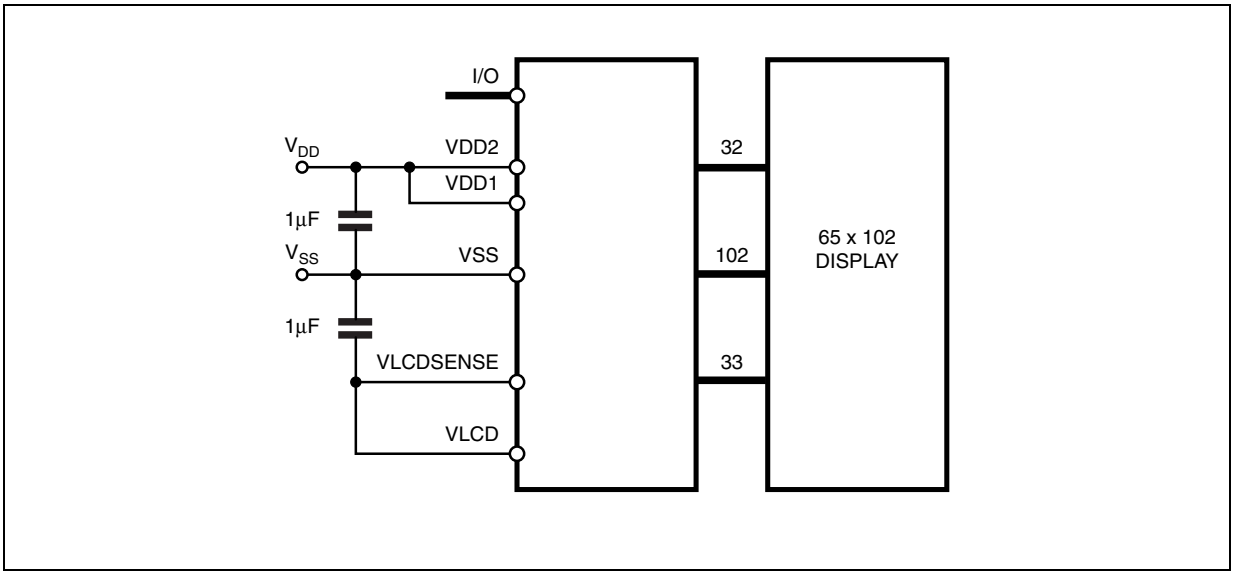
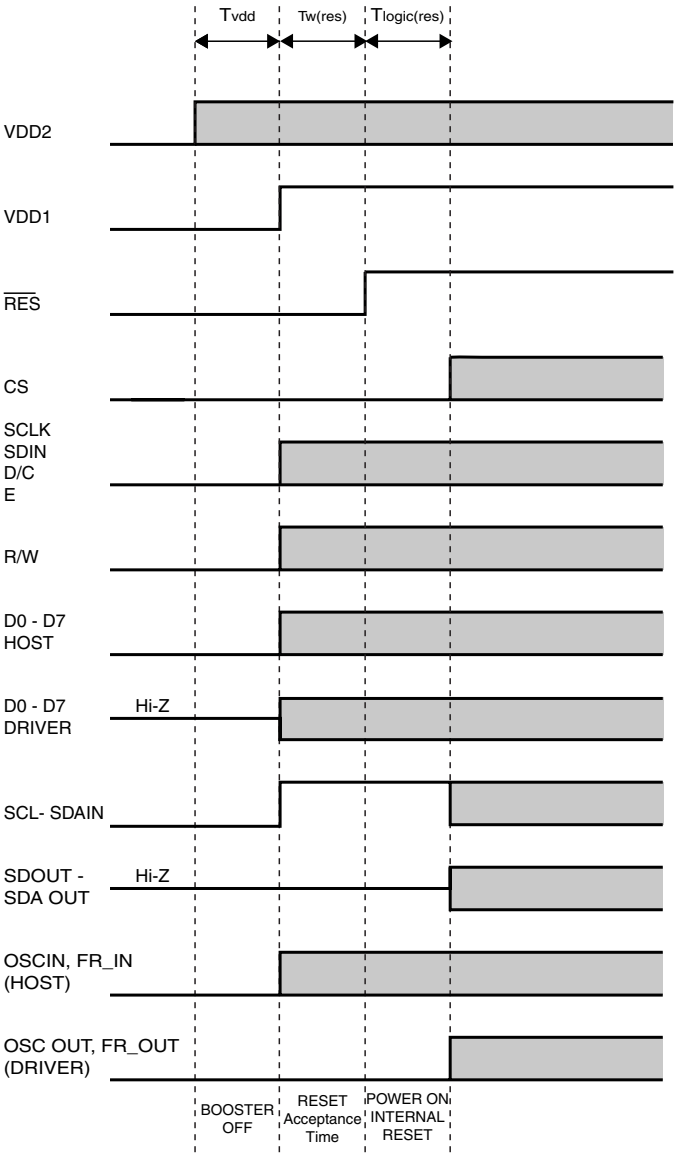


Figure 67. Power-ON timing diagram



LR0208

Figure 68. Power-OFF timing diagram

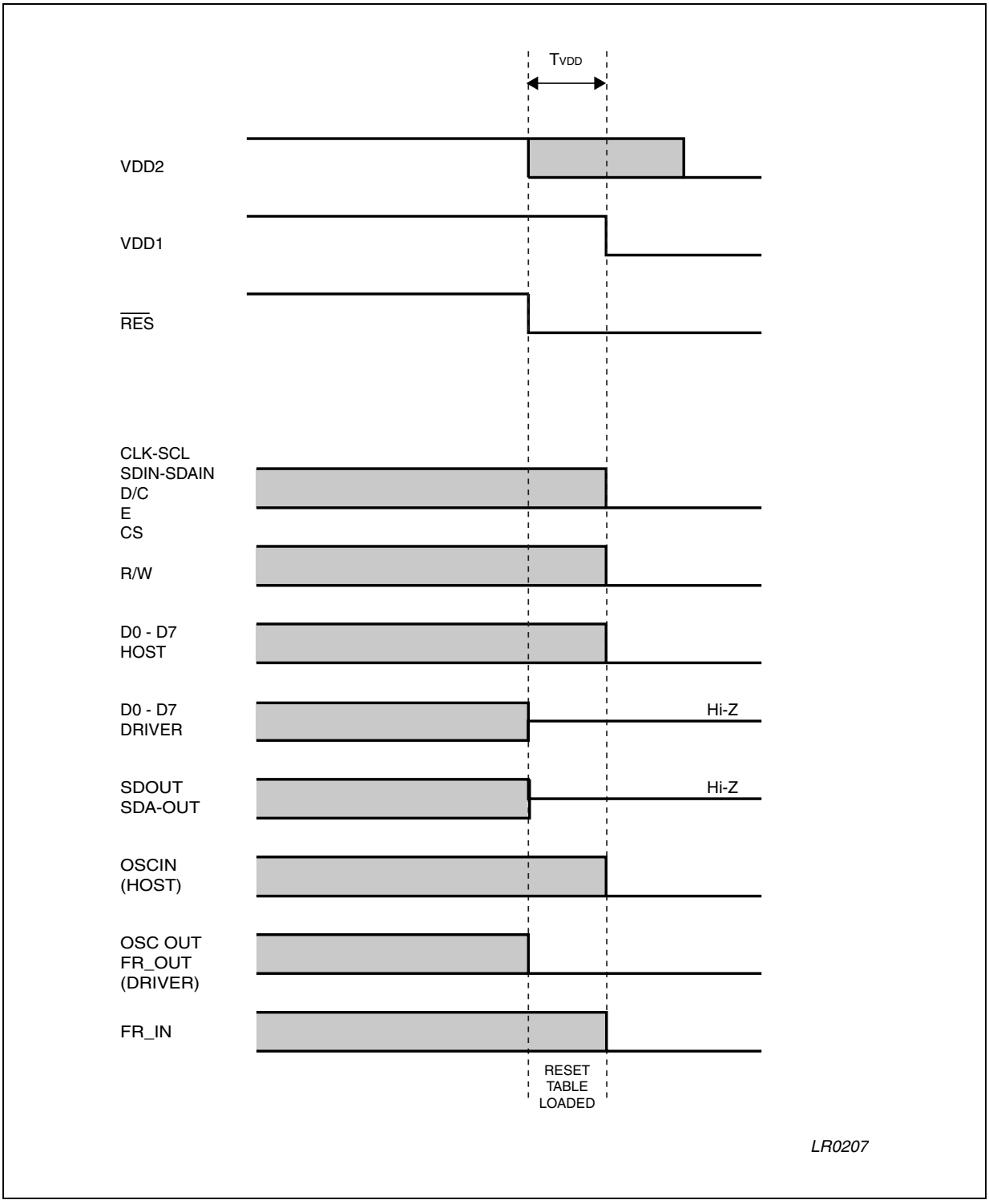


Figure 69. Initialization with built-in Booster

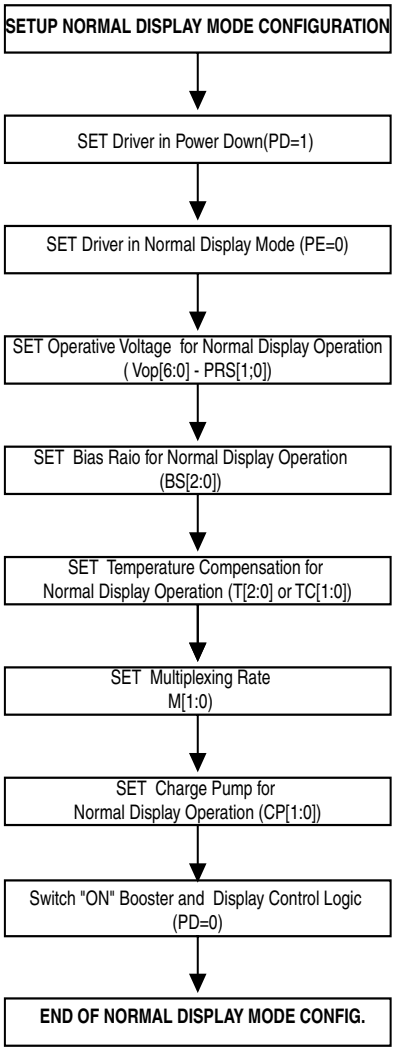


Figure 70. DATA RAM to display Mapping

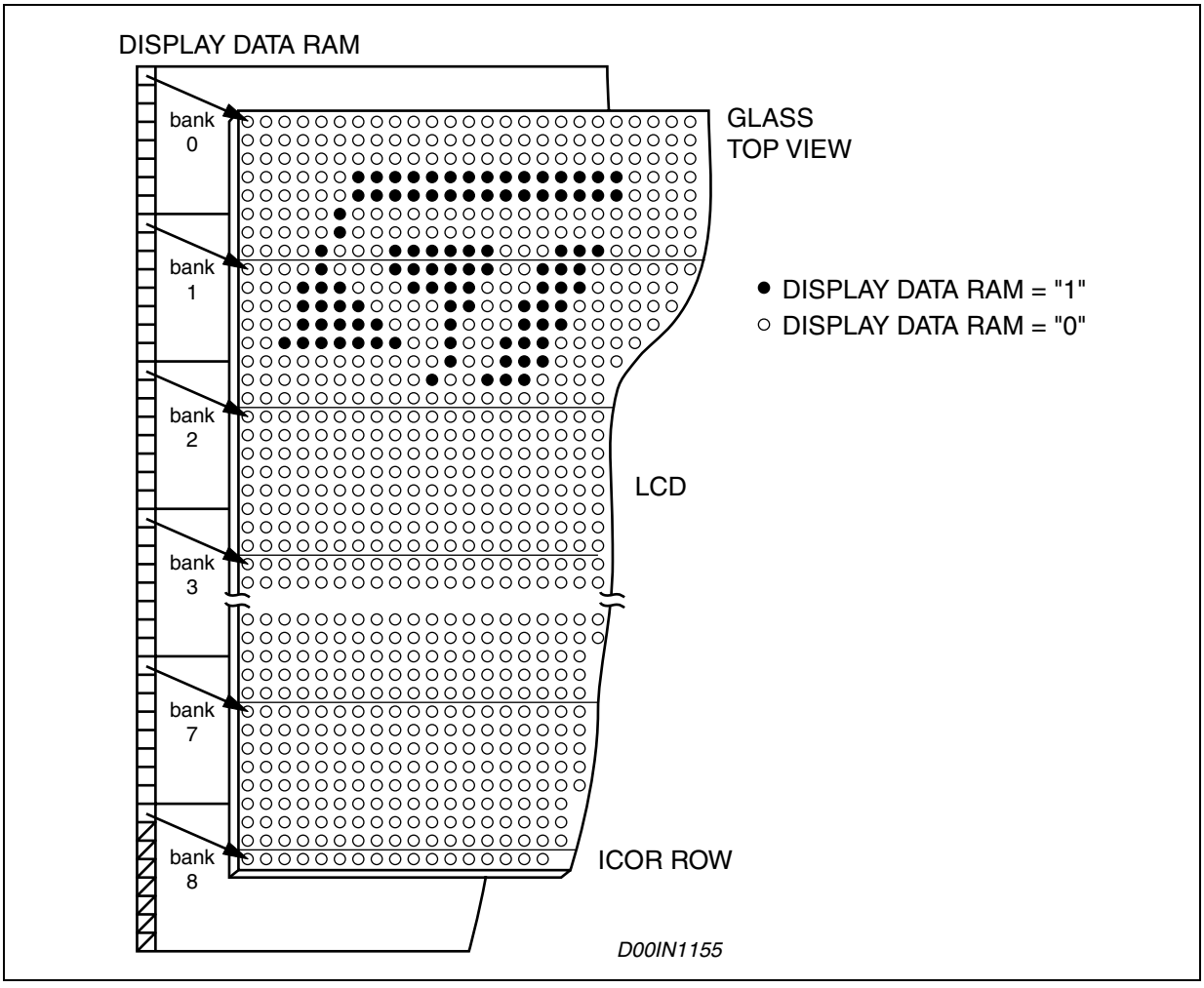


Table 25. Test Pin Configuration

Test Pin	Pin Configuration
TEST_VREF	OPEN
TEST_MODE	GND

Table 26. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD1}	Supply Voltage Range	- 0.5 to + 5	V
V_{DD2}	Supply Voltage Range	- 0.5 to + 7	V
V_{LCD}	LCD Supply Voltage Range	- 0.5 to + 15	V
I_{SS}	Supply Current	- 50 to +50	mA
V_i	Input Voltage (all input pads)	-0.5 to V_{DD1} + 0.5	V
I_{in}	DC Input Current	- 10 to + 10	mA
I_{out}	DC Output Current	- 10 to + 10	mA
P_{tot}	Total Power Dissipation (T_j = 85°C)	300	mW
P_o	Power Dissipation per Output	30	mW
T_j	Operating Junction Temperature	-40 to + 85	°C
T_{stg}	Storage Temperature	- 65 to 150	°C

Table 27. ELECTRICAL CHARACTERISTICS

DC OPERATION

(V_{DD1} = 1.7 to 3.6 V; V_{DD2} = 1.75 to 4.5 V; Vss1,2 = 0V; VLCD = 4.5 to 15 V; Tamb =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltages						
V_{DD1}	Supply Voltage	Note 9	1.7		3.6	V
					V_{DD2}	V
V_{DD2}	Supply Voltage	LCD Voltage Internally generated	1.75		4.5	V
V_{LCD}	LCD Supply Voltage	LCD Voltage Supplied externally	4.5		14.5	V
	LCD Supply Voltage	Internally generated; note 1	4.5		14.5	V
$I(V_{DD1})$	Supply Current	V_{DD1} = 2.8V; V_{LCD} = 10V; f_{sclk} = 0;T_{amb} = 25°C; Parallel Port; note 3,8.	15	20	40	µA
	Supply Current Write Mode	V_{DD2} = 2.8V; V_{LCD} = 10V; f_{sclk} = 1Mhz;T_{amb} = 25°C; OSC_IN=GND; Note8.		100	200	µA
$I(V_{DD2})$	Voltage Generator Supply Current	with V_{OP} = 0 and PRS = [0:0] with external V_{LCD}			5	µA
		V_{DD2} = 2.8V; V_{LCD} = 10V; f_{sclk}=0; T_{amb} = 25°C; no display load; 5x charge pump; note 2,3,6,		60	150	µA
$I(V_{DD1,2})$	Total Supply Current	V_{DD2} = 2.8V; V_{LCD} = 10V; 5x charge pump; f_{sclk} = 0; T_{amb} = 25°C; no display load; note 2, 3, 6		80	190	µA
		Power down Mode with internal or External VLCD. Note 4		3	15	µA
$I(V_{LDCIN})$	External LCD Supply Voltage Current	V_{DD} =2.8V; V_{LCD} =10V;no display load; f_{sclk} = 0; T_{amb} = 25°C; note 3.			25	µA
Logic Outputs						
V_{0H}	High logic Level Output Voltage	IOH=-500µA	0.8V_{DD1}		V_{DD1}	V
V_{OL}	Low logic Level Output Voltage	IOL=+500µA	V_{SS}		0.2V_{DD1}	V

DC OPERATION (continued)

(V_{DD1} = 1.7 to 3.6 V; V_{DD2} = 1.75 to 4.5 V; Vss1,2 = 0V; VLCD = 4.5 to 15 V; Tamb =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Logic Inputs						
V_{IL}	Logic LOW voltage level		V_{SS}		0.3 V_{DD1}	V
V_{IH}	Logic HIGH Voltage Level		0.7 V_{DD1}		V_{DD2}	V
I_{in}	Input Current	V_{in} = V_{SS1} or V_{DD1}	-1		1	µA
Logic Inputs/Outputs						
V_{IL}	Logic LOW voltage level		V_{SS}		0.3 V_{DD1}	V
V_{IH}	Logic HIGH Voltage Level		0.7 V_{DD1}		V_{DD1} + 0.5	V
Column and Row Driver						
R_{row}	ROW Output Resistance			3K	5K	kohm
R_{col}	Column Output resistance			5K	10K	kohm
V_{col}	Column Bias voltage accuracy	No load	-50		+50	mV
V_{row}	Row Bias voltage accuracy		-50		+50	mV
LCD Supply Voltage						
V_{LCD}	LCD Supply Voltage accuracy; Internally generated	V_{DD} = 2.8V; V_{LCD} = 10V; fsclk=0; T_{amb}=25 C; no display load;note 2, 3, 6 & 7, VOP=69h, PRS=2Hex	-2		+2	%
TC0	Temperature coefficient			$-0.0 \cdot 10^{-3}$		1/°C
TC1				$-0.35 \cdot 10^{-3}$		1/°C
TC2				$-0.7 \cdot 10^{-3}$		1/°C
TC3				$-1.05 \cdot 10^{-3}$		1/°C
TC4				$-1.4 \cdot 10^{-3}$		1/°C
TC5				$-1.75 \cdot 10^{-3}$		1/°C
TC6				$-2.1 \cdot 10^{-3}$		1/°C
TC7				$-2.3 \cdot 10^{-3}$		1/°C

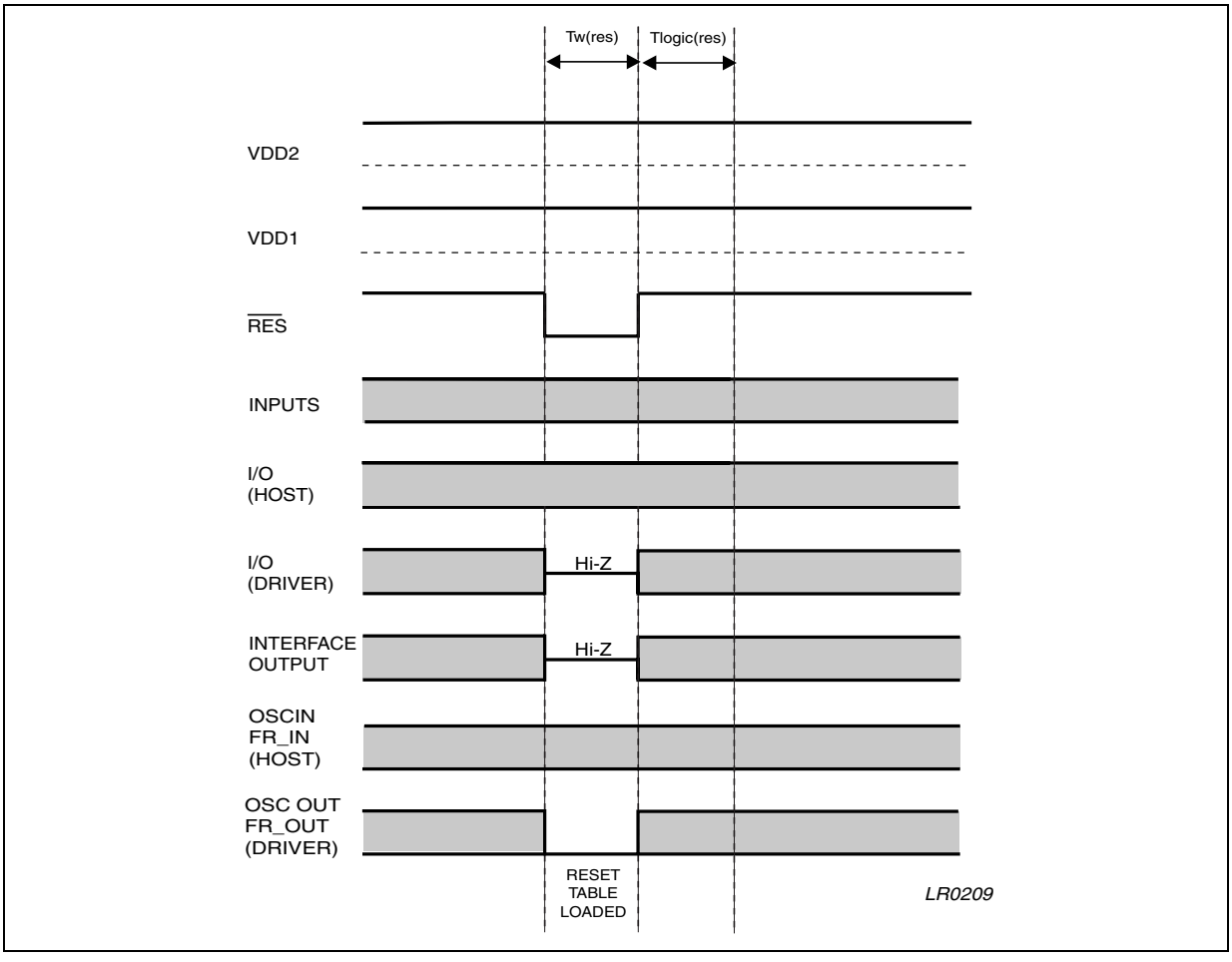
Notes: 1. The maximum possible V_{LCD} voltage that can be generated is dependent on voltage, temperature and (display) load.
2. Internal clock
3. When f_{sclk} = 0 there is no interface clock.
4. Power-down mode. During power-down all static currents are switched-off.
5. If external V_{LCD}, the display load current is not transmitted to I_{DD}
6. Tolerance depends on the temperature; (typically zero at T_{amb} = 27°C), maximum tolerance values are measured at the temperature range limit.
7. For TC0 to TC7
8. Data Byte Writing Mode
9. VDD1<=VDD2

AC OPERATION

(VDD1 = 1.7 to 3.6 V; VDD2 = 1.75 to 4.5 V; Vss1,2 = 0V; VLCD = 4.5 to 15 V; Tamb =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INTERNAL OSCILLATOR						
F_{OSC}	Internal Oscillator frequency	V_{DD} = 2.8V; Tamb = -20 to +70 °C	61	72	83	kHz
F_{EXT}	External Oscillator frequency		20		100	kHz
F_{FRAME}	Frame frequency	fosc or fext = 72 kHz; note 1		75		Hz
$T_{w(RES)}$	$\overline{RES}$ LOW pulse width		5			µs
	Reset Pulse Rejection				1	µs
T_{LOGIC} (RES)	Internal Logic Reset Time				5	µs
T_{VDD}	VDD1 vs. VDD2 Delay		0			µs

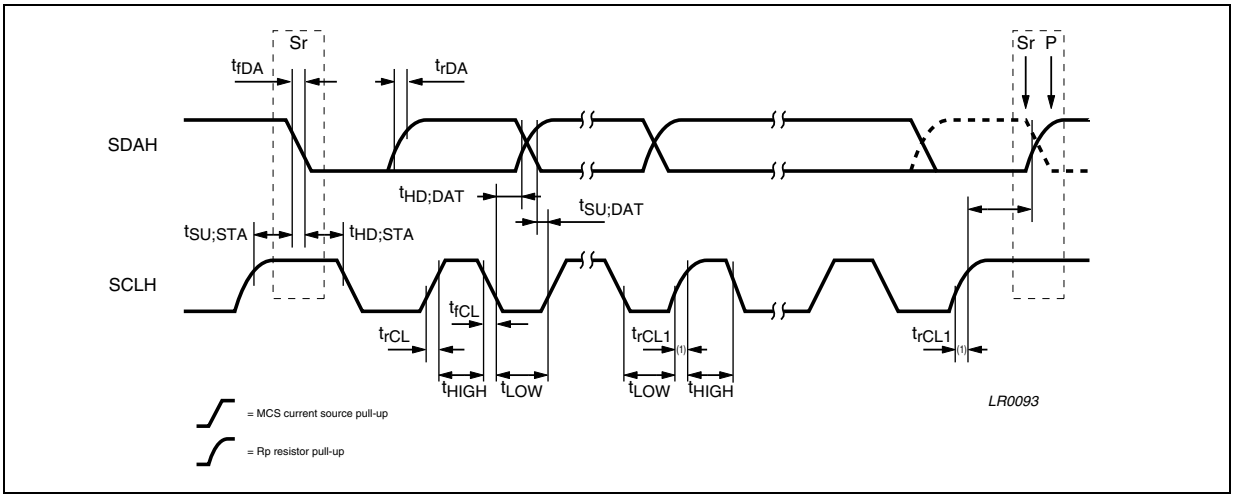
Figure 71. RESET timing diagram



AC OPERATION(continued)
(VDD1 = 1.7 to 3.6 V; VDD2 = 1.75 to 4.5 V; Vss1,2 = 0V; VLCD = 4.5 to 15 V; Tamb =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I²C BUS INTERFACE (See note 4, 7)						
F_{SCL}	SCL Clock Frequency	Fast Mode	DC		400	kHz
		High Speed Mode; Cb=100pF (max);note 6;V_{DD1}=2	DC		3.4	MHz
		High Speed Mode; Cb=400pF (max);note 6; V_{DD1}=2	DC		1.7	MHz
		Fast Mode; note 6; V_{DD1}=1.7V			400	KHz
$T_{SU;STA}$	Set-up time (repeated) START Condition	Note 2,3, Cb = 100pF	160			ns
$T_{HD;STA}$	Hold Time (repeated) START Condition	Note 2,3, Cb = 100pF	160			ns
T_{LOW}	Low Period of SCLH Clock	Note 2,3, Cb = 100pF	160			ns
T_{HIGH}	HIGH Period of SCLH Clock	Note 2,3, Cb = 100pF	160			ns
$T_{SU;DAT}$	Data set-up Time	Note 2,3, Cb = 100pF	60			ns
$T_{HD;DAT}$	Data Hold Time	Note 2,3, Cb = 100pF	10			ns
$T_{r;CL}$	Rise Time of SCLH Signal	Note 2,3, Cb = 100pF	10			ns
$T_{r;CL1}$	Rise Time of SCLH Signal after a repeated START condition and aftyer an Acknowledge bit	Note 2,3, Cb = 100pF	10			ns
$T_{f;CL}$	Fall time of SCLH signal	Note 2,3, Cb = 100pF	10			ns
$T_{r;DA}$	Rise time of SCLH signal	Note 2,3, Cb = 100pF	10			ns
$T_{f;DA}$	Fall time of SDAH signal	Note 2,3, Cb = 100pF	10		80	ns
$T_{r;DA}$	Rise Time of SDAH signal	Note 2,3, Cb = 400pF	20			ns
$T_{f;DA}$	Fall Time of SDAH signal	Note 2,3, Cb = 400pF	20		160	ns
$T_{SU;STO}$	Setup Time for STOP condition	Note 2,3, Cb = 100pF	160			ns
Cb	Capacitive Load for SDAH and SCLH		100		400	pF
Cb	Capacitive Load for SDAH +SDA line and SCLH +SCL Line				400	pF

Figure 72. I²C-bus timings



ELECTRICAL CHARACTERISTICS (continued)
AC OPERATION
(VDD1 = 1.7 to 3.6 V; VDD2 = 1.75 to 4.5V; Vss1,2 = 0V; VLCD = 4.5 to 15 V; Tamb =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PARALLEL INTERFACE						
T_{CYC}	System Cycle Time	V_{DD1} = 1.7V; Read & Write	125			ns
T_{CLW}	Control Low Pulse Width (WR)		20			ns
T_{CHW}	Control High Pulse Width (WR)		75			ns
T_{CLR}	Control Low Pulse Width (RD)		40			ns
T_{CHR}	Control High Pulse Width (RD)		55			ns
T_{EWHW}	Enable High Pulse Width (Write)		60			ns
T_{EWLW}	Enable Low Pulse Width (Write)		60			ns
T_{EWHR}	Enable High Pulse Width (Read)		60			ns
T_{EWLR}	Enable Low Pulse Width (Read)		60			ns
$T_{SU(A)}$	Address Set-up Time		10			ns
$T_{H(A)}$	Address Hold Time		10			ns
T_{SU1}	Data Set-Up Time		30			ns
T_{H1}	Data Hold Time		30			ns
T_{SU2}	Read Access Time				40	ns
T_{H2}	Output Disable Time		0		30	ns

Figure 73. 68000-series Parallel interface timing

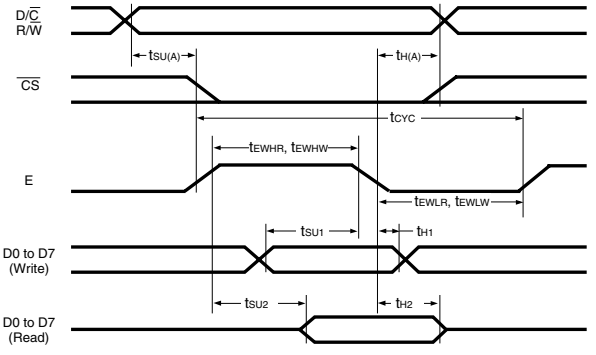
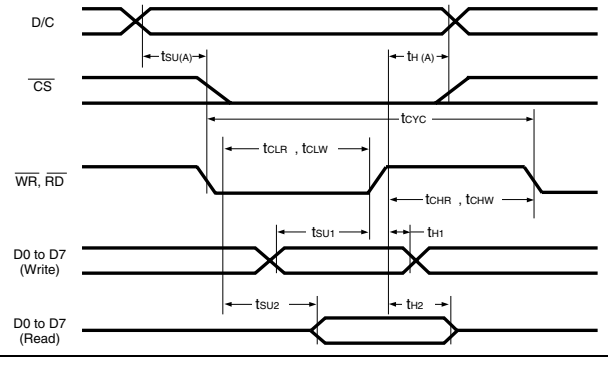


Figure 74. 8080-series parallel Interface timing

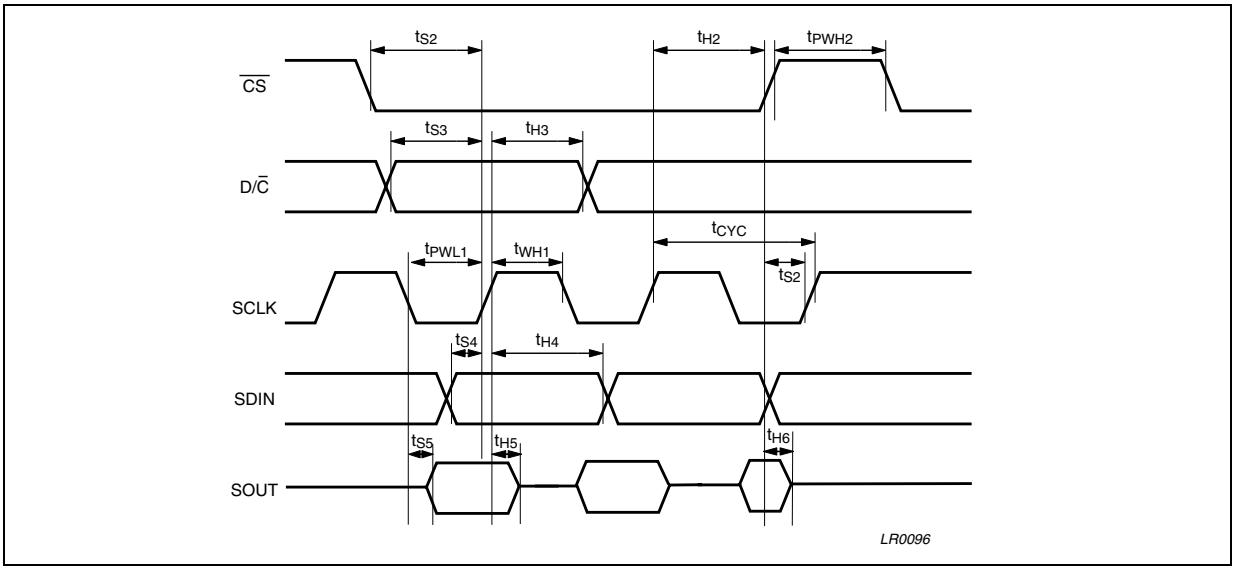


AC OPERATION

(VDD1 = 1.7 to 3.6 V; VDD2 = 1.75 to 4.5 V; Vss1,2 = 0V; VLCD = 4.5 to 15 V; Tamb =-40 to 85°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SERIAL INTERFACE						
F_{SCLK}	Clock Frequency	V_{DD1} = 1.7V;	8			MHz
T_{CYC}	Clock Cycle SCLK		125			ns
T_{PWH1}	SCLK pulse width HIGH		60			ns
T_{PWL1}	SCLK Pulse width LOW		60			ns
T_{S2}	$\overline{CS}$ setup time	V_{DD1} = 1.7V	40			ns
T_{H2}	$\overline{CS}$ hold time		50			ns
T_{PWH2}	$\overline{CS}$ minimum high time		50			ns
T_{S3}	SD/$\overline{C}$ setup time		30			ns
T_{H3}	SD/$\overline{C}$ hold time		30			ns
T_{S4}	SDIN setup time		30			ns
T_{H4}	SDIN hold time		40			ns
T_{S5}	SDOUT Access Time				30	ns
T_{H5}	SDOUT Disable Time vs. SCLK		0		20	ns
T_{H6}	SDOUT Disable Time vs. CS		0		20	ns

Figure 75. Serial interface Timing



Notes: 1. $F_{frame} = \frac{f_{osc}}{960}$

2. All timing values are valid within the operating supply voltage and ambient temperature ranges and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}
3. Cb is the capacitive load for each bus line.
4. For bus line loads Cb between 100 and 400pF the timing parameters must be linearly interpolated
5. C_{VLCD} is the filtering CApacitor on VLCD
6. Trise and Tfall (30%-70%) -10ns
7. I^2C bus AC Characteristics are tested by correlation

Table 28. Pad Coordinates

NAME	PAD	X (µm)	Y(µm)
R5	1	-2632.5	-532.8
R4	2	-2587.5	-532.8
R3	3	-2542.5	-532.8
R2	4	-2497.5	-532.8
R1	5	-2452.5	-532.8
R0	6	-2407.5	-532.8
C0	7	-2362.5	-532.8
C1	8	-2317.5	-532.8
C2	9	-2272.5	-532.8
C3	10	-2227.5	-532.8
C4	11	-2182.5	-532.8
C5	12	-2137.5	-532.8
C6	13	-2092.5	-532.8
C7	14	-2047.5	-532.8
C8	15	-2002.5	-532.8
C9	16	-1957.5	-532.8
C10	17	-1912.5	-532.8
C11	18	-1867.5	-532.8
C12	19	-1822.5	-532.8
C13	20	-1777.5	-532.8
C14	21	-1732.5	-532.8
C15	22	-1687.5	-532.8
C16	23	-1642.5	-532.8
C17	24	-1597.5	-532.8
C18	25	-1552.5	-532.8
C19	26	-1507.5	-532.8
C20	27	-1462.5	-532.8
C21	28	-1417.5	-532.8
C22	29	-1372.5	-532.8
C23	30	-1327.5	-532.8
C24	31	-1282.5	-532.8

Table 28. Pad Coordinates (continued)

NAME	PAD	X (µm)	Y(µm)
C25	32	-1237.5	-532.8
C26	33	-1192.5	-532.8
C27	34	-1147.5	-532.8
C28	35	-1102.5	-532.8
C29	36	-1057.5	-532.8
C30	37	-1012.5	-532.8
C31	38	-967.5	-532.8
C32	39	-922.5	-532.8
C33	40	-877.5	-532.8
C34	41	-832.5	-532.8
C35	42	-787.5	-532.8
C36	43	-742.5	-532.8
C37	44	-697.5	-532.8
C38	45	-652.5	-532.8
C39	46	-607.5	-532.8
C40	47	-562.5	-532.8
C41	48	-517.5	-532.8
C42	49	-472.5	-532.8
C43	50	-427.5	-532.8
C44	51	-382.5	-532.8
C45	52	-337.5	-532.8
C46	53	-292.5	-532.8
C47	54	-247.5	-532.8
C48	55	-202.5	-532.8
C49	56	-157.5	-532.8
C50	57	-112.5	-532.8
C51	58	112.5	-532.8
C52	59	157.5	-532.8
C53	60	202.5	-532.8
C54	61	247.5	-532.8
C55	62	292.5	-532.8

Table 28. Pad Coordinates (continued)

NAME	PAD	X (µm)	Y(µm)
C56	63	337.5	-532.8
C57	64	382.5	-532.8
C58	65	427.5	-532.8
C59	66	472.5	-532.8
C60	67	517.5	-532.8
C61	68	562.5	-532.8
C62	69	607.5	-532.8
C63	70	652.5	-532.8
C64	71	697.5	-532.8
C65	72	742.5	-532.8
C66	73	787.5	-532.8
C67	74	832.5	-532.8
C68	75	877.5	-532.8
C69	76	922.5	-532.8
C70	77	967.5	-532.8
C71	78	1012.5	-532.8
C72	79	1057.5	-532.8
C73	80	1102.5	-532.8
C74	81	1147.5	-532.8
C75	82	1192.5	-532.8
C76	83	1237.5	-532.8
C77	84	1282.5	-532.8
C78	85	1327.5	-532.8
C79	86	1372.5	-532.8
C80	87	1417.5	-532.8
C81	88	1462.5	-532.8
C82	89	1507.5	-532.8
C83	90	1552.5	-532.8
C84	91	1597.5	-532.8
C85	92	1642.5	-532.8
C86	93	1687.5	-532.8

Table 28. Pad Coordinates (continued)

NAME	PAD	X (µm)	Y(µm)
C87	94	1732.5	-532.8
C88	95	1777.5	-532.8
C89	96	1822.5	-532.8
C90	97	1867.5	-532.8
C91	98	1912.5	-532.8
C92	99	1957.5	-532.8
C93	100	2002.5	-532.8
C94	101	2047.5	-532.8
C95	102	2092.5	-532.8
C96	103	2137.5	-532.8
C97	104	2182.5	-532.8
C98	105	2227.5	-532.8
C99	106	2272.5	-532.8
C100	107	2317.5	-532.8
C101	108	2362.5	-532.8
R32	109	2407.5	-532.8
R33	110	2452.5	-532.8
R34	111	2497.5	-532.8
R35	112	2542.5	-532.8
R36	113	2587.5	-532.8
R37	114	2632.5	-532.8
R38	115	2773.8	-472.5
R39	116	2773.8	-427.5
R40	117	2773.8	-382.5
R41	118	2773.8	-337.5
R42	119	2773.8	-292.5
R43	120	2773.8	-247.5
R44	121	2773.8	-202.5
R45	122	2773.8	-157.5
R46	123	2773.8	-112.5
R47	124	2773.8	-67.5

Table 28. Pad Coordinates (continued)

NAME	PAD	X (µm)	Y(µm)
R48	125	2773.8	-22.5
R49	126	2773.8	22.5
R50	127	2773.8	67.5
R51	128	2773.8	112.5
R52	129	2773.8	157.5
R53	130	2773.8	202.5
R54	131	2773.8	247.5
R55	132	2773.8	292.5
R56	133	2773.8	337.5
R57	134	2773.8	382.5
R58	135	2773.8	427.5
R59	136	2773.8	472.5
R60	137	2632.5	532.8
R61	138	2587.5	532.8
R62	139	2542.5	532.8
R63	140	2497.5	532.8
R64/ICON	141	2452.5	532.8
VDD1 AUX	142	2227.5	532.8
FR IN	143	2182.5	532.8
OSC IN	144	2137.5	532.8
Vsns_Slave	145	2092.5	532.8
TEST_VREF	146	1777.5	532.8
VSSAUX	147	1732.5	532.8
SA1	148	1687.5	532.8
SA0	149	1642.5	532.8
M/S	150	1597.5	532.8
EXT_SET	151	1552.5	532.8
SEL3	152	1507.5	532.8
SEL2	153	1462.5	532.8
SEL1	154	1417.5	532.8
ICON	155	1372.5	532.8

Table 28. Pad Coordinates (continued)

NAME	PAD	X (µm)	Y(µm)
VDD1	156	1327.5	532.8
VDD1	157	1282.5	532.8
VDD1	158	1237.5	532.8
VDD1	159	1192.5	532.8
VDD1	160	1147.5	532.8
VDD1	161	1102.5	532.8
VDD1	162	1057.5	532.8
VDD1	163	1012.5	532.8
VDD2	164	967.5	532.8
VDD2	165	922.5	532.8
VDD2	166	877.5	532.8
VDD2	167	832.5	532.8
VDD2	168	787.5	532.8
VDD2	169	742.5	532.8
VDD2	170	697.5	532.8
VDD2	171	652.5	532.8
_RES	172	337.5	532.8
-CS	173	247.5	532.8
D/C	174	157.5	532.8
RW-RD	175	67.5	532.8
E-WR	176	-22.5	532.8
VSSAUX	177	-67.5	532.8
SDA_OUT	178	-157.5	532.8
SDIN_SDAIN	179	-202.5	532.8
SDOUT	180	-247.5	532.8
SCLK_SCL	181	-337.5	532.8
D7	182	-382.5	532.8
D6	183	-427.5	532.8
D5	184	-472.5	532.8
D4	185	-517.5	532.8
D3	186	-562.5	532.8

Table 28. Pad Coordinates (continued)

NAME	PAD	X (µm)	Y(µm)
D2	187	-607.5	532.8
D1	188	-652.5	532.8
D0	189	-697.5	532.8
VSSAUX	190	-742.5	532.8
TEST_MODE	191	-1102.5	532.8
VSS	192	-1147.5	532.8
VSS	193	-1192.5	532.8
VSS	194	-1237.5	532.8
VSS	195	-1282.5	532.8
VSS	196	-1327.5	532.8
VSS	197	-1372.5	532.8
VSS	198	-1417.5	532.8
VSS	199	-1462.5	532.8
VSS	200	-1507.5	532.8
VSS	201	-1552.5	532.8
VSS	202	-1597.5	532.8
VSS	203	-1642.5	532.8
VLCD_SNS	204	-1867.5	532.8
VLCD	205	-1912.5	532.8
VLCD	206	-1957.5	532.8
VLCD	207	-2002.5	532.8
VLCD	208	-2047.5	532.8
VLCD	209	-2092.5	532.8
OSC_OUT	210	-2227.5	532.8
FR_OUT	211	-2272.5	532.8
R31	212	-2497.5	532.8
R30	213	-2542.5	532.8
R29	214	-2587.5	532.8
R28	215	-2632.5	532.8
R27	216	-2773.8	472.5

Table 28. Pad Coordinates (continued)

NAME	PAD	X (µm)	Y(µm)
R26	217	-2773.8	427.5
R25	218	-2773.8	382.5
R24	219	-2773.8	337.5
R23	220	-2773.8	292.5
R22	221	-2773.8	247.5
R21	222	-2773.8	202.5
R20	223	-2773.8	157.5
R19	224	-2773.8	112.5
R18	225	-2773.8	67.5
R17	226	-2773.8	22.5
R16	227	-2773.8	-22.5
R15	228	-2773.8	-67.5
R14	229	-2773.8	-112.5
R13	230	-2773.8	-157.5
R12	231	-2773.8	-202.5
R11	232	-2773.8	-247.5
R10	233	-2773.8	-292.5
R9	234	-2773.8	-337.5
R8	235	-2773.8	-382.5
R7	236	-2773.8	-427.5
R6	237	-2773.8	-472.5

Table 29. Alignment marks coordinates

MARKS	X	Y
mark1	-2780.55	-539.55
mark2	2780.55	-539.55
mark3	-2160.0	539.55
mark4	484.89	539.55

Figure 76. Alignment marks dimensions

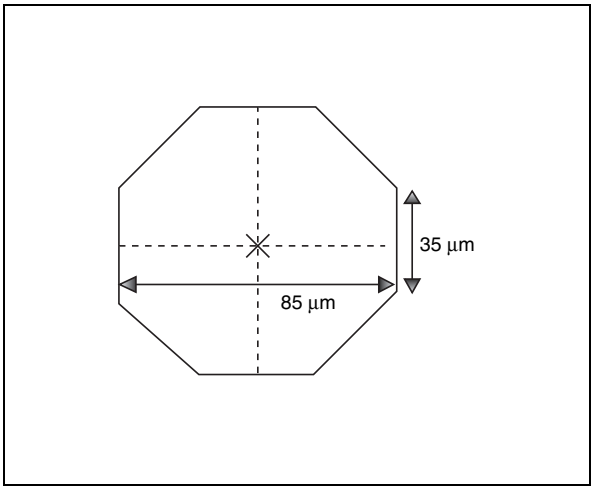


Table 30. Bumps

	Bump Number	Dimensions
Bumps Size		28µmX97µmX17.5µm
Pad Size		35µm X 104µm
Pad Pitch		45µm
Spacing between Bumps		17µm

Table 31. Die Mechanical Dimensions

Die Size (X x Y)	5.815mm x 1.333mm
Wafers Thickness	500µm

Table 32. Revision History

Date	Revision	Description of Changes
September 2005	1	First Issue