TECHNICAL NOTE

Single-chip built-in FET type Switching Regulator Series

High Efficiency Step-down Switching Regulator

BD9102FVM, BD9104FVM, BD9106FVM

●Description

ROHM's high efficiency step-down switching regulator (BD910□FVM) is a power supply designed to produce a low voltage including 1.24 volts from 5 volts power supply line. Offers high efficiency with our original pulse skip control technology and synchronous rectifier. Employs a current mode control system to provide faster transient response to sudden change in load.

●Features

1) Offers fast transient response with current mode PWM control system.
2) Offers highly efficiency for all load range with synchronous rectifier (Nch/Pch FET) and SLLM (Simple Light Load Mode)
3) Incorporates soft-start function.
4) Incorporates thermal protection and ULVO functions.
5) Incorporates short-current protection circuit with time delay function.
6) Incorporates shutdown function
7) Employs small surface mount package MSOP8

●Use

Power supply for HDD, power supply for portable electronic devices like PDA, and power supply for LSI including CPU and ASIC

●Lineup

Parameter	BD9102FVM	BD9104FVM	BD9106FVM
Vcc voltage	4.0～5.5V	4.5～5.5V	4.0～5.5V
Output voltage	1.24V±2%	3.30V±2%	Adjustable(1.0～2.5V)
Output current	0.8A Max.	0.9A Max.	0.8A Max.
UVLO Threshold voltage	2.7V Typ.	4.1V Typ.	3.4V Typ.
Short-current protection with time delay function	built-in	built-in	built-in
Soft start function	built-in	built-in	built-in
Standby current	0μA Typ.	0μA Typ.	0μA Typ.
Operating temperature range	-25～+85℃	-25～+85℃	-25～+85℃
Package	MSOP8	MSOP8	MSOP8

●Absolute Maximum Rating (Ta=25℃)

Parameter	Symbol	Limits	Unit
VCC voltage	Vcc	-0.3～+7 [*1]	V
PVCC voltage	PVcc	-0.3～+7 [*1]	V
EN voltage	EN	-0.3～+7	V
SW,ITH voltage	SW,ITH	-0.3～+7	V
Power dissipation 1	Pd1	387.5[*2]	mW
Power dissipation 2	Pd2	587.4[*3]	mW
Operating temperature range	Topr	-25～+85	℃
Storage temperature range	Tstg	-55～+150	℃
Maximum junction temperature	Tjmax	+150	℃

[*1] Pd should not be exceeded.

[*2] Derating in done 3.1mW/℃ for temperatures above Ta=25℃.

[*3] Derating in done 4.7mW/℃ for temperatures above Ta=25℃,Mounted on 70mm×70mm×1.6mm Glass Epoxy PCB.

Apr.2008

●Recommended Operating Conditions (Ta=25℃)

Parameter	Symbol	BD9102FVM		BD9104FVM		BD9106FVM		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
VCC voltage	VCC	4.0	5.5	4.5	5.5	4.0	5.5	V
PVCC voltage	PVCC [*4]	4.0	5.5	4.5	5.5	4.0	5.5	V
EN voltage	EN	0	VCC	0	VCC	0	VCC	V
SW average output current	Isw [*4]	-	0.8	-	0.8	-	0.8	A

[*4] Pd should not be exceeded.

●Electrical Characteristics

◎BD9102FVM(Ta=25℃,VCC=5V,EN=VCC unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Standby current	ISTB	-	0	10	μA	EN=GND
Bias current	ICC	-	250	400	μA	
EN Low voltage	VENL	-	GND	0.8	V	Standby mode
EN High voltage	VENH	2.0	VCC	-	V	Active mode
EN input current	IEN	-	1	10	μA	VEN=5V
Oscillation frequency	FOSC	0.8	1	1.2	MHz	
Pch FET ON resistance [*5]	RONP	-	0.35	0.60	Ω	PVCC=5V
Nch FET ON resistance [*5]	RONN	-	0.25	0.50	Ω	PVCC=5V
Output voltage	VOUT	1.215	1.24	1.265	V	
ITH sink current	ITHSI	10	20	-	μA	VOUT=H
ITH source current	ITHSO	10	20	-	μA	VOUT=L
UVLO threshold voltage	VUVLOTh	2.6	2.7	2.8	V	VCC=H→L
UVLO hysteresis voltage	VUVLOHys	50	100	200	mV	
Soft start time	TSS	0.5	1	2	ms	
Timer latch time	TLATCH	0.5	1	2	ms	

[*5] Design Guarantee（Outgoing inspection is not done on all products）

◎BD9104FVM(Ta=25℃,VCC=5V,EN=VCC unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Standby current	ISTB	-	0	10	μA	EN=GND
Bias current	ICC	-	250	400	μA	
EN Low voltage	VENL	-	GND	0.8	V	Standby mode
EN High voltage	VENH	2.0	VCC	-	V	Active mode
EN input current	IEN	-	1	10	μA	VEN=5V
Oscillation frequency	FOSC	0.8	1	1.2	MHz	
Pch FET ON resistance [*5]	RONP	-	0.35	0.60	Ω	PVCC=5V
Nch FET ON resistance [*5]	RONN	-	0.25	0.50	Ω	PVCC=5V
Output voltage	VOUT	3.234	3.300	3.366	V	
ITH sink current	ITHSI	10	20	-	μA	VOUT=H
ITH source current	ITHSO	10	20	-	μA	VOUT=L
UVLO threshold voltage	VUVLOTh	3.9	4.1	4.3	V	VCC=H→L
UVLO hysteresis voltage	VUVLOHys	50	100	200	mV	
Soft start time	TSS	0.5	1	2	ms	
Timer latch time	TLATCH	0.5	1	2	ms	

[*5] Design Guarantee（Outgoing inspection is not done on all products）

◎BD9106FVM(Ta=25℃,VCC=5V,EN=VCC,R1=20kΩ,R2=10kΩ unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Standby current	ISTB	-	0	10	μA	EN=GND
Bias current	ICC	-	250	400	μA	
EN Low voltage	VENL	-	GND	0.8	V	Standby mode
EN High voltage	VENH	2.0	VCC	-	V	Active mode
EN input current	IEN	-	1	10	μA	VEN=5V
Oscillation frequency	FOSC	0.8	1	1.2	MHz	
Pch FET ON resistance [*5]	RONP	-	0.35	0.60	Ω	PVCC=5V
Nch FET ON resistance [*5]	RONN	-	0.25	0.50	Ω	PVCC=5V
ADJ reference voltage	VADJ	0.780	0.800	0.820	V	
Output voltage	VOUT	-	1.200	-	V	
ITH sink current	ITHSI	10	20	-	μA	ADJ=H
ITH source current	ITHSO	10	20	-	μA	ADJ=L
UVLO threshold voltage	VUVLOTh	3.2	3.4	3.6	V	VCC=H→L
UVLO hysteresis voltage	VUVLOHys	50	100	200	mV	
Soft start time	TSS	1.5	3	6	ms	
Timer latch time	TLATCH	0.5	1	2	ms	

[*5] Design Guarantee（Outgoing inspection is not done on all products）

●Characteristics data

■VCC-VOUT

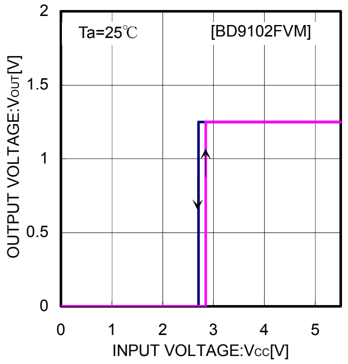


Fig.1 VCC-VOUT

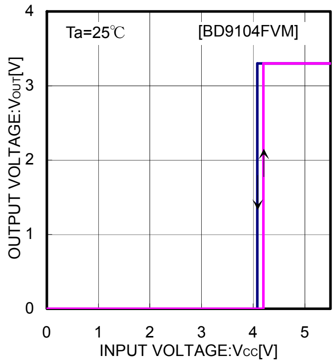


Fig.2 VCC-VOUT

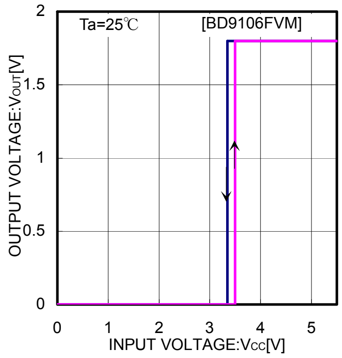


Fig.3 VCC-VOUT

■VEN-VOUT

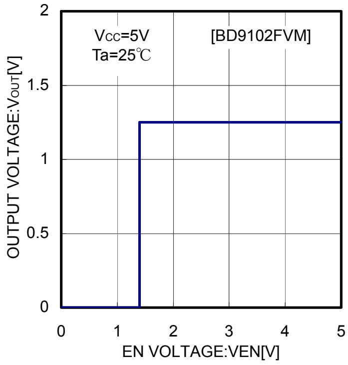


Fig.4 VEN-VOUT

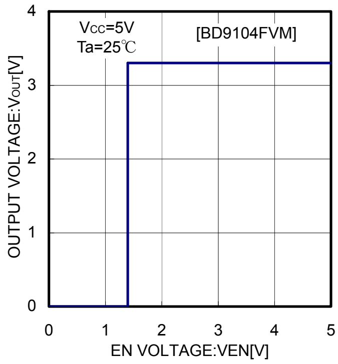


Fig.5 VEN-VOUT

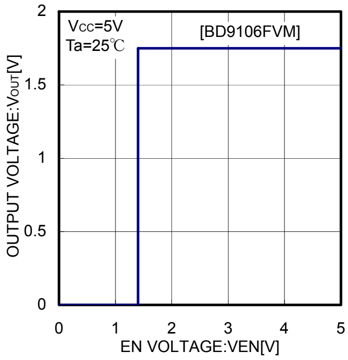


Fig.6 VEN-VOUT

■IOUT-VOUT

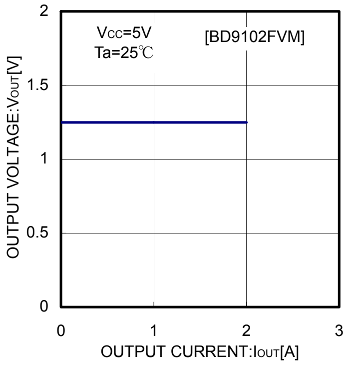


Fig.7 IOUT-VOUT

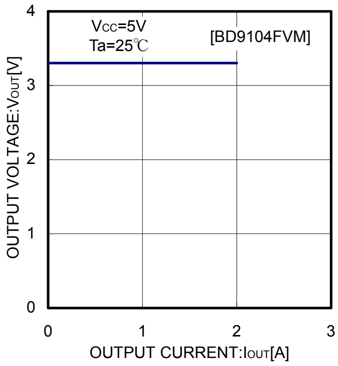


Fig.8 IOUT-VOUT

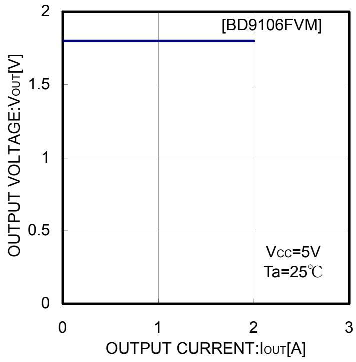


Fig.9 IOUT-VOUT

■Soft start

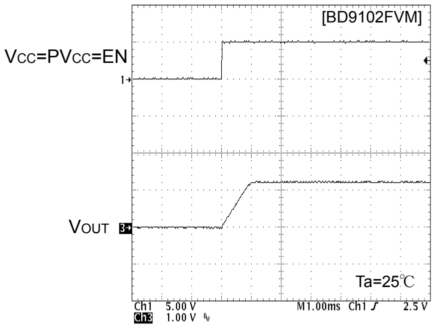


Fig.10 Soft start waveform

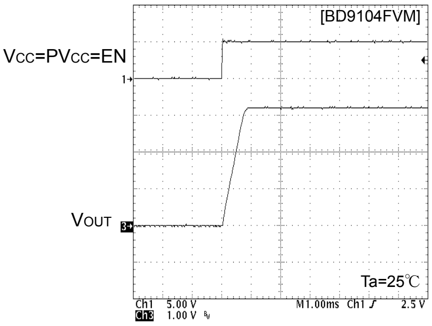


Fig.11 Soft start waveform

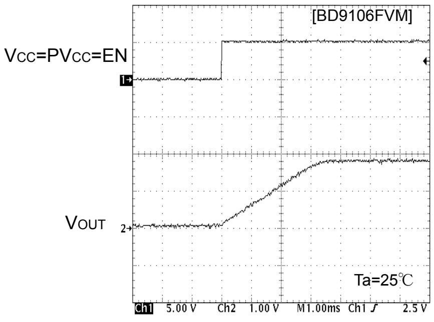


Fig.12 Soft start waveform

■SW waveform IO=10mA

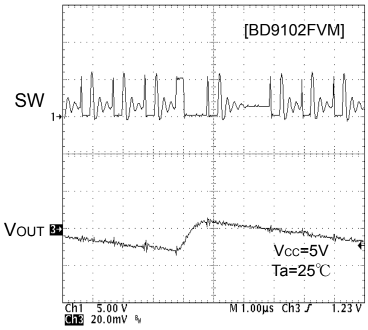


Fig.13 SW waveform
Io=10mA(SLLM control)

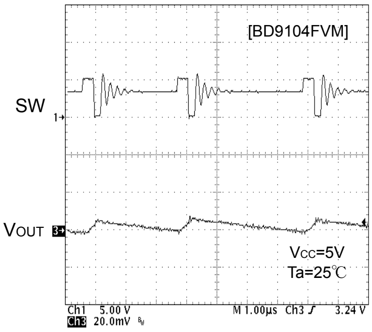


Fig.14 SW waveform
Io=10mA(SLLM control)

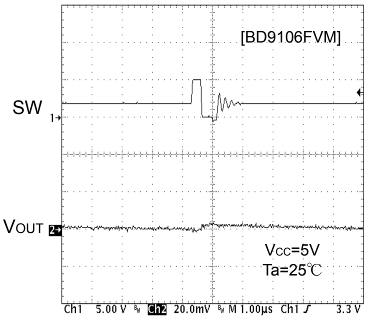


Fig.15 SW waveform
Io=10mA(SLLM control VOUT=1.8V)

■SW waveform IO=200mA

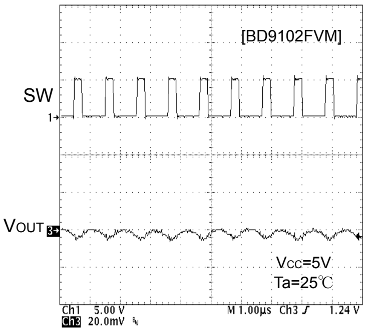


Fig.16 SW waveform
Io=200mA(PWM control)

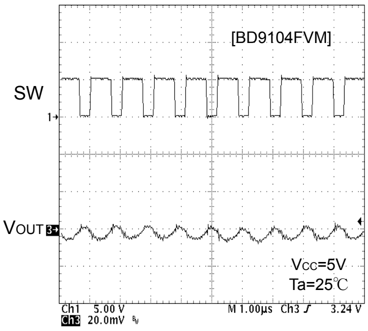


Fig.17 SW waveform
Io=200mA(PWM control)

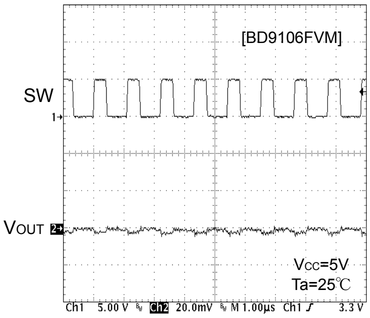


Fig.18 SW waveform
Io=200mA(PWM control VOUT=1.8V)

■Transient response IO=100mA→600mA

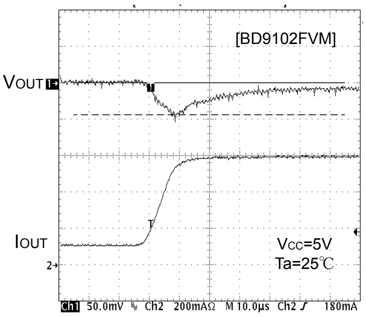


Fig.19 Transient response
Io=100→600mA(10 μ s)

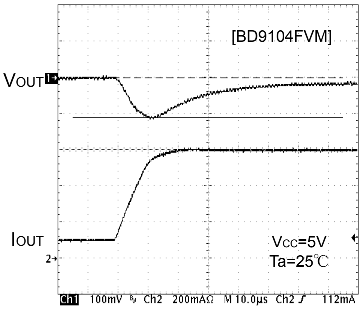


Fig.20 Transient response
Io=100→600mA(10 μ s)

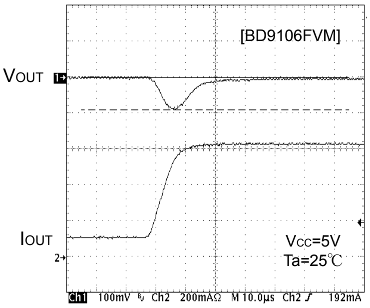


Fig.21 Transient response
Io=100→600mA(10 μ s)
(VOUT=1.8V)

■Transient response IO=600mA→100mA

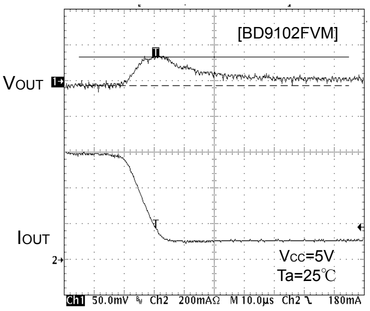


Fig.22 Transient response
Io=600→100mA(10 μ s)

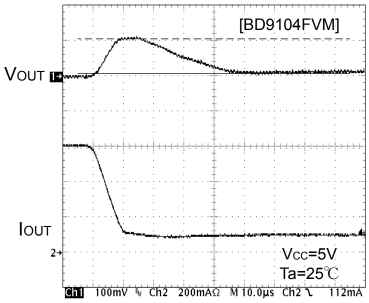


Fig.23 Transient response
Io=600→100mA(10 μ s)

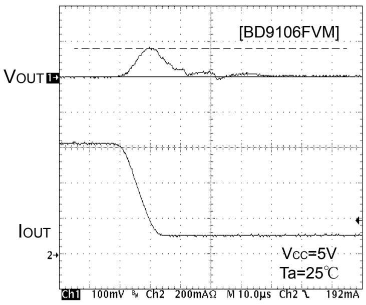


Fig.24 Transient response
Io=600→100mA(10 μ s)
(VOUT=1.8V)

■Ta-VOUT

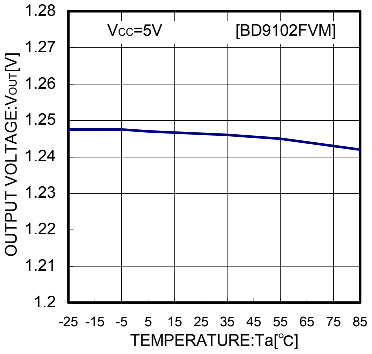


Fig.25 Ta-VOUT

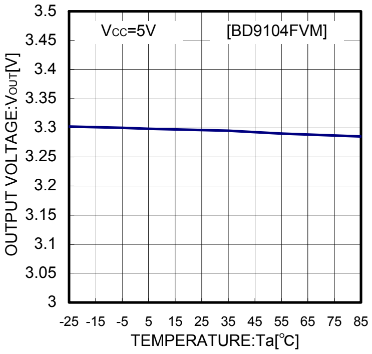


Fig.26 Ta-VOUT

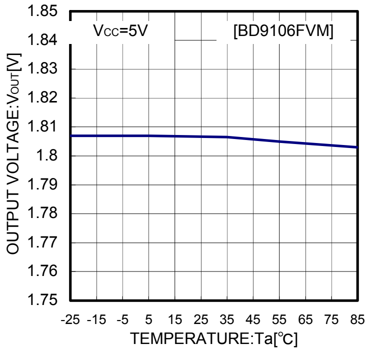


Fig.27 Ta-VOUT

■Efficiency

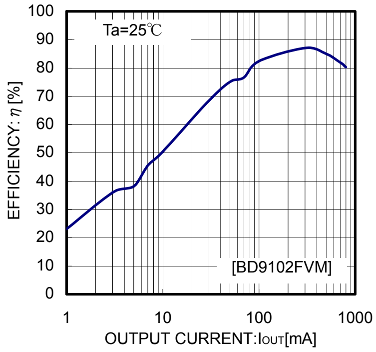


Fig.28 Efficiency
(VCC=EN=5V,VOUT=1.24V)

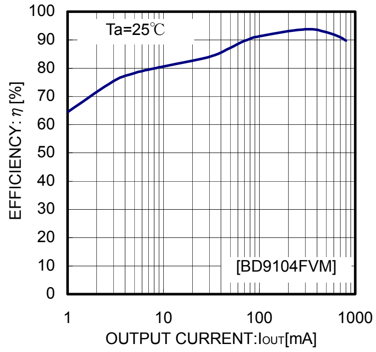


Fig.29 Efficiency
(VCC=EN=5V,VOUT=3.3V)

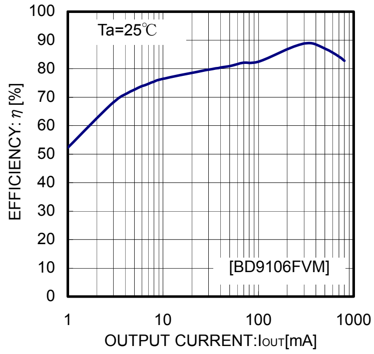


Fig.30 Efficiency
(VCC=EN=5V,VOUT=1.8V)

■Reference characteristics

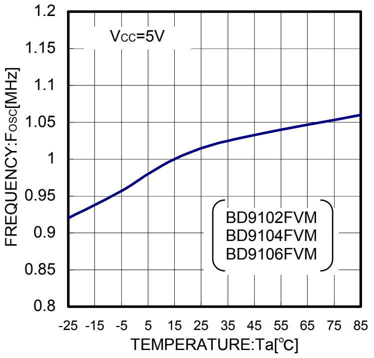


Fig.31 Ta-FOSC

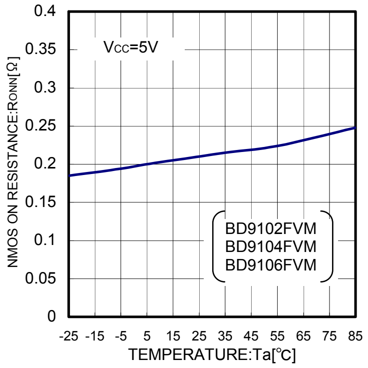


Fig.32 Ta-RONN

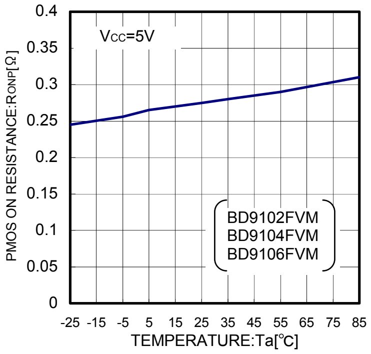


Fig.33Ta-RONP

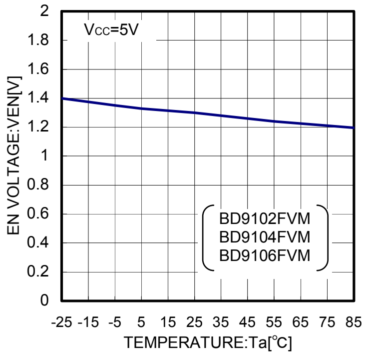


Fig.34 Ta-VEN

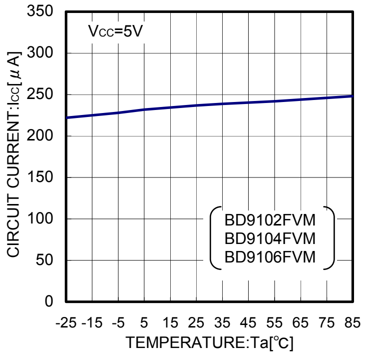


Fig.35 Ta-ICC

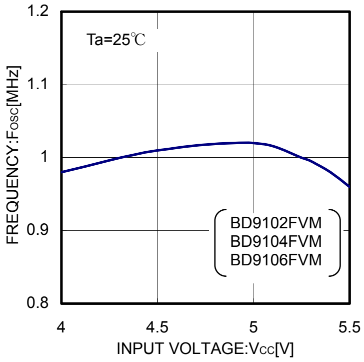


Fig.36 VCC-FOSC

●Block diagram, Application circuit

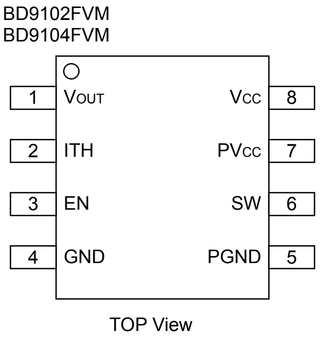


Fig.37 BD9102FVM TOP View
BD9104FVM

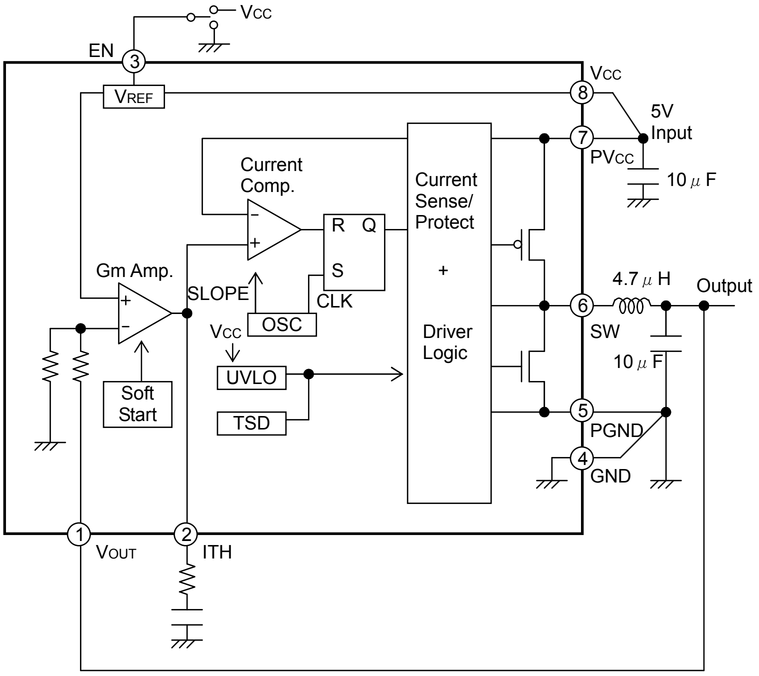


Fig.38 BD9102FVM Block diagram
BD9104FVM

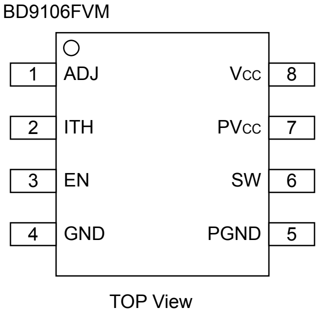


Fig.39 BD9106FVM TOP View

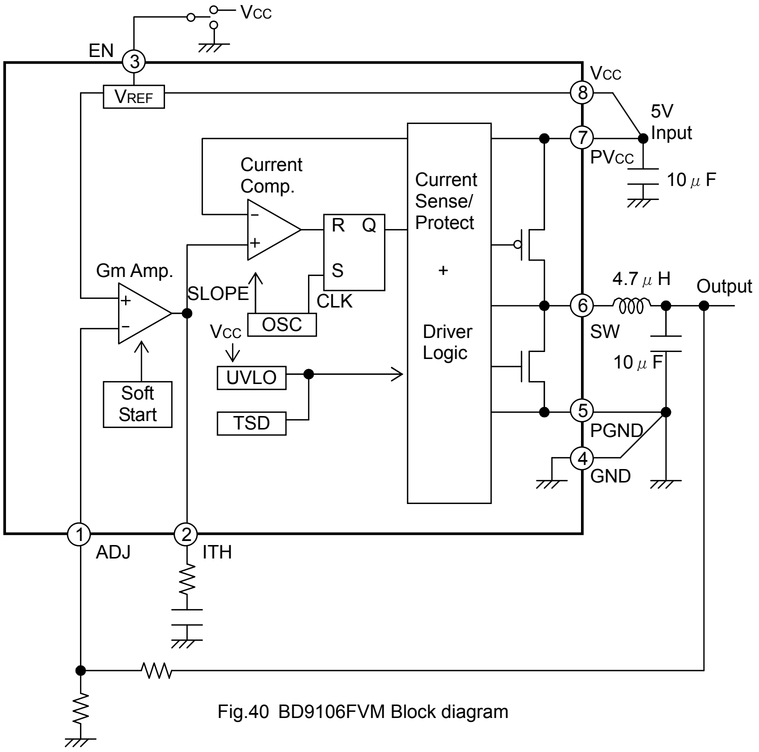


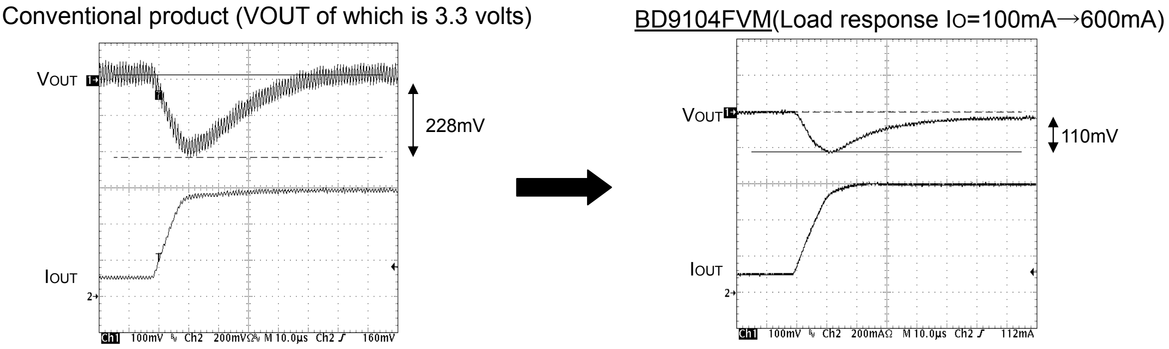
Fig.40 BD9106FVM Block diagram

●Pin No. & function table

Pin No.	Pin name	PIN function
1	VOUT/ADJ	Output voltage detect pin/ ADJ for BD9106FVM
2	ITH	GmAmp output pin/Connected phase compensation capacitor
3	EN	Enable pin(Active High)
4	GND	Ground
5	PGND	Nch FET source pin
6	SW	Pch/Nch FET drain output pin
7	PVCC	Pch FET source pin
8	VCC	VCC power supply input pin

●Information on advantages

Advantage 1 : Offers fast transient response with current mode control system.


Conventional product (VOUT of which is 3.3 volts)

BD9104FVM(Load response IO=100mA→600mA)

Voltage drop due to sudden change in load was reduced by 50%.

Fig.41 Comparison of transient response

Advantage 2 : Offers high efficiency for all load range.

・For lighter load:

Utilizes the current mode control mode called SLLM for lighter load, which reduces various dissipation such as switching dissipation (P_{SW}), gate charge/discharge dissipation, ESR dissipation of output capacitor (P_{ESR}) and on-resistance dissipation (P_{RON}) that may otherwise cause degradation in efficiency for lighter load.

Achieves efficiency improvement for lighter load.

・For heavier load:

Utilizes the synchronous rectifying mode and the low on-resistance MOS FETs incorporated as power transistor.

ON resistance of P-channel MOS FET: 0.35 Ω (Typ.)
ON resistance of N-channel MOS FET: 0.25 Ω (Typ.)

Achieves efficiency improvement for heavier load.

Offers high efficiency for all load range with the improvements mentioned above.

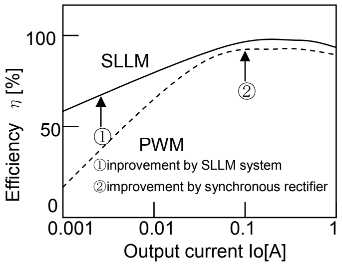


Fig.42 Efficiency

Advantage 3 : ・Supplied in smaller package like MOSP8 due to small-sized power MOS FET incorporated.
・Allows reduction in size of application products

・Output capacitor Co required for current mode control: 10 µF ceramic capacitor
・Inductance L required for the operating frequency of 1 MHz: 4.7 µH inductor

Reduces a mounting area required.

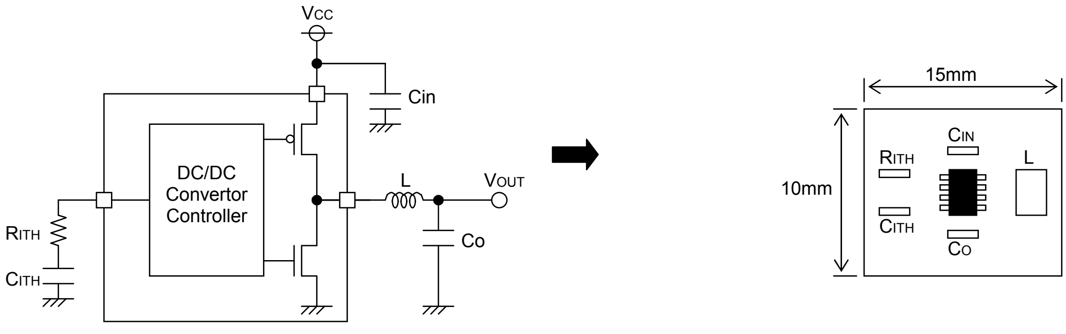


Fig.43 Example application

●Operation

BD910□FVM is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes SLLM (Simple Light Load Mode) operation for lighter load to improve efficiency.

○Synchronous rectifier

It does not require the power to be dissipated by a rectifier externally connected to a conventional DC/DC converter IC, and its P.N junction shoot-through protection circuit limits the shoot-through current during operation, by which the power dissipation of the set is reduced.

○Current mode PWM control

Synthesizes a PWM control signal with a inductor current feedback loop added to the voltage feedback.

・PWM (Pulse Width Modulation) control

The oscillation frequency for PWM is 1 MHz. SET signal form OSC turns ON a P-channel MOS FET (while a N-channel MOS FET is turned OFF), and an inductor current I_L increases. The current comparator (Current Comp) receives two signals, a current feedback control signal (SENSE: Voltage converted from I_L) and a voltage feedback control signal (FB), and issues a RESET signal if both input signals are identical to each other, and turns OFF the P-channel MOS FET (while a N-channel MOS FET is turned ON) for the rest of the fixed period. The PWM control repeat this operation.

・SLLM (Simple Light Load Mode) control

When the control mode is shifted from PWM for heavier load to the one for lighter load or vise versa, the switching pulse is designed to turn OFF with the device held operated in normal PWM control loop, which allows linear operation without voltage drop or deterioration in transient response during the mode switching from light load to heavy load or vise versa. Although the PWM control loop continues to operate with a SET signal from OSC and a RESET signal from Current Comp, it is so designed that the RESET signal is held issued if shifted to the light load mode, with which the switching is tuned OFF and the switching pulses are thinned out under control. Activating the switching intermittently reduces the switching dissipation and improves the efficiency.

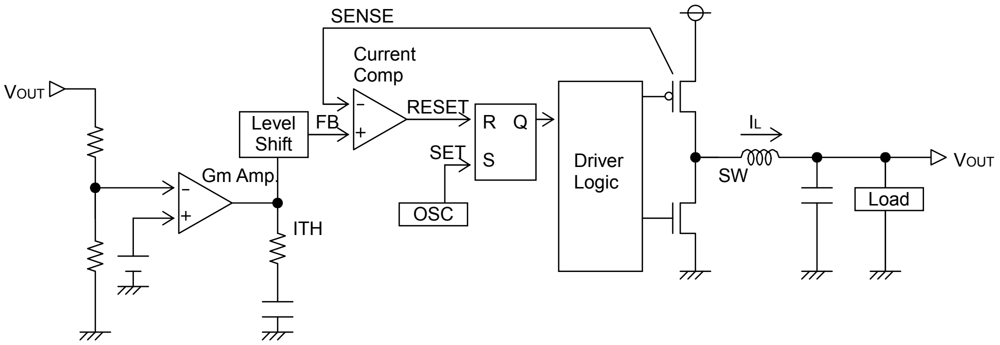
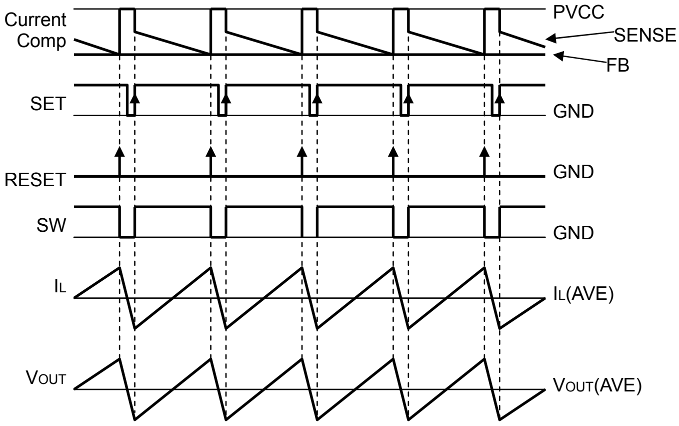


Fig.44 Diagram of current mode PWM control



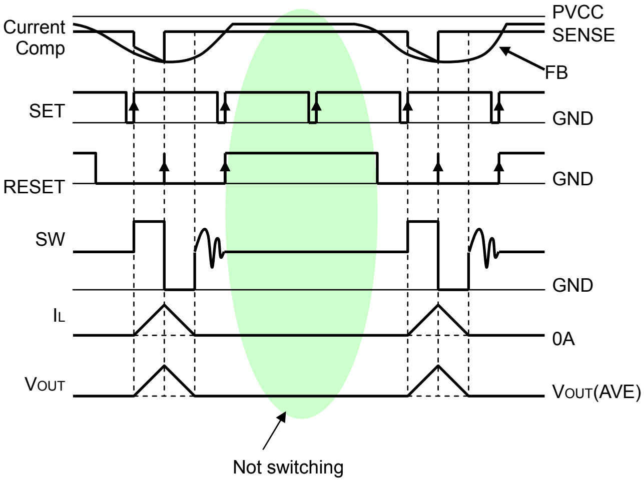


Fig.45 PWM switching timing chart

Fig.46 SLLM switching timing chart

●Description of operations

・Soft-start function

EN terminal shifted to “High” activates a soft-starter to gradually establish the output voltage with the current limited during startup, by which it is possible to prevent an overshoot of output voltage and an inrush current.

・Shutdown function

With EN terminal shifted to “Low”, the device turns to Standby Mode, and all the function blocks including reference voltage circuit, internal oscillator and drivers are turned to OFF. Circuit current during standby is 0 μF (Typ.).

・UVLO function

Detects whether the input voltage sufficient to secure the output voltage of this IC is supplied. And the hysteresis width of 100 mV (Typ.) is provided to prevent output chattering.

・BD9102FVM BD9104FVM

T_{SS}=1msec(typ.)

・BD9106FVM

T_{SS}=3msec(typ.)

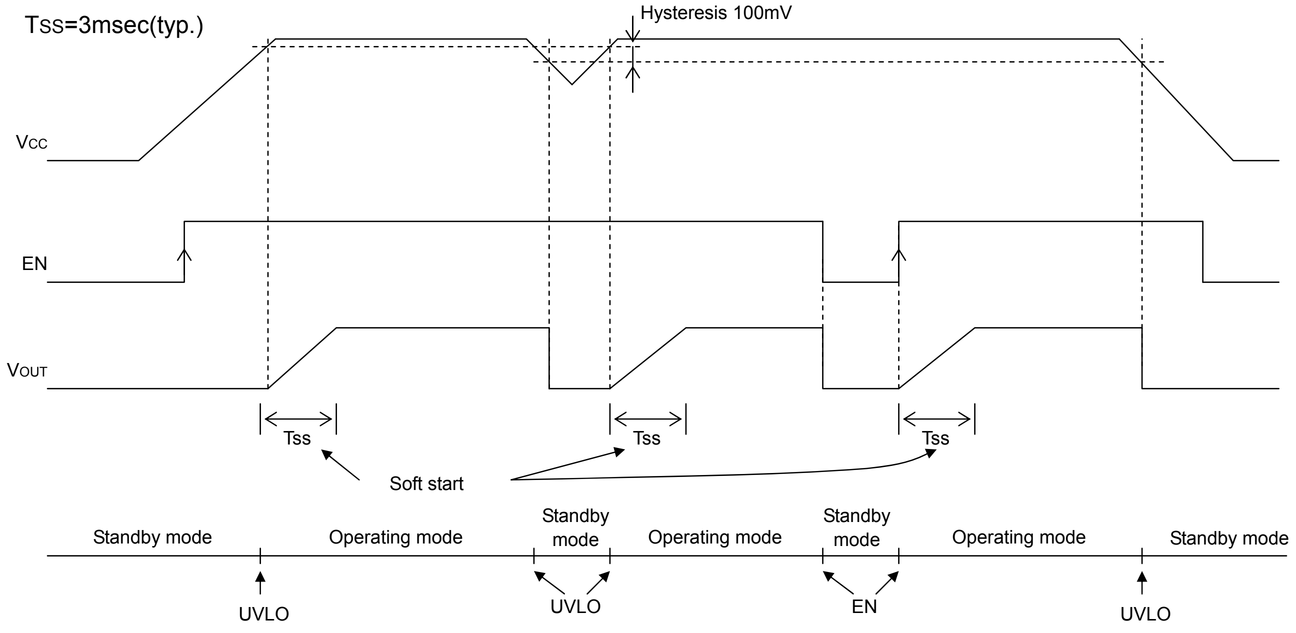


Fig.47 Soft start, Shutdown, UVLO timing chart

・Short-current protection circuit with time delay function

Turns OFF the output to protect the IC from breakdown when the incorporated current limiter is activated continuously for at least 1 ms. The output thus held tuned OFF may be recovered by restarting EN or by re-unlocking UVLO.

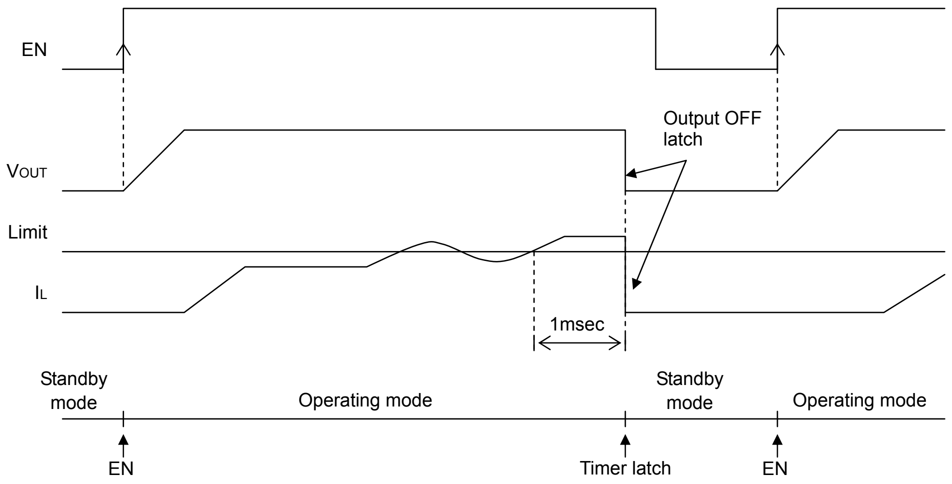


Fig.48 Short-current protection circuit with time delay timing chart

●Switching regulator efficiency

Efficiency η may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{Vin \times Iin} \times 100[\%] = \frac{P_{OUT}}{Pin} \times 100[\%] = \frac{P_{OUT}}{P_{OUT}+P_{D}\alpha} \times 100[\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors $P_D\alpha$ as follows:

Dissipation factors:
1) ON resistance dissipation of inductor and FET：$PD(I^2R)$
2) Gate charge/discharge dissipation：PD(Gate)
3) Switching dissipation：PD(SW)
4) ESR dissipation of capacitor：PD(ESR)
5) Operating current dissipation of IC：PD(IC)

1)$PD(I^2R)=I_{OUT}^2 \times (R_{COIL} \times R_{ON})$ ($R_{COIL}[\Omega]$：DC resistance of inductor, $R_{ON}[\Omega]$：ON resistance of FET
$I_{OUT}[A]$：Output current.)
2)$PD(Gate)=Cgs \times f \times V$ (Cgs[F]：Gate capacitance of FET,f[H]：Switching frequency,V[V]：Gate driving voltage of FET)
3)$PD(SW)=\dfrac{Vin^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$ ($C_{RSS}[F]$：Reverse transfer capacitance of FET,$I_{DRIVE}[A]$：Peak current of gate.)
4)$PD(ESR)=I_{RMS}^2 \times ESR$ ($I_{RMS}[A]$：Ripple current of capacitor,ESR[Ω]：Equivalent series resistance.)
5)$PD(IC)=Vin \times I_{CC}$ ($I_{CC}[A]$：Circuit current.)

●Consideration on permissible dissipation and heat generation

As this IC functions with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON resistance of FET are considered. Because the conduction losses are considered to play the leading role among other dissipation mentioned above including gate charge/discharge dissipation and switching dissipation.

$P=I_{OUT}^2 \times (R_{COIL}+R_{ON})$
$R_{ON}=D \times R_{ONP}+(1-D)R_{ONN}$

D：ON duty ($=V_{OUT}/V_{CC}$)
R_{COIL}：DC resistance of coil
R_{ONP}：ON resistance of P-channel MOS FET
R_{ONN}：ON resistance of N-channel MOS FET
I_{OUT}：Output current

If $V_{CC}=5V$, $V_{OUT}=3.3V$, $R_{COIL}=0.15\Omega$, $R_{ONP}=0.35\Omega$, $R_{ONN}=0.25\Omega$
$I_{OUT}=0.8A$, for example,
$D=V_{OUT}/V_{CC}=3.3/5=0.66$
$R_{ON}=0.66 \times 0.35+(1-0.66) \times 0.25$
$=0.231+0.085$
$=0.316[\Omega]$

$P=0.8^2 \times (0.15+0.316)$
$\fallingdotseq 298[mV]$

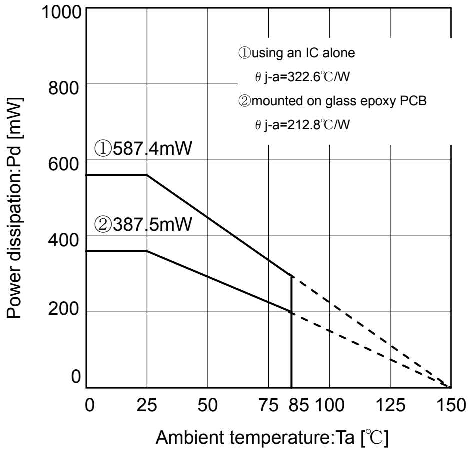


Fig.49 Thermal derating curves

As R_{ONP} is greater than R_{ONN} in this IC, the dissipation increases as the ON duty becomes greater. With the consideration on the dissipation as above, thermal design must be carried out with sufficient margin allowed.

●Selection of components externally connected

1. Selection of inductor (L)

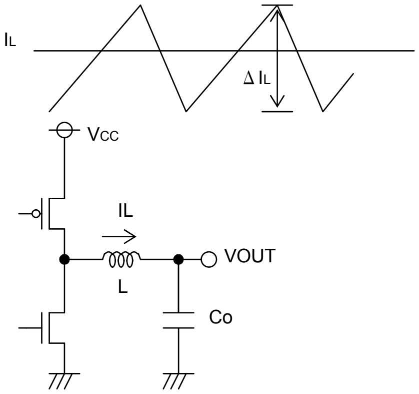


Fig.50 Output ripple current

The inductance significantly depends on output ripple current. As seen in the equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{L\times V_{CC}\times f}\ [A]\cdot\cdot\cdot(1)$$

Appropriate ripple current at output should be 30% more or less of the maximum output current.

$$\Delta I_L = 0.3\times I_{OUT}\text{max.}\ [A]\cdot\cdot\cdot(2)$$

$$L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{\Delta I_L\times V_{CC}\times f}\ [H]\cdot\cdot\cdot(3)$$

(ΔI_L: Output ripple current, and f: Switching frequency)

*Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

If V_{CC}=5V, V_{OUT}=3.3V, f=1MHz, $\Delta I_L=0.3\times 0.8A=0.24A$, for example,

$$L = \frac{(5-3.3)\times 3.3}{0.24\times 5\times 1M} = 4.675\mu \rightarrow 4.7[\mu H]$$

*Select the inductor of low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

2. Selection of output capacitor (CO)

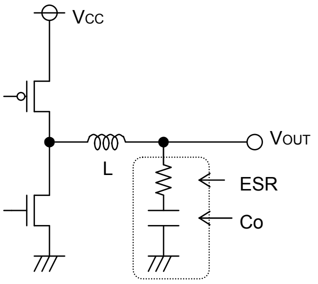


Fig.51 Output capacitor

Output capacitor should be selected with the consideration on the stability region and the equivalent series resistance required to smooth ripple voltage.
Output ripple voltage is determined by the equation (4) :

$$\Delta V_{OUT} = \Delta I_L\times ESR\ [V]\cdot\cdot\cdot(4)$$

(ΔI_L: Output ripple current, ESR: Equivalent series resistance of output capacitor)

*Rating of the capacitor should be determined allowing sufficient margin against output voltage. Less ESR allows reduction in output ripple voltage.

As the output rise time must be designed to fall within the soft-start time, the capacitance of output capacitor should be determined with consideration on the requirements of equation (5):

$$Co \leqq \frac{T_{SS}\times(I_{limit}-I_{OUT})}{V_{OUT}}\ \cdot\cdot\cdot(5)$$

Tss: Soft-start time
Ilimit: Over current detection level, 2A(Typ)

In case of BD9104FVM, for instance, and if V_{OUT}=3.3V, I_{OUT}=0.8A, and T_{SS}=1ms,

$$Co \leqq \frac{1m\times(2-0.8)}{3.3} \fallingdotseq 364\ [\mu F]$$

Inappropriate capacitance may cause problem in startup. A 10 μF to 100 μF ceramic capacitor is recommended.

3. Selection of input capacitor (Cin)

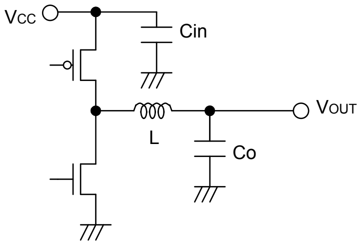


Fig.52 Input capacitor

Input capacitor to select must be a low ESR capacitor of the capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current IRMS is given by the equation (6):

$$I_{RMS} = I_{OUT}\times\frac{\sqrt{V_{CC}(V_{CC}-V_{OUT})}}{V_{CC}}\ [A]\cdot\cdot\cdot(6)$$

< Worst case > $I_{RMS(max.)}$

When VCC is twice the Vout, $I_{RMS} = \frac{I_{OUT}}{2}$

If V_{CC}=5V, V_{OUT}=3.3V, and I_{OUT}max.=0.8A,

$$I_{RMS} = 0.8\times\frac{\sqrt{5(5-3.3)}}{5} = 0.46[A_{RMS}]$$

A low ESR 10μF/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

4. Determination of RITH, CITH that works as a phase compensator

As the Current Mode Control is designed to limit a inductor current, a pole (phase lag) appears in the low frequency area due to a CR filter consisting of a output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR. So, the phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.

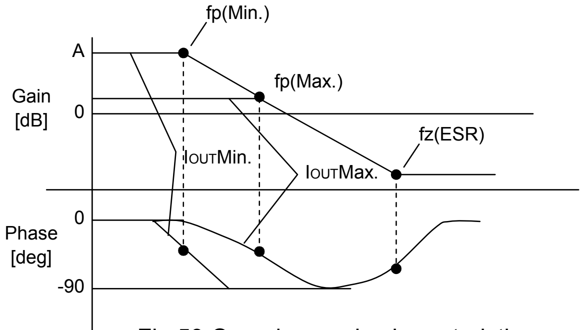


Fig.53 Open loop gain characteristics

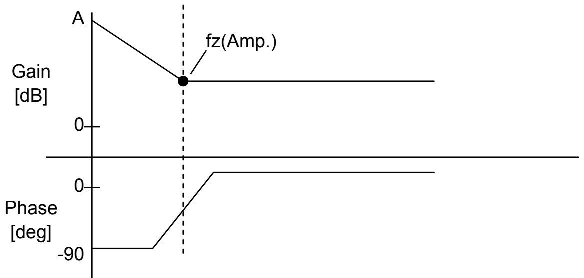


Fig.54 Error amp phase compensation characteristics

$$fp = \frac{1}{2\pi \times R_O \times C_O}$$

$$fz_{(ESR)} = \frac{1}{2\pi \times ESR \times C_O}$$

Pole at power amplifier

When the output current decreases, the load resistance Ro increases and the pole frequency lowers.

$$fp_{(Min.)} = \frac{1}{2\pi \times R_{OMax.} \times C_O} \quad \text{[Hz]} \leftarrow \text{with lighter load}$$

$$fp_{(Max.)} = \frac{1}{2\pi \times R_{OMin.} \times C_O} \quad \text{[Hz]} \leftarrow \text{with heavier load}$$

Zero at power amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change. (This is because when the capacitance is doubled, the capacitor ESR reduces to half.)

$$fz_{(Amp.)} = \frac{1}{2\pi \times R_{ITH.} \times C_{ITH}}$$

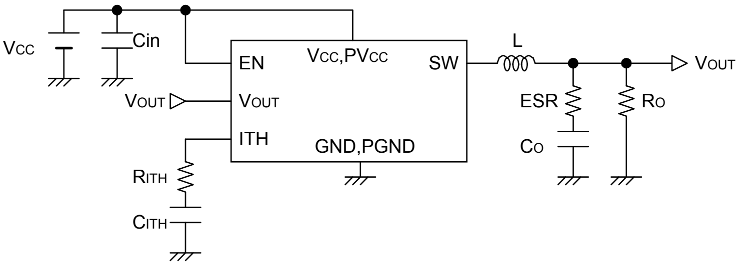


Fig.55 Typical application

Stable feedback loop may be achieved by canceling the pole fp (Min.) produced by the output capacitor and the load resistance with CR zero correction by the error amplifier.

$$fz_{(Amp.)} = fp_{(Min.)}$$

$$\longrightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times R_{OMax.} \times C_O}$$

5. Determination of output voltage (for BD9106FVM only)

The output voltage V_{OUT} is determined by the equation (7):

$V_{OUT} = (R2/R1+1) \times V_{ADJ}$ ・・・(7) V_{ADJ}: Voltage at ADJ terminal (0.8V Typ.)

With R1 and R2 adjusted, the output voltage may be determined as required.

(Adjustable output voltage range : 1.0V～2.5V)

Use 1 kΩ～100 kΩ resistor for R1. If a resistor of the resistance higher than 100 kΩ is used, check the assembled set carefully for ripple voltage etc.

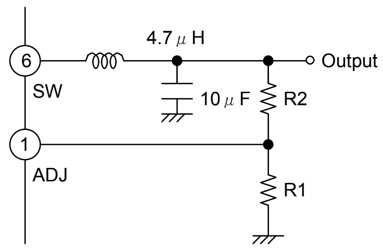


Fig.56 Determination of output voltage

●BD910□FVM　Cautions on PC Board layout

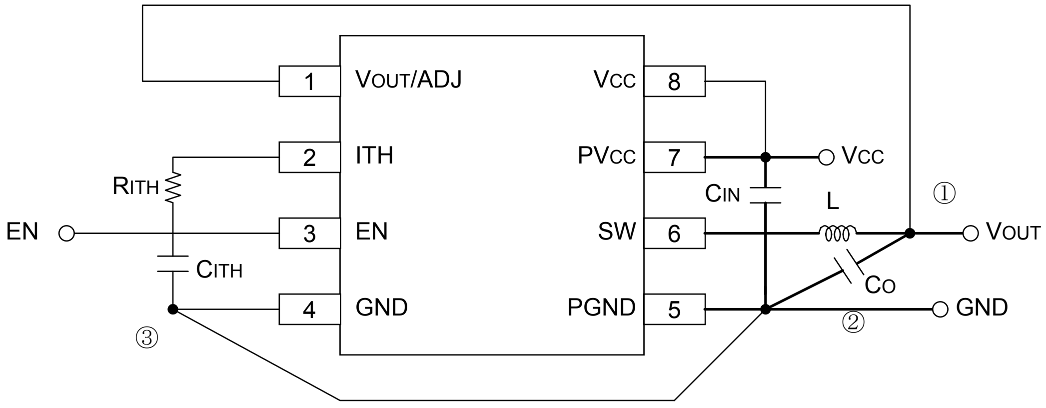


Fig.57 Layout diagram

① For the sections drawn with heavy line, use thick conductor pattern as short as possible.
② Lay out the input ceramic capacitor CIN closer to the pins PVCC and PGND, and the output capacitor Co closer to the pin PGND.
③ Lay out CITH and RITH between the pins ITH and GND as neat as possible with least necessary wiring.

Table1.Recommended parts list of application [BD9102FVM]

symbol	part	value	manufacturer	series
L	Inductor	4.7 μ H	Sumida	CMD6D11B
CIN	Ceramic capacitor	10 μ F	Kyocera	CM316X5R106M10A
CO	Ceramic capacitor	10 μ F	Kyocera	CM316X5R106M10A
CITH	Ceramic capacitor	330pF	murata	GRM18series
RITH	Resistor	30kΩ	ROHM	MCR10 3002

Table2. Recommended parts list of application [BD9104FVM]

symbol	part	value	manufacturer	series
L	Inductor	4.7 μ H	Sumida	CMD6D11B
CIN	Ceramic capacitor	10 μ F	Kyocera	CM316X5R106M10A
CO	Ceramic capacitor	10 μ F	Kyocera	CM316X5R106M10A
CITH	Ceramic capacitor	330pF	murata	GRM18series
RITH	Resistor	51kΩ	ROHM	MCR10 5102

Table3.Recommended parts list of application [BD9106FVM]

symbol	part	value	manufacturer	series
L	Inductor	4.7μH	Sumida	CMD6D11B
C_{IN}	Ceramic capacitor	10μF	Kyocera	CM316X5R106M10A
C_O	Ceramic capacitor	10μF	Kyocera	CM316X5R106M10A
C_{ITH}	Ceramic capacitor	750pF	murata	GRM18series

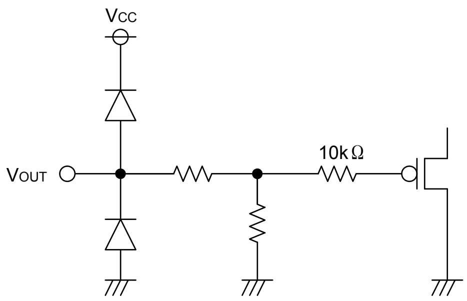
table4.BD9106FVM R_{ITH} recommended value

V_{OUT}[V]	R_{ITH}
1.0	18kΩ
1.2	22kΩ
1.5	22kΩ
1.8	27kΩ
2.5	36kΩ

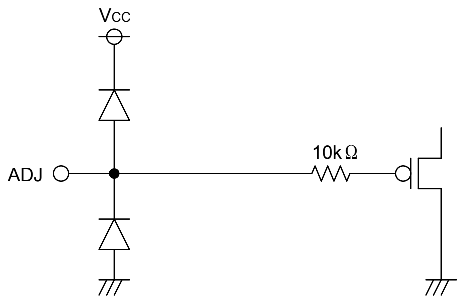
*BD9106FVM: As the resistance recommended for RITH depends on the output voltage, check the output voltage for determination of resistance.

●I/O equivalence circuit

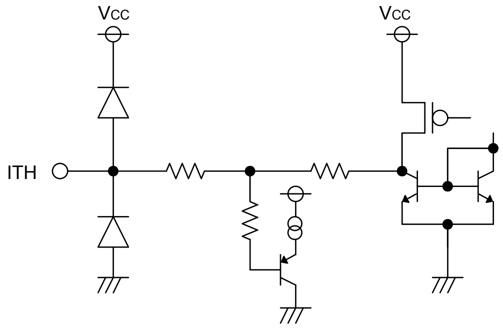
1pin(V_{OUT})



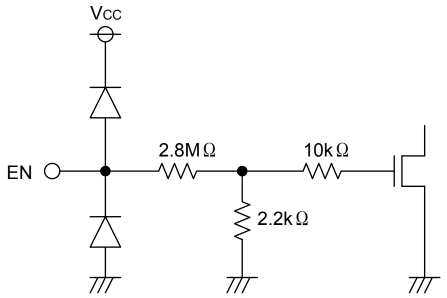
※BD9106FVM 1pin(ADJ)



2pin(ITH)



3pin(EN)



6pin(SW)

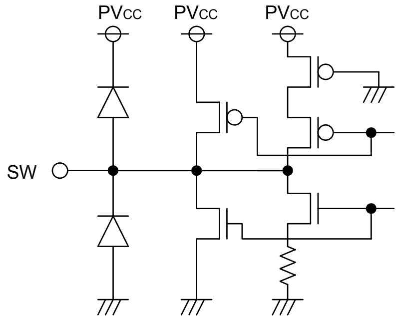


Fig.58 I/O equivalence circuit

●Cautions on use

1. Absolute Maximum Ratings

While utmost care is taken to quality control of this product, any application that may exceed some of the absolute maximum ratings including the voltage applied and the operating temperature range may result in breakage. If broken, short-mode or open-mode may not be identified. So if it is expected to encounter with special mode that may exceed the absolute maximum ratings, it is requested to take necessary safety measures physically including insertion of fuses.

2. Electrical potential at GND

GND must be designed to have the lowest electrical potential In any operating conditions.

3. Short-circuiting between terminals, and mismounting

When mounting to pc board, care must be taken to avoid mistake in its orientation and alignment. Failure to do so may result in IC breakdown. Short-circuiting due to foreign matters entered between output terminals, or between output and power supply or GND may also cause breakdown.

4.Operation in Strong electromagnetic field

Be noted that using the IC in the strong electromagnetic radiation can cause operation failures.

5. Thermal shutdown protection circuit

Thermal shutdown protection circuit is the circuit designed to isolate the IC from thermal runaway, and not intended to protect and guarantee the IC. So, the IC the thermal shutdown protection circuit of which is once activated should not be used thereafter for any operation originally intended.

6. Inspection with the IC set to a pc board

If a capacitor must be connected to the pin of lower impedance during inspection with the IC set to a pc board, the capacitor must be discharged after each process to avoid stress to the IC. For electrostatic protection, provide proper grounding to assembling processes with special care taken in handling and storage. When connecting to jigs in the inspection process, be sure to turn OFF the power supply before it is connected and removed.

7. Input to IC terminals

This is a monolithic IC with P^+ isolation between P-substrate and each element as illustrated below. This P-layer and the N-layer of each element form a P-N junction, and various parasitic element are formed.

If a resistor is joined to a transistor terminal as shown in Fig 59:

○P-N junction works as a parasitic diode if the following relationship is satisfied; GND>Terminal A (at resistor side), or GND>Terminal B (at transistor side); and

○if GND>Terminal B (at NPN transistor side),
a parasitic NPN transistor is activated by N-layer of other element adjacent to the above-mentioned parasitic diode.

The structure of the IC inevitably forms parasitic elements, the activation of which may cause interference among circuits, and/or malfunctions contributing to breakdown. It is therefore requested to take care not to use the device in such manner that the voltage lower than GND (at P-substrate) may be applied to the input terminal, which may result in activation of parasitic elements.

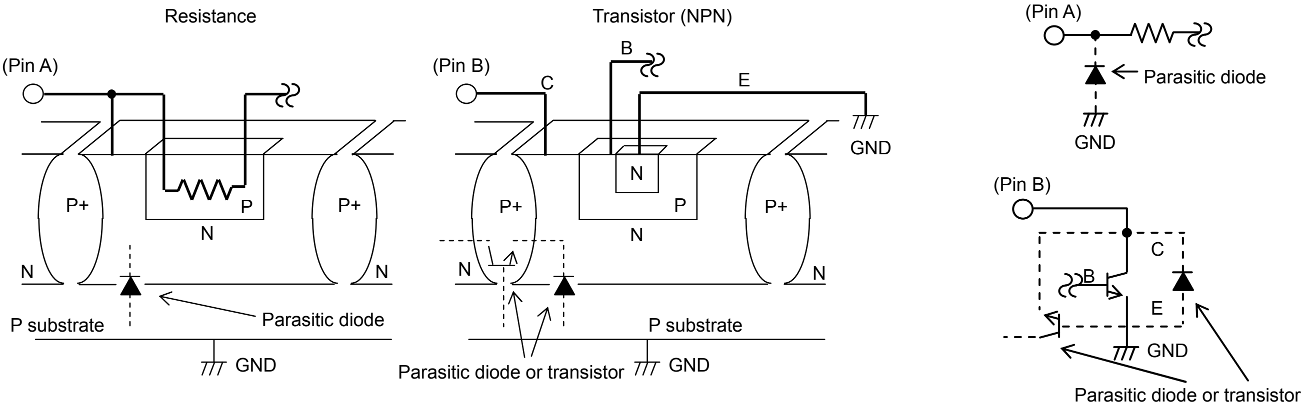


Fig.59 Simplified structure of monorisic IC

8. Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

●Ordering part number

B	D	9	1	0		F	V	M	–	T	R

ROHM part number

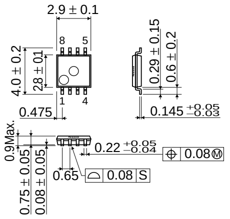
Type
2 : 1.24V output
4 : 3.3V output
6 : Adjustable

Package
FVM : MSOP8

Package specification
TR : Embossed taping

MSOP8

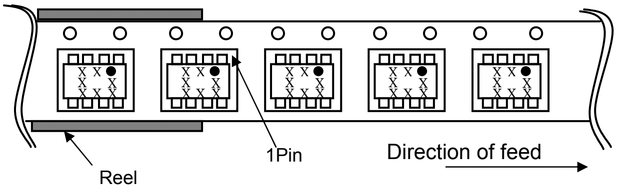
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper light when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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