3-V to 20-V INTEGRATED FET HOT SWAP CONTROLLER

Check for Samples: TPS2420

FEATURES

- **Integrated 30-mΩ Pass MOSFET**
- **3.0-V to 20-V Bus Operation**
- **Programmable Fault Current**
- **Programmable Hard Current Limit**
- **Programmable Fault Timer**
- **Internal MOSFET Power Limiting Foldback**
- **Latching and Auto-Retry Operation**
- **Analog Current Monitor Output**
- **Powergood Output**
- **Fault Output Indicator**
- **4 mm × 4 mm QFN**
- **–40°C to 125°C Junction Temperature Range**
- **UL Listed - File Number E169910**

APPLICATIONS

- **RAID Arrays**
- **Telecommunications**
- **Plug-In Circuit Boards**
- **Disk Drives**

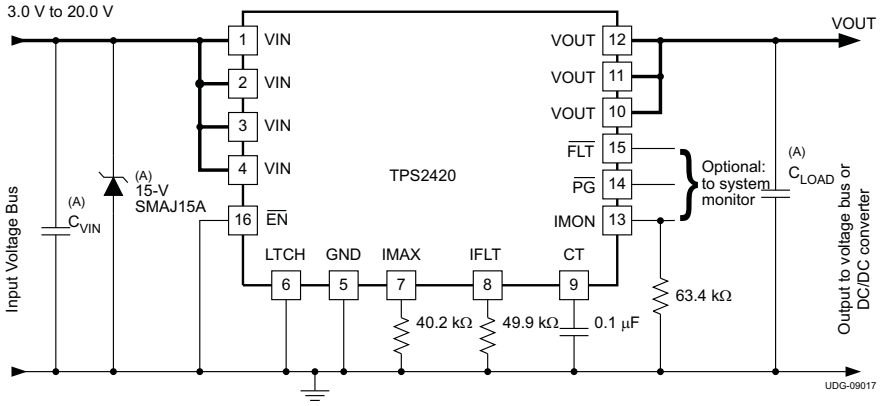
DESCRIPTION

The TPS2420 provides highly integrated load protection for 3-V to 20-V applications. The TPS2420 protects loads, minimizes inrush current, and safely shuts down in the event of a fault. The programmable fault current threshold starts the fault timer while allowing the current to pass to the load uninhibited. The programmable current limit threshold sets the maximum current allowed into the load, for both inrush and severe load faults. Both events use the programmable timer which inhibits all current to the load when it expires.

The dual protection thresholds are useful in applications such as disk drives. The start-up and seek currents are typically higher than the nominal current and during this time the load needs a low impedance path to deliver the power. If a failure at the load occurs, the current limit does not allow the current to exceed the programmed threshold. This protects both the load and the integrity of the power supply. The internal MOSFET is protected by power limit circuitry which ensures that the MOSFET remains within its safe operating area (SOA) during all operating states.

The TPS2420 also allows the system to monitor load currents with no need for a shunt in the power path. The gain of the current monitor can be scaled to the application. Fault and power good outputs are provided for improved system management and sequencing control.

This device can be programmed to either latch-off or retry in the event of a fault. All of this functionality is packed into a 16-pin 4 × 4 mm QFN package.



(A) Required only in systems with lead and/or load inductance.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPad is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT INFORMATION(1)

DEVICE	JUNCTION TEMPERATURE	PACKAGE	MARKING
TPS2420	–40°C to 125°C	RSA (4-mm × 4-mm QFN)	TPS2420

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{IN}, V_{OUT}	Voltage range	–0.3 to 25	V
$\overline{FLT}$, $\overline{PG}$	Voltage range	–0.3 to 20	
I_{FAULT}, I_{MAX}, C_T	Voltage	1.75	
$\overline{FLT}$, $\overline{PG}$	Output sink current	10	mA
$\overline{EN}$	Input voltage range	–0.3 to 6	V
LTCH	Input current (LTCH internally clamped to 3 V) LTCH = 0 V	35	µA
	Voltage range CT(3), IFLT(3), IMAX, IMON(3), LTCH	–0.3 to 3	V
	ESD rating, HBM	2500	
	ESD rating, CDM	400	
T_J	Operating junction temperature range	Internally Limited	°C
T_{stg}	Storage temperature range	–65 to 150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Do not apply voltage to these pins.

DISSIPATION RATINGS(1)

PACKAGE	θ_{JA} LOW K(2), °C/W	θ_{JA} HIGH K(3), °C/W	θ_{JA} BEST(4), °C/W
RSA	211	55	50

(1) Tested per JEDEC JESD51, natural convection. The definitions of high-k and low-k are per JESD 51-7 and JESD 51-3.
(2) Low-k (2 signal – no plane, 3-inch by 3-inch board, 0.062 inch thick, 1 oz. copper) test board with the pad soldered, and an additional 0.12 inch 2 of top-side copper added to the pad.
(3) High-k is a (2 signal – 2 plane) test board with the pad soldered.
(4) The best case thermal resistance is obtained using the recommendations per SLMA002A (2 signal – 2 plane with the pad connected to the plane).

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MIN	MAX	UNIT
VIN, VOUT	Voltage range	3	20	V
$\overline{EN}$	Voltage range	0	5	V
$\overline{FLT}$, $\overline{PG}$	Voltage range	0	20	V
$\overline{FLT}$, $\overline{PG}$	Output sink current	0	1	mA
LTCH	Voltage range	0	3	V
CT		0.1	100	µF
T_J	Junction temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

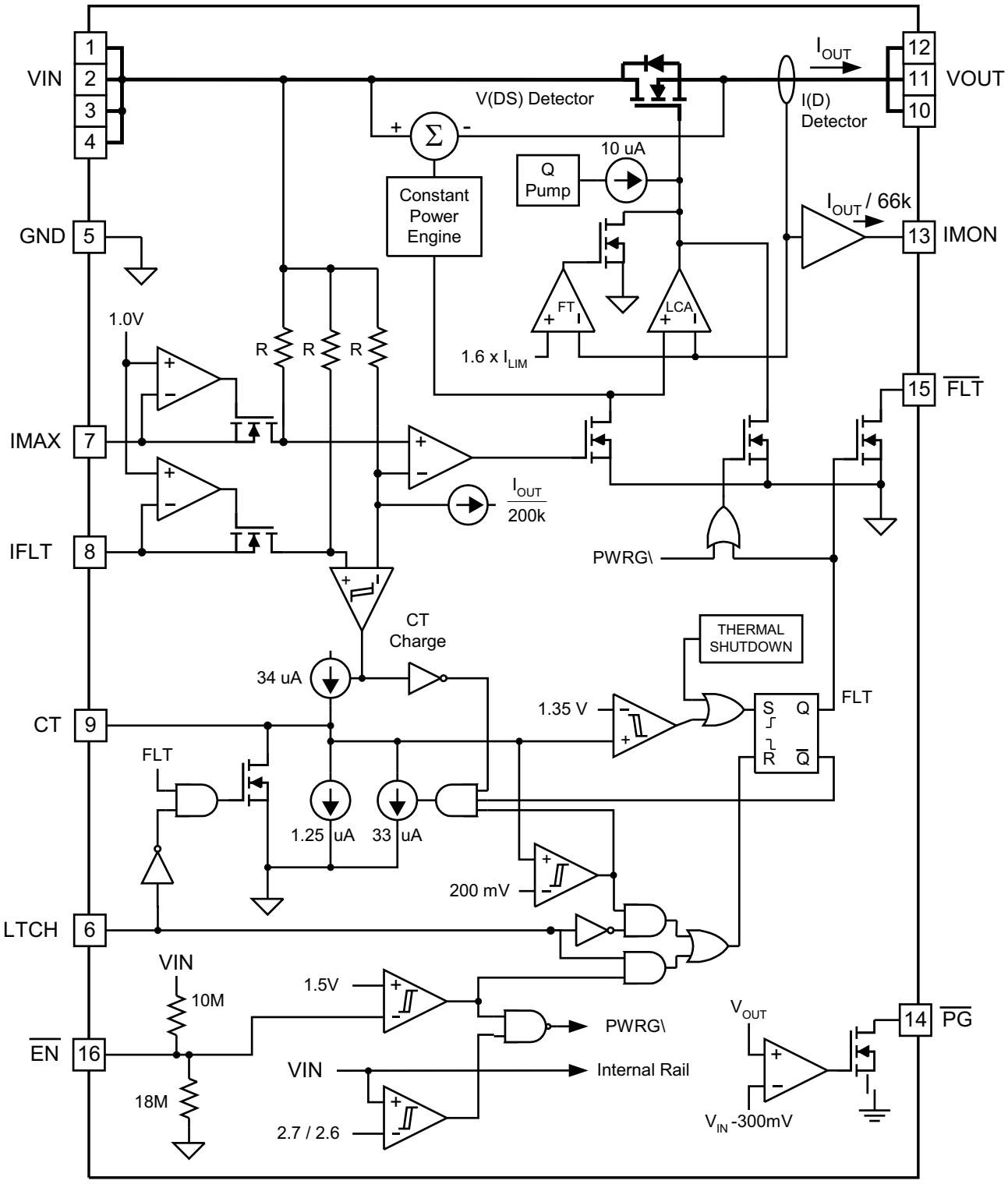
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (V_{IN})						
V_{UVLO}	Undervoltage lockout	V_{IN} increasing	2.6	2.85	2.9	V
		Hysteresis		150		mV
	Bias current	$V_{\overline{EN}}$ = 2.4 V		25	100	µA
		$V_{\overline{EN}}$ = 0 V		3.9	5	mA
INPUT/OUTPUT						
R_{ON}	On-resistance	$R_{VIN-VOUT}$, I_{VOUT} < I_{IMAX} or I_{VOUT} < (I_{SET} × 1.25), 1 A ≤ I_{VOUT} ≤ 4.5 A		33	50	mΩ
P_{LIMIT}	Power limit	V_{IN}= 12 V, C_{OUT} = 1000 µF EN: 3V → 0 V	3	5	7.5	W
	Reverse diode voltage	V_{OUT} > V_{IN}, $\overline{EN}$ = 5 V, I_{IN} = –1 A		0.77	1.0	V
FAULT CURRENT ($_{\overline{FLT}}$)						
$I_{\overline{FLT}}$	Fault current threshold	I_{VOUT} increasing, I_{CT} from sinking to sourcing, pulsed test				A
		$R_{\overline{FLT}}$ = 200 kΩ	0.8	1	1.2	
		$R_{\overline{FLT}}$ = 100 kΩ	1.8	2	2.2	
		$R_{\overline{FLT}}$ = 49.9 kΩ	3.6	4	4.4	
CURRENT LIMIT (IMAX)						
I_{IMAX}	Current limit program I_{VOUT} ↑, $V_{VIN-VOUT}$ = 0.3 V, pulsed test	R_{IMAX} = 100 kΩ	1.6	2	2.4	A
		R_{IMAX} = 66.5 kΩ	2.6	3	3.4	
		R_{IMAX} = 40.2 kΩ	4.6	5	5.4	
FAULT TIMER (CT)						
	Charge/Discharge current	I_{CT} sourcing, V_{CT} = 1 V, In current limit	29	35	41	µA
		I_{CT} sinking, V_{CT} = 1 V, drive CT to 1 V, measure current	1.0	1.4	1.8	
	Threshold voltage	V_{CT} increasing	1.3	1.4	1.5	V
		V_{CT} decreasing	0.1	0.16	0.3	
D	ON/OFF fault duty cycle	V_{VOUT} = 0 V	2.8%	3.7%	4.6%	
ENABLE ($_{EN}$)						
	Threshold voltage	$V_{\overline{EN}}$ decreasing	0.8	1.0	1.5	V
		Hysteresis	50	150	250	mV
	Input bias current	$V_{\overline{EN}}$ = 2.4 V (sinking)	–1.5	0	0.5	µA
		$V_{\overline{EN}}$ = 0.2 V (sourcing)	2	1	0.5	
	Turn on propagation delay	V_{IN} = 3.3 V, I_{LOAD} = 1 A, $V_{\overline{EN}}$: 2.4 V → 0.2 V, VOUT: ↑ 90% × V_{IN}		350	500	µs
	Turn off propagation delay	V_{IN} = 3.3 V, I_{LOAD} = 1 A, $V_{\overline{EN}}$: 0.2 V → 2.4V, V_{OUT}: ↓ 10% × V_{IN}		30	50	

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

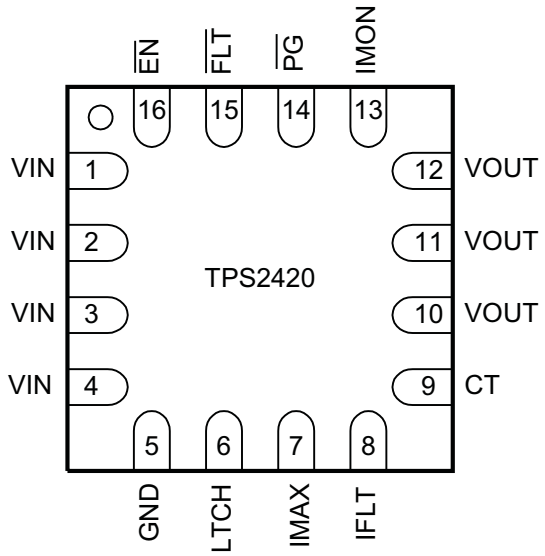
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FAULT (IFLT)						
V_{OL}	Low-level output voltage	V_{CT} = 1.8 V, $I_{\overline{FLT}}$ = 1 mA		0.2	0.4	V
I_{IFLT}	Leakage current	$V_{\overline{FLT}}$ = 18 V			1	µA
POWERGOOD ($\overline{PG}$)						
$V_{\overline{PG}}$	PG threshold	$V_{(VIN-VOUT)}$ decreasing	0.4	0.5	0.65	V
		Hysteresis	0.1	0.25	0.4	
V_{OL}	Low-level output voltage	$I_{\overline{PG}}$ = 1 mA		0.2	0.4	
$I_{\overline{PG}}$	Leakage current	$V_{\overline{PG}}$ = 18 V			1	µA
CURRENT MONITOR (IMON)						
	Ratio I_{LOAD}/I_{IMON}	I_{OUT} = 500 mA	30	56	80	A/mA
		I_{OUT} = 2.0 A	50	61	70	
		I_{OUT} = 4.50 A	56	61	66	
	Offset current (sourcing)	I_{VIN} = 0 A	–10	–2	0	µA
	Clamp voltage		2.6	2.75	2.9	V
LATCH FUNCTION (LTCH)						
	Low threshold voltage	Auto retry mode			0.8	V
	High threshold	Latch mode	2.0			
	Input bias current	V_{LTCH} = 3.0 V	–1.0	0.2	1.0	µA
		V_{LTCH} = 0.2 V	–50	–25	0	
THERMAL SHUTDOWN						
	Thermal shutdown	Junction temperature increasing		160		°C
		Hysteresis		10		

TPS2420 FUNCTIONAL BLOCK DIAGRAM



DEVICE INFORMATION

PINOUT DIAGRAM



TERMINAL FUNCTIONS

NAME	PIN NO.	I/O	DESCRIPTION
$\overline{EN}$	16	I	Device is enabled when this pin is pulled low.
VIN	1	I	Power in and control supply voltage .
	2		
	3		
	4		
LTCH	6	I	If low, the TPS2420 will attempt to restart after an overcurrent fault. If floating (high) the device will latch off after an overcurrent fault and will not attempt to restart until $\overline{EN}$ or V_{IN} is cycled off and on.
GND	5	—	Ground.
IMAX	7	I	A resistor to ground sets the current limit level.
IFLT	8	I	A resistor to ground sets the fault current level.
CT	9	I/O	A capacitor to ground sets the fault time.
IMON	13	O	A scaled down current which indicates the current through the device.
VOUT	10	O	Output to the load.
	11		
	12		
$\overline{PG}$	14	O	Power Good low represents the output voltage is within 300 mV of the input voltage.
$\overline{FLT}$	15	O	Fault low indicated the fault time has expired and the FET is switched off.

PIN DESCRIPTION

CT: Connect a capacitor form CT to GND to set the fault time. The fault timer starts when the fault current threshold is exceeded, charging the capacitor with 36 µA from GND towards an upper threshold of 1.4 V. If the capacitor reaches the upper threshold, the internal pass MOSFET is turned off. The MOSFET will stay off until $\overline{EN}$ is cycled if a latching version is used. If an auto-retry version is used, the capacitor will discharge at 5 µA to 0.2 V and then re-enable the pass MOSFET. When the device is disabled, CT is pulled to GND through a 100-kΩ resistor.

The timer period must be chosen long enough to allow the external load capacitance to charge. The fault timer period is selected using the following formula where T_{FAULT} is the minimum timer period in seconds and C_{CT} is in Farads.

$$C_{CT} = \frac{T_{FAULT}}{38.9 \times 10^3} \quad (1)$$

This equation does not account for component tolerances. In autoretry versions, the second and subsequent retry timer periods will be approximately 85% as long as the first retry period.

In autoretry versions, the fault timer discharges the capacitor for a nominal T_{SD} in seconds with C_{CT} in Farads per the following equation.

$$T_{SD} = 1.0 \times 10^6 \times C_{CT} \quad (2)$$

The nominal ratio of on to off times represents about a 3% duty cycle when a hard fault is present on the output of an autoretry version device.

$\overline{FLT}$: Open-drain output that pulls low on any condition that causes the output to open. These conditions are either an overload with a fault time-out, or a thermal shutdown. $\overline{FLT}$ becomes operational before UV, when V_{IN} is greater than 1 volt.

GND: This is the most negative voltage in the circuit and is used as reference for all voltage measurements unless otherwise specified.

IFLT: A resistor connected from this pin to ground sets the fault current threshold (I_{FAULT}). Currents between the fault current threshold and the current limit are permitted to flow unimpeded for the period set by the fault timer programmed on C_T. This permits loads to draw momentary surges while maintaining the protection provided by a lower average-current limit. IFLT may not be set below 1 A to maintain the Fault Current Limit threshold accuracy listed in Electrical Characteristics. Some parts may not current limit or fault as expected.

The fault timer implemented by C_T starts charging C_T when current through V_{IN} exceeds I_{FAULT}. If the current doesn't drop below the I_{FAULT} level before V_{CT} reaches its upper threshold, the output will be shut off. The fault current resistor is set by the following formula where I_{FAULT} is in Amperes and R_{RFLT} is in ohms.

$$R_{IFLT} = \frac{200\,k\Omega}{I_{FAULT}} \quad (3)$$

IMAX: A resistor connected from this pin to ground sets I_{MAX}. The TPS2420 will limit current to I_{MAX}. If the current does not drop below the I_{FAULT} level before the timer times out then the output will be shut off. R_{MAX} is set by the formula:

$$R_{IMAX} = \frac{201k\Omega}{I_{IMAX}} \quad (4)$$

I_{MAX} must be set sufficiently larger than I_{FAULT} to ensure that I_{MAX} could never be less than I_{FAULT}, even after taking tolerances into account.

$\overline{EN}$: When this pin is pulled low, the device is enabled. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit. $\overline{EN}$ is pulled to V_{IN} by a 10-MΩ resistor, pulled to GND by 16.8 MΩ and is clamped to ground by a 7-V Zener diode. Because high impedance pullup/down resistors are used to reduce current draw, any external FET controlling this pin should be low leakage.

VIN: Input voltage to the TPS2420. The recommended operating voltage range is 3 V to 18 V. All VIN pins should be connected together and to the power source.

VOUT: Output connection for the TPS2420. When switched on the output voltage will be approximately:

$$V_{OUT} = V_{IN} - 0.04 \times I_{OUT} \quad (5)$$

All V_{OUT} pins should be connected together and to the load.

LTCH: When pulled low the 2420 will attempt to restart after a fault. If left floating or pulled high the TPS2420 will latch off after a fault. This pin is internally clamped at 3 V and is pulled to the internal 3-V supply by diode in series with a 100-kΩ resistor.

$\overline{\text{PG}}$: Active low, Open Drain output, Power Good indicates that there is no fault condition and the output voltage is within 0.5 V of the input voltage. $\overline{\text{PG}}$ becomes operational before UV, whenever V_{IN} is greater than 1 V.

IMON: This is a scaled analog output of I_{VIN}. Select R_{IMON} based on the maximum allowed A/D input voltage (V_{AD_FS}) and the desired full-scale current in VIN (I_{VIN_FS}) per the following equation

$$R_{IMON} = \frac{63\,k\Omega \times V_{AD\_IN(max)}}{I_{LOAD(max)}} \quad (6)$$

This pin is clamped at 2.5 V to protect A/D converters. It is reccomended that I_{MON} be ignored until after $\overline{\text{PG}}$ asserts because the I_{MON} output is accurate only after V_{OUT} > 3 V.

TYPICAL CHARACTERISTICS

CURRENT LIMIT vs JUNCTION TEMPERATURE

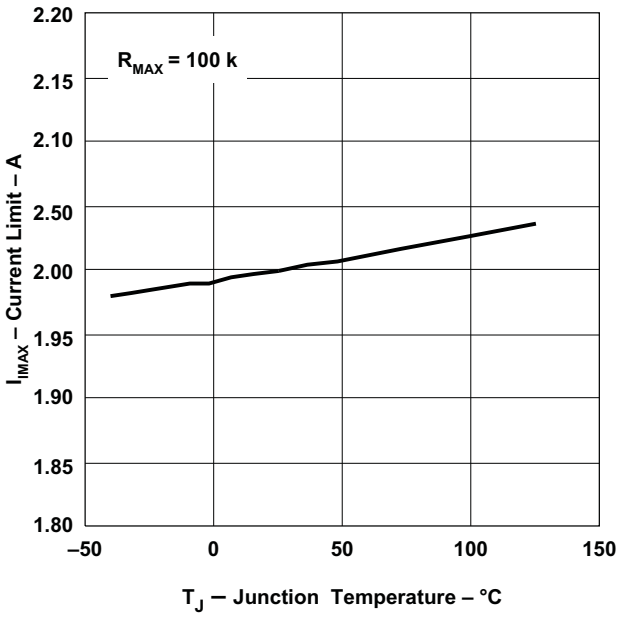


Figure 1.

FAULT CURRENT vs JUNCTION TEMPERATURE

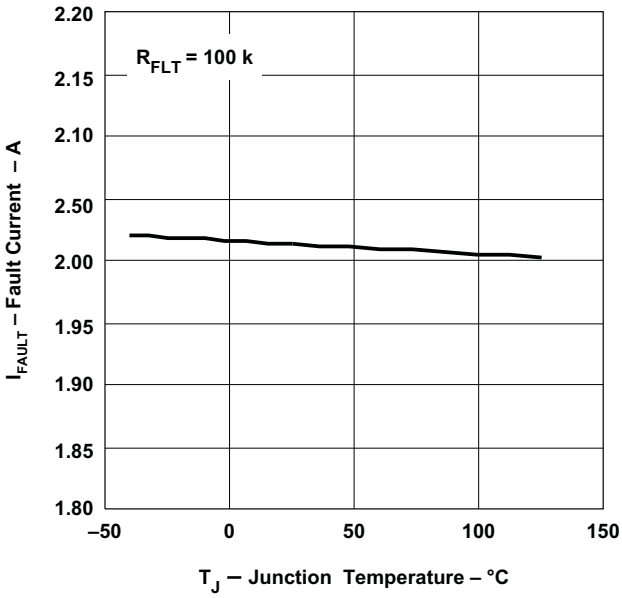


Figure 2.

POWER LIMIT vs JUNCTION TEMPERATURE

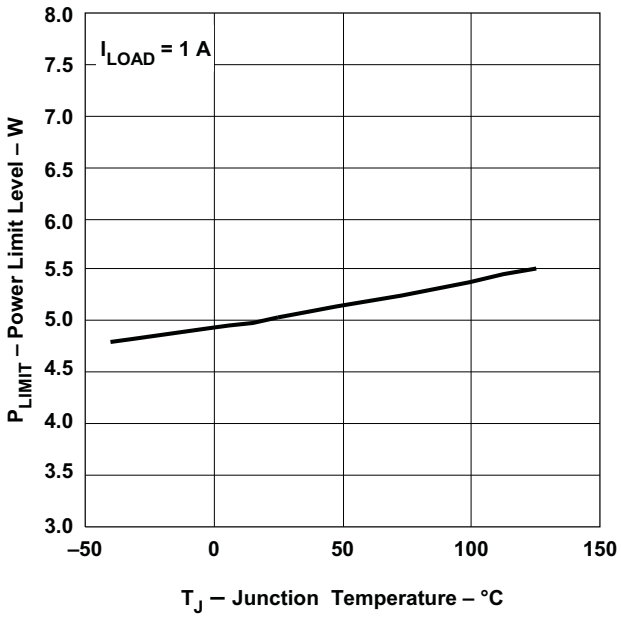


Figure 3.

SUPPLY CURRENT vs JUNCTION TEMPERATURE

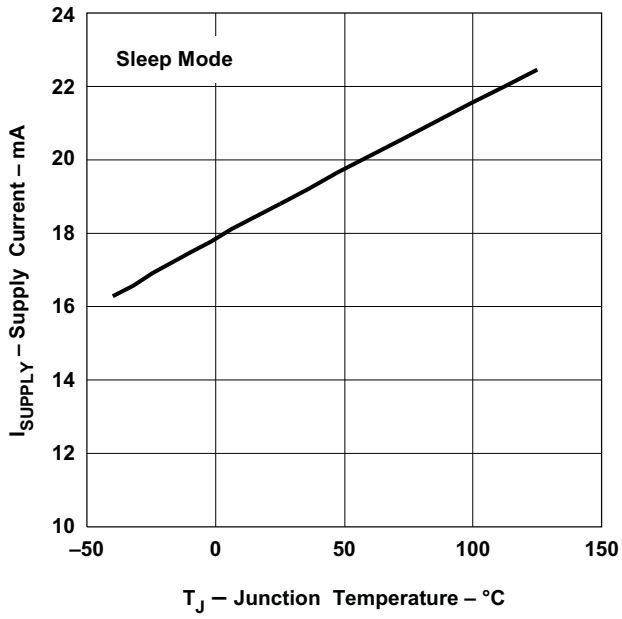


Figure 4.

TYPICAL CHARACTERISTICS (continued)

OUTPUT CURRENT vs JUNCTION TEMPERATURE

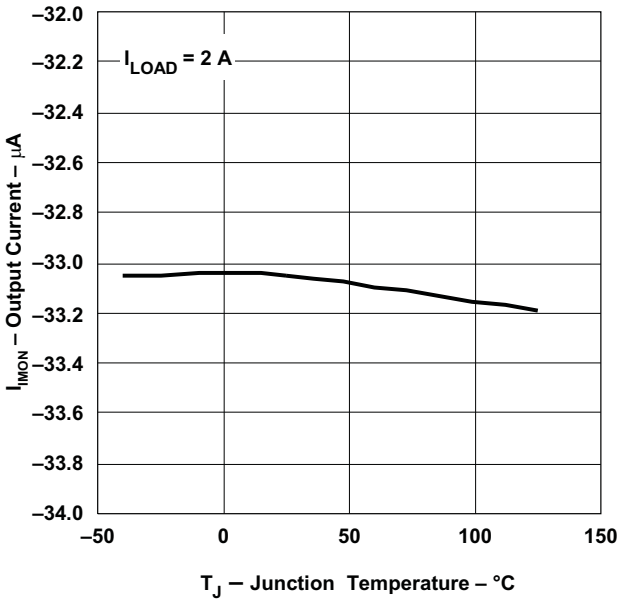


Figure 5.

FAULT TIMER THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

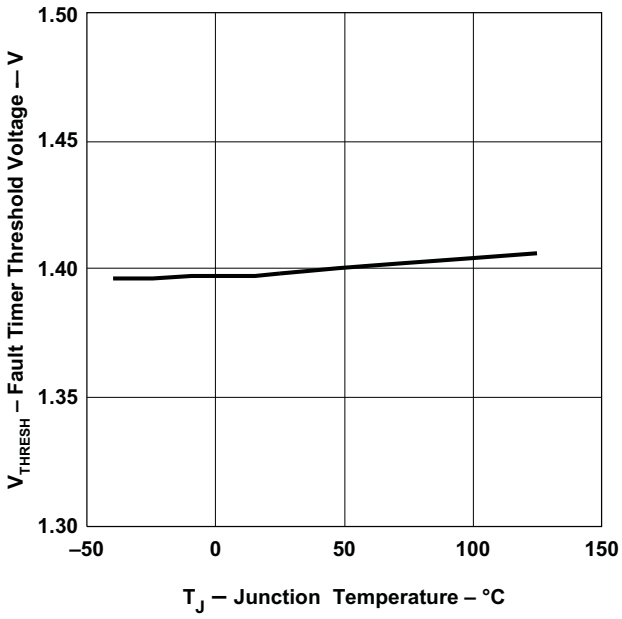


Figure 6.

TYPICAL CHARACTERISTICS

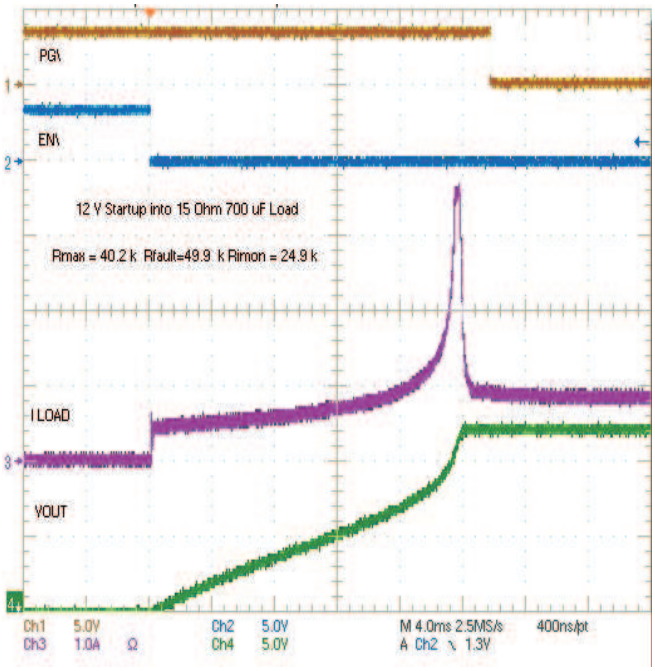


Figure 7. 12-V Startup into 15-Ω, 700-µF Load

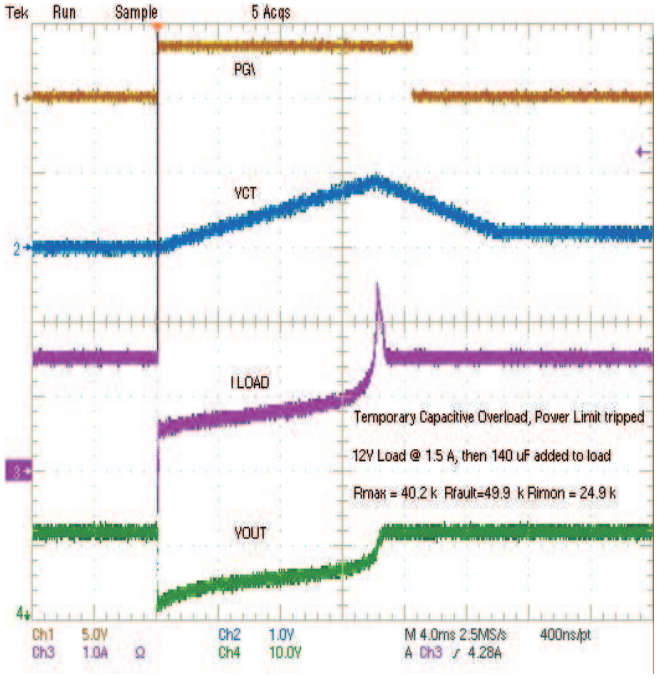


Figure 8. 12-V Input Addded to an 8-Ω Load

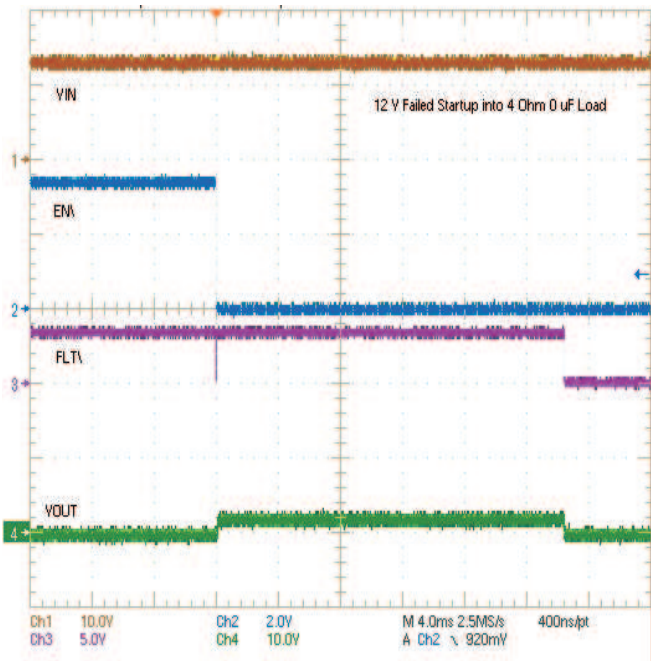


Figure 9. Failed Startup into a 4-Ω Load

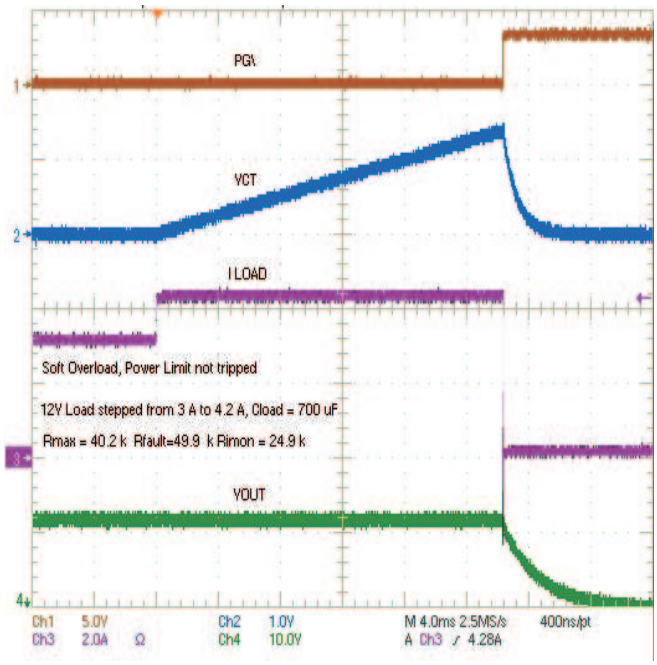


Figure 10. 12-V Soft Overload, 3-A to 4.2-A, Power Limit Not Tripped

TYPICAL CHARACTERISTICS (continued)

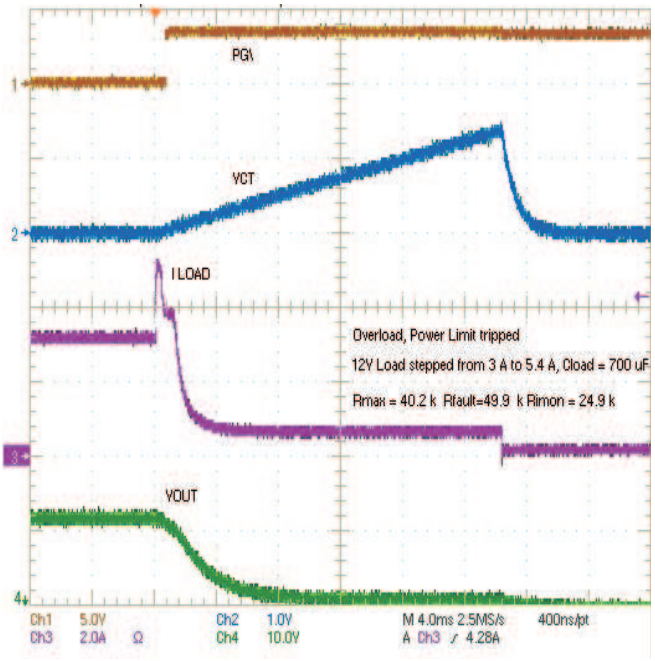


Figure 11. Firm Overload, 3-A to 5.4 A, Power Limit Tripped

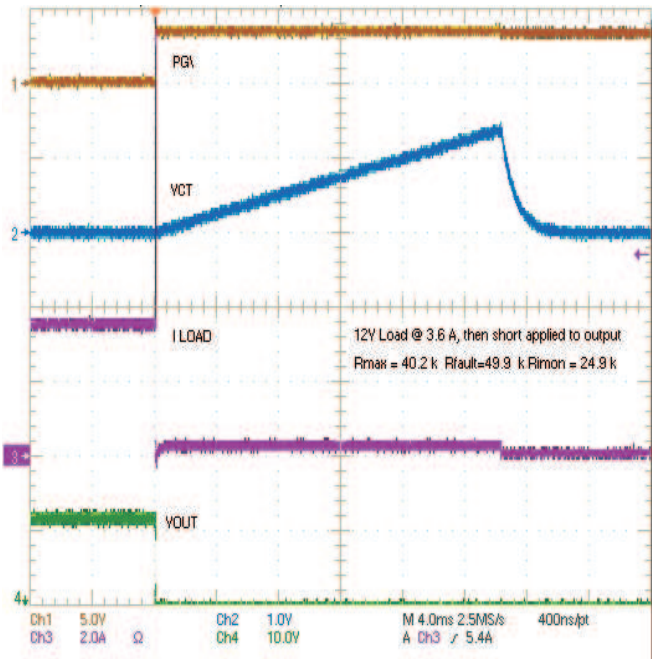


Figure 12. 12-V Hard Overload, 3.6-A Load then Short

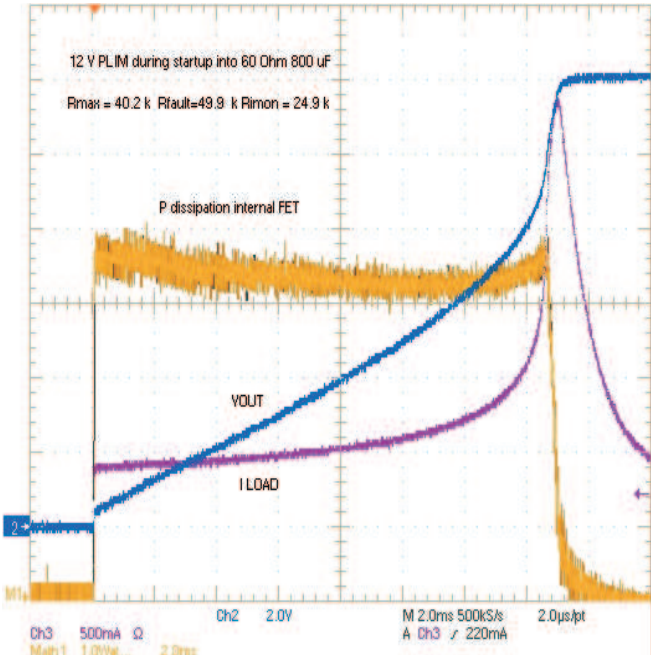


Figure 13. Power Dissipation During 12-V Startup into a 60-Ω, 800-µF Load

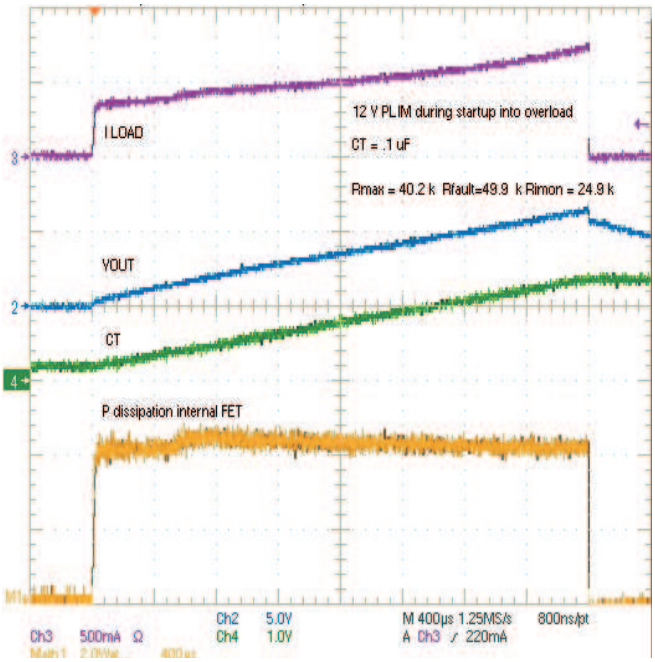


Figure 14. Power Dissipation During 12-V Startup into a 15-Ω, 140-µF Load

TYPICAL CHARACTERISTICS (continued)

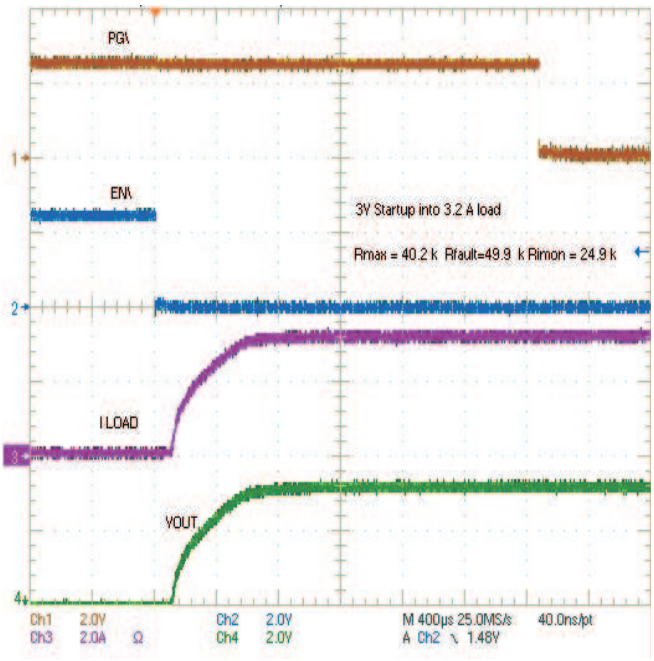


Figure 15. Startup into a 1-Ω Load

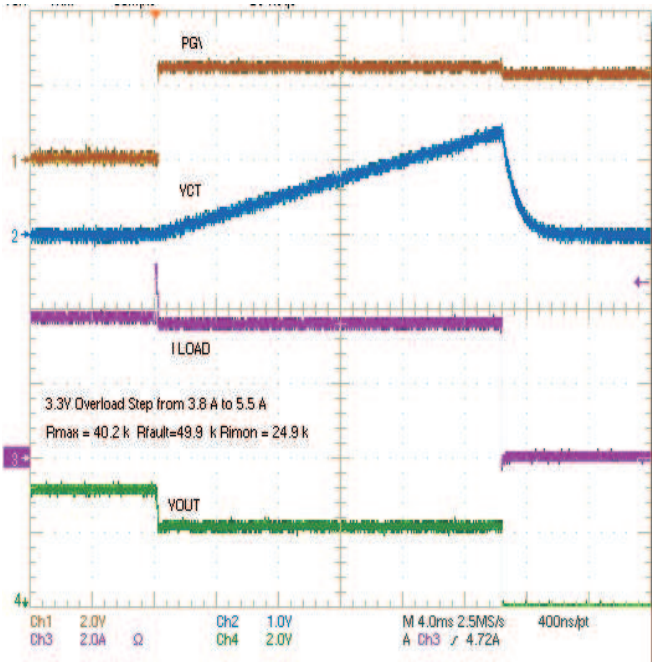


Figure 16. Firm Overload, Load Stepped From 3.8 A to 5.5 A

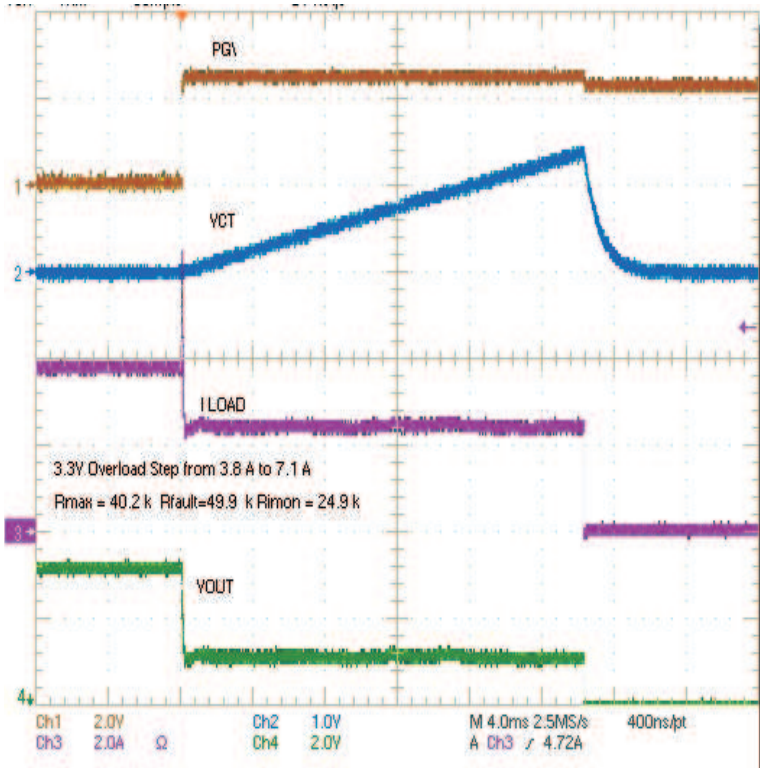


Figure 17. Hard Overload, Load Stepped from 3.8 A to 7.1 A

APPLICATION INFORMATION

If $\overline{EN}$ is tied to GND at startup and V_{IN} does not ramp quickly the TPS2420 may momentarily turn off then on during startup. This can happen if a capacitive load momentarily pulls down the input voltage below the UV threshold. If necessary, this can be avoided by delaying $\overline{EN}$ assertion until V_{IN} is fully up.

Maximum Load

The power limiting function of the TPS2420 provides very effective protection for the internal FET. Expectedly, there is a supply voltage dependent maximum load which the device will be able to power up. Loads above this level may cause the device to shut off current before startup is complete. Neglecting any load capacitance, the maximum load (minimum load resistance) is calculated using the equation;

$$R_{MIN} = \frac{V_{IN}^2}{12} \tag{7}$$

Adding load capacitance may reduce the maximum load which can be present at start up.

Transient Protection

The need for transient protection in conjunction with hot-swap controllers should always be considered. When the TPS2420 interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. Such transients can easily exceed twice the supply voltage if steps are not taken to address the issue. Typical methods for addressing transients include;

- Minimizing lead length/inductance into and out of the device
- Voltage Suppressors (TVS) on the input to absorb inductive spikes
- Shottky diode across the output to absorb negative spikes
- A combination of ceramic and electrolytic capacitors on the input and output to absorb energy
- Use PCB GND plane

The following equation estimates the magnitude of these voltage spikes:

$$V_{SPIKE(absolute)} = V_{NOM} + I_{LOAD} \times \sqrt{L/C} \tag{8}$$

where

- V_{NOM} is the nominal supply voltage
- I_{LOAD} is the load current
- C is the capacitance present at the input or output of the TPS2420
- L equals the effective inductance seen looking into the source or the load

Calculating the inductance due to a straight length of wire is shown in Equation 9.

$$L_{straightwire} \approx 0.2 \times L \times \ln\left(\frac{4 \times L}{D} - 0.75\right) (nH) \tag{9}$$

where

- L is the length of the wire
- D is diameter of the wire

Some applications may require the addition of a TVS to prevent transients from exceeding the absolute ratings if sufficient capacitance cannot be included.

APPLICATION INFORMATION

Operation

When load current exceeds the user programmed fault limit (I_{FAULT}) during normal operation the fault timer starts. If load current drops below the I_{FAULT} threshold before the fault timer expires, normal operation continues. If load current stays above the I_{FAULT} threshold the fault timer expires and a fault is declared. When a fault is declared a device operating in latch mode turns off and can be restarted by cycling power or toggling the $\overline{EN}$ signal. A device operating in retry mode attempts to turn on at a 3% duty cycle until the fault is cleared. When the I_{MAX} limit is reached during a fault the device goes into current limit and the fault timer keeps running. I_{MAX} can be programmed by the user by connecting a resistor from the IMAX pin to GND.

Startup

When power is first applied to a load with discharged capacitors there is a large inrush current. The inrush is controlled by the TPS2420 by initially entering the power limit mode and turning on the fault timer. See Figure 19. As the charge builds on the capacitor, the current increases to I_{MAX}. When the capacitor is fully charged, current output is set by the dc load value, The fault timer is turned off. The FET is then fully enhanced and the power good signal is true.

In order to start properly, the fault timer must be set to exceed the capacitor charge time.

When the load has a resistive component as well as capacitive, the fault time needs to be increased because current to the resistive load is unavailable to charge the capacitor. The startup time for some selected loading is given in Table 1.

Table 1 data was taken with I_{FAULT} set to 4 A and I_{MAX} set to 5 A. Lower current settings of TPS2420 do not have a great influence on the start up timer because of operation at power limit. Load capacitance and dc resistance was selected for a measured start time. The start time is measured from the assertion of the $\overline{EN}$ pin to the assertion of the $\overline{PG}$ pin.

Table 1. Start Time for Input Voltage and Output Loading (1)

INPUT VOLTAGE (V)	LOAD CAPACITANCE (µF)	DC LOAD RESISTANCE (Ω)	START TIME (ms)
5	220	OPEN	2.5
		5	2.7
		12	2.6
	1000	OPEN	4
		5	4
		12	4
12	220	OPEN	4.4
		5	No start
		12	7
	1000	OPEN	14
		5	No start
		12	23

(1) I_{FAULT} = 4 A, I_{MAX} = 5 A.

Some combinations of loading and current limit settings exceed the 5-W power limit of the internal MOSFET. The output voltage will not turn on regardless of the fault time setting. One way to work with the physical limits that create this problem is to allow the power manager to charge only the capacitive component of the load and use the $\overline{PG}$ signal to turn on the resistive component. This is common usage in dc-to-dc converters and other electrical equipment with power good inputs.

Start Up Into a Short

The controller attempts to power on into a short for the duration of the timer. Figure 20 shows a small current resulting from power limiting the internal MOSFET. This happens only once for the latch off mode. For the retry mode, Figure 24 shows this cycle repeating at an interval based on the C_T time.

Shutdown Modes

Hard Overload - Fast Trip

When a hard overload causes the load current to exceed 1.6 × I_{MAX} the TPS2420 immediately shuts off current to the load without waiting for the fault timer to expire. After such a shutoff the TPS2420 enters into startup mode and attempts to apply power to the load.

If the hard overload is caused by a current transient, then a normal startup can be expected with a low probability of disruption to the load, assuming there is sufficient load capacitance to hold up the load during the fractions of a millisecond that make up the fast trip/restart cycle.

If the hard overload is caused by a real, continuous failure then the TPS2420 goes into current limit during the attempt at restart. The timer starts and eventually runs out, shutting off current to the load. See the fast trip figures 22 and 23. When the hard overload occurs the current is turned off, the $\overline{PG}$ pin becomes false, and the $\overline{FLT}$ pin stays false. The $\overline{FLT}$ pin becomes true only when the fault timer times out.

Overcurrent Shutdown

Overcurrent shutdown occurs when the output current exceeds I_{MAX} for the duration of the fault timer. Overcurrent shutdown is the circuit breaker type protection of equipment. Figure 23 shows the step rise in output current. The increased current is on for the duration of the timer. At conclusion of the timer, the output is turned off.

Design Example

The TPS2420 Design shown in Figure 25 supports 12 V to operate a hot plugged disk drive.

The 12 V specification for a disk drive is approximately 1-A operating current and 2-A typical spin-up. Selecting a 2.5 A setting for I_{FAULT} would allow some margin for the operating current and satisfy the start current requirements.

Calculate R_{RFLT} using equation Equation 10 or select it using Table 2.

$$R_{IFLT} = \frac{200\,k\Omega}{I_{FAULT}} \times \frac{200{,}000}{2.5} = 80\ (k\Omega) \tag{10}$$

The I_{MAX} setting, 3.5 A, is set by R_{RMAX} in Equation 11.

$$R_{IMAX} = \frac{201k\Omega}{I_{IMAX}} \times \frac{201{,}000}{3.5} = 57.4\ (k\Omega) \tag{11}$$

Because I_{FAULT} satisfies the spin up current, the timer can be set for the additional loading of charging the capacitor. Estimate approximately 20 ms. Use either Equation 12 or Table 2 to estimate the capacitance.

$$C_{CT} = \frac{T_{FAULT}}{38.9 \times 10^{3}} = 20 \times \frac{10^{-3}}{38.9} \times 10^{3} = 0.514 \times 10^{-6} \quad (12)$$

For a scaled analog readback of the current from V_{IN}, set the I_{MON} resistor. In Equation 13 , the V_{AD_INMAX} is the desired full scale A/D converter voltage. The largest value of V_{AD_INMAX} 2.5 V. $I_{LOADMAX}$ is the full scale current, 2.5 A.

$$R_{IMON} = \frac{\left(63{,}000 \times V_{AD\_IN(max)}\right)}{I_{LOAD(max)}} = \frac{\left(63{,}000 \times 2.5\right)}{2.5} = 63\ \left(k\Omega\right) \quad (13)$$

The read-back voltage at the IMON pin, V_{IMON}, indicates the instantaneous current output. Using equation Equation 14 again, determine the current output for example, a 1.8-V V_{IMON}. Substitute V_{IMON} for V_{AD_INMAX} and I_{LOAD} for $I_{LOADMAX}$ and solve for I_{LOAD}, (Equation 14).

$$I_{LOAD} = \frac{\left(63{,}000 \times V_{IMON}\right)}{R_{IMON}} = \frac{\left(63{,}000 \times 1.8\right)}{62{,}500} = 1.81\left(A\right) \quad (14)$$

Layout

Support Components

Locate all TPS2420 support components, R_{SET}, C_T, etc. or any input or output voltage clamps, close to their connection pin. Connect the other end of the component to the inner layer GND without trace length.

PowerPad™

When properly mounted the PowerPad package provides significantly greater cooling ability than an ordinary package. To operate at rated power the Power Pad must be soldered directly to the PC board GND plane directly under the device. The PowerPad is at GND potential and can be connected using multiple vias to inner layer GND. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications.

Refer to Technical Briefs: *PowerPAD™ Thermally Enhanced Package* (TI Literature Number SLMA002) and *PowerPAD™ Made Easy* (TI Literature Number SLMA004) for more information on using this PowerPadTM package.These documents are available at www.ti.com (Search by Keyword).

APPLICATION PLOTS

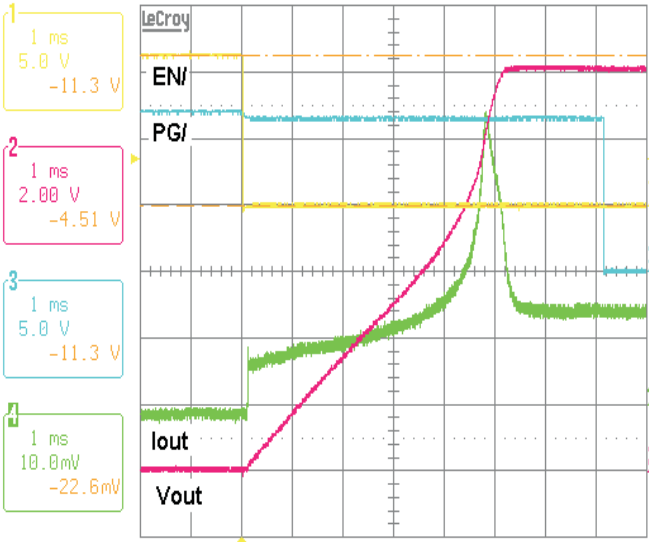


Figure 18. Start Up Into an RC Load ($\overline{PG}$)

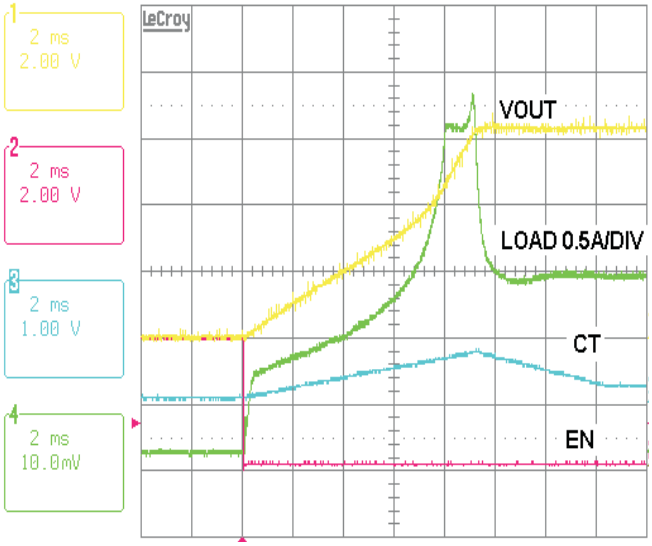


Figure 19. Start Up Into an RC Load (CT)

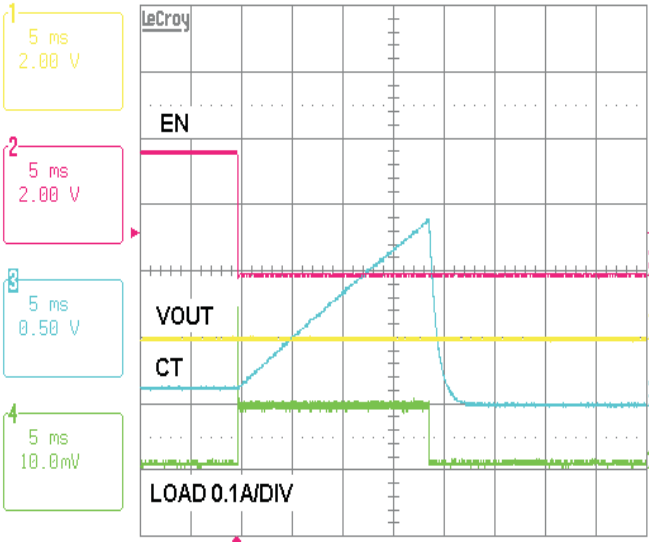


Figure 20. Startup Into a Short Circuit Output

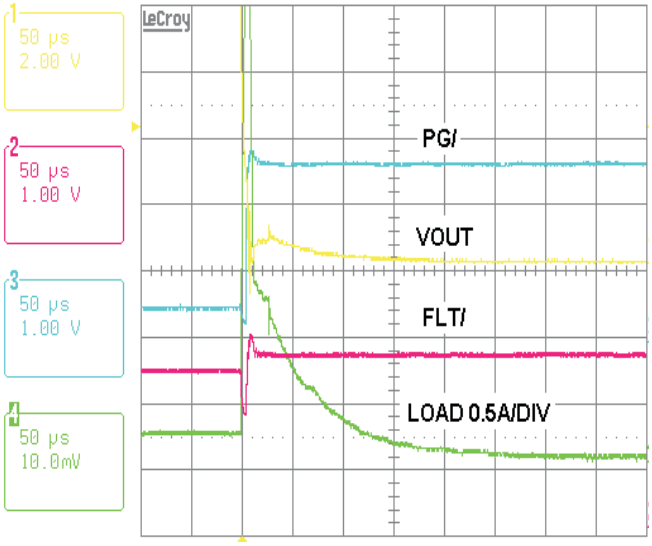


Figure 21. Device Output Short

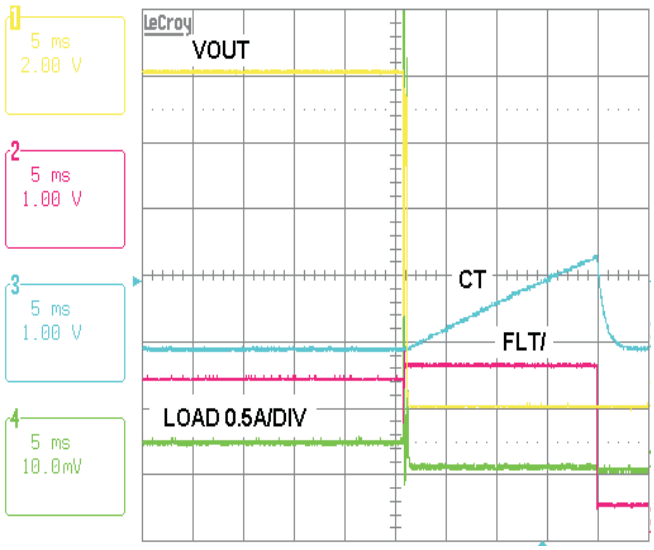


Figure 22. $\overline{\text{FLT}}$ on Device Output Short

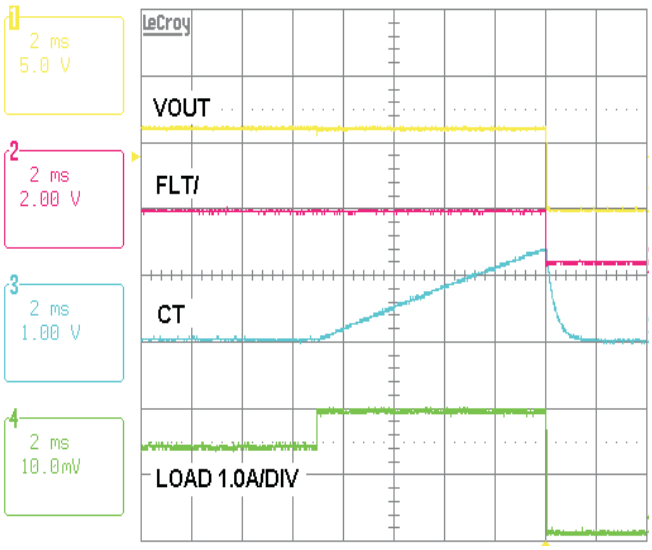


Figure 23. Overcurrent Shutdown

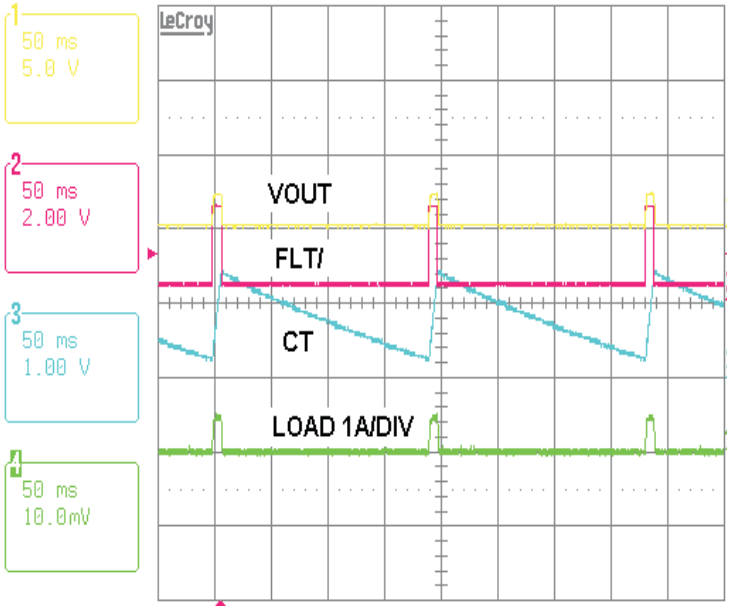


Figure 24. Retry Into an Output Short Circuit

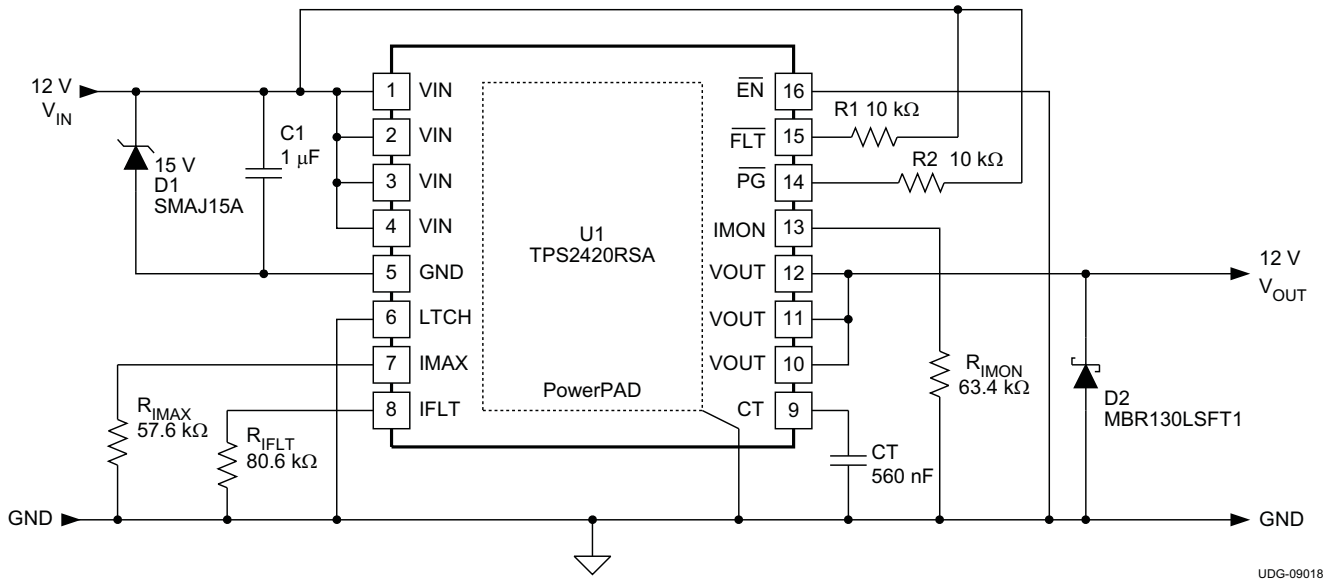


Figure 25. TPS2420 Reference Design, 12-V, 2.5-A Steady State Current, 5-A Max Current

NOTE

D1, D2, and C1 are required only in systems with significant feed and/or load inductance.

To alter parameters I_{IAX}, I_{FAULT}, I_{IMON} or C_{CT} use the formulas in the *Pin Description* section or use Table 2 .

Table 2. Typical Design Examples

I_{FAULT} (A)	R_{IFLT} (kΩ)	I_{IMAX} (A)	R_{IMAX} (kΩ)	C_{CT} (µF)	T_{FAULT} (ms)	T_{SD} (ms)	$I_{LOAD(max)}$ (A)	R_{IMON} (kΩ)
1	200	2	100	0.022	0.86	22	1	158
1.5	133	2.5	80.6	0.047	1.83	47	1.5	105
2	100	3	65.5	0.1	3.89	100	2	78.7
2.5	80.6	3.5	56.2	0.22	8.56	220	2.5	63.4
3	65.5	4	49.9	0.47	18.28	470	3	52.3
3.5	56.2	4.5	44.2	0.68	26.45	680	3.5	45.3
4	49.9	5	40.2	1	38.9	1000	4	39.2

REVISION HISTORY

Changes from Revision A (March, 2010) to Revision B **Page**

- Changed PRODUCT INFORMATION Note 1 to: "For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com." 2
- Changed T_{SD} (ms) column values 20

Changes from Revision B (July 2010) to Revision C **Page**

- Added UL Listed - File Number E169910 1

Changes from Revision C (August 2010) to Revision D **Page**

- Changed CURRENT LIMIT (IMAX) to CURRENT IMAX 3
- Added IFLT may not be set below 1 A to maintain the Fault Current Limit threshold accuracy listed in the Electrical Characteristics table. Some parts may not current limit or fault as expected. 7
- Changed I_{ILIM} to I_{MAX} 15
- Changed I_{ILIM} to I_{MAX} 15
- Changed I_{ILIMIT} to I_{MAX} 16
- Changed I_{ILIMIT} to I_{MAX} 16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS2420RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2420RSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

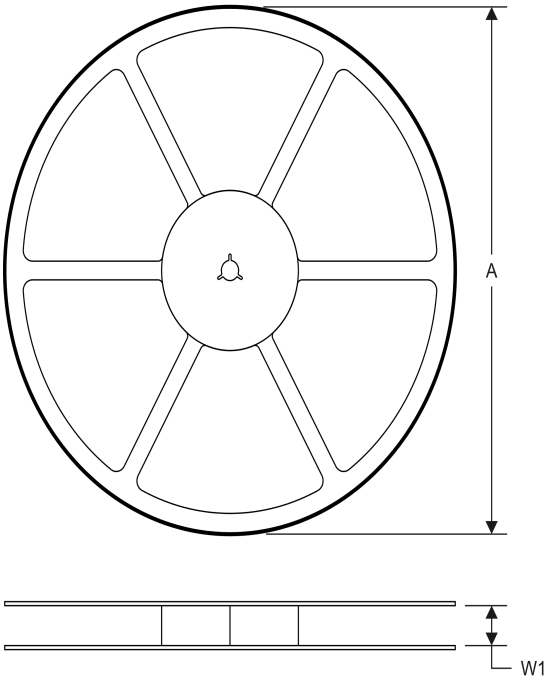
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

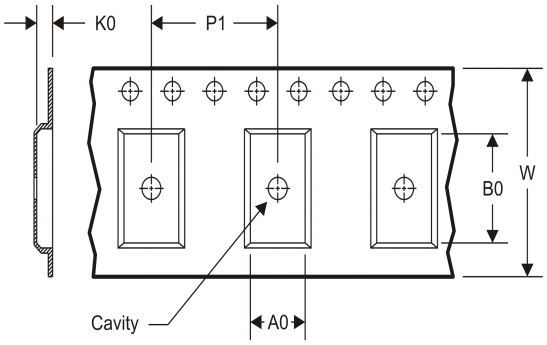
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



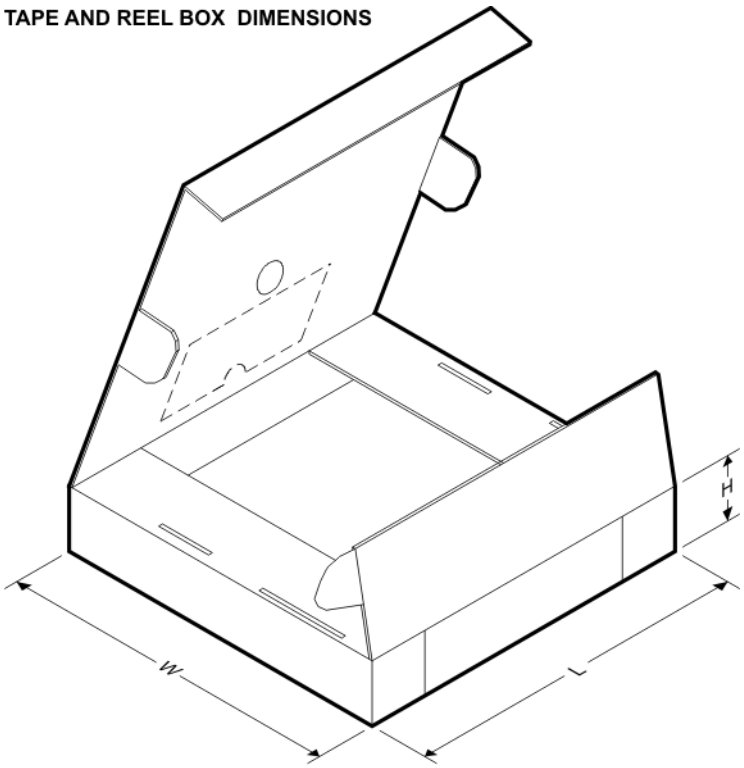
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2420RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS2420RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

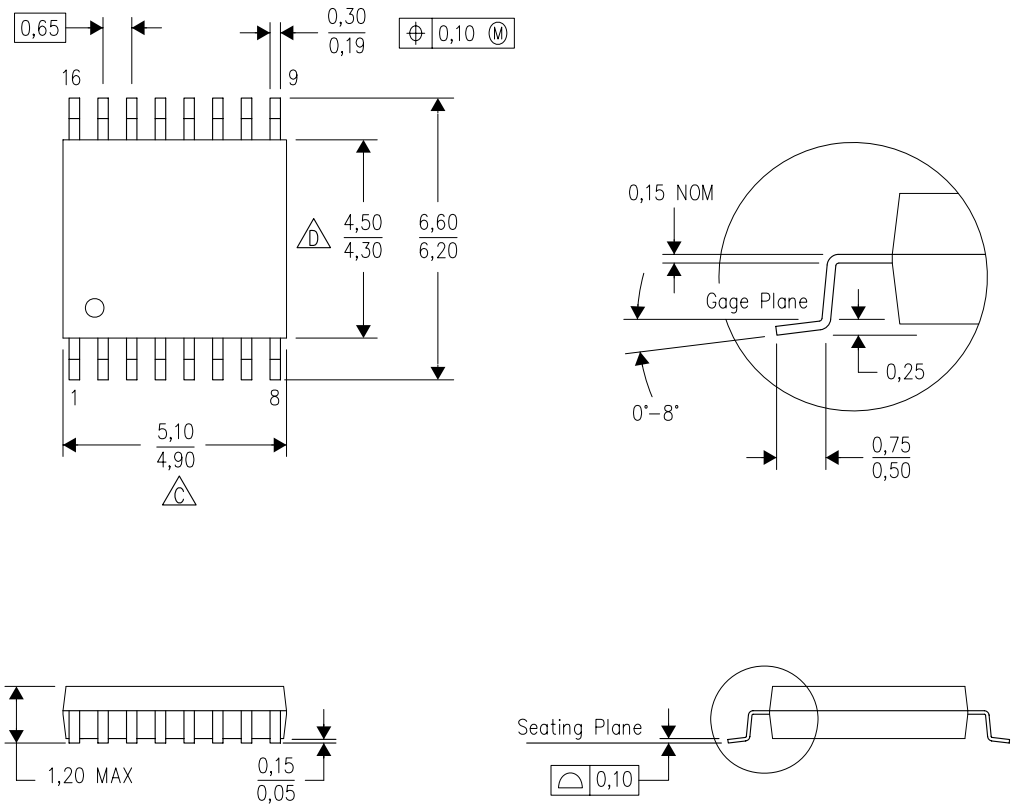
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2420RSAR	QFN	RSA	16	3000	346.0	346.0	29.0
TPS2420RSAT	QFN	RSA	16	250	210.0	185.0	35.0

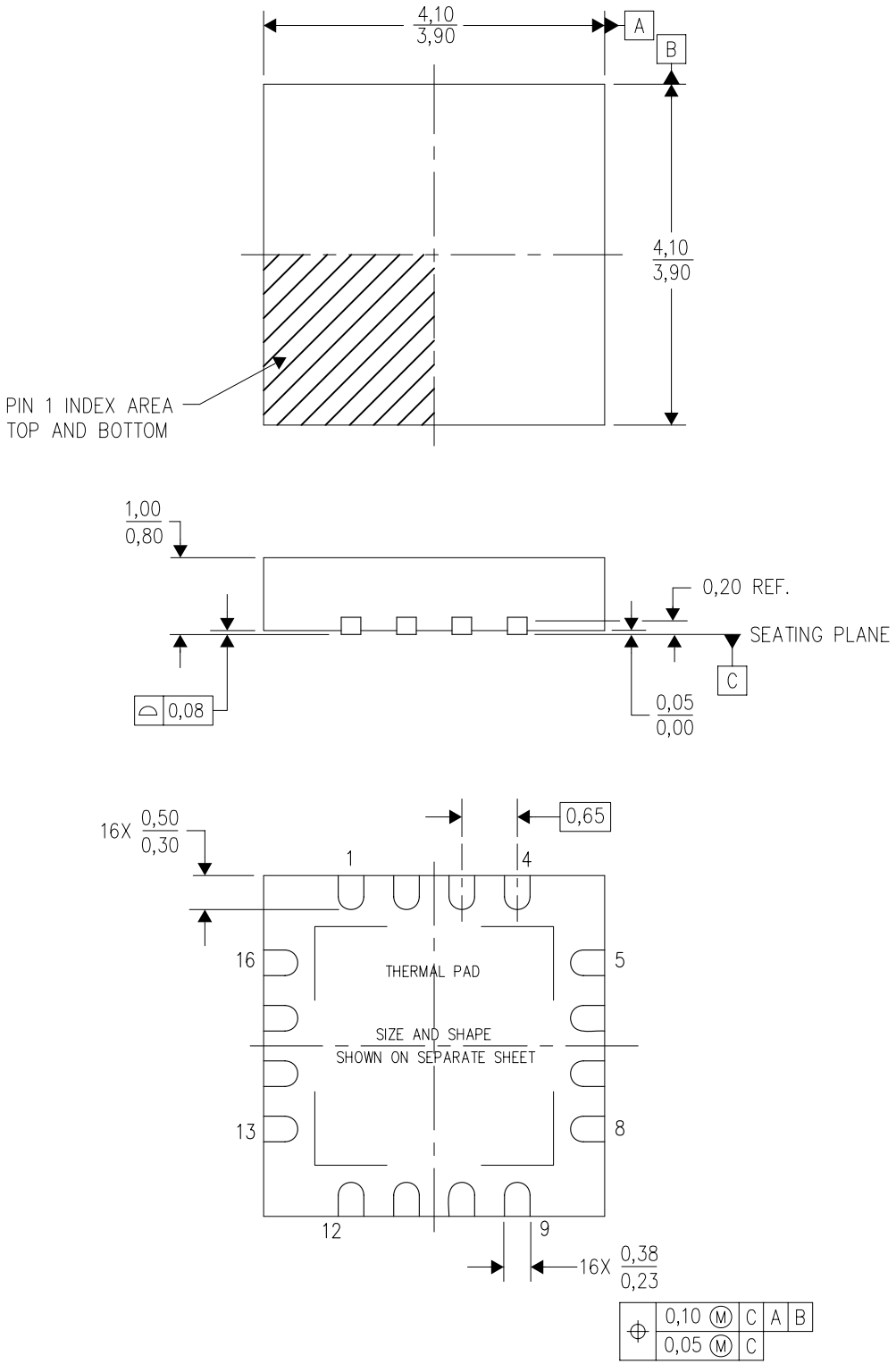
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

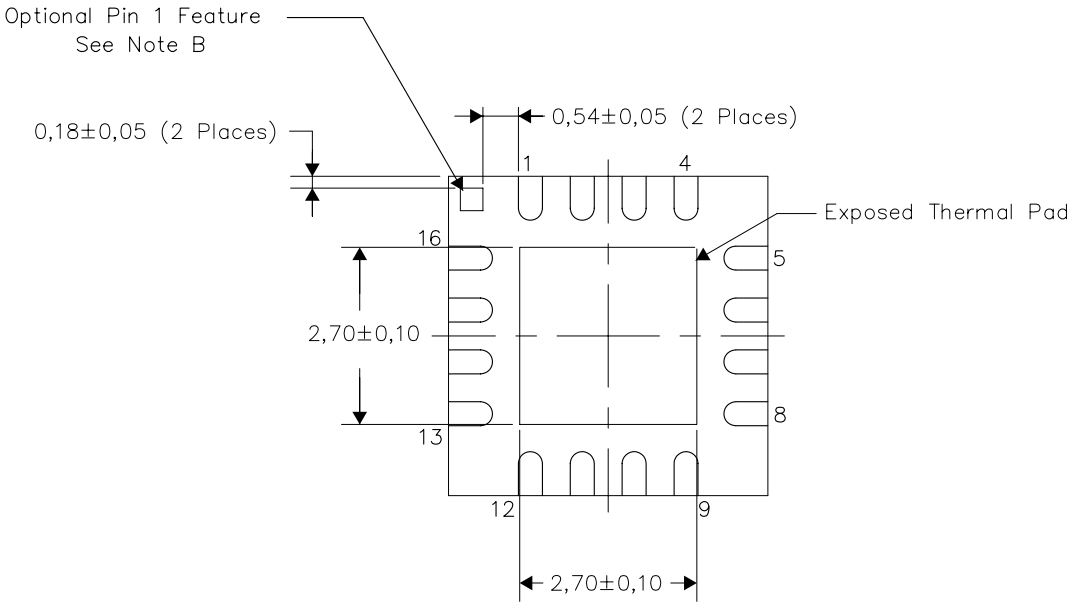
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

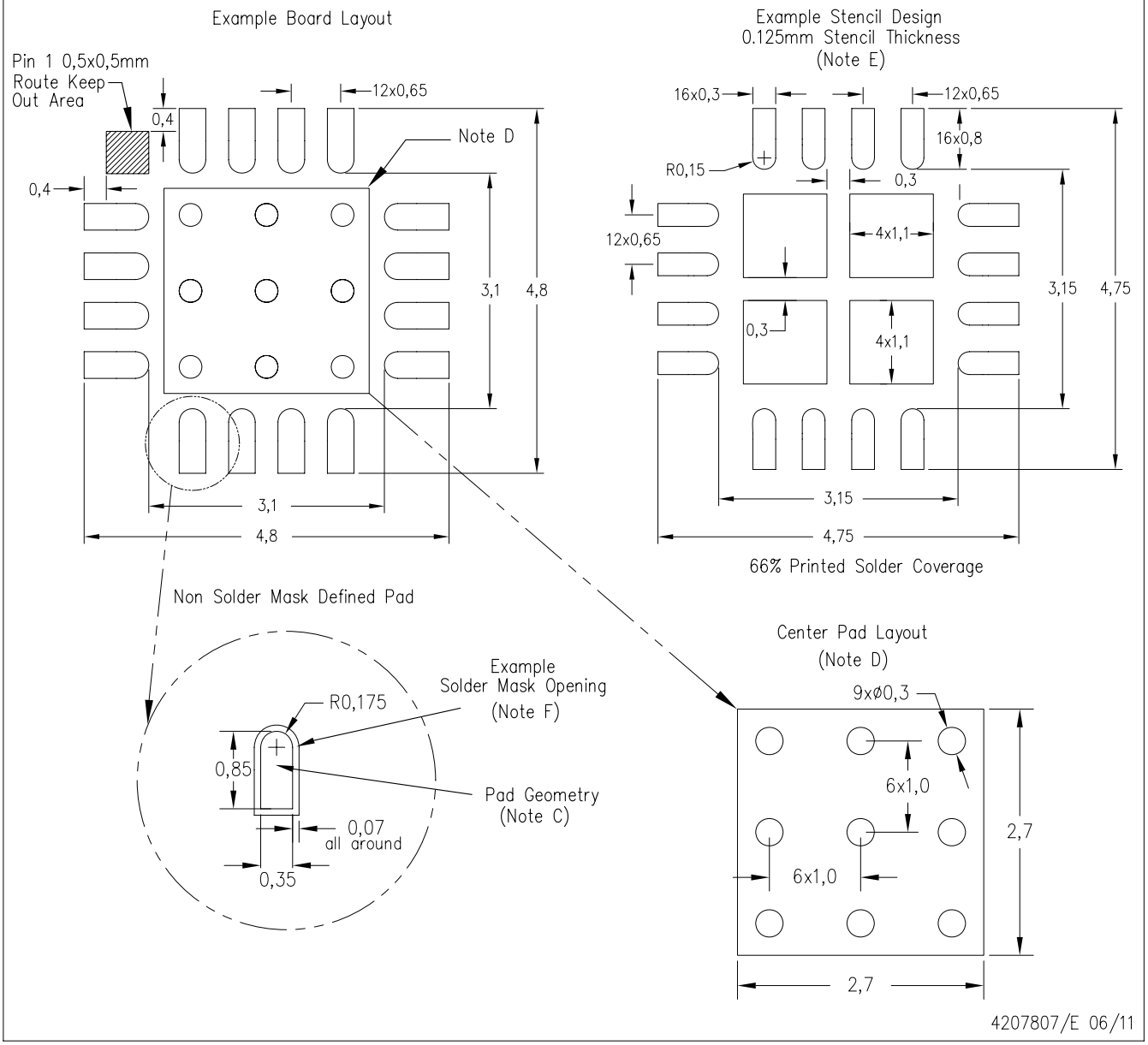
4206364/K 06/11

NOTES:

A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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